Stability Constrained Transient Overcurrent Capability Enhancement of Grid Forming Converters Based on Switching Frequency Adjustment

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***Abstract*—The short-term overcurrent capability is critical for grid forming (GFM) converters to provide support during grid fault transient. Although the transient overcurrent (TOC) capability enhancement strategy based on customized and oversized design for power converters has developed in recent studies, these solutions are still difficult to promote due to their high cost and complex hardware structures. To address this issue, this article introduces the switching frequency as the degree of freedom to improve the TOC capability of GFM converter at the software level. By actively reducing the switching frequency in the TOC stage, the rise in junction temperature caused by overrated current can be suppressed effectively. Moreover, the inherent control stability issue of the inner voltage vector control loop under the substantial decrease of the switching frequency is quantitatively studied. On this basis, a multiparameters coregulation strategy is further proposed to ensure sufficient stability margin of the control loop during the TOC stage with the decreasing switching frequency. This strategy solves the contradiction between control stability and thermal demands in the switching frequency-based TOC method and it can further enhance the TOC capability without redesigning the hardware. Finally, the proposed TOC capability enhancement strategy is verified in both the electrothermal simulation and experiment.**

***Index Terms*—Control loop stability, grid fault, grid forming (GFM), switching frequency, transient overcurrent (TOC) capability.**

I. Introduction

As the penetration of renewable energy sources significantly increases, grid-connected converters are widely used in the generation [1], [2], transmission [3], [4], and distribution [5], [6] of electric power. The grid following (GFL) algorithm based on grid voltage phase tracking and fast current regulation ability is generally adopted in traditional grid-connected converters due to its simple control structure and flexible power adjustment dynamics [7]. However, the classical GFL converters usually have problems of lacking good capability for voltage and frequency support and its normal operation would rely on good synchronization with a sufficiently strong grid [8]. As a result, the oscillation and instability accidents has occurred in a series of high-proportion power electronic systems, which threatens the safety and reliability for the future power electronics-dominated power system [9].

Recently, the grid forming (GFM) control strategy has attracted much attention since it can establish the system voltage and frequency autonomously. Thus, it can maintain good synchronization with the weak grid and even independently support the local loads [10], [11], which makes up for the shortcomings of GFL control. Thanks to the emerging development and evolution in the aspects of inertia emulation [12], [13], reactive power regulation [14], and oscillation suppression [15], [16], the GFM converter can achieve almost perfect imitation and even better performance of the synchronous generators in long-term operating characteristics. It has good capability to participate the power generation and dispatch of the power system in normal operation stage. However, in the case of large disturbances, such as grid faults, the GFM converter usually triggers current limiting control due to the fragility of power devices [17], [18]. The current limiting-based fault ride-through strategy would cause the GFM converters to degrade into GFL behavior and, thus, significantly increase the risk of system transient instability [19], [20], [21].

To solve this issue, solutions with virtual impedances have been proposed to assist the converter in maintaining GFM characteristics under grid fault conditions [22], [23], [24], but the GFM converter still could not provide sufficient voltage and frequency support in transient processes because it only changes the port characteristics but still lacks the transient overcurrent (TOC) capability. Also, the switching in and switching out of these current limiter strategies would introduce additional risks of small-signal and large-signal instability problems. In order

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to fundamentally improve the GFM function of grid-connected converters during the fault stage, the TOC capability needs to be further investigated, and the suppression of the significantly increased junction temperature caused by the overrated current is the core of improving the TOC capability for GFM converters.

A series of methods, including oversized design [25], circuit reconstruction [26], and package improvement [27] have been developed to enhance the TOC capability from the hardware level. However, the solutions with equipment customization are very costly and also need to consider their negative impact on the normal operation of the power converters, such as steady-state cooling performance degradation and power density reduction [28], which may not be suitable for large-scale promotion. It is worth noting that some control variables are loss-dependent in power converters, including switching frequency, dc-side voltage, and duty cycle and the heat accumulation can be dynamically adjusted through these variables to control the junction temperature without any hardware changing [29]. Among these temperature-related control variables, switching frequency obtains wide application because of its high efficiency in power loss regulation and ease of adjustment. To reduce the junction temperature of power modules, switching frequency is used in an active thermal control (ATC) algorithm with proportional integral (PI) controller [30], but the proposed algorithm is only adopted in a single power device and it does not consider specific application scenarios. Then, the customized ATC control is proposed considering the thermal characteristics of the electric drive system [31], proving the feasibility and effectiveness of power loss adjustment based on the switching frequency at the converter level. Furthermore, an optimization design method of ATC is derived for switching frequency smooth adjustment in grid-connected converters [32], which simultaneously meets the requirement of grid codes and equipment thermal stress reduction. However, the state-of-art applications of switching frequency regulation mainly serve the target of lifetime management [33] and they have not yet been applied to the TOC capability enhancement in a short timescale.

Furthermore, the switching frequency would decrease significantly as TOC capability is required to be improved as much as possible. The accompanying changes in time delay will certainly affect the stability performance of the digital control in GFM converter. Although existing research on converter control has studied the impact of digital control delay on the inductor current control [34], capacitor voltage control [35], and inner dual cascade loops [36], [37] in GFM converters, they mainly focus on the optimizing controller performance at a fixed switching frequency with certain time delay. The impact of switching frequency variation on the electrical characteristics of GFM converters with multitimescale control loops, especially on the stability performance, has not been evaluated in detail. Also, the control algorithm that can ensure stability when the switching frequency changes significantly is not fully investigated. It leaves obstacles to the stable control and effective use of the switching frequency for TOC enhancement of GFM converters under transient process.

To fill this gap, the switching frequency is presented as a degree of freedom in this article for TOC capability enhancement of the GFM converter based on the thermal modeling and power loss calculation. The active adjustment of switching frequency can immediately reduce the power losses of the GFM converter and effectively help the converter enhance its TOC capability. Then, the inherent stability issue of inner control loops with the decreased switching frequency during TOC operation is revealed and investigated quantitively. Furthermore, a controller parameter regulation strategy is proposed to ensure the stability margin of the cascaded control loop at the decreased switching frequency. In this manner, the switching frequency can be adjusted in a wide range to improve the TOC capability, while the GFM converter can still maintain the stable voltage source characteristics under the fault transient stage. Finally, the effectiveness of the proposed scheme has been verified on both simulation and experimental platforms. The main purpose of this article is to reduce the power losses of GFM converter in the TOC operation state by decreasing the switching frequency at software level, which can improve its TOC capability without additional cost or hardware adjustments. Another purpose of this article is to avoid the additional stability problem caused by the drastic adjustment of switching frequency.

The major contributions of this article can be summarized as follows.

1) The switching frequency is introduced to improve the TOC capability of GFM converter. It can reduce transient heat accumulation by decreasing the total power loss without additional hardware adjustment.
2) The impact of switching frequency decrease on the stability boundary of the cascaded inner control loop in GFM converter is analytically investigated and quantitatively characterized.
3) The multiparameter coregulation strategy (MPCR) is proposed to ensure the stability margin of the cascaded control loop at the decreased switching frequency so that the GFM converter can maintain its controlled voltage source characteristics while significantly reducing the switching frequency for TOC operation.

The rest of this article is organized as follows. Section II first analyzes the principle of the enhanced TOC capability through switching frequency reduction and discusses the potential negative impact from the decrease of switching frequency on the stability of the vector voltage control. In Section III, the effect of switching frequency in control stability is investigated quantitatively, and the MPCR strategy for the inner loop controller is proposed to maintain the stable and controlled voltage source characteristics of the GFM converter during the fault stage. Sections IV and V demonstrate the electrothermal verification and experimental validation, respectively. Finally, Section VI concludes this article.

II. TOC Capability Enhancement of GFM Converters Based on Switching Frequency Adjustment

This section introduces the typical control structure of the grid-connected GFM converter first. Then, the thermal modeling of the GFM converter is presented, and the enhancement mechanism of the TOC capability by reducing the switching

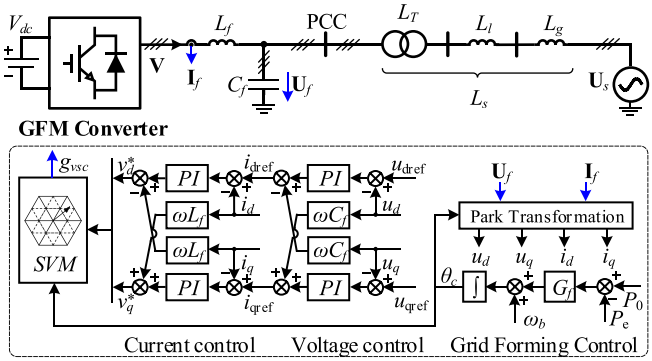

Fig. 1. Circuit and control structure of the grid-connected GFM converter.

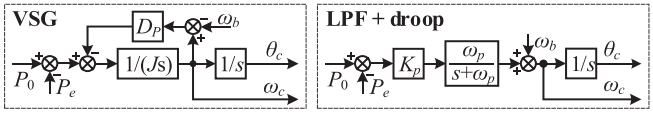

Fig. 2. Typical GFM control. (a) VSG control. (b) Droop control with an LPF.

frequency is discussed. Also, the stability issue introduced by the substantial reduction of switching frequency is analyzed in detail.

A. Control of Grid-Connected GFM Converters

Fig. 1 illustrates the one-line diagram of grid-connected GFM converters. The grid is equivalent to an ideal voltage source named $\mathbf{U}_s$ in series with the system inductance L_s, which includes the transformer inductance L_T, the transmission line inductance L_l, and the grid inductance L_g. The GFM converter is connected to the point of the common coupling (PCC) via a typical *LC*-type filter for ripple suppression.

The GFM loop is applied as the outer power loop of the converter control algorithm to achieve grid synchronization and active power regulation. Various types of GFM control can be implemented through the transfer function G_f, including virtual synchronous generator (VSG) control and droop control with a low-pass filter (LPF) [10], [38], as shown in Fig. 2.

It has been proved in [39] that these two typical schemes are identical, and their equivalence can be expressed as

$$K_P = \frac{1}{D_P}, \omega_P = \frac{D_P}{J} \tag{1}$$

where K_p is the droop coefficient, ω_p is the cut-off frequency in droop based GFM loop, and J and D_p are the inertia and damping coefficient, respectively, in VSG based GFM loop.

The dual loop based terminal voltage vector control is equipped as inner loop to regulate the terminal voltage actively. The current loop usually uses a PI controller to generate the modulation signal of the GFM converter, which can be described as

$$\begin{cases} v_d^* = G_c(s)(i_{dref} - i_d) - \omega L_f i_q \\ v_q^* = G_c(s)(i_{qref} - i_q) + \omega L_f i_d \end{cases} \tag{2}$$

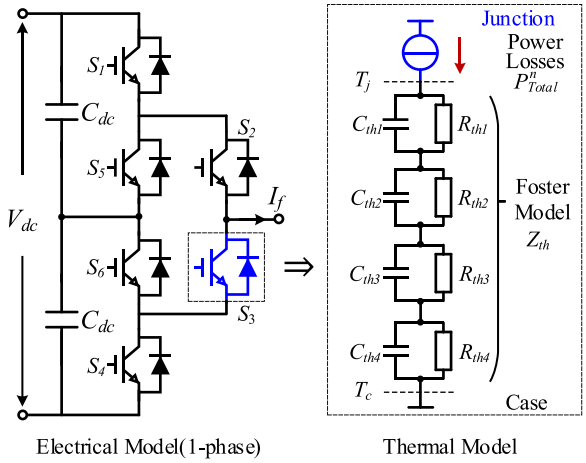

Fig. 3. Thermal model of a power semiconductor device in GFM converter.

where $G_\mathrm{c}(\mathrm{s}) = K_\mathrm{pc} + K_\mathrm{ic}/\mathrm{s}$ is the transfer function of the PI current controller, the reference of the current loop is generated from the voltage controller, whose dynamic is expressed as

$$\begin{cases} i_{dref} = G_v(s)(u_{dref} - u_d) - \omega C_f u_q \\ i_{qref} = G_v(s)(u_{qref} - u_q) + \omega C_f u_d \end{cases} \tag{3}$$

where $G_v(\mathrm{s}) = K_\mathrm{pv} + K_\mathrm{iv}/\mathrm{s}$ is the PI regulator in the voltage control loop. Through the dual inner loop control, the GFM converter can exhibit the characteristics of a well-controlled voltage source.

B. TOC Capability Through Switching Frequency Decrease

In order to discover the loss-dependent control variables, which suitable for TOC capability enhancement and explain its operating principle, the fundamental thermal modeling, and power loss calculation of converter is present in this section. The loss of power devices is the determining factor of their thermal stress performance. To analyze the operating process of each semiconductor device, the duty cycle $D(t)$ with modulation index m can be expressed as follows, which is the input to calculate the device power losses:

$$D(t) = 0.5 + \frac{m}{\sqrt{3}} \sin\left(2\pi f_0 \cdot t + \varphi\right) + \frac{m}{6\sqrt{3}} \sin 3\left(2\pi f_0 \cdot t + \varphi\right). \tag{4}$$

With the output current $I_{xf} = \mathrm{I}_{xfm}\sin(2\pi f_0 \cdot \mathrm{t})(x = \mathrm{a,b,c})$ determined by the circuit structure and control response in Fig. 1, the total power losses of the n_th switching cycle T_sw can be calculated as for each output current cycle

$$P_\mathrm{Total}^n = V_\mathrm{CE}^n\left(I_{xf}^n, T_j^n\right) \cdot I_{xf}^n \cdot D(t) + E_\mathrm{SW}\left(I_{xf}^n, T_j^n\right) \cdot f_\mathrm{SW} \tag{5}$$

where V_CE is the ON-state voltage drop of insulated gate bipolar transistor (IGBT), which is the function of output current I_{xf} and junction temperature T_j. f_sw is the switching frequency of GFM converter and E_sw is the switching energy (turn-ON and turn-OFF) of the power semiconductor devices, which is also dependent on the load current I_{xf} and junction temperature T_j. Based on the modeling of power loss, the thermal model of a single switch in a GFM converter is shown in Fig. 3, and the three-level active

neutral point clamped (ANPC) topology is applied without loss of generality.

In Fig. 3, $T_{\rm j}$ and $T_{\rm c}$ are the junction temperature and the case temperature of the IGBT, respectively. A typical Foster model with four layers is established from the parameters that can be obtained from the datasheet or experimental test. Based on this model, the thermal impedance can be expressed as

$$Z_{th} = \sum_{i=1}^{4} R_{thi}\left[1 - e^{-t/\tau_i}\right] \tag{6}$$

where $\tau_{\rm i} = R_{thi}C_{thi}$, which is the time constant of junction temperature. Therefore, the junction temperature of power devices can be calculated

$$T_j = P_{\rm Total}^{n} Z_{th} + T_c. \tag{7}$$

Since the time scale of grid faults is usually on the millisecond level, which is much smaller than the time constant of the case and heatsink [29], T_c is assumed to be a constant under the discussion of the junction temperature behavior during TOC stage for simplification. It can be seen from (7) that for a completely designed GFM converter, Z_{th} and $T_{\rm c}$ are fixed, and power loss is the only factor affecting junction temperature in this time scale. It is worth noting that the switching frequency $f_{\rm sw}$ appears in the expression of power loss, which is also a controllable variable that can be adjusted independently through the modulation stage. When the GFM converter enters the TOC operating state, the switching loss of the GFM converter can be reduced by actively and immediately decreasing the switching frequency, and the pump rise of junction temperature can be suppressed in the transient process.

The above idea is essentially a kind of ATC, which usually serves for long-term reliability management of power converters with small-range adjustment of switching frequency. Since the range of switching frequency change is small enough in this situation that the effect on the electrical control loop is negligible, the control structure of the electrical variable can remain fixed. However, the switching frequency value needs to be reduced significantly in the short term to maximize the TOC capability. It will cause conflicts between electrical control and thermal demand and further have a negative impact on the stability of the GFM converter, which will be analyzed next.

C. Stability Issue Caused By Switching Frequency Decrease

The parameters of the GFM loop shown in Fig. 2 are usually designed according to the operating requirements of the power system, which causes it to have a relatively slow response compared to the inner control loops. The dynamics of GFM loop can be neglected in this study. Assuming that the coupling between the *d*-and *q*-axis is decoupled well due to the use of the cross-couple decoupling technique [40], the dynamics of inner cascade control loop can be described in Fig. 4.

Since the digital control is generally adopted for GFM converters, the inevitable control delay $T_{\rm d}$ is produced and determined by switching frequency. The delay is modeled as

$$G_d(s) = {\rm e}^{-sT_d} \tag{8}$$

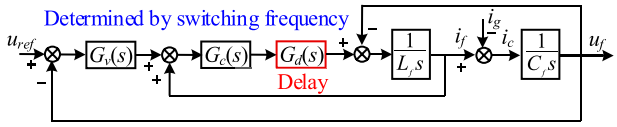

Fig. 4. Control block diagram of inner dual-loop voltage control.

TABLE I
ELECTRICAL PARAMETERS OF SIMULATION AND EXPERIMENTAL PROTOTYPE

Parameter	Value
Rated power $S_{\rm N}$	11.5 kW
Rated frequency f_0	50 Hz
Rated voltage (line-to-line) $U_{\rm sN}$	190 V
Rated Current $I_{\rm fN}$	35A
Filter Inductance L_f	840 μH (0.11 p.u.)
Filter Capacitance C_f	80 μF(0.06 p.u.)
System Inductance L_s	3.1 mH (0.4 p.u.)

TABLE II
CONTROL PARAMETERS OF SIMULATION AND EXPERIMENTAL PROTOTYPE

Category	Parameter	Value
Modulation and thermal	Switching frequency f_{sw}	10 kHz
	Sampling frequency f_s (=2f_{sw})	20 kHz
	Switching frequency (OC) f_{sw_oc}	2.5 kHz
	Sampling frequency (OC) f_{s_oc} (=2 f_{sw_oc})	5 kHz
	Sampling rate N (= f_s /f_{sw})	2
Current loop	Proportional gain $K_{\rm pc}$	14.44
	Integral gain $K_{\rm ic}$	25.137
Voltage loop	Proportional gain $K_{\rm pv}$	0.0731
	Integral factor $K_{\rm iv}$	32
GFM loop	GFM Loop Cut-off Frequency ω_p	2π×2rad/s
	GFM Loop Droop Gain $K_{\rm p}$	0.02 p.u.

where the total delay T_d equals 1.5 times the control period T_s, with $1T_s$ delay due to one control cycle and $0.5T_s$ delay due to the zero-order-hold mechanism during modulation [34].

Under the fixed sample and hold mode in digital controller, the total delay T_d is inversely proportional to the switching frequency $f_{\rm sw}$ and the open loop transfer function of dual-inner loop control can be expressed in s-domain

$$T_v(s) = \frac{G_v(s)\omega_r^2}{s^2 + sG_c(s)G_d(s)/L_f + \omega_r^2} = G_v(s)G_{LC\_R}(s) \tag{9}$$

where ω_r is resonance frequency of the *LC* filter, which can be expressed as

$$\omega_r = \sqrt{\frac{1}{L_f C_f}} = 2\pi f_r. \tag{10}$$

According to the electrical and control paraments given in Tables I and II. The impact of switching frequency reduction on inner cascaded control loop stability can be investigated in Fig. 5.

If the control parameters are maintained constant at steady-state designed values, the stability margin of the control loop will reduce significantly as the switching frequency decreases and even instability occurs at $f_{\rm sw} = 6$ kHz, as shown in Fig. 5. Since the parameters of inner loop control are usually designed

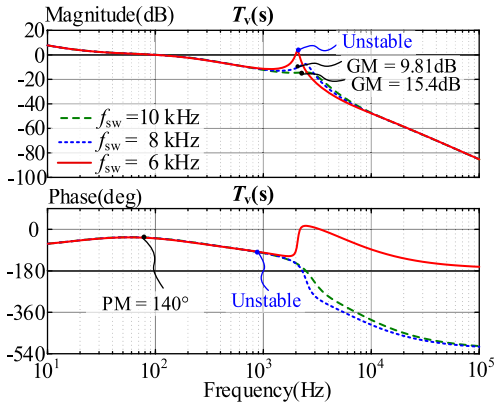

Fig. 5. Bode diagram of $T_v(s)$ with fixed controller parameters under switching frequency f_{sw} decrease.

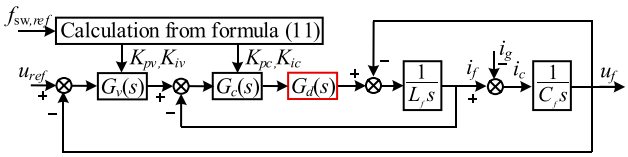

Fig. 6. Control block diagram of inner dual-loop voltage control with reconfigured controller gain.

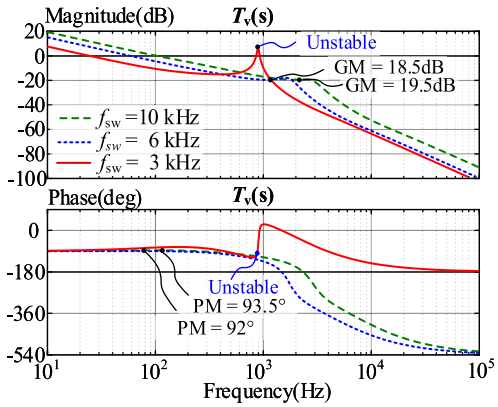

Fig. 7. Bode diagram of $T_v(s)$ with reconfigured controller parameters under switching frequency f_{sw} decrease.

related to the switching frequency [40], as shown in

$$\begin{cases} K_{pc} = \omega_i L_f \\ K_{ic} = \omega_i R_f \\ K_{pv} = \omega_v C_f \\ K_{iv} = \omega_v^3 C_f/\omega_i \end{cases} \tag{11}$$

where $\omega_i = N2\pi f_{sw}/10$ and $\omega_v = 1.6\omega_i/10$, the sample rate $N = f_s/f_{sw}$. Thus, the controller parameters can be easily reconfigured through digital controller according to this design rules used in steady-state operation with new operating switching frequency, illustrated in Fig. 6.

Based on this method, the stability performance can be investigated in Fig. 7. Since the design of the control bandwidth is usually proportional to the switching frequency, this method has a certain potential to adapt to the switching frequency changes. It can be seen that the instability problem has been alleviated but still exists under a lower switching frequency value ($f_{sw} = 3$ kHz) because the design method of controller parameters in (11) rarely considers switching frequency variation effect. It means that the simple and linear adjustment of the bandwidth of the cascade controller based on the switching frequency would be difficult to ensure stability under large changes in the switching frequency of the GFM converter.

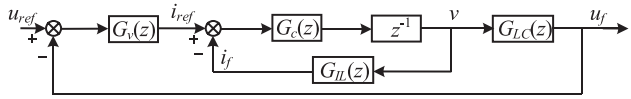

Fig. 8. Control block diagram of inner dual-loop voltage control in z-domain.

In light of this analysis and discussion, the stability issue of the electrical control loop has become a constraint in reducing the switching frequency to achieve TOC capability in the GFM converter. Thus, the control strategies need to be explored in the following for enhancement of the stability performance under a wide range reduction of switching frequency to further serve the needs of TOC operation during grid fault.

III. Multiparameters Coregulation Strategy for Stability Constrained TOC Operation

In this section, the stability boundary of the cascaded inner control loop in the GFM converter is quantitatively characterized based on z-domain modeling. Then, a controller MPCR strategy is further proposed to satisfy the stability constraint with a wide range decrease in switching frequency under the TOC stage.

A. Delay Dependent Current Loop Stability Analysis

In order to accurately and quantitatively analyze the impact of switching frequency f_{sw} changes on the cascade inner loop control of GFM converters, modeling and analysis work is carried out in the z-domain, as shown in Fig. 8.

The impact of delay on the loop can be described by a linear transfer function with trigonometric coefficients as follows and the sampling period is calculated through $T_s = 1/Nf_{sw}$:

$$G_{IL}(z) = \frac{i_f(z)}{v(z)} = \frac{\sin(\omega_r T_s)}{\omega_r L_1} \frac{z-1}{z^2 - 2z\cos\omega_r T_s + 1} \tag{12}$$

$$G_{LC}(z) = \frac{u_f(z)}{v(z)} = (1-\cos\omega_r T_s) \frac{z+1}{z^2 - 2z\cos\omega_r T_s + 1}. \tag{13}$$

For current loop, its main function is to reshape the mid and high frequency dynamics of the control loop and dampen the resonance of the *LC* filter, which is mainly dominated by its proportional gain [41]. Thus, the constraint of switching frequency adjustment on the proportional gain of the current controller is considered in this article. The characteristics of the inner current loop dynamics can be expressed as follows:

$$G_{LC\_R}(z) = \frac{(z+1)(1-\cos\omega_r T_s)}{z(z^2 - 2z\cos\omega_r T_s + 1) + K_{PC}\frac{\sin(\omega_r T_s)}{\omega_r L_1}(z-1)} \tag{14}$$

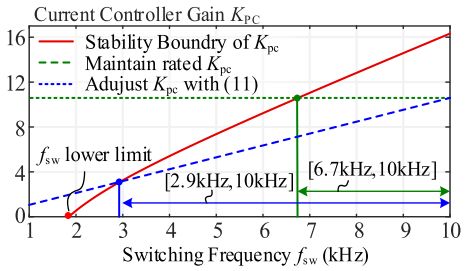

Fig. 9. Stability boundary of current inner loop gain K_{pc} under switching frequency f_{sw} decrease.

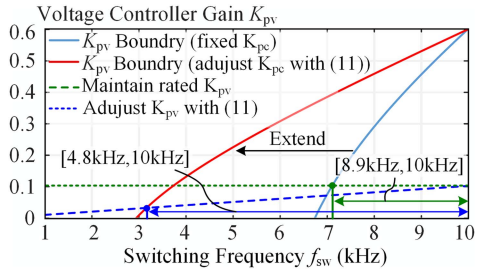

Fig. 10. Stability boundary of voltage outer loop gain K_{pv} under switching frequency f_{sw} decrease.

where $G_{LC\_R}(z) = u_f(z)/v(z)$ and K_{pc} is the proportional gain of the current controller. Thus, the stability of the system expressed in (14) is determined by the characteristic equation as follows:

$$z\left(z^2 - 2z\cos\omega_r T_s + 1\right) + K_{PC}\frac{\sin(\omega_r T_s)}{\omega_r L_1}(z-1) = 0. \tag{15}$$

Furthermore, the stable range of the inner current loop gain under the influence of sampling period T_s can be obtained from the Routh criterion in the discrete domain

$$0 < K_{PC} < \frac{(2\cos\omega_r T_s - 1)\omega_r L_1}{\sin\omega_r T_s}. \tag{16}$$

Define the upper limit of proportional gain as $K_{\mathrm{pc\_lim}} = (2\cos\omega_r T_s - 1)\,\omega_r L_1/\sin\omega_r T_s$, the change of stability boundary with switching frequency can be analyzed as follows:

$$\frac{dK_{\mathrm{pc\_lim}}}{dT_s} = \frac{\omega_r^2 L_1}{\sin^2\omega_r T_s}(\cos\omega_r T_s - 2) < 0. \tag{17}$$

As switching frequency f_{sw} decreases, i.e., the sampling period T_s increases, the proportional gain boundary of the current controller will decrease monotonically, which is illustrated in Fig. 9. If the gain K_{pc} is fixed, the allowable adjustment range of the switching frequency under stability constraints is 6.7 kHz to 10 kHz. Although dynamic adjustment of K_{pc} can further expand the adjustment range of switching frequency, it is still limited by current loop stability.

B. Voltage Loop Stability Boundary Consider Current Effect

Since the proportional gain of the voltage controller mainly affects the stability performance and it is more sensitive to time delay [40], the proportional gain K_{pv} is analyzed in this section. Based on the modeling and stability analysis of current inner control, the open-loop transfer function of the voltage outer loop can be expressed as

$$\begin{aligned} G_{vo}(z) &= G_{LC\_R}(z)K_{PV}K_{PC} \\ &= \frac{K_{pv}K_{pc}(z+1)(1-\cos\omega_r T_s)}{z(z^2 - 2z\cos\omega_r T_s + 1) + K_{PC}\frac{\sin(\omega_r T_s)}{\omega_r L_1}(z-1)}. \end{aligned} \tag{18}$$

According to Figs. 5 and 7, the following conditions need to be met at the frequency ω_{cp}, where the phase characteristics of $G_{vo}(z)$ crossing $-180°$ to ensure voltage control loop keep stable

$$\begin{cases} \mathrm{Im}\left[G_{\mathrm{vo}}(z = e^{j\omega_{cp}T_s})\right] = 0 \\ \mathrm{Re}\left[G_{\mathrm{vo}}(z = e^{j\omega_{cp}T_s})\right] < 1. \end{cases} \tag{19}$$

Substituting the conditions (19) into (18), the proportional gain boundary of the voltage controller can be obtained as follows:

$$0 < K_{PV} < \frac{2A - 2B + \sqrt{C} - 1}{2K_{PC}(A-1)} \tag{20}$$

where

$$\begin{cases} A = \cos\omega_r T_s \\ B = K_{PC}\sin\omega_r T_s/\omega_r L_1 \\ C = (2A+1)^2 - 8B. \end{cases} \tag{21}$$

It can be seen that the stability boundary of the voltage loop gain is related to the control delay and the configuration of the current inner loop. Define the upper limit of proportional gain as $K_{\mathrm{pv\_lim}} = (2\mathrm{A} - 2\mathrm{B} + \sqrt{C} - 1)/2K_{\mathrm{pc}}(\mathrm{A}-1)$, the change of stability boundary with switching frequency can be analyzed as follow:

$$\begin{cases} \frac{dK_{\mathrm{pv\_lim}}}{dT_s} = \frac{K_1}{2K_{PC}(A-1)} + \left(2A - 2B + \sqrt{C} - 1\right)\frac{dA}{dT_s} \\ K_1 = \left(2 + 2\left(\frac{2A+1}{\sqrt{C}}\right)\frac{dA}{dT_s} - 2\left(2 + \frac{4}{\sqrt{C}}\right)\frac{dB}{dT_s}\right. \end{cases} \tag{22}$$

where

$$\begin{cases} \frac{dA}{dT_s} = -\omega_r\sin\omega_r T_s \\ \frac{dB}{dT_s} = K_{PC}\cos\omega_r T_s/L_1 \end{cases}. \tag{23}$$

Due to the constraints of current loop stability in (17), $\cos\omega_r T_s > 1/2$ is satisfied. Which can derive $dA/dT_{\mathrm{s}} < 0$ and $dB/dT_{\mathrm{s}} > 0$, so K_1 is less than 0 in this condition. Thus, the $dK_{\mathrm{pv\_lim}}/dT_{\mathrm{s}} < 0$ is determined in the grid-tied GFM converter. This means that no matter how the current inner loop gain is configured, as the switching frequency f_{sw} decreases, the sampling period T_s increases, the gain boundary of the voltage controller also decreases monotonically, as shown in Fig. 10.

Although the current controller gain K_{pc} cannot change the tendency of the controller gain boundary in the voltage control loop to decrease over time delay, adjusting the current loop gain can help the voltage controller maintain stability within a wider switching frequency range. Therefore, it is necessary to achieve codesign of the voltage controller and current controller to improve the stability performance of the controller under a wider range of switching frequency changes.

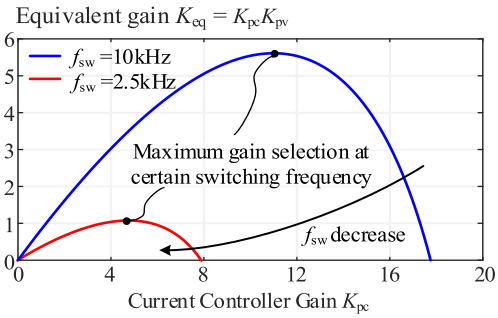

Fig. 11. Stability boundary of equivalent gain K_{eq} under switching frequency f_{sw} decrease.

C. MPCR Strategy for Stability Enhancement in TOC Stage

It can be seen from Figs. 9 and 10 that if the number of loading times of digital controller is fixed in one control cycle, as the switching frequency decreases, the sampling frequency decreases significantly in proportion. If the controller continues to use the control parameters designed under normal operating conditions, the stability margin will decrease or even become unstable. Adjusting the control gain to follow the switching frequency according to a certain method can help the control loop adapt to a wider range of switching frequency changes. However, since traditional control parameter designs generally do not consider large-scale changes in switching frequency, it is still difficult to guarantee stability.

For the inner dual-loop controller, its main task is to achieve good regulation capability of the terminal voltage dynamics, which relies on the loop gain to be increased as much as possible. It is worth noting that the loop gain of the dual inner loop is essentially determined by the product of the voltage controller proportional coefficients K_{pv} and current controller proportional coefficients K_{pc}. Therefore, the optimization of voltage loop dynamics essentially requires optimizing the two parameters K_{eq} and K_{pc}. Under a fixed switching frequency, their analytical relationship can be represented in Fig. 11.

It can be concluded that for a GFM converter with a determined switching frequency, there is a set of optimal parameter combinations to achieve the highest voltage loop gain. Since the constraint expressed by (20) is consistent with the definition of gain margin (GM). Considering the stability margin of the voltage loop, the stability boundary can be expressed as follows:

$$K_{\mathrm{eq\_lim}} = \mathrm{GM}\frac{2A - 2B + \sqrt{C} - 1}{2\left(A - 1\right)}. \tag{24}$$

The analytical expression of the highest loop gain can be calculated by $\mathrm{d}K_{\mathrm{eq\_lim}}/\mathrm{d}K_{\mathrm{PC}} = 0$, and further, the proportional coefficient combination of the dual-loop controller can be calculated to satisfy the gain margin demand as follows:

$$\begin{cases} K_{PC} = \frac{\omega_r L_1}{\sin \omega_r T_s}\left(\frac{1}{8}(2A+1)^2 - \frac{1}{2}\right) \\ K_{PV} = \frac{K_{eq}}{K_{PC}} \end{cases} \tag{25}$$

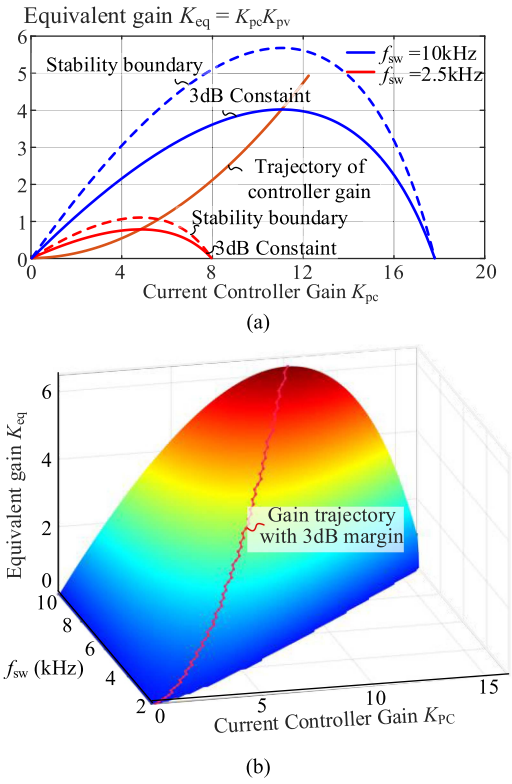

Fig. 12. Controller gain trajectory of proposed MPCR strategy. (a) Two-dimensional diagram with normal and TOC operation frequency. (b) Three-dimensional diagram with continuous decrease of switching frequency.

where

$$\begin{cases} A = \cos(\omega_r T_s) \\ K_{eq} = \frac{\mathrm{GM}}{2}\frac{-A^2+A-1/4}{A-1} \\ T_s = N/f_{sw}(N \text{ is the sample rate}). \end{cases} \tag{26}$$

In this manner, the inner loop gain of the GFM converter is uniquely determined by the switching frequency, and it can ensure that the voltage loop reaches the maximum gain under the stability margin constraint at the fixed switching frequency. Choosing a gain margin of 3 dB as an example, the value trajectory of the controller gain is shown in Fig. 12. It can be seen in Fig. 12(a) that the proposed control method can ensure a stable margin of the control loop under a certain switching frequency value, and at the same time, the maximum gain can be achieved while ensuring the stability margin. Fig. 12(b) shows that the proposed control method has the good potential to serve the continuous smooth adjustment of switching frequency and provide a good interface for the ATC algorithm. The integral coefficient of the voltage controller can remain unchanged from the original design because it is relatively decoupled from the proportional coefficient in dual inner loop control [40].

It is worth noting that when the upper limit of proportional gain of current controller K_{pc_lim} is equal to 0, the switching frequency cannot be further reduced. It means that no matter how the control parameter is configured, the controller cannot meet the requirements of LC resonance damping, and the control object of the voltage outer loop will become unstable. This

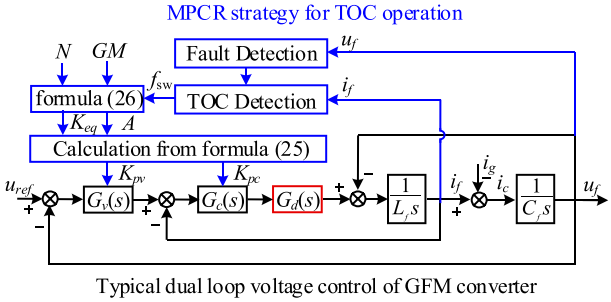

Fig. 13. Control block diagram of inner dual-loop voltage control with proposed MPCR strategy.

boundary can be simplified as $2\cos\omega_r T_s - 1 > 0$ because the other parts are all positive in K_{pc_lim}. Therefore, the controller sampling frequency $f_s = 1/T_s$ needs to be greater than six times the resonant frequency, i.e., $f_s > 6f_r$.

Based on the proposed MPCR control algorithm, the TOC controller of the GFM converter can be illustrated in Fig. 13. The sample rate N and gain margin GM is predesigned and needs to input for controller gain calculation. The inverter side current i_f is used for determine whether the converter enters TOC state and PCC voltage u_f is used for whether a power grid failure occurs. When TOC state is detected, the GFM converter will switch to a lower switching frequency operating mode and calculate the current controller gain according to (25) and (26) to ensure the stability of the loop for terminal voltage support and overload current output.

When the proportional resonant (PR) controller with positive and negative sequence regulation capability is equipped, the GFM converter is enabled to regulate its positive and negative sequence currents and voltage independently without changing control loop structure [42], [43], [44]. For the PR controller, the proportional gain design is exactly the same as that of the PI controller. Also, the resonant gain is similar to the integral coefficient in the PI controller, and it would always work in the low-frequency band and decoupled from the proportional gain [40], [41]. Therefore, the MPCR strategy has the good potential to be extended to the cascaded dual inner loop control based on the PR controller, and the GFM converter would have the ability to regulate the positive and negative sequence components while maintaining the TOC state in asymmetrical fault.

D. Evaluation of Transient Stability and Grid Impedance Effect

Due to the TOC capability of GFM converter being enhanced through decreasing switching frequency, the converter could maintain its GFM control in fault transient. The large signal behavior of power angle can be described through swing equation [8], [9], which is written as

$$J\ddot{\delta} = P_0 - P_e - D_p\dot{\delta} = P_0 - U_s U_f \sin\delta/X_s - D_p\dot{\delta} \quad (27)$$

where $\delta = \theta - \theta_s$ is defined as power angle, and it is the phase difference between the terminal voltage U_f and grid voltage U_s. X_s is the equivalent impedance between the PCC and the grid. J and D_p are the inertia and damping coefficients, respectively.

The transient stability boundary is usually characterized by Lyapunov function with UEP in postfault [45], [46], and it is calculated with the postfault grid voltage U_{spf} as

$$\delta_{eu} = \pi\text{-arcsin}\left(\frac{P_0 X_s}{U_{spf}U_f}\right). \quad (28)$$

In the characterization of the transient stability boundary, it is usually assumed that the UEP is a zero potential energy point. Thus, the total transient energy of GFM system after fault clearance is written as follows:

$$V_{pf}\left(\delta,\dot{\delta}\right) = \frac{J\dot{\delta}^2}{2} + P_0\left(\delta_{eu}-\delta\right) + \frac{U_{spf}U_f}{X_s}\left(\cos\delta_{eu} - \cos\delta\right). \quad (29)$$

Transient angle stability is guaranteed by the condition that there is no additional total energy at the UEP. Therefore, the transient stability boundary can be characterized by

$$V_{pf}\left(\delta_c,\dot{\delta}_c\right) = V_{pf}\left(\delta_{eu},0\right) = 0. \quad (30)$$

If the fault is cleared within this boundary, the transient stability can be guaranteed.

Moreover, the stability performance of proposed MPCR strategy consider gird impedance (L_s) effects is evaluated. In the per-unit value representation, the short circuit ratio (SCR) with the definition SCR $=1/L_s$ is used in following evaluation [9], [15]. The MPCR strategy only configures the parameters according to different switching frequencies without changing the dual inner loop control structure. The output impedance $Z_{\mathrm{GFM}}(s)$ with dual inner loop can be derived as

$$Z_{\mathrm{GFM}}(s) = \frac{Z_C(s)}{1 + Z_C(s)Z_i(s) + Z_C(s)G_v(s)T_i(s)} \quad (31)$$

where $T_i(s)$ and $Z_i(s)$ are the close loop transfer functions of inner current control, which can be written as

$$\begin{cases} T_i(s) = \frac{i_f(s)}{i_{fref}(s)} = \frac{G_c(s)G_d(s)Z_L(s)}{1+G_c(s)G_d(s)Z_L(s)} \\ Z_i(s) = \frac{i_f(s)}{u_f(s)} = \frac{Z_L(s)(1-H_iG_d(s))}{1+G_c(s)G_d(s)Z_L(s)} \end{cases} \quad (32)$$

$Z_L(s) = 1/sL_f$ and $Z_C(s) = 1/sC_f$, respectively. H_i is the voltage feedforward coefficient in the current control loop to improve the current response at the instant of grid voltage drop. It has no effect on the control loop stability but affects the output impedance, so it is considered in (32) and $H_i = 0.5$ is selected [48]. In addition, the virtual impedance and the current feedforward of the voltage loop are not used. The bode diagram of output impedance under different switching frequency with proposed MPCR strategy is drawn in Fig. 14 and verified through the frequency sweep in the MATLAB/Simulink.

The grid impedance can be modeled as $Z_s(s) = 1/sL_s$. The stability performance can be further evaluated through the impedance ratio $Z_{\mathrm{GFM}}(s)/Z_s(s)$ [24], [47], [48]. Bode diagram of impedance ratio with different SCR is shown in Fig. 15, it can be seen that the MPCR strategy can also maintain stability with SCR varying from 1.5 to 10 under the switching frequency of normal state with 10 kHz and TOC operating state with 2.5 kHz in this article.

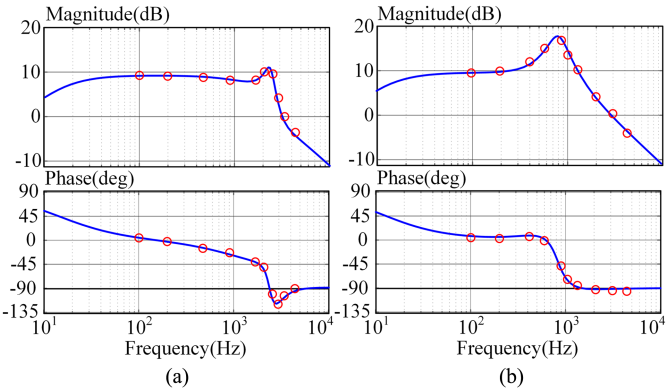

Fig. 14. Bode diagram of impedance Z_{GFM} with proposed MPCR strategy. (a) $f_{sw} = 10$ kHz. (b) $f_{sw} = 2.5$ kHz.

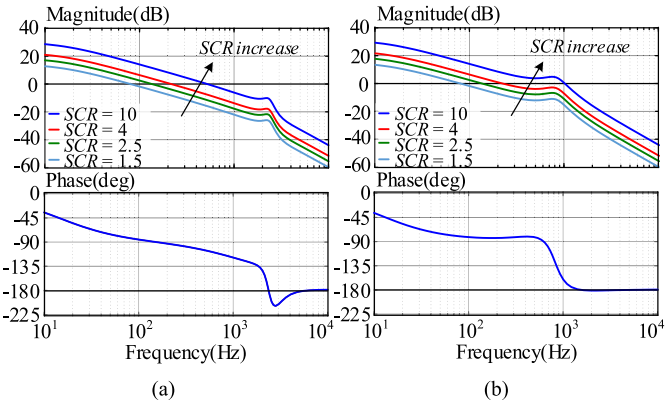

Fig. 15. Bode diagram of impedance ratio with different SCR. (a) $f_{sw} = 10$ kHz. (b) $f_{sw} = 2.5$ kHz.

TABLE III
FOSTER MODEL PARAMETERS OF POWER DEVICE USED IN SIMULATION

Parameter	Value
First-order Thermal Resistance R_{th1}	0.0130 K/W
First-order Thermal Capacitance C_{th1}	0.0699 J/K
Second-order Thermal Resistance R_{th2}	0.0321 K/W
Second-order Thermal Capacitance C_{th2}	0.3396 J/K
Third-order Thermal Resistance R_{th3}	0.0769 K/W
Third-order Thermal Capacitance C_{th3}	0.5969 J/K
Fourth-order Thermal Resistance R_{th4}	0.0533 K/W
Fourth-order Thermal Capacitance C_{th4}	0.5779 J/K

IV. SIMULATION STUDIES

The simulation is presented based on the gird-connected GFM converter in Fig. 1 with electrical and control parameters listed in Tables I and II to verify the effectiveness of switching frequency decrease for TOC capability enhancement. And the simulation studies also demonstrate the stability performance of each control scheme with switching frequency variation conditions.

A 11.5 kW ANPC converter is chosen for simulation, which is consisted of silicon IGBT devices. The parameters of the foster model in Fig. 3 are obtained by testing the power semiconductor device used in the experiment platform and they are shown in Table III. Due to the double sampling being used, the switching frequency should be greater than three times the resonant frequency, i.e., $f_{sw} > 3f_r$. The switching frequency value should be greater than 1.842 kHz, as calculated from the parameters in Table I. Considering that a certain stability margin needs to be left in the outer loop design, 2.5 kHz is finally selected, which is close to the theoretical switching frequency limit for loop stability.

A. Analysis of Inherent TOC Capability

The inherent TOC capability of the used converters at a rated switching frequency of 10 kHz is first tested. The steady-state output current of the converter is set at 35 A, and the steady-state operating junction temperature is 115 °C, which is set as the base junction temperature value for simulations. In order to ensure that the device does not get damaged due to overheating, set the junction temperature limit of the device at 125 °C. A symmetrical fault is triggered at 0 s with a voltage drop to 0.6 p.u., and the grid voltage is recovered to 1 p.u. at 0.2 s. The PCC voltage, grid current and junction temperature of three power devices (the devices conduct complementary) of the bridge arm A-phase of the power converter are shown in Fig. 16.

It can be seen that after grid fault occurs, the converter exhibits voltage source characteristics due to the GFM control strategy and outputs 1.7 p.u. TOC current. The max junction temperature reaches 125 °C, which means that the GFM converter has reached the maximum output capability under the junction temperature constraint, which is its inherent TOC capability without any enhancement strategy. It is worth noting that in ANPC topology, the junction temperature of high-frequency operating devices T_3 will rise faster due to its high switching frequency, which is also the main constraint on improving the TOC capability of the power converter.

B. Power Loss Evaluation With Switching Frequency Decrease

In order to evaluate the effect of switching frequency decrease on the electrothermal characteristics of the GFM converter in detail, the power loss behavior of GFM converter with switching frequency decrease is evaluated in PLECS simulation platform. The IGBT device is consistent with the experimental test in Section V, and its parameters are derived from the corresponding datasheet. Since the IGBT device T_3 is high-frequency operated and its junction temperature is closest to the upper limit, as shown in Fig. 16. Its conduction loss, switching loss, and total loss are evaluated in detail at different switching frequencies. The results are illustrated in Fig. 17(a), (b), and (c), respectively. In addition, the current ripple increase introduced by switching frequency reduction is also evaluated with the THD of converter side current, as shown in Fig. 17(d).

Since the lowest switching frequency value used in this article is 2.5 kHz, which is still much higher than the resonant frequency of *LC*-filter, and so even after significantly reducing the switching frequency, the fundamental component still accounts for a large proportion of the total converter side current. The impact of the ripple on the power loss is not significant compared with the overrated output current. The conduction loss is mainly related to the current of fundamental frequency and is not significantly affected by the switching frequency, as shown in Fig. 17(a) and

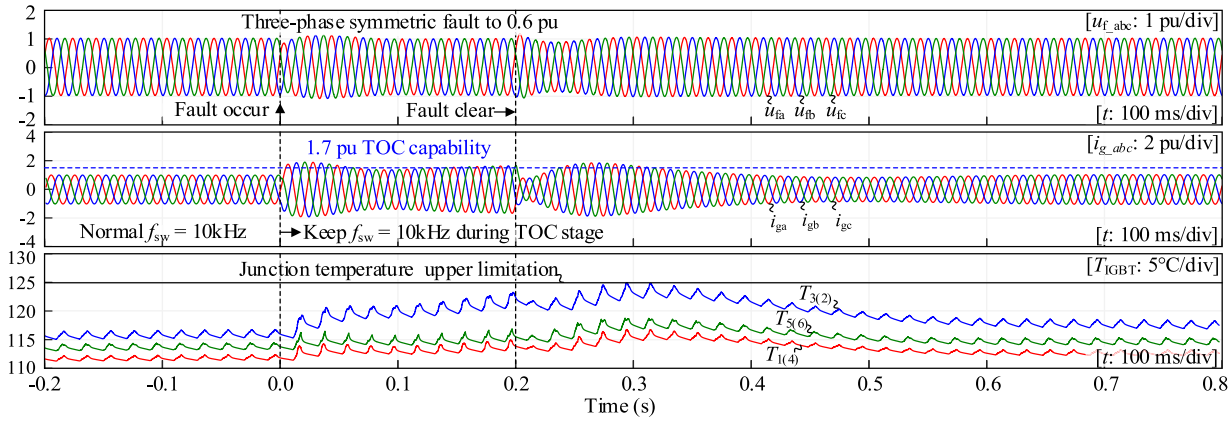

Fig. 16. Electrothermal simulation result of GFM converter under grid fault with fixed switching frequency.

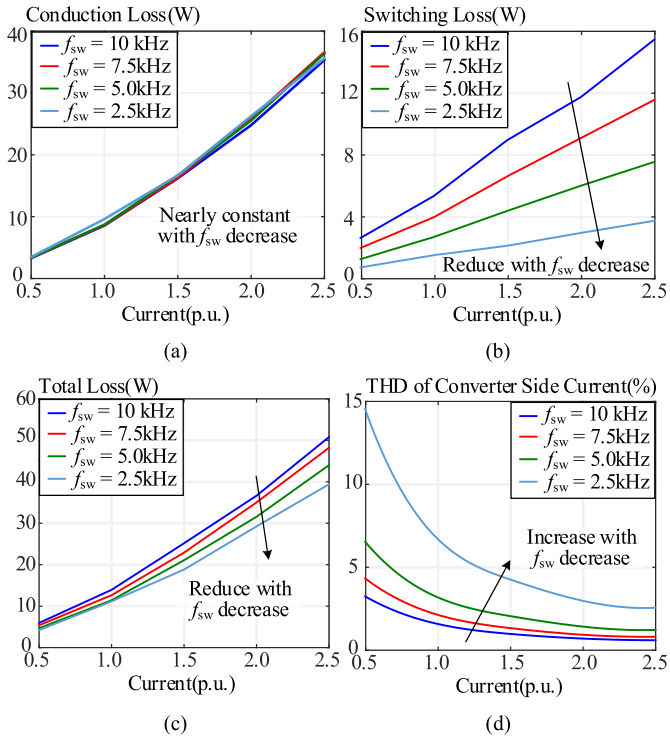

Fig. 17. Simulation result of electrothermal behavior of GFM converter under different switching frequencies and output currents. (a) Conduction loss. (b) Switching loss. (c) Total loss. (d) THD of converter side current.

(d). In this manner, the switching frequency could significantly reduce the switching losses and further reduce the total loss, especially in TOC state, as shown in Fig. 17(b) and (c). It could help the converter tolerate a larger output current without overheating damage to the semiconductor device.

Furthermore, the variation of junction temperature of the high-frequency operating device T_3 at different switching frequencies is also evaluated to demonstrate the necessity of power loss reduction to the TOC capability enhancement, which is shown in Fig. 18. The grid voltage symmetrically drops to the 0.25 p.u. and the GFM converter outputs 2.5 p.u. overrated current at 0.1 s. It can be seen from Fig. 17(c) that the increase of current will

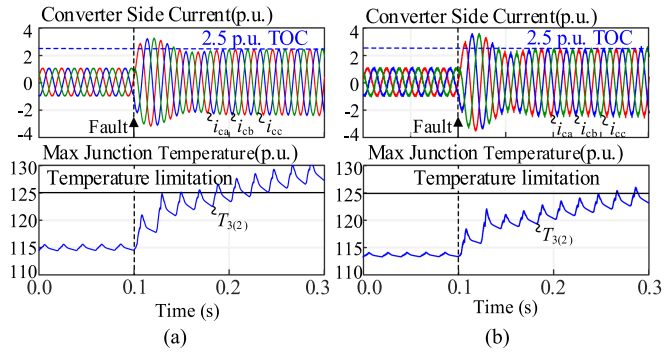

Fig. 18. Simulation result of junction temperature variation during fault. (a) f_{sw} = 10 kHz. (b) f_{sw} = 2.5 kHz.

lead to a doubling of the power loss. Since the thermal response of the device is very fast, the junction temperature will quickly accumulate and exceed the junction temperature limitation in a short time, as shown in Fig. 18(a). When the power loss is reduced appropriately by lowering the switching frequency, the rise in junction temperature will be alleviated, which is shown in Fig. 18(b).

C. Stability Evaluation With Switching Frequency Decrease

In order to verify the theoretical analysis results and the effectiveness and feasibility of the proposed MPCR strategy, the stability performance with fixed controller parameters, adjusted controller with formula (11) and proposed MPCR strategy are tested in this section. The strategy of fixed controller parameters under switching frequency is evaluated first, as shown in Fig. 19. The GFM converter can operate stably at the rated switching frequency of 10 kHz. At 0.2 s, the switching frequency is reduced to 6 kHz, which causes the inner control loop to become unstable, and a high frequency oscillation occurs in voltage and current waveform. This means that the decrease of the switching frequency reduces the stability margin, and the grid-tied GFM converter cannot provide stable voltage support.

Then, the stability performance of adjusting controller with the formula (11) is evaluated in the simulation and the result is

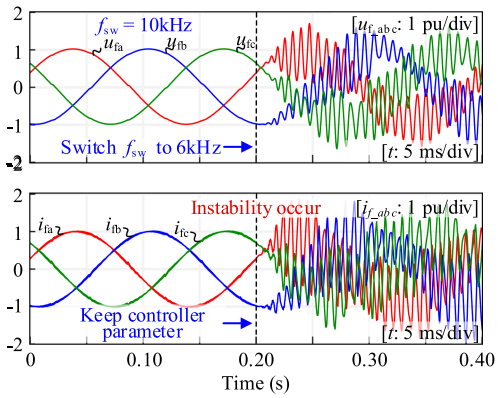

Fig. 19. Simulation result of fixed controller parameters with switching frequency decrease from 10 kHz to 6 kHz.

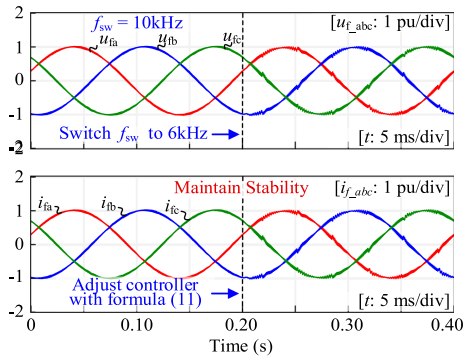

Fig. 20. Simulation result of adjusting controller using formula (11) with switching frequency decrease from 10 kHz to 6 kHz.

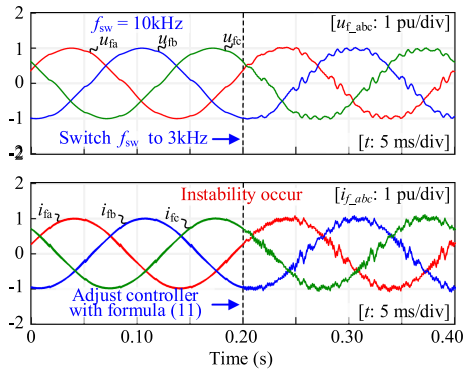

Fig. 21. Simulation result of adjusting controller using formula (11) with switching frequency decrease from 10 kHz to 3 kHz.

shown in Figs. 20 and 21. In Fig. 20, the GFM converter can maintain stable operation at the switching frequency of 6 kHz by adjusting the controller parameters with (11). However, when the switching frequency of GFM converter is further reduced to 3 kHz in Fig. 21, the oscillation occurs again, which means that the stability margin of the inner loop is insufficient in this condition. Although controller gain adjustment can improve stability performance, a suitable adjustment scheme needs to be designed to achieve a wider adjustment range of switching frequency.

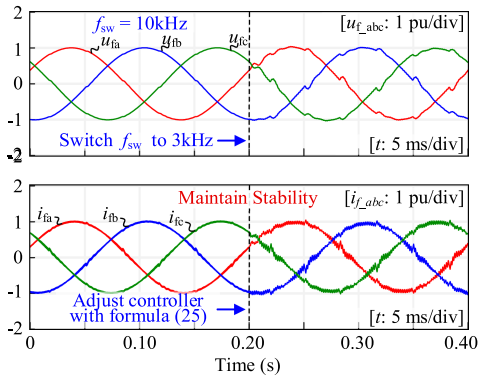

Fig. 22. Simulation result of proposed MPCR strategy with switching frequency decrease from 10 kHz to 3 kHz.

Furthermore, the proposed MPCR strategy is equipped in the inner loop of GFM converter and test in simulation. It can be seen in Fig. 22 that after adopting the proposed control strategy, the GFM converter can still maintain stable operation at switching frequency of 3 kHz. There is no oscillation occurrence in the voltage and current waveform, which means the inner control loop can adapt to a wide range of switching frequency decrease and maintain the stable controlled voltage source characteristics for TOC operation. Thus, the increase in delay introduced by reducing the switching frequency will inevitably weaken the stability performance of the inner loop controller, but a suitable gain configuration strategy can avoid the deterioration of stability performance as much as possible. The simulation results are consistent with theoretical analysis, proving the feasibility of the proposed MPCR scheme.

D. TOC Capability Evaluation With Switching Frequency Decrease Method

On the premise of ensuring the inner voltage vector control loop stability, the TOC capability based on the switching frequency decrease is further evaluated in simulation and shown in Fig. 23. In the simulation, more severe grid fault conditions are set up to test the TOC of the GFM converter.

A symmetrical fault is triggered at 0s with voltage drop to 0.3 p.u. and the fault is cleared at 0.2 s when the grid voltage is set to 1 p.u. If the controller detects a fault through the grid voltage drop and the output current is greater than 1.1 p.u., the switching frequency of the GFM converter will be actively reduced to 2.5 kHz and operated in TOC mode. It is worth noting that the control structure of the GFM converter and the parameters of the outer GFM loop controller will not change. When the junction temperature reaches the limitation temperature, which is 125 °C, the maximum TOC output capability of the GFM converter can reach 2.2 p.u. It has been significantly improved compared with the inherent TOC capability shown in Fig. 16.

In summary, this section uses simulation to evaluate the effect of a large-scale reduction in switching frequency on TOC capability enhancement of GFM converters. And the stability performance of different inner loop operation strategies under

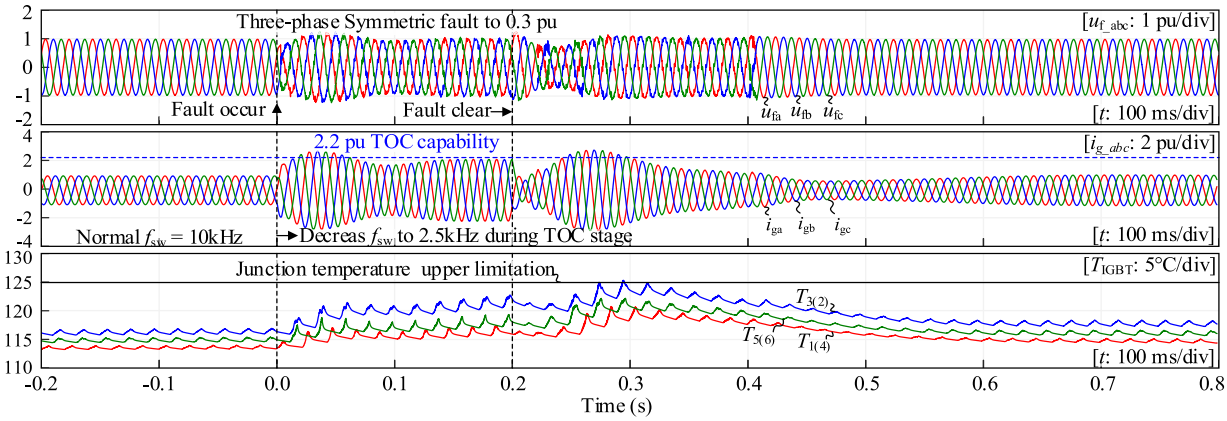

Fig. 23. Electrothermal simulation result of GFM converter under grid fault with reduced switching frequency to 2.5 kHz.

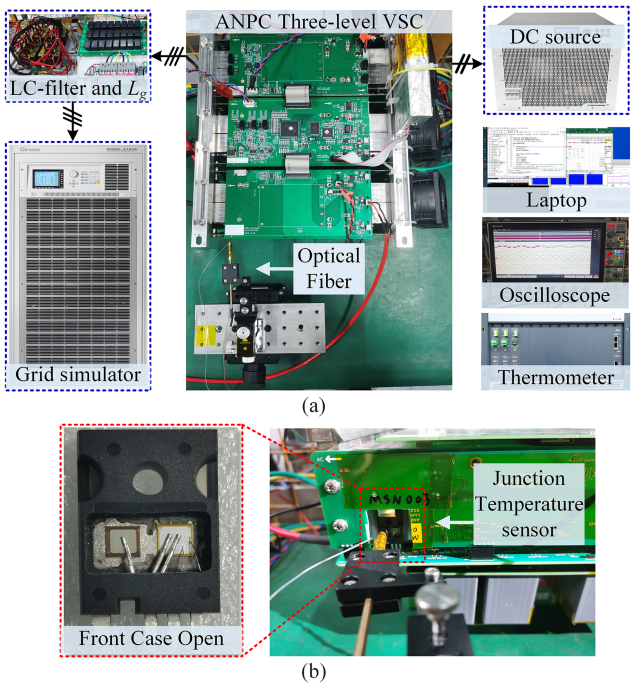

Fig. 24. Experimental setup of grid-connected GFM converter with (a) electrical test platform. (b) Device junction temperature online measurement.

wide range decrease in switching frequency reaches a good agreement with the analysis in Sections II and III.

V. Experimental Results

The feasibility and effectiveness of TOC capability enhancement with switching frequency reduction of GFM converters is further tested in a three-level ANPC topology-based voltage source converter (VSC) platform shown in Fig. 24 with electrical parameters in Table I and control parameters in Table II.

The IGBT devices used in this grid-connected GFM converter test platform is FGHL50T65MQDTL4. The converter with LC-type filter is connected to a grid simulator via the inductance to realize the emulation of inductive transmission line L_g in Fig. 1, and its dc link is kept constant by a dc source. The grid-tied converter platform is controlled by the central controller based on TMS320 F28377D to execute the GFM algorithm using droop control with LPF and verify the strategy proposed in this paper. In order to measure the junction temperature of the power semiconductor device online during the entire process of the GFM converter TOC operation, the front case of the power semiconductor device is opened and the junction temperature is measured through the optical fiber thermometer shown in Fig. 24(b).

A. Experimental Test of Inherent TOC Capability

The inherent TOC capability of the GFM experimental platform is tested in this section at the rated switching frequency of 10 kHz, and the steady-state output current of the converter is set to 35 A. The junction temperature upper limit of the power device is 125 °C, which is same to the simulation. A symmetrical fault is triggered at 0 s with voltage drop to 0.5 p.u. and the grid voltage is recovered to 1 p.u. at 0.2 s. The PCC voltage, grid current and junction temperature are shown in Fig. 25. Due to the IGBT S_3 shown in Fig. 3 is the device with the greatest power loss in this converter due to its high-frequency switching operation mode, the junction temperature of T_3 is focused on during the experiment test.

The steady-state operating junction temperature of T_3 reaches 115 °C, which complies with the common usage of power device. After fault occurs, the GFM converter supports the PCC voltage to around 1 p.u. and outputs 1.5 p.u. current. The max junction temperature reaches 125 °C, which means that the equipment has reached its maximum TOC capability. If the output current is further increased, the IGBT device in test platform may be damaged due to heat accumulation.

B. Stability Test of Switching Frequency Decrease

Furthermore, the stability performance of different inner loop operation strategies under switching frequency decrease is evaluated in the GFM experimental platform. The GFM converter initially runs at the rated switching frequency of 10 kHz. At 0.2 s, the digital controller will trigger the switching frequency to decrease to the lower value actively to evaluate the stability of

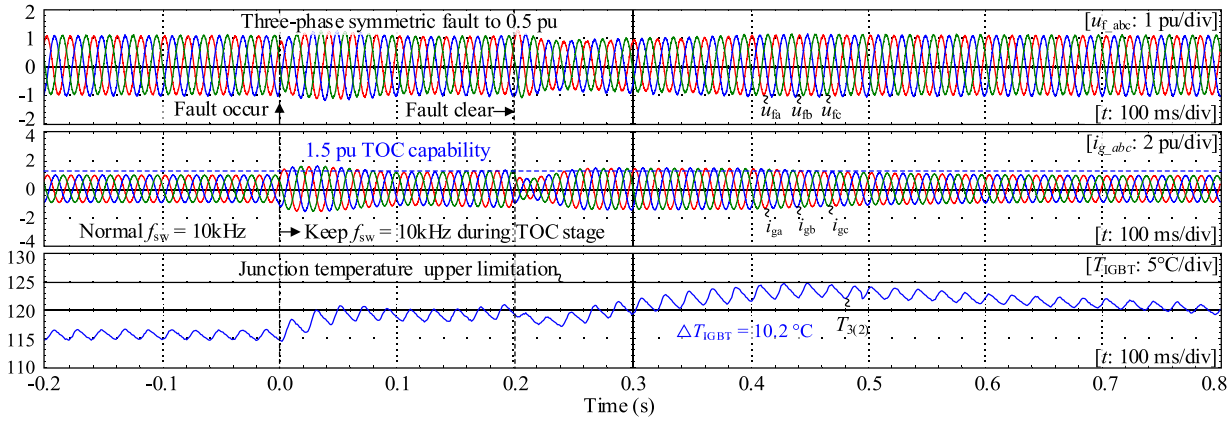

Fig. 25. Electrothermal experimental test result of GFM converter under grid fault with fixed switching frequency.

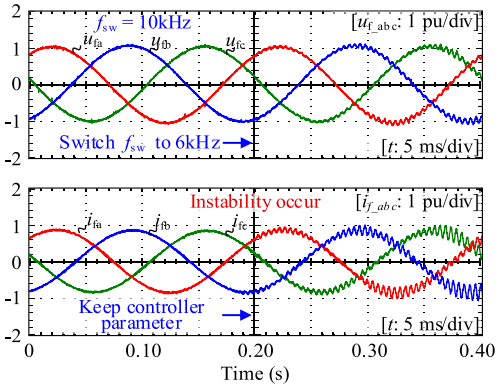

Fig. 26. Experimental test result of fixed controller parameters with switching frequency decrease from 10 kHz to 6 kHz.

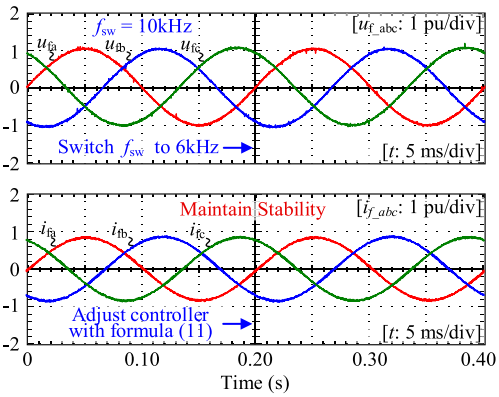

Fig. 27. Experimental test result of adjust controller using Formula (11) with switching frequency decrease from 10 kHz to 6 kHz.

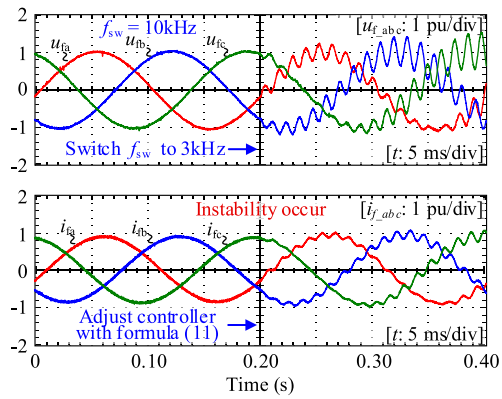

Fig. 28. Experimental test result of adjust controller using Formula (11) with switching frequency decrease from 10 kHz to 3 kHz.

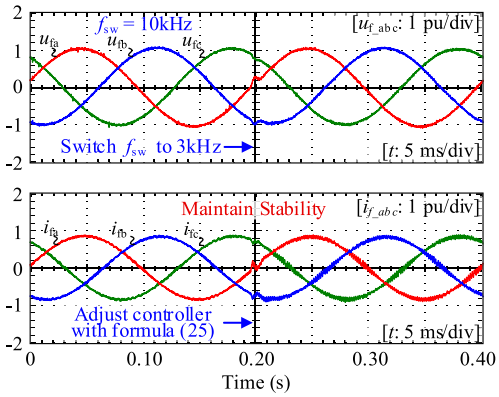

Fig. 29. Experimental test result of proposed MPCR strategy with switching frequency decrease from 10 kHz to 3 kHz.

the inner loop control. Thanks to the superior peripheral and configuration flexibility in digital controllers (TMS320 F28377D is used in the experimental test platform), the seamless transition of the switching frequency from one fixed value to another fixed value can be achieved through the register configuration when entering and exiting the TOC state. Moreover, the digital control algorithm can maintain good synchronization with the switching action of converter with the help of EPWM interrupt in the used digital controller.

The stability performance with fixed controller parameters is tested in Fig. 26 first. With the switching frequency decreasing to 6 kHz, the inner control of GFM converter becomes unstable, and voltage and current oscillations occur, which accords to the simulation result in Fig. 19. It shows that the change in control

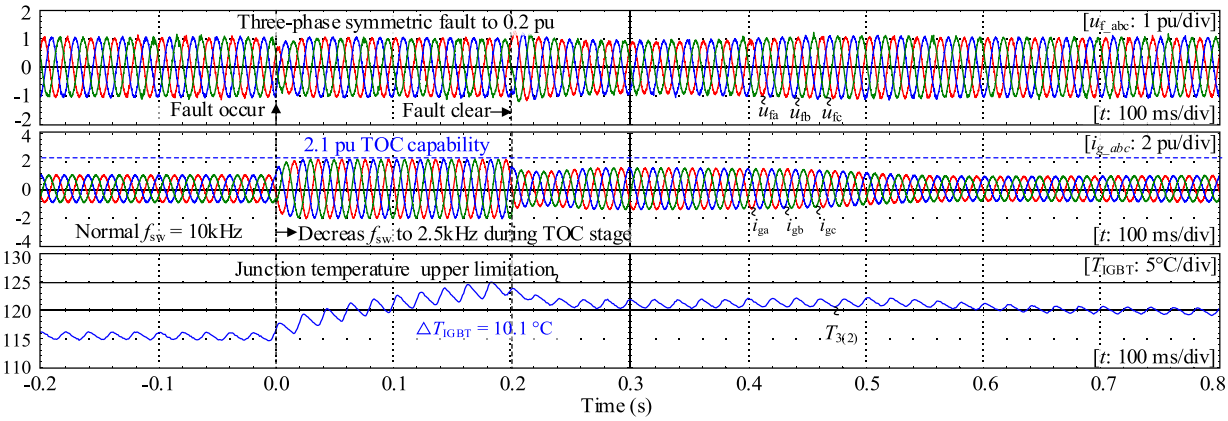

Fig. 30. Electrothermal experimental test result of GFM converter under grid fault with reduced switching frequency to 2.5 kHz.

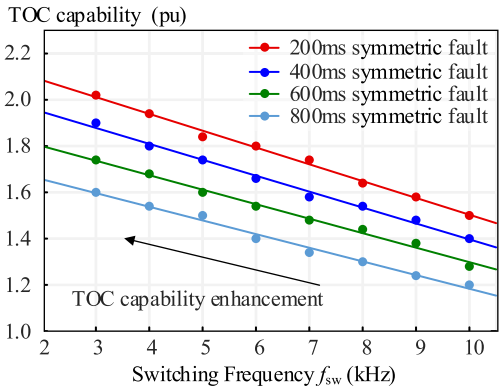

Fig. 31. Switching frequency decrease based TOC capability test result under different fault duration times.

delay caused by the reduction of switching frequency makes the control loop become unstable at low switching frequency. Then, through the adjustment of controller parameter with formula (11), the above stability problem can be solved and illustrated in Fig. 27. However, when the GFM converter changes the switching frequency in a wider range, it cannot work well and the inner loop will become instability again at $f_{sw} = 3$ kHz, which is shown in Fig. 28. The test result is consistent with the simulation result in Figs. 20 and 21.

The performance of the proposed MPCR method was tested in the platform. The switching frequency is the input variable of MPCR strategy, while the gains of voltage controller and current controller are the outputs of this algorithm variable. When the switch command is issued, the controller will update the counter register corresponding to the lower switching frequency, and it will also automatically obtain the corresponding controller parameters through the proposed MPCR algorithm. In the next digital control cycle, the converter will enter the TOC state with a low switching frequency value with its corresponding control parameter calculated from proposed control method. As shown in Fig. 29, when the proposed MPCR scheme is adopted, the GFM converter can control the terminal voltage and output current well in both high and low switching frequency operation states and achieve good switching dynamics. This is consistent with the simulation results in Fig. 22 and demonstrates the effectiveness of the proposed scheme in improving GFM stability under wide range reduction in switching frequency.

C. TOC Capability Test With Switching Frequency Decrease

Based on the implementation of proposed MPCR algorithm through a digital controller to ensure the stability of the experimental prototype, the TOC capability enhancement with switching frequency decrease method is tested in this section on the platform. In the experimental test of TOC capability, the switching frequency is set to 10 kHz during the steady state and changed to 2.5 kHz in the TOC state to maximize the TOC improvement of GFM converter. Therefore, the switching frequency only changes from a fixed value to another fixed value after the converter enters the TOC state when a fault occurs or when the converter exits the TOC state after the fault is cleared. The switching frequency remains constant at 2.5 kHz during TOC state and it does not change over time.

A symmetrical fault is triggered through the grid emulator at 0 s with voltage drop to 0.3 p.u. and the fault is cleared at 0.2 s when the grid voltage is recovered to 1 p.u. The conditions that trigger TOC operation of GFM converter in the experimental test are the same as in the simulation. When the PCC voltage drop is detected and the output current exceeds the set threshold (1.1 p.u.), the converter will actively enter the TOC operation mode and reduce its switching frequency to 2.5 kHz. After entering the TOC operation state, only the inner loop gain changes following the switching frequency, and the control structure and the rest of control parameters do not change. Experimental result is shown in Fig. 30, when the fault occurs, the GFM converter outputs the overload current of 2.1 p.u. to support the PCC voltage to 1 p.u. At the same time, it can be seen that by reducing the switching frequency, the junction temperature can be maintained within 125 °C while outputting a larger overload current compared to its inherent TOC capability shown

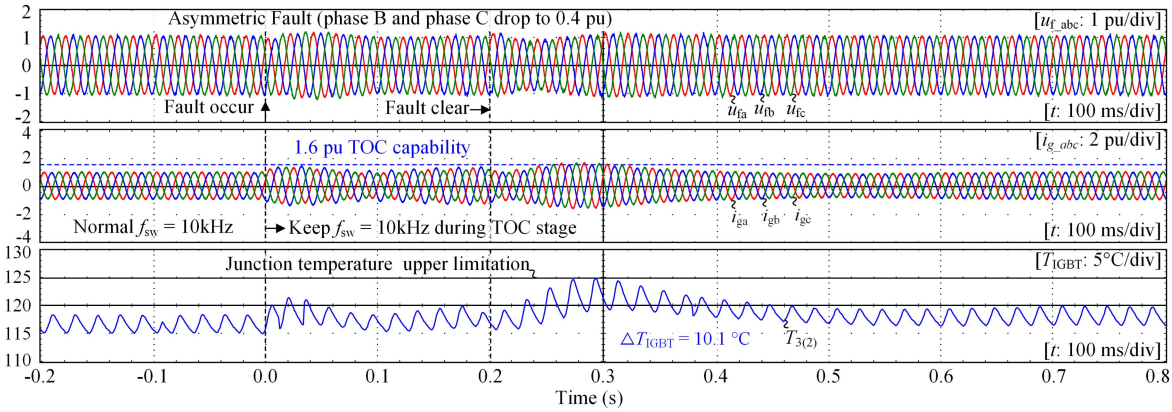

Fig. 32. Electrothermal experimental test result of GFM converter under asymmetric grid fault with fixed switching frequency.

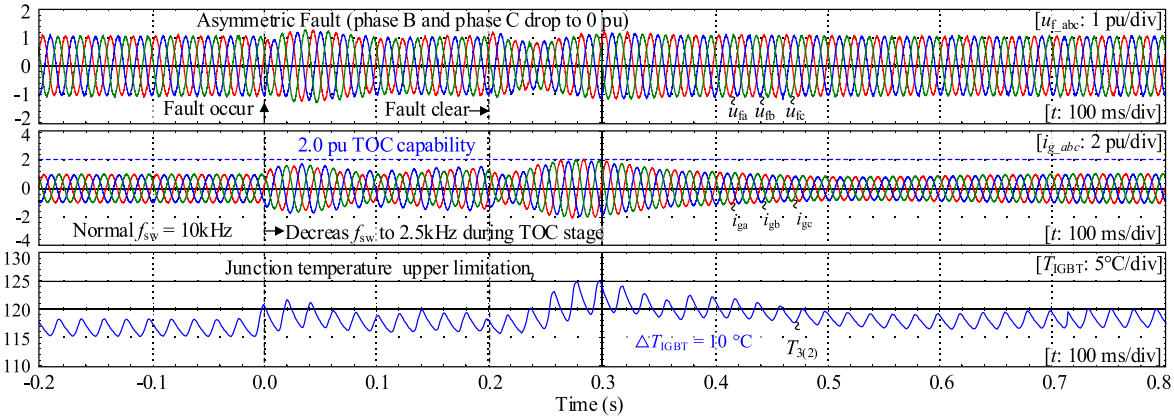

Fig. 33. Electrothermal experimental test result of GFM converter under asymmetric grid fault with reduced switching frequency to 2.5 kHz.

in Fig. 25, which verified the feasibility of switching frequency decrease based TOC capability enhancement.

The detailed testing of the proposed switching frequency reduction strategy for improvement of the TOC capability is further carried out. In this test, the steady-state junction temperature of the GFM converter is set to 115 °C uniformly with the current of 35 A in rms value. To ensure the conservativeness of the TOC capability test of the platform, the converter is set to generate the constant output current through current feedback control like the GFL mode in both normal and fault stages, and this is the worst TOC operating condition of the converter under the same fault duration. On this basis, the symmetrical voltage drop fault experiments are carried out with different fault duration times conducted in this platform. The converter adjusts its output current value to achieve the junction temperature reaching the maximum upper limit during the fault stage, which is set to 125 °C. The test results of the improvement effect of different switching frequency values on TOC capability are shown in Fig. 31.

It can be seen that the longer the fault occurs, the smaller the TOC capability of the power converter is under the junction temperature limitation. This is because the junction temperature did not reach its steady state during the fault time. As the fault duration increases, the power device will continue to heat up and under long-term fault conditions, the maximum current allowed by the converter will be lower. The specific value of TOC capability obtained by reducing the switching frequency is closely related to the semiconductor device thermal behavior, converter power loss characteristics, and grid fault scenarios [28], [29], [33]. However, under a certain electron thermal condition, the methods based on decreasing switching frequency will effectively improve the TOC capability, as shown in Fig. 31.

D. TOC Capability Test Under Asymmetrical Fault Condition

In addition, the TOC capability enhancement with switching frequency decrease method has been tested under the asymmetrical grid fault conditions. The inner control loop of the GFM converter test platform is equipped with PR controller. It replaces the PI controller to enable the control capability of negative sequence voltage and current, and the proposed MPCR strategy is extended and applied to the cascaded dual inner loop control based on the PR controller to enhance the overcurrent capability. In this manner, the GFM converter would have the ability to regulate the positive and negative sequence components at the same time and also hold the TOC capability in asymmetrical fault.

The inherent TOC capability of the GFM experimental platform is tested first with fixed switching frequency of 10 kHz,

and the other settings are the same as the previous test under the symmetrical fault. An asymmetrical fault is triggered at 0 s with the grid voltage of phase B and phase C dropping to 0.4 p.u., and they recover to 1 p.u. at 0.2 s. The PCC voltage, grid current, and junction temperature are shown in Fig. 32. The steady-state operating junction temperature of T_3 reaches 115 °C. After fault occurs, the GFM converter supports the PCC voltage to around 1 p.u. and it maintains three-phase voltage balance. The GFM converter outputs about 1.6 p.u. unbalanced current and the maximum junction temperature reaches 125 °C during the asymmetrical fault, which is close to the device limitation as the previous symmetrical fault test.

The TOC capability enhancement test with reduced switching frequency to 2.5 kHz is further carried out, which is shown in Fig. 33. An asymmetrical fault is triggered at 0 s with grid voltage of phase B and phase C drop deep to 0 p.u. and they are recovered to 1 p.u. at 0.2 s. When the output current of any phase exceeds the set threshold (1.1 p.u.), the converter will actively enter the TOC operation mode and reduce its switching frequency to 2.5 kHz. It can be seen that within the same junction temperature range of 125 °C, the GFM converter can output about 2 p.u. unbalanced overloading current to support the PCC voltage to reach around 1 p.u. and maintain balance. It also verified that the proposed MPCR strategy can be applied in PR controller to maintain control stability under asymmetrical faults and also enhance the overcurrent capability.

In summary, the experiment result of TOC capability with switching frequency decrease method accords well with the simulation in Section IV, and the effectiveness of the proposed MPCR strategy is verified and validated by the theoretical analysis and simulation results.

VI. Conclusion

This article first introduces the technique of switching frequency reduction for the TOC capability enhancement of the GFM converter during the grid fault stage, which would not require any extra customized and oversized hardware design. Then, the inherent stability issue of inner control loops in GFM converters caused by the large range reduction of switching frequency is revealed and investigated quantitively through z-domain modeling. It is found that the stability problem limits the adjustment range of the switching frequency in GFM converters and further restricts the effect of the TOC capability enhancement. On the basis of this, the MPCR strategy for the inner loop controller is further proposed to enhance the stability performance of the cascade inner control under a wide range of switching frequency changes, which ensures the GFM converter exhibits the essential characteristics of stable voltage source during the grid fault transient stage with controlled overcurrent capability. Finally, the feasibility and effectiveness of the proposed TOC strategy have been validated by both time domain simulation and experimental results. This method can achieve 2.1 times TOC capability in 200 ms with switching frequency reduced from 10 kHz to 2.5 kHz, which may provide a promising solution for the TOC capability of GFM converter in software level without any unexpected changes in hardware.

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