Small-Signal Modeling and Loop Analysis of Ultrafast Series Capacitor Trans-Inductor Voltage Regulator With Constant On-Time Control

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***Abstract*—In this article, a comprehensive small-signal model is developed for multiphase series capacitor trans-inductor voltage regulator (SCTLVR) with current mode constant-on time (CM-COT) control. The transfer function of the power stage is thoroughly derived by decoupling the SC structure and the trans-inductor. The modeling of the CMCOT modulator is conducted using the describing function (DF) method, known for its high accuracy, particularly in the high-frequency domain. This method ensures precise prediction and analysis of the dynamic response. To address the demands of ultra-high current applications, the model is extended to accommodate multiple modules, allowing for a detailed closed-loop analysis. Validation through SIMPLIS simulations and experimental results demonstrates the model's accuracy and reliability. The established model provides qualitative guidance on optimally designing the SCTLVR controller under various operating conditions.**

***Index Terms*—Constant on-time (COT), describing function (DF), series capacitor (SC), small-signal model, trans-inductor voltage regulator.**

I. Introduction

With the rapid evolution of artificial intelligence (AI), GPU accelerators feature an outstanding thermal design power, and require efficient, compact, and ultra-fast dynamic response [1], [2], [3]. As the bus voltage of data center motherboards shifts from 12 V to 48 V [4], there is a pressing need for power supplies that can achieve higher voltage step-down ratios while maintaining ultra-fast dynamic response (1000 A/μs) at the load point. However, these new requirements present challenges for conventional Buck converters. A higher voltage step-down ratio results in increased switching stress and losses. In addition, to enhance dynamic response, the number of Buck phases must be increased, leading to larger volume and potential instability.

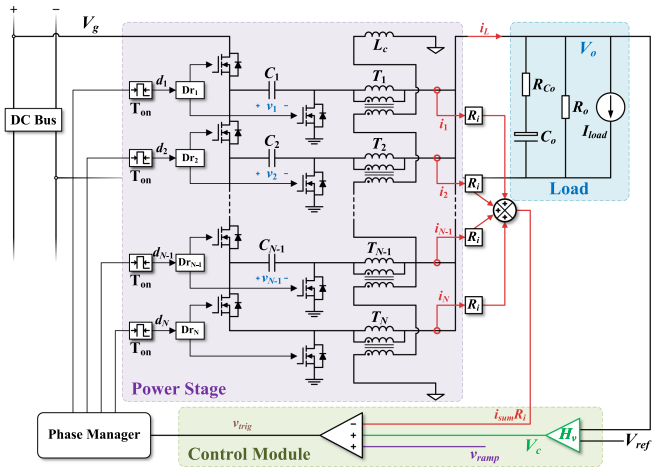

Fig. 1. Schematic of multiphase TLVR with COT control.

In industrial applications, the multiphase series capacitor (SC) Buck converter is an excellent choice, as it extends the voltage step-down ratio and reduces losses [5], [6], [7]. In addition to increasing the number of phases, modifying the traditional inductance structure can also lead to faster dynamic responses. While coupled inductors can enhance performance [8], their design cost and limited scalability restrict their industrial applications. Consequently, the trans-inductor (TL) is being adopted as a replacement for conventional coupled inductors, owing to its superior scalability and comparable dynamic performance [9], [10]. For the control module design, current mode constant on-time (COT) control is widely utilized to enhance dynamic response capabilities, offering ample bandwidth and low switching delays [11], [12]. To address the requirements of 48 V data centers, a multiphase series capacitor trans-inductor voltage regulator (SCTLVR) with COT control is proposed in [13], demonstrating significant application potential. Its structure is illustrated in Fig. 1, and the modulation waveform of COT control interleaved by the phase manager is presented in Fig. 2.

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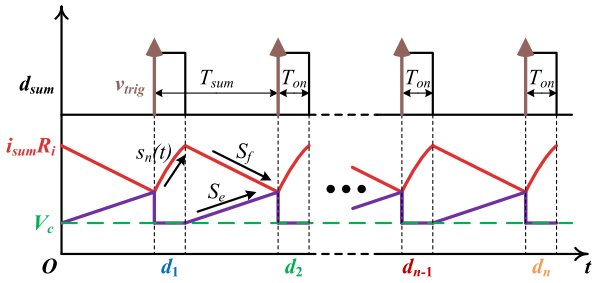

Fig. 2. COT modulation waveform of multiphase SCTLVR at steady state.

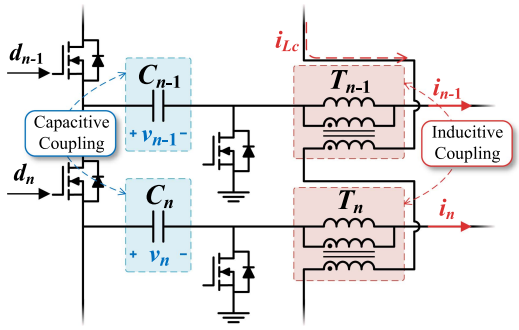

Fig. 3. Phase coupling of multiphase SCTLVR.

Small-signal modeling is a crucial technique in power electronics, providing a quantitative way to analyze, design, and optimize the control parameters. It transforms complex nonlinear behaviors into manageable linear approximations, facilitating an approach to perform the frequency response analysis, stability analysis, and controller optimization.

Various small-signal modeling methods for the ripple-based control structure have been investigated. But the accuracy of current loop modeling may be compromised by the influence of switching frequency sideband components. To increase accuracy at high frequencies, Li [14] used the describing function (DF) method in current mode control modeling , which offers a lighter computational burden and high accuracy. Yan [15] extends Li's model to the unified three-terminal case [15], and Tian [16], [17] incorporated external ramp compensation into this unified model. In [18], based on the DF method, a small signal model of the V^2 COT controlled Buck converter is developed. And it is extended to the capacitor current ramp compensation case [19]. Cheng[20] further refines the small-signal model considering modulation waveform ripples, while Liu [21] accounts for duty cycle-independent quality factors in COT control modeling. Sridhar analyzed [22], [23], [24] the model and stability of the COT and V^2 COT control with phase overlapping. In addition to the DF method, other modeling methods have been explored. In [25], a small-signal model of a multiphase Buck converter is constructed using a harmonic-balance approach. Yan [26] introduced a sampled-data modeling approach for ripple-based control, which is also applied to COT control modeling [27]. Leng [28] proposed an improved average model for the ripple-based switching converter. Cheng [29] combined a genetic algorithm with the modeling process in . Furthermore, Cui and Avestruz [30] presented a new model and design methodology for performing switching cycle event-driven digital control.

In terms of open-loop analysis for the power stage, the small-signal characteristics of SC Buck converters have been investigated using the common-mode and differential-mode methods in [31]. For the output inductor, Chadha [32] analyzed the small signal model of the tapped-inductor. The equivalent models for coupled inductors are constructed in [33], and the nonlinear properties of the inductors are examined in [34]. Xu [35] developed a small-signal model for a multiphase Buck converter using coupled inductors. Zhu [36] discussed the equivalent inductor model for TL.

As shown in Fig. 3, the presence of SCs and TLs leads to an inter-phase coupling within the multiphase SCTLVR system. Consequently, the complexity of the system's frequency response poses significant challenges for direct analysis using conventional analytical techniques. This article is composed mainly to address those challenges. Its main contributions include. 1) A decoupling method is proposed to derive the small-signal model of the SCTLVR power stage. 2) A reduced-order small-signal model of the CMCOT control module is constructed and evaluated, streamlining the dynamic analysis. The enhancement of the system's transient performance by TLs is demonstrated in the frequency domain. 3) A loop analysis is performed, focusing on its stability and load transient response. The derived small-signal models have been verified through both simulation and experimental validation.

The rest of this article is organized as follows. Section II presents the decoupling derivation of the power stage module. Section III introduces the DF method to construct the small-signal model of the entire system. Section IV extends the model to the multimodule case. Loop analysis, stability analysis, and transient analysis are conducted in Section V. The simulation verification is completed in Section VI. Experimental verification using Bode 100 is completed in Section VII. Finally, Section VIII concludes this article.

II. Power Stage Analysis and Modeling

A. Steady-State Analysis

Fig. 1 shows the schematic of the multiphase SCTLVR. The converter features a SC and a multiphase trans-inductor design. The power stage consists of N Buck cells, along with $N-1$ SCs that divide the input voltage. This configuration helps achieve a higher voltage step-down ratio, improving efficiency at the load point. The driver signal for each high-side switch can be defined as a periodic pulse signal d_n with period T_s and frequency f_s. Each driver signal is interleaved by a phase manager with phase difference $d_n = d_{n-1}(t - T_s/N)$, which is equal to $180°/N$. The dc component of d_n is duty ratio D. The overall driver signal d_{sum} can be expressed as the sum of d_n. The period of d_{sum} is $T_{\text{sum}} = T_s/N$. Its dc component in steady state is ND. A SC C_n is interposed between the two Buck units, blocking the dc voltage bias. C_n is assumed to be sufficiently large, maintaining a constant voltage throughout the switching cycle.

Fig. 4 shows the working mode of the n-th phase. Define the voltage across the SC as v_n, where $1 \le n \le N-1$. In Mode

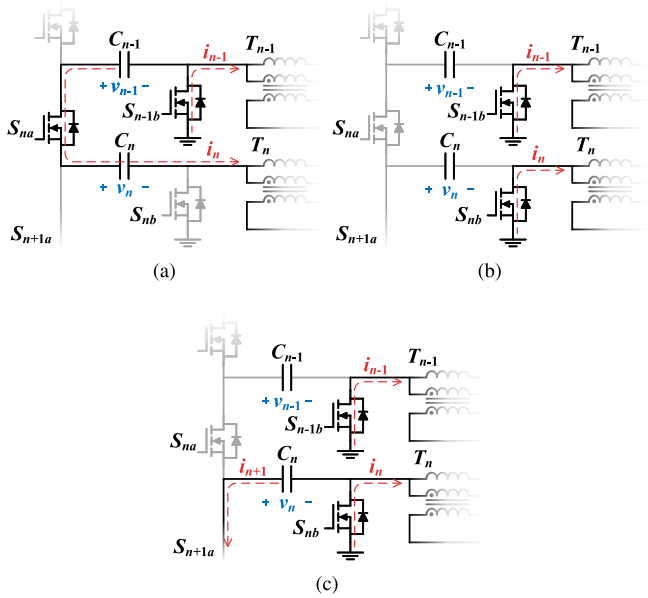

Fig. 4. Equivalent circuit of the n-th phase of multi-phase SC structure in different modes controlled by d. (a) Mode I, S_{na} on, S_{nb} OFF, C_n and is charged by C_{n-1}. (b) Mode II, S_{na} and S_{nb} OFF, the SC voltage v_n is remaining. (c) Mode III, S_{na} OFF, S_{n+1a} ON, C_n is discharged by C_{n+1}.

I, S_{na} and S_{n-1b} are turned ON. i_n is increased and the SC C_n is charged by C_{n-1} through i_n. The voltage across T_n is $(v_{n-1} - v_n) - v_o$. In Mode II, S_{na} is turned OFF, S_{n-1b} and S_{nb} are turned ON. The currents i_{n-1} and i_n freewheel through S_{n-1b} and S_{nb}. There is no current through the SCs. In Mode III, S_{n+1a} and S_{nb} are turned ON. C_n is discharged by C_{n+1} through i_{n+1}. In these two modes, the voltage across T_n is $-v_o$. For the first phase, when S_{1a} turns ON, C_1 is directly charged by v_g. In the last phase, as shown in Fig. 1, there is no SC placed between the two switches. C_{N-1} is connected to T_N without a voltage drop. For clarity, supplementary define that $i_{N+1} = 0$, $v_0 = v_g$ and $v_N = 0$. Assuming that all SCs have equal capacitance C_s, the charging and discharging behavior can be described for the range $1 \le n \le N$ as

$$C_s \frac{dv_n}{dt} = i_n d_n - i_{n+1} d_{n+1}. \tag{1}$$

The voltage across T_n can be expressed as

$$v_{T_n} = (v_{n-1} - v_n) d_n - v_o. \tag{2}$$

The structure of TLs is illustrated in Fig. 5. Compared to the conventional multiphase Buck topology, TLs replace isolated inductors with coupled inductors. All the coupled inductors featuring a 1:1 turns ratio. The secondary windings of all coupled inductors are connected in a series loop, along with a compensation inductor L_c. This configuration electrically couples all output inductors, streamlining the magnetic design and reducing complexity. To simplify the analysis, neglecting the leakage inductance, the current flow through L_m and L_c can be expressed

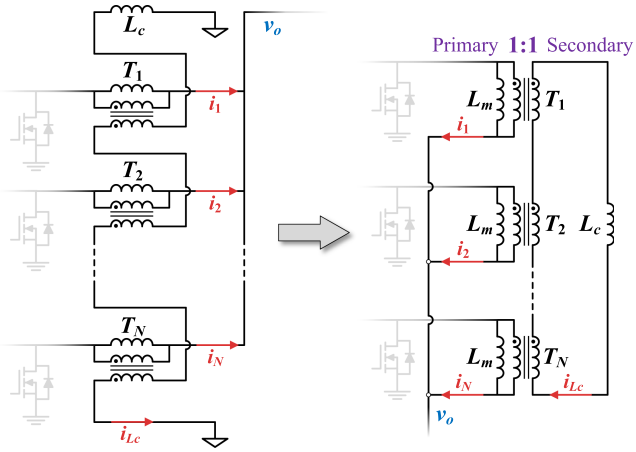

Fig. 5. Electrical simplification of TLs module.

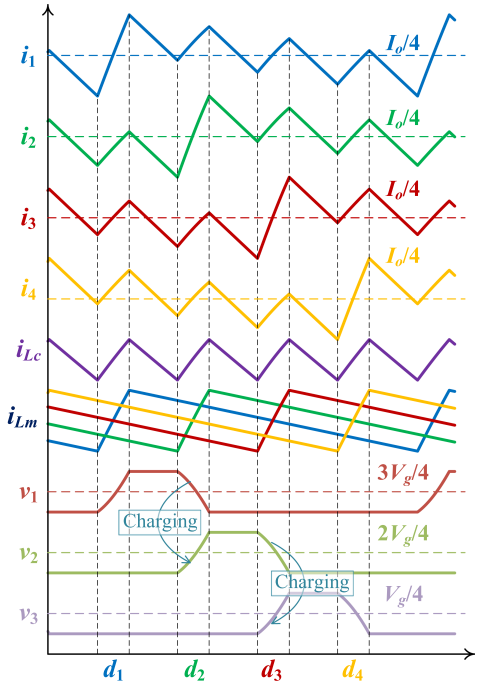

Fig. 6. Critical steady-state waveforms where $N = 4$.

using the basic properties of inductance as follows:

$$\begin{cases} L_m \frac{di_{Lm}^{(n)}}{dt} = v_{T_n} = (v_{n-1} - v_n) d_n - v_o \\ L_c \frac{di_{Lc}}{dt} = \sum_{n=1}^{N} v_{T_n} = \sum_{n=1}^{N} (v_{n-1} - v_n) d_n - N v_o \\ i_n = i_{L_m}^{(n)} + i_{L_c} \end{cases}. \tag{3}$$

The critical waveforms for $N = 4$ case are illustrated in Fig. 6. Suppose the converter is working at steady state, the inductive devices reach volt–second balance. Performing a small ripple approximation for v_n and i_n can get

$$\begin{cases} 0 &= D(I_n - I_{n+1}) \\ 0 &= D(V_{n-1} - V_n) - V_o \end{cases}. \tag{4}$$

Summing both sides of the above equation from 0 to N, the dc components of the converter can be solved as

$$D = \frac{NV_o}{V_g},\ V_{n-1} = \frac{N-(n-1)}{N}V_g,\ I_n = I_{n+1} = \frac{I_o}{N}. \quad (5)$$

B. Coupling Analysis of SC Module

Based on (3), introduce small-signal perturbations for each variable. The small signal state equation can be derived as

$$\begin{cases} sC_s\hat{v}_{n-1} = (D+\hat{d}_n)(I_n+\hat{i}_n - I_{n+1} - \hat{i}_{n+1}) \\ sL_m\hat{i}_{L_m}^{(n)} = (V_g/N + \hat{v}_{n-1} - \hat{v}_n)(D+\hat{d}_n) - (V_o+\hat{v}_o) \\ sL_c\hat{i}_{L_c} = \sum_{n=1}^{N}(V_g/N + \hat{v}_{n-1} \\ \qquad -\hat{v}_n)(D+\hat{d}_n) - N(V_o+\hat{v}_o) \end{cases}. \quad (6)$$

It can be found that the perturbation of each phase's duty ratio $\hat{d}_n$ is equal to the perturbation of the summation: $\hat{d}_n = \hat{d}_{\text{sum}}$. After simplifying, it can be obtained

$$\begin{cases} sC_s\hat{v}_{n-1} = D(\hat{i}_{n-1} - \hat{i}_n) \\ sL_m(\hat{i}_n - \hat{i}_{L_c}) = D(\hat{v}_{n-1} - \hat{v}_n) + \frac{V_g}{N}\hat{d}_{\text{sum}} - \hat{v}_o \\ sL_c\hat{i}_{L_c} = D\hat{v}_g + V_g\hat{d}_{\text{sum}} - N\hat{v}_o \end{cases}. \quad (7)$$

By integrating (7) and neglect the perturbation of input and output, the transfer function from duty ratio to phase current can be obtained as

$$F_{i_n d} = \frac{\hat{i}_n}{\hat{d}_{\text{sum}}} = \frac{\frac{s(NL_m+L_c)C_sV_g}{2ND^2L_c} + \frac{1}{2}[F_{i_{n-1}d} + F_{i_{n+1}d}]}{1+\frac{s^2}{\omega_{sc}^2}} \quad (8)$$

where $\omega_{sc} = D\sqrt{\frac{2}{L_mC_s}}$. a resonance phenomenon can be observed during the process of the automatic phase current balancing, affected by the front and rear phases. However, based on the expression for ω_{sc}, the secondary loop of the TLs module is not affected by this resonance due to common-mode cancellation on i_{L_c}. Therefore, focusing solely on the common-mode parameters is essential for establishing a decoupled small-signal model.

C. Small-Signal Decoupling of Power Stage

The TLs module of the converter can be simplified as shown in Fig. 5. Based on the T-shape model for the transformer, considering the leakage inductance, the TLs topology can be further equated, as shown in Fig. 7, where the current flow through the secondary side bridge of each phase and compensating inductor L_c. Define the secondary bridge current as i_{L_c}, and utilize Kirchhoff's laws for each phase of the primary side, the relationship can be expressed as

$$v_{T_n} - L_m\frac{d(i_n+i_{L_c})}{dt} - L_k\frac{di_n}{dt} = 0. \quad (9)$$

Summing up (9) from 0 to N can get

$$\sum_{n=1}^{N} v_{T_n} - (L_m+L_k)\frac{di_{\text{sum}}}{dt} - NL_m\frac{di_{L_c}}{dt} = 0. \quad (10)$$

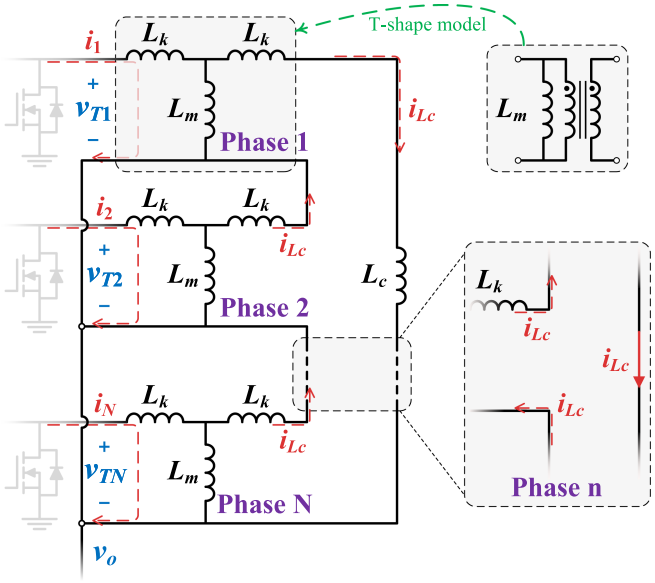

Fig. 7. Electrical equivalent of TLs module with T-shape model for the transformer.

For the secondary side, also utilize Kirchhoff's laws, the relationship can be expressed as

$$\sum_{n=1}^{N}\left[L_m\frac{d(i_n+i_{L_c})}{dt} + L_k\frac{di_{L_c}}{dt}\right] + L_c\frac{di_{L_c}}{dt} = 0$$

$$\Rightarrow L_m\frac{di_{\text{sum}}}{dt} + [N(L_m+L_k)+L_c]\frac{di_{L_c}}{dt} = 0. \quad (11)$$

Combing (9) and (11), the relationship between v_n, v_o, d_n, and i_{sum} can be expressed as

$$\tilde{L}_{\text{eq}}\frac{di_{\text{sum}}}{dt} = \sum_{n=1}^{N}(v_{n-1}-v_n)d_n - Nv_o \quad (12)$$

where $\tilde{L}_{\text{eq}}$ is defined as

$$\tilde{L}_{\text{eq}} \doteq \frac{NL_k{}^2 + 2NL_mL_k + L_mL_c + L_cL_k}{N(L_m+L_k)+L_c}. \quad (13)$$

Define P as the number of interleaving phases. And $\kappa = \frac{L_m}{L_k}$, $\beta = \frac{L_m}{L_c}$. $\tilde{L}_{\text{eq}}$ can be expressed as

$$\tilde{L}_{\text{eq}} = L_m\frac{P(2\kappa+1)\beta + \kappa(\kappa+1)}{P\kappa(\kappa+1)\beta + \kappa^2}. \quad (14)$$

In topology design, κ is only determined by the structure of the coupled inductance. Consider $\kappa = 40$, the ratio of $\tilde{L}_{\text{eq}}$ to L_m for TLs with the impact of β and phase number is shown in Fig. 8. It can be observed that as P and β increase, their impact on the ratio gradually decreases.

Same as (6), introduce small-signal perturbations for each variable. Eliminating dc components and high-order small-signal components, and turning into frequency domain, the equation can be simplified as

$$s\tilde{L}_{\text{eq}}\hat{i}_{\text{sum}} = V_g\hat{d}_{\text{sum}} + D\hat{v}_g - N\hat{v}_o. \quad (15)$$

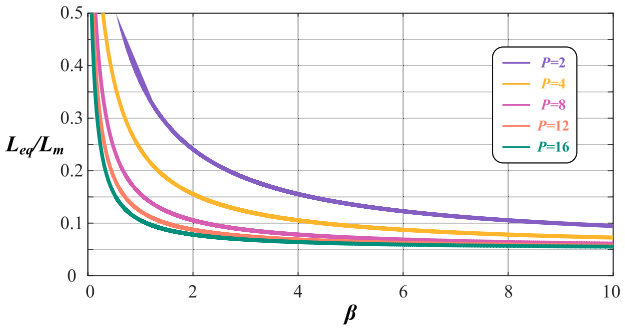

Fig. 8. Ratio of $\tilde{L}_{\text{eq}}$ to L_m for TLs with the impact of β and phase number.

Let $\hat{v}_g = \hat{v}_o = 0$, we can get the transfer function from duty ratio to total current F_{id} as

$$F_{id}(s) = \frac{\hat{i}_{\text{sum}}}{\hat{d}_{\text{sum}}} = \frac{V_g}{s\tilde{L}_{\text{eq}}}. \tag{16}$$

In the output resistance and load module, the small signal relationship can be expressed as

$$\hat{v}_o = [\hat{i}_{\text{sum}} - \hat{i}_{\text{load}}]\frac{R_o(1 + sR_{C_o}C_o)}{1 + s(R_o + R_{C_o})C_o}. \tag{17}$$

Let $\hat{i}_{\text{load}} = 0$, we can get the open loop output resistance Z_{RC} as

$$Z_{\text{RC}}(s) = \frac{1}{Y_{\text{RC}}(s)} = \frac{\hat{v}_o}{\hat{i}_{\text{sum}}} = \frac{R_o(1 + sR_{C_o}C_o)}{1 + s(R_o + R_{C_o})C_o}. \tag{18}$$

The coupling of the SCs is cancelled out through the superposition of differential mode quantities, which also decouples the TLs. By considering the power stage as a whole, the decoupling model of the power stage is derived. To construct the small signal model of the entire control system, the closed-loop transfer function of the current loop will be derived by DF method in the following section.

III. Modeling of COT Control Module

To mitigate the impact of switching frequency side-band components in the current loop and to establish an accurate small-signal model of the COT control module, the describe function (DF) method is employed [14]. As depicted in Fig. 9, the power stage module of the converter is abstracted as a feedback system with input variables v_g, d_{sum}, v_o, and output variable i_{sum}. The switching frequency per phase is f_s, and the period is T_s. For N phases interleaving condition, the frequency of i_{sum} is Nf_s, and the period is $T_{\text{sum}} = T_s/N$. The current is sensed from the overall inductor current by resistance R_i. Based on (12), the rising slew rate and the falling slew rate of the sensing current can be expressed as follows:

$$s_{\text{on}}(t) = R_i\frac{(v_{n-1} - v_n) - Nv_o}{\tilde{L}_{\text{eq}}}$$

$$s_f(t) = R_i\frac{Nv_o}{\tilde{L}_{\text{eq}}}. \tag{19}$$

Suppose that v_g and v_o remain constant, a sinusoidal signal with magnitude $\hat{v}_c$ and frequency f_p is injected into the control signal

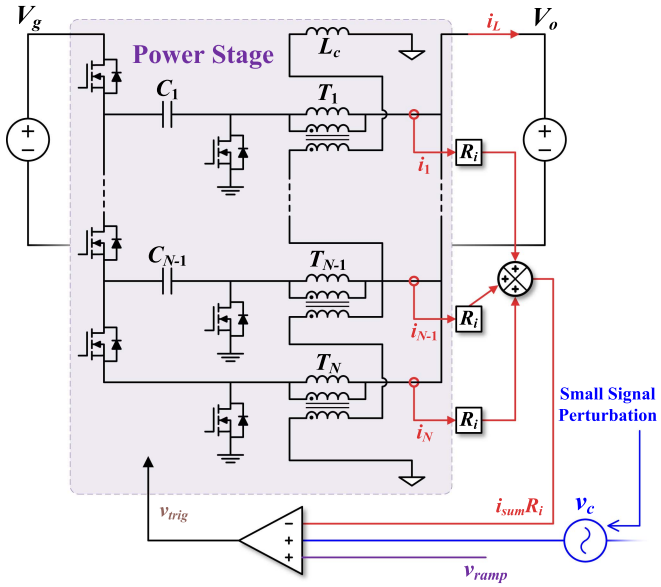

Fig. 9. DF modeling for control-to-duty ratio transfer function.

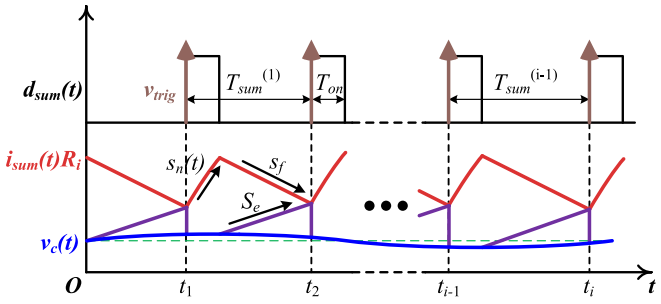

Fig. 10. Typical waveforms with perturbation injected into the control signal.

v_c, resulting in the perturbed waveform shown in Fig. 10. v_c can be expressed as

$$v_c(t) = V_c + \hat{v}_c\sin(2\pi f_p t - \theta). \tag{20}$$

Suppose that $T_{\text{sum}}^{(i)}$ is the turn OFF time of the ith period. And $T_{\text{sum}}^{(i)} = t_i - t_{i-1} = T_{\text{sum}} + \Delta T_{\text{sum}}^{(i)}$. From the control principle of COT control, combing with Fig. 10 can get

$$v_c(t)\Big|_{t_i}^{t_{i-1}} = S_f\Delta T_{\text{sum}}^{(i-1)} + S_e(\Delta T_{\text{sum}}^{(i-1)} - \Delta T_{\text{sum}}^{(i-2)}) \tag{21}$$

where $Qf_p = Nf_s, NT_p = QT_{\text{sw}}$. From this equation, the relationship between t_i and v_c can be extracted as

$$\begin{aligned} &S_f\Delta T_{\text{sum}}^{(i-1)} + S_e(\Delta T_{\text{sum}}^{(i-1)} - \Delta T_{\text{sum}}^{(i-2)}) \\ &\approx -2\hat{v}_c\cos[\pi f_p(2i-1)T_{\text{sum}} - \theta]\sin[\pi f_p T_{\text{sum}}]. \end{aligned} \tag{22}$$

Accordingly, the expression of perturbed trigger signal v_{trig} can be expressed by t_i as $v_{\text{trig}} = \sum_{i=1}^{\infty}\delta(t - t_i)$. The driver signal is produced by the T_{on} generator, which is triggered by the trigger signal. According to the principle of COT control, the gate driver signal can be expressed as $d_{\text{sum}} = \int_0^{\infty}[\delta_{\text{sum}}(t) - \delta_{\text{sum}}(t - T_{\text{on}})]dt$. Hence, the frequency-domain expression of d_{sum} can be derived based on Fourier analysis. The Fourier coefficient of the

perturbation frequency c_d can be extracted as

$$\begin{aligned} c_d &= \frac{1}{T_p}\int_0^{T_p} d_{\text{sum}} e^{-j2\pi f_p t} dt \\ &= j\frac{1}{2\pi}(1-e^{-j2\pi f_p T_{\text{on}}})\sum_{i=0}^{Q} e^{-j2\pi f_p t_i} \\ &\approx f_p(1-e^{-j2\pi f_p T_{\text{on}}})\sum_{i=0}^{Q} e^{-j2\pi f_p i T_{\text{sum}}} \sum_{k=1}^{i} \Delta T_{\text{sum}}^{(k)}. \end{aligned} \tag{23}$$

Combine (22), c_d can be simplified as

$$c_d = -j\frac{\hat{v}_c}{2}\frac{N f_s(1-e^{-j2\pi f_p T_{\text{on}}})}{S_f + S_e(1-e^{-j2\pi f_p T_{\text{sum}}})} e^{-j\theta}. \tag{24}$$

For the sinusoidal perturbation $v_c(t)$, its Fourier coefficient on f_p can be expressed as

$$c_{v_c} = \frac{1}{T_p}\int_0^{T_p} \hat{v}_c \sin(2\pi f_p t - \theta) e^{-j2\pi f_p t} dt = -j\frac{\hat{v}_c}{2} e^{-j\theta}. \tag{25}$$

According to the mathematical relationship between c_d and c_{v_c}, the transfer function from control signal to trigger signal can be expressed in frequency domain

$$F_m(s) = \frac{\hat{d}_{\text{sum}}}{\hat{v}_c} = \frac{c_d}{c_{v_c}} = \frac{N f_s(1-e^{-sT_{\text{on}}})}{S_f + S_e(1-e^{-sT_s/N})}. \tag{26}$$

Combining with the previous derivation on the transfer function of the power stage and utilizing Padé approximation, the transfer function from control signal to inductor current F_i can be derived

$$F_i(s) = \frac{\hat{i}_{\text{sum}}}{\hat{v}_c} = F_m \cdot F_{id} \approx \frac{1}{R_i}\frac{(1+s/\omega_{z_0})}{(1+s/\omega_{p_0})}\frac{1}{\text{den}(s)}. \tag{27}$$

Define $E = S_e/S_f$, the pole and zero can be expressed as

$$\begin{aligned} \omega_{z_0} &= 2N f_s, \quad \omega_{p_0} = \frac{2N f_s}{1+2E} \\ \text{den}(s) &= 1 + \frac{s}{Q_0\omega_0} + \frac{s^2}{{\omega_0}^2} \end{aligned} \tag{28}$$

where $Q_0 = 2/\pi$, $\omega_0 = \pi/T_{\text{on}}$.

For the input port, suppose that v_c and v_o remain constant, introduce sinusoidal perturbation signal:

$$v_g(t) = V_g + \hat{v}_g \sin(2\pi f_p t - \theta) \tag{29}$$

as shown in Fig. 11, based on (15), during the process of small-signal modeling, the perturbation across SC v_n can be approximated as $(N-n)v_g/N$. Accordingly, the relationship between t_i and v_g can be expressed as

$$\begin{aligned} &\int_{t_i}^{t_i+T_{\text{on}}} R_i \frac{v_{i-1}-v_i}{\tilde{L}_{eaq}} dt \approx \int_{t_i}^{t_i+T_{\text{on}}} R_i \frac{v_g(t)/N}{\tilde{L}_{\text{eq}}} dt \\ &= S_f T_{\text{sum}}^{(i)} + S_e(\Delta T_{\text{sum}}^{(i)} - \Delta T_{\text{sum}}^{(i-1)}). \end{aligned} \tag{30}$$

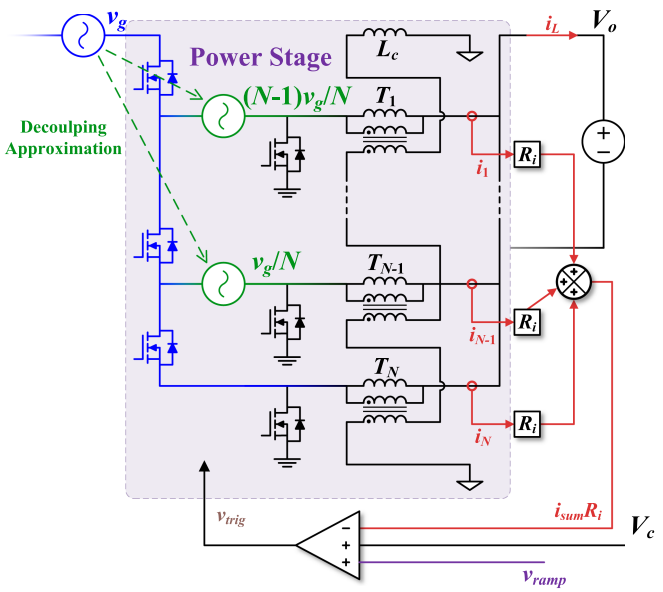

Fig. 11. DF modeling for input-to-control transfer function with approximate equivalent perturbation.

Same as the derivation of F_m, the transfer function from input to duty ratio can be derived

$$\begin{aligned} \frac{\hat{d}_{\text{sum}}(s)}{\hat{v}_g(s)} &= -\frac{1-e^{sT_{\text{on}}}}{1-e^{sT_s/N}}\frac{f_s(1-e^{-sT_{\text{on}}})}{S_f + S_e(1-e^{-sT_s/N})}\frac{R_i}{s\tilde{L}_{\text{eq}}} \\ &\quad + \frac{f_s T_{\text{on}}}{V_g} \approx \frac{T_{\text{on}} R_i(1+2E)}{2N\tilde{L}_{\text{eq}}} F_m. \end{aligned} \tag{31}$$

Similarly, the transfer function from output to duty ratio can be derived by injecting the perturbation signal into the output voltage

$$\begin{aligned} \frac{\hat{d}_{\text{sum}}(s)}{\hat{v}_o(s)} &= \frac{N f_s(1-e^{-sT_{\text{on}}})}{S_f + S_e(1-e^{-sT_s/N})}\frac{R_i}{s\tilde{L}_{\text{eq}}} - \frac{N}{V_g} \\ &\approx -\frac{N T_{\text{on}} R_i(1+2E/D)}{2\tilde{L}_{\text{eq}}} F_m. \end{aligned} \tag{32}$$

Then the input-to-control transfer function F_g and the output-to-control transfer function F_v can be derived, respectively:

$$F_g(s) = \frac{\hat{v}_c}{\hat{v}_g} = \frac{T_{\text{on}} R_i(1+2E)}{2N\tilde{L}_{\text{eq}}} \tag{33}$$

$$F_v(s) = \frac{\hat{v}_c}{\hat{v}_o} = \frac{R_i(N T_{\text{on}} + 2E/f_s)}{2\tilde{L}_{\text{eq}}}. \tag{34}$$

The feedback system can be expressed as a block diagram shown in Fig. 12. By the block diagram, with the feedback theorem, The current loop closed-loop transfer function from control signal to output G_{vc} can be derived as follows:

$$\begin{aligned} G_{\text{vc}}(s) &= \frac{\hat{v}_o}{\hat{v}_c} = \frac{F_i Z_{\text{RC}}}{1+T_i} = \frac{F_i}{Y_{\text{RC}} + F_v F_i} \\ &\approx G_{c0}\frac{(1+s/\omega_{z_0})}{(1+s/\omega_{p_0})}\frac{(1+s/\omega_{z_1})}{(1+s/\omega_{p_1})}\frac{1}{\text{den}(s)} \end{aligned} \tag{35}$$

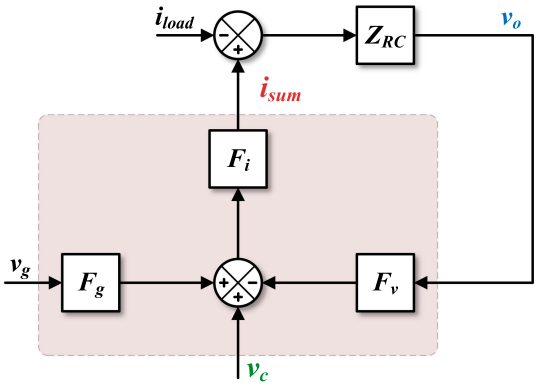

Fig. 12. Small signal block diagram of SC TLVR with COT control (Without voltage loop).

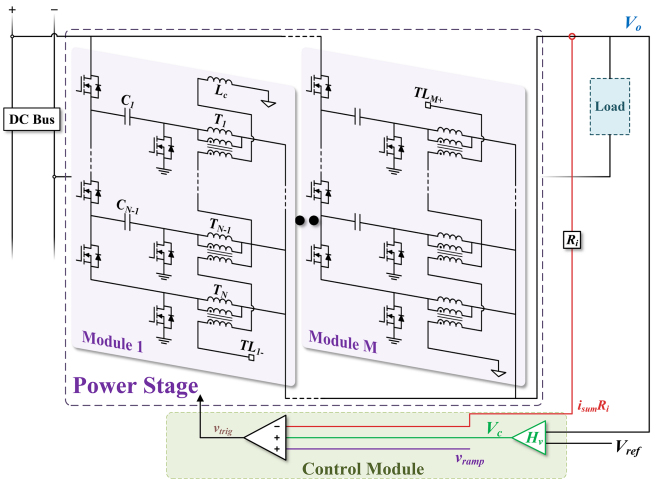

Fig. 13. Schematic of multimodule SCTLVR with COT control.

where G_{c0}, ω_{z_1}, and ω_{p_1} can be simplified as follows:

$$G_{c0} = \frac{R_o}{R_i + F_v R_o}, \quad \omega_{z_1} = \frac{1}{R_{C_o} C_o}$$
$$\omega_{p_1} = \frac{R_i + F_v R_o}{(R_o + R_{C_o}) R_i C_o + F_v R_o R_{C_o} C_o}. \tag{36}$$

IV. Extension to Multimodule Case

To adapt to high load current and fast dynamic demands in data center applications, the SC topology can be designed as a multimodule structure shown in Fig. 13. The small signal modeling also needs to consider this condition. Suppose the multimodule structure has M modules and each module has N phases. For the TL module, the end node of each module is connected with the initial node of the next module, which couples all MN phases. Similar to the analysis in Sections II and III, the equivalent inductance for each module $\tilde{L}_{\text{eq}}$ can be derived by substituting $P = MN$. Suppose the gate driver signal for the multimodule case is fully interleaved, the phase difference between each module is T_s/M. So, the frequency of the overall output current is M times the frequency for each module. Since

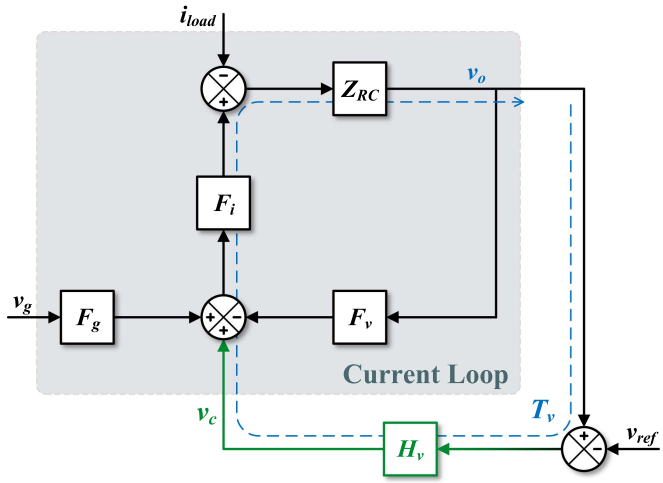

Fig. 14. Closed-loop block diagram of SCTLVR with COT control.

all modules are paralleled, the slew rate of the overall inductor sensing current can be expressed separately as

$$s_{\text{on\_}M}(t) \approx R_i \frac{v_g/N - MNv_o}{\tilde{L}_{\text{eq}}} = R_i \frac{(v_g/M)/N - (Nv_o)}{(\tilde{L}_{\text{eq}}/M)}$$
$$s_{f\_M}(t) = R_i \frac{MNv_o}{\tilde{L}_{\text{eq}}} = R_i \frac{Nv_o}{(\tilde{L}_{\text{eq}}/M)}. \tag{37}$$

The derivation of the transfer function within the control module is mainly based on the slew rate. Consequently, by the multiphase equivalent analysis in [17], the equivalent value can be expressed as

$$\tilde{L}_{\text{eq\_}M} = L_m \frac{P(2\kappa+1)\beta + \kappa(\kappa+1)}{M[P\kappa(\kappa+1)\beta + \kappa^2]}$$
$$f_{s\_M} = Mf_s, \quad v_{g\_M} = \frac{v_g}{M}. \tag{38}$$

For the input-to-output transfer function, as slew rate $s_{\text{on\_}M}$ shown in (37), the input voltage should consider additional linear factor $1/M$. Therefore, the dc gain can be expressed as $G_{g0\_M} = G_{g0}/M$. Hence the model for the multimodule case can be derived by substituting the above equivalent values into the single case.

When $N = 1$, the topology simplifies to an M-phase TLVR without SCs. The extended model remains applicable to this configuration.

V. Loop Analysis

A. Closed-Loop Transfer Function

In practical applications, to enhance the steady-state and transient performance of the system, the compensation of the voltage loop is necessary. Therefore, a comprehensive model must incorporate the voltage loop. The small signal block diagram of the overall system is illustrated in Fig. 14. And the compensation gain is H_v. With the feedback theorem, the voltage loop gain T_v

can be expressed as

$$T_v(s) = H_v G_{vc}. \tag{39}$$

The system has three input small signal variables: $\hat{v}_{\text{ref}}$, $\hat{v}_g$ and $\hat{i}_{\text{load}}$. Based on the feedback theorem, the closed-loop transfer function from reference voltage to output G_{vr} can be easily calculated:

$$G_{vr}(s) = \frac{\hat{v}_o}{\hat{v}_{\text{ref}}}\bigg|_{\hat{v}_g=\hat{i}_{\text{load}}=0} = \frac{T_v}{1+T_v}. \tag{40}$$

Since the DF modeling method treats the current control module and power stage as a cohesive unit, there are no alternative small-signal conduction paths from input to output. Therefore, the closed-loop analysis is more concise. The power supply rejection ratio (PSRR) can be calculated as follows:

$$\begin{aligned}\text{PSRR}(s) &= \frac{\hat{v}_o}{\hat{v}_g}\bigg|_{\hat{v}_{\text{ref}}=\hat{i}_{\text{load}}=0} = \frac{1}{1+T_v}\frac{F_g F_i Z_{\text{RC}}}{1+F_v F_i Z_{\text{RC}}} \\ &= \frac{F_g F_i}{(Y_{\text{RC}}+F_v F_i)(1+T_v)}.\end{aligned} \tag{41}$$

Similarly, the equivalent output impedance can be calculated as follows:

$$\begin{aligned}Z_{\text{out}}(s) &= \frac{\hat{v}_o}{-\hat{i}_{\text{load}}}\bigg|_{\hat{v}_{\text{ref}}=\hat{v}_g=0} = \frac{1}{1+T_v}\frac{Z_{\text{RC}}}{1+F_v F_i Z_{\text{RC}}} \\ &= \frac{1}{(Y_{\text{RC}}+F_v F_i)(1+T_v)}.\end{aligned} \tag{42}$$

B. Stability Analysis

The stability of a closed-loop system can be predicted by analyzing the open-loop transfer function. According to the discussions in Section IV, the poles and zeros of the open-loop transfer function G_{vc} can be easily expressed. The two zeros ω_{z0} and ω_{z1}, along with the quadratic pole ω_0 are only influenced by duty ratio, switching frequency, and load. These poles and zeros consistently remain in the negative real plane. Since $S_f = R_i P V_o / \tilde{L}_{\text{eq}}$, if S_e remains constant, the parameter E will vary with $\tilde{L}_{\text{eq}}$. Consequently, the two poles ω_{p0} and ω_{p1} shift with changes in the parameter β. To illustrate the stability, consider a typical COT control SCTLVR system with following parameters: $D = 0.1$, $V_o = 1.2$ V, $L_m = 200$ nH, $f_s = 500$ kHz, $M = 2$, and $N = 4$. The ramp compensation is set to $S_e = 1.2$ V/μs, which ensures that when $\beta = 0$, $E = 5$. The pole-zero plot of the open-loop transfer function G_{vc} is shown in Fig. 15, illustrating how, as β increases, the poles ω_{p0} and ω_{p1} are pushed further to the left in the complex plane, eventually converging towards the zeros ω_{z0} and ω_{z1}. Thus, all poles and zeros of the open-loop transfer function remain negative.

Furthermore, the Nyquist plot of G_{vc}, depicted in Fig. 16, shows that as β increases, the Nyquist curve does not encircle the critical point $(-1, 0)$. Based on the Nyquist stability criterion, this indicates that provided the system is stable when $\beta = 0$, the closed-loop system remains stable, and the phase margin improves as β increases.

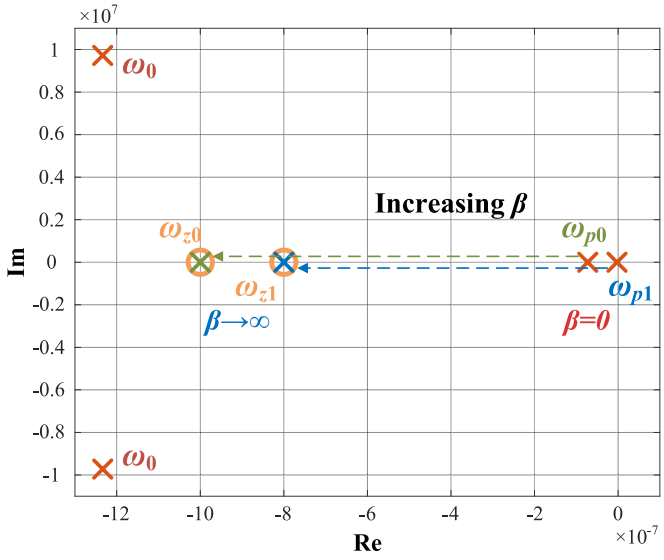

Fig. 15. Poleâzero map of control-to-output transfer function G_{vc} with increasing β.

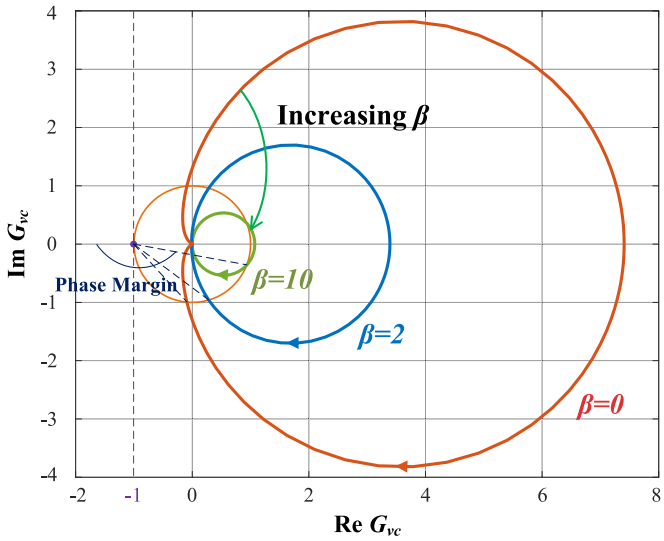

Fig. 16. Nyquist plot of control-to-output transfer function G_{vc} with increasing β.

C. Load Transient Analysis

In practical application, the anti-interference and transient response capabilities of the converter are the most crucial design criteria which can be analyzed and predicted by the small signal model. Hence, the prediction of transient response by small signal models also needs to be validated. Practically, the load point current slew rate of i_{load} can exceed 1000 A/μs. Hence, $\hat{i}_{\text{laod}}$ can be emulated by a step function $u(t)$

$$\hat{i}_{\text{load}}(t) = \Delta I u(t - t_0) + I_{\text{load}} \tag{43}$$

where ΔI is the step amplitude and t_0 is step time. By the output impedance Z_{out}, the response of output voltage can be expressed in frequency domain as

$$\hat{v}_o(s) = \mathscr{L}[\hat{i}_{\text{load}}(t)] Z_{\text{out}}(s) = \frac{\Delta I e^{-st_0}}{s} Z_{\text{out}}(s). \tag{44}$$

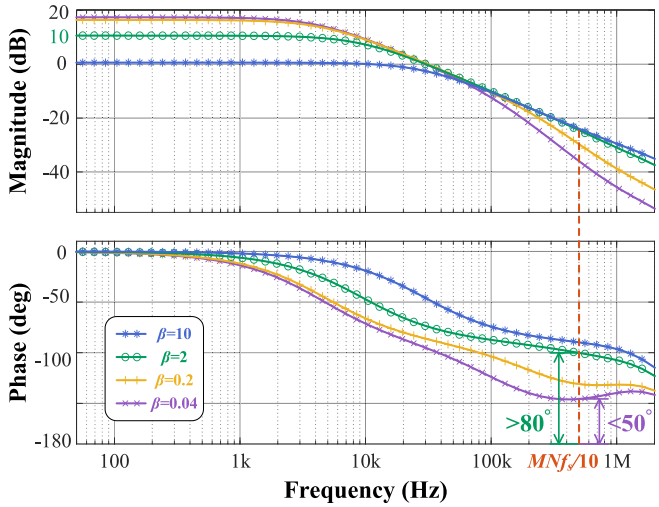

Fig. 17. Control-to-output transfer function $G_{\rm vc}$ for COT control SCTLVR with the impact of β.

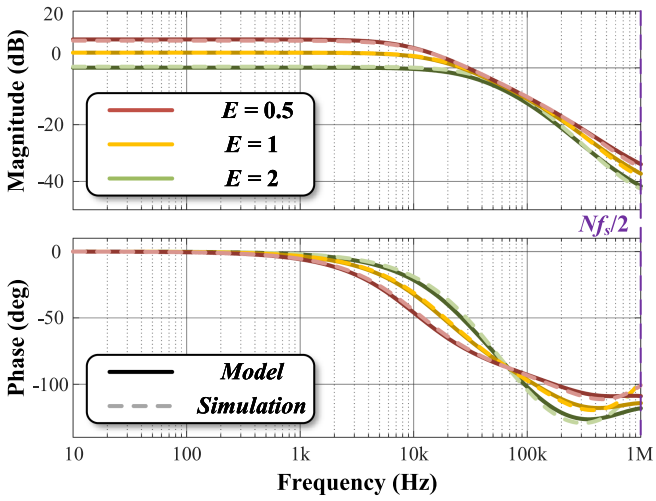

Fig. 18. SIMPLIS verification of control-to-output transfer function $G_{\rm vc}$ for a COT control four-phase SCTLVR with different external compensation.

Implement the Laplace inverse transformation, the time domain expression of output voltage can be obtained as

$$v_o(t) = \mathscr{L}^{-1}[\hat{v}_o(s)] + V_o. \tag{45}$$

The overshoot and undershoot voltages during load transients have a positive correlation with the magnitude of $Z_{\rm out}$. Suppose the gain crossover frequency of T_v is f_c. Based on (42), when $f \ll f_c$, $\|T_v\| \gg 1$, the magnitude of $Z_{\rm out}$ at low frequency can be approximated as

$$\|Z_{\rm out}\| \approx \left\| \frac{(Y_{\rm RC} + F_v F_i)^{-1}}{H_v G_{\rm vc}} \right\|. \tag{46}$$

Conversely, when $f \gg f_c$, $\|T_v\| \ll 1$, the magnitude of $Z_{\rm out}$ at high frequency can be estimated as

$$\|Z_{\rm out}\| \approx \left\| (Y_{\rm RC} + F_v F_i)^{-1} \right\|. \tag{47}$$

To mitigate voltage fluctuations during load transients, it is essential to increase the magnitude of F_v, G_{vc}, and f_c. By (34), F_v can be simplified as

$$F_v = R_i \frac{NT_{\rm on}}{2L_m}(1 + P\beta) + \frac{S_e}{f_s {\rm PV}_o}. \tag{48}$$

F_v linearly increases with β. So $\|Z_{\rm eq}\|$ will decrease with β.

Fig. 17 illustrates the Bode plot of $G_{\rm vc}$ as β increases. The parameters align with the stability analysis. It is observed that G_{c0} decreases with increasing β, while the phase drop of $G_{\rm vc}$ diminishes. Notably, when β small, the decrease in G_{c0} is minimal, yet the reduction in phase drop is significant. This indicates that the control loop can achieve a larger bandwidth design range and enhanced stability while maintaining a higher low-frequency gain, ultimately leading to improved transient performance.

VI. Simulation Verification

A. Verification of Single Module Case

To validate the accuracy of the proposed small-signal model, SIMPLIS simulation of a four-phase COT mode SCTLVR is conducted with the following parameters: $V_g = 48$ V, $V_o = 1.2$ V, $R_o = 10\,\Omega$, $C_o = 1$ mF, $R_{Co} = 0.1\,\Omega$, $R_i = 5\,\Omega$, $L_m = 200$ nH, $\beta = 2$, $\kappa = 0$, $f_s = 500$ kHz and $N = 4$. The comparison results between the simulation and the model for control-to-output transfer function $G_{\rm vc}$ with $E = 0.5$, $E = 1$ and $E = 2$ are shown in Fig. 18. By the comparisons, the proposed model predicts the frequency response behavior accurately below half of the equivalent switching frequency in different conditions.

B. Verification of Multimodule Case

To validate the accuracy of the multimodule equivalent, SIMPLIS simulation of a two-module four-phase COT mode SCTLVR with external ramp compensation is conducted. The basic circuit parameters of each module are identical to the simulation model of single module case. The comparison between the simulation results and the model for control-to-output transfer function $G_{\rm vc}$ are shown in Fig. 19. By the comparisons, the extension model can predict the frequency response behavior accurately below half of the equivalent switching frequency.

C. Verification of Closed-Loop Transfer Function

To validate the accuracy of the input-to-output transfer function and the equivalent impedance, the compensation of the voltage loop should be designed. SIMPLIS simulation model and parameters in the verification of the multimodule case will continue to be utilized with $E = 0.5$. In order to filter out output ripple while achieving sufficient bandwidth to meet the system's transient performance requirements, the design target of the gain crossover frequency is set at $f_c = MNf_s/10 = 400$ kHz. And in order to satisfy the system's stability under high bandwidth, the phase margin should be greater than 60°. To fulfill the design targets, a type 2 error compensator is introduced as

$$H_v = A_v \frac{(1 + s/\omega_z)}{s(1 + s/\omega_p)}. \tag{49}$$

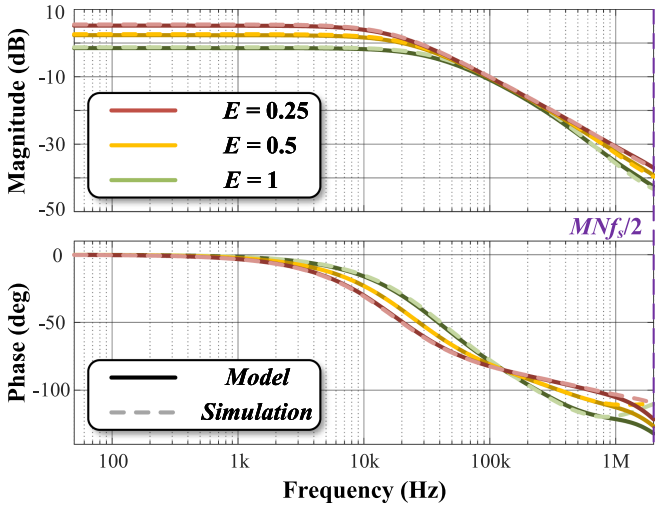

Fig. 19. SIMPLIS verification of control-to-output transfer function G_{vc} for a COT control two-module four-phase SCTLVR with different external compensation.

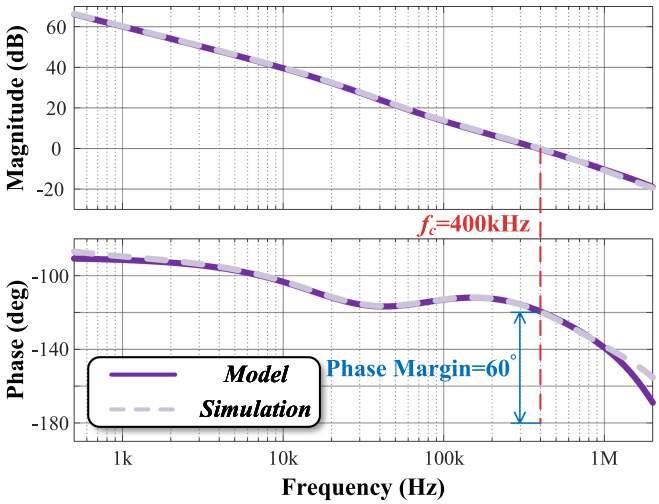

Fig. 20. SIMPLIS verification of voltage loop gain T_v. With 400 kHz bandwidth and 60° phase margin.

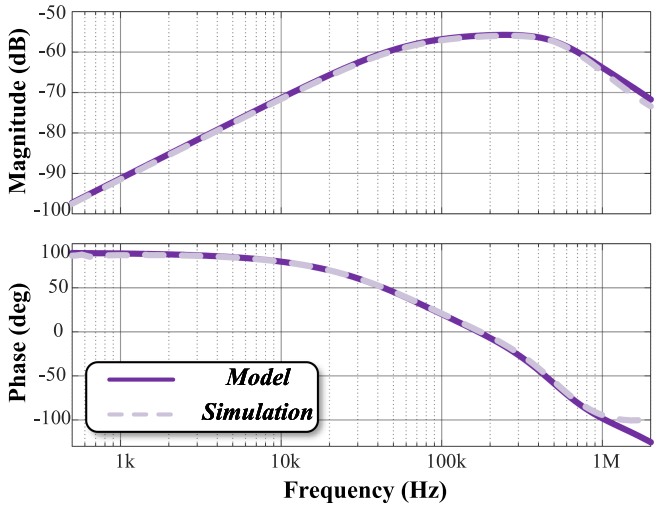

Fig. 21. SIMPLIS verification of PSRR.

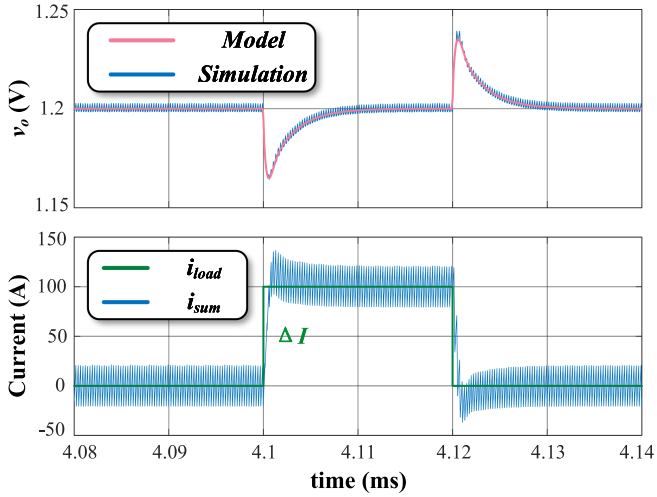

Fig. 22. SIMPLIS verification of the output resistance, performed by the response to a 100 A load current step.

The parameters of H_v are set as: $A_v = 22.92$ dB, $f_z = \omega_z/2\pi = 56.84$ kHz and $f_p = \omega_p/2\pi = 2.33$ MHz. The corresponding simulation circuit is also built. Fig. 20 shows the comparison between the simulation result and the model for T_v. And the comparison of PSRR and Z_{out} are also simulated by the model. The results are shown in Fig. 21, which also indirectly verifies the accuracy of F_g.

A step current source is utilized in the SILMPLIS model with 100 A step amplitude. The time domain calculation is conducted in MATLAB. Fig. 22 shows the comparison of the waveform between the calculation and the simulation. As indicated, the proposed model accurately predicts the load transient response, the calculation of the equivalent output impedance is accurate.

VII. Experimental Verification

To validate the accuracy of the proposed small signal model experimentally, a two-module two-phase SCTLVR evaluation board with COT control shown in Fig. 23 is designed and tested. TPS53667 from Texas Instruments is utilized as the interface controller chip [37]. And other hardware parameters are: $C_o = 5$ mF, $R_{Co} = 0.3$ mΩ, $R_i = 5$ mΩ, $L_m = 200$ nH, $\beta = 2$, $\kappa = 40$, $f_s = 300$ kHz and $M = N = 2$. The input voltage V_g is set at 12 V. And the reference voltage V_{ref} is set at 1.2 V to achieve $D = 0.2$ per phase. A 10 Ω output resistance is connected. Fig. 24 shows the current waveform detected by the current probe and the current sensing waveform detected by the voltage probe at steady state of one phase. It can be proven that the resistance of R_i is 5 mΩ.

The testing is based on Bode 100 frequency response analyzer from OMICRON Lab. As shown in Fig. 23, a small signal perturbation is injected into the voltage loop through an isolation transformer. Then Bode 100 detects the magnitude and

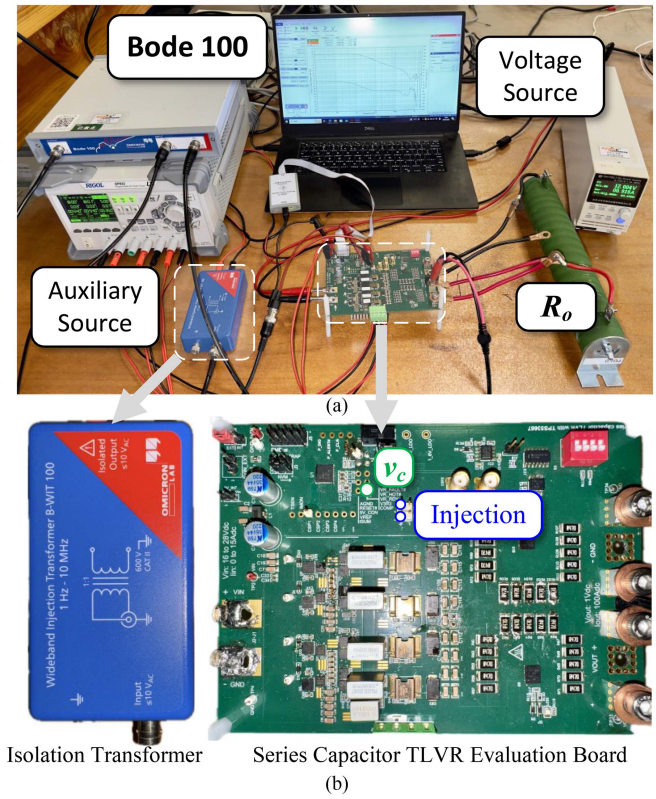

Fig. 23. (a) Experimental testing environment based on Bode 100. (b) Two-module four-phase SCTLVR evaluation board based on TPS53667.

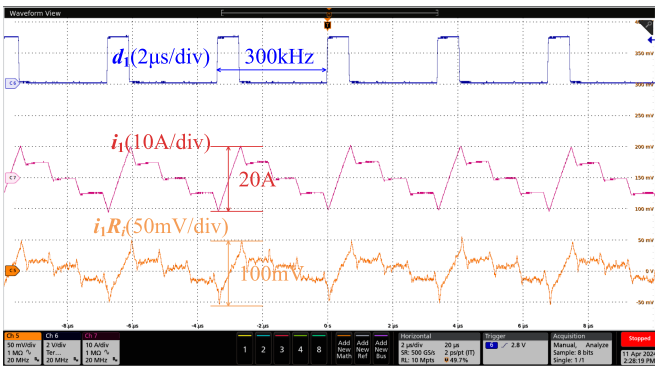

Fig. 24. Steady-state current waveform and the current sampling waveform with 5 mΩ sampling resistance for phase one.

the phase of the control signal port and the output port. The comparisons between the model and the experiment results are shown in Fig. 25. The proposed model matches the experimental results well with different external compensations. The inductive parasitic parameters of the experimental circuit lead to minor errors in magnitude and phase value at high frequency.

VIII. Conclusion

In this article, a detailed exploration and development of a small-signal model for SCTLVR with CMCOT control are presented, addressing a significant gap in the existing literature. The open-loop transfer function of the SC and TLs among different

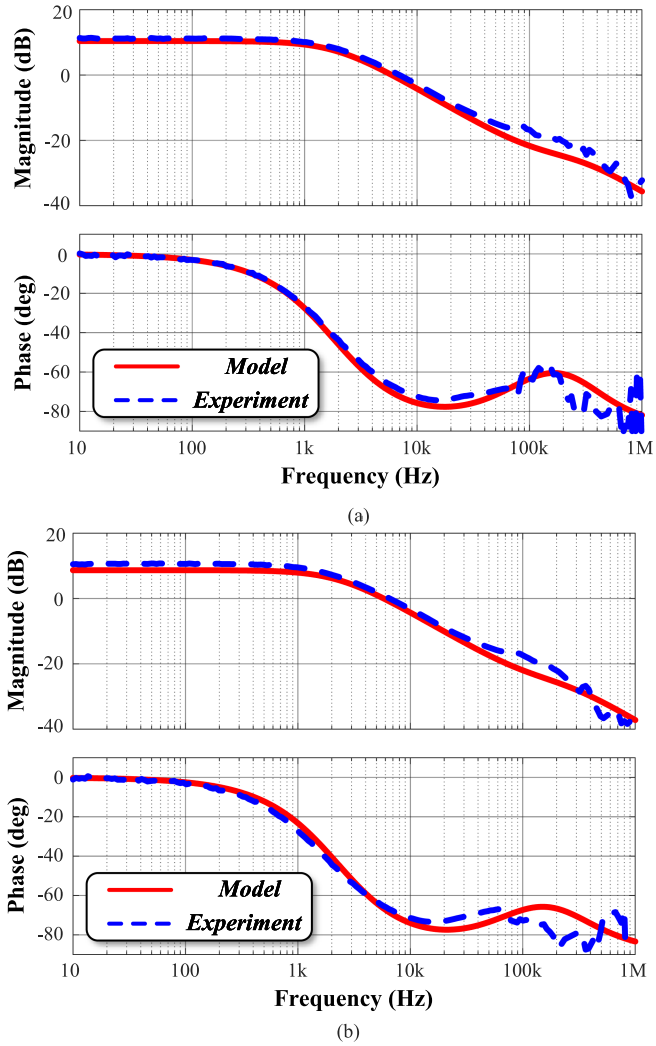

Fig. 25. Experimental verification of the control-to-output transfer function G_{vc} with (a) $E = 0.26$ and (b) $E = 0.45$.

phases are derived by leveraging a simplified decoupling equivalent. This decoupling facilitates the construction of a more manageable closed-loop small-signal model, enabling a thorough analysis of the systems frequency-domain characteristics and transient response. The improvement of the system's transient performance by TLs in Part I is revealed in the frequency domain. The proposed model has been rigorously validated through both SIMPLIS simulations and experiments, demonstrating strong agreement below half of the switching frequency and thereby confirming its accuracy and applicability. These findings provide a robust foundation for further optimization and application of multiphase SCTLVR in advanced power electronics systems.

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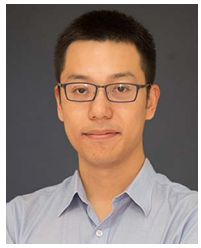

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