# Letters

# Monolithically Integrated Bidirectional Gate ESD Protection Scheme of p-GaN Power HEMT by Dual-Gate Device Technology

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***Abstract*—This letter proposes a monolithically integrated bidirectional gate electrostatic discharge protection scheme for p-GaN power high-electron-mobility transistors (HEMTs), in which a dual-gate HEMT is designed as the discharging transistor. With this protection scheme, the forward/reverse transmission line pulsing failure current is enhanced from 0.156 A/0.08 A to 1.36 A/5.26 A, almost without sacrificing performances of the p-GaN power HEMT. Thanks to the bidirectional switching characteristics of the dual-gate device by sharing the drift region, only one discharging transistor is required in the scheme; as a result, the area of this protection scheme can be effectively saved by 40.8% compared to state-of-the-art scheme with the same protection capability.**

***Index Terms*—Dual gate, electrostatic discharge (ESD), gallium nitride (GaN), high-electron-mobility transistors (HEMTs), transmission line pulsing (TLP).**

## I. Introduction

ENHANCEMENT-MODE GaN-based power high-electron -mobility transistors with p-type gate cap (p-GaN power HEMTs) have received increasing attentions in the next-generation high-frequency high-power density electronic systems due to their remarkable electrical characteristics [1]. However, p-GaN power HEMTs still suffer from electrostatic discharge (ESD) problems [2]. Since the energies introduced by forward and reverse ESD events are difficult to be discharged by the back-to-back Schottky diodes and p-i-n diodes in gate stack, the gate is easily to be destroyed [3], [4], [5], [6], [7]. Thus, it is extremely important to improve bidirectional gate ESD capability for p-GaN power HEMT. Typically, Si-based and SiC-based devices employ grounded-gate n-type metal–oxide–semiconductor, silicon-controlled rectifier, etc., to realize ESD protection [8]. Unfortunately, due to the lack of bipolar transistor and avalanche capability in commercial GaN-on-Si platform, the ESD protection of GaN device is mainly provided by external Si-based elements or monolithically integrated protection circuits. However, the external Si-based elements, including transient voltage suppressors (TVS), etc., will result in larger parasitic inductance and lower the switching frequency. Although monolithically integrated protection circuits can discharge the ESD energy by triggering a bypass discharging transistor, a huge area is usually required.

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To maintain the characteristic of high working frequency of p-GaN power HEMTs, monolithically integrated ESD protection is becoming a mainstream solution. Some monolithically integrated circuits are proposed for gate ESD protection [9], [10], [11], [12], the area of which is mainly dominated by the bypass discharging transistors. This drawback is even magnified when multiple discharge paths and multiple discharge transistors are utilized to meet the requirement of bidirectional gate ESD protection [13], [14], [15].

In this letter, a monolithically integrated bidirectional gate ESD protection scheme of p-GaN power HEMT taking dual-gate HEMT (DG-HEMT) as the discharging transistor is proposed to achieve area and cost saving without sacrificing ESD protection capability. Meanwhile, this technique also provides an effective solution of bidirectional ESD protection for various unipolar devices.

## II. Protection Structure and Operation Mechanism

The schematic of the proposed protection structure is shown in Fig. 1(a), which includes a forward trigger circuit, a reverse trigger circuit, and a DG-HEMT as a discharging transistor. The schematic structure of the DG-HEMT is shown in Fig. 1(b), in which two gates are controlled by the forward trigger circuit and the reverse trigger circuit, respectively. The forward trigger circuit consists of a rectifier diode chain ($M_{\text{F1-4}}$) and a resistor

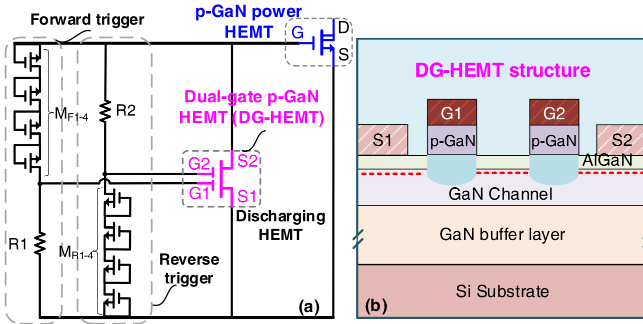


Fig. 1. (a) Proposed bidirectional gate ESD protection scheme based on dual-gate HEMT (DG-HEMT) as discharging transistor. (b) Schematic cross section of DG-HEMT structure.

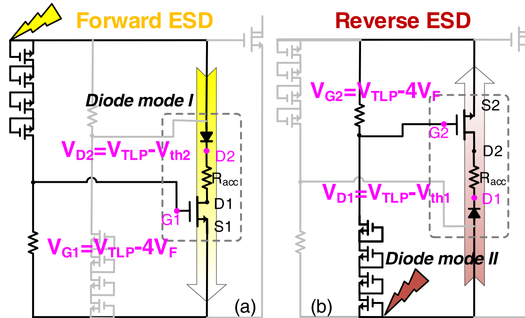


Fig. 2. Working principles of the proposed ESD protection scheme while undergoing (a) forward and (b) reverse TLP events.

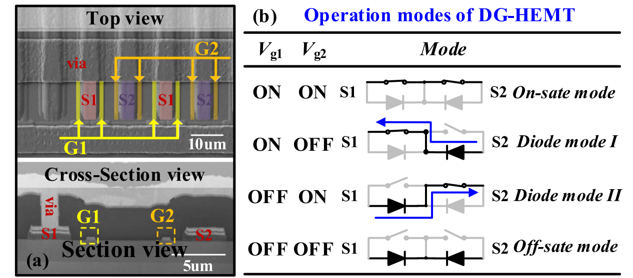


Fig. 3. (a) SEM images of fabricated DG-HEMT. (b) Operation modes of DG-HEMT.

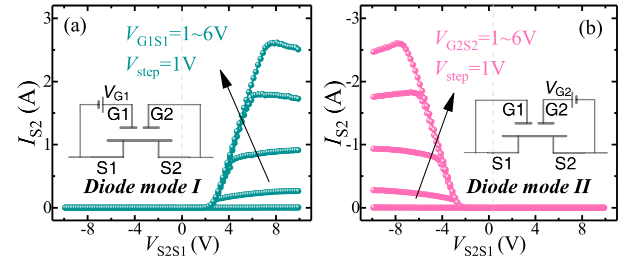


Fig. 4. Electrical performances of DG-HEMT corresponding to the scenarios of (a) forward ESD event and (b) reverse ESD event.

($R_1$), in which the resistance value is 25 kΩ and the gate width of the rectifier diode is 50 $\mu$m, the same as in the reverse trigger circuit. In regard to the p-GaN power HEMTs with the protection scheme, the forward rectifier diode anode is monolithically integrated to the gate and the reverse rectifier diode anode to the source.

When the gate of the protected device suffers from a forward ESD event, a larger transient voltage can be introduced and drops on the protection circuit. Then, the $M_{\text{F1-4}}$ chain is turned ON and withstands a part of the transient voltage. Other part of the transient voltage will increase G1 to S1 voltage ($V_{\text{G1S1}}$) and cause G1 to be turned ON. At the same time, the $M_{\text{R1-4}}$ chain is turned OFF and withstands most of the transient voltage, resulting in a very small G2 to S2 voltage ($V_{\text{G2S2}}$). In this way, the discharging transistor can work as a forward-biased diode and a resistor in series; consequently, the energy of forward ESD event can be discharged, as shown in Fig. 2(a). The energy of reverse ESD event can be discharged as the same manner, as shown in Fig. 2(b). The bidirectional ESD discharge is enabled by only a single DG-HEMT, while total two devices or more are required for the conventional one.

## III. Experimental Results and Discussion

The fabrication processes of DG-HEMT are consistent with a normal p-GaN power HEMT. The rectifier diodes are formed by shorting the gate and source of the p-GaN HEMT, and the resistors are 2DEG channel resistor. Therefore, the fabrication process of the protection scheme is completely compatible with the traditional p-GaN power HEMT, namely, the protection structure is very convenient to be monolithically integrated with the p-GaN power HEMTs.

### A. Design and Performances of the Dual-Gate Device

The DG-HEMT features a 1-$\mu$m gate-to-source length, a 1-$\mu$m gate length, a 6-$\mu$m gate-to-gate length, 18-mm gate width, and the scanning electron microscope (SEM) images of the DG-HEMT are presented in Fig. 3(a). The two gates of the DG-HEMT are controlled by $V_{\text{G1S1}}$ and $V_{\text{G2S2}}$, which can provide four operation modes, including bidirectional conduction, blocking, and two types of unidirectional diode conduction [see Fig. 3(b)]. When $V_{\text{G1S1}}$ is high and $V_{\text{G2S2}}$ is low, the DG-HEMT discharges the energy from the forward ESD event and vice versa for the energy from the reverse ESD event. The electrical performances of the DG-HEMT operating in aforementioned two scenarios are shown in Fig. 4. In addition, the gate ESD voltage of p-GaN power HEMT (also namely $V_{\text{S2}}$) is very high, so the DG-HEMT has been mainly operated in the saturation region. And the DG-HEMT shares the same substrate with the protected device. In the proposed protection scheme, the common substrate is connected to the source of p-GaN power HEMT (also named S1 in the DG-HEMT).

### B. Protection Results

To achieve effective ESD protection, the design of monolithically integrated diodes and resistors in the scheme is also important. Fig. 5 shows electrical performances of the resistor, rectifier diodes, and the protected p-GaN power HEMT with a gate width of 46.4 mm. The voltage drop of the diode chain

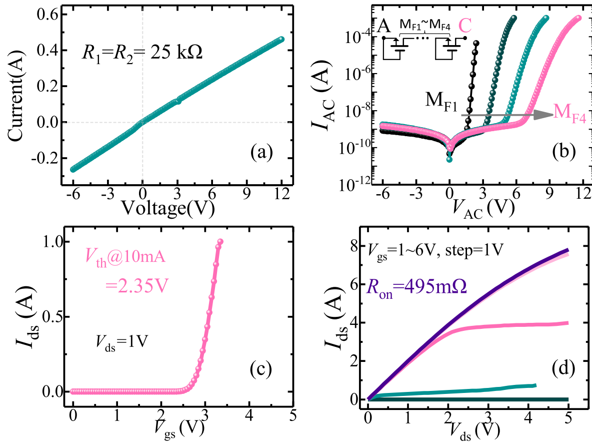


Fig. 5. Electrical performances of (a) resistance and (b) rectifier diodes in series. (c) Transfer and (d) output curves of the protected p-GaN power HEMT.

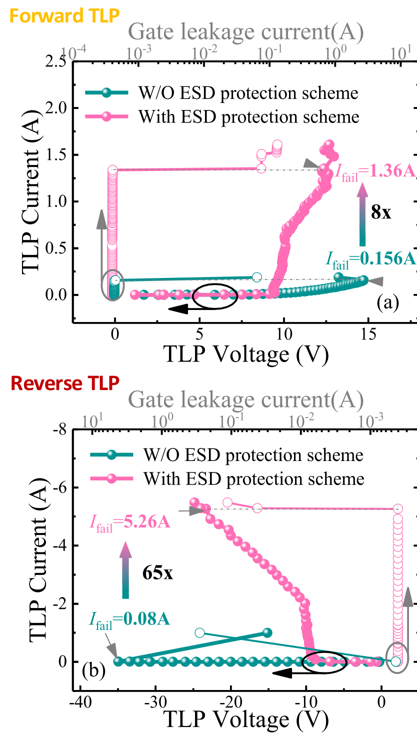


Fig. 6. (a) Forward and (b) reverse TLP $I$–$V$ characteristics of the p-GaN power HEMT with the proposed ESD protection scheme.

determines the operating range of the protection circuit; thus, it should exceed the gate operating voltage of the protected device.

The ESD reliability can be evaluated by the widely used transmission line pulsing (TLP) test, in which the TLP failure current ($I_{\text{fail}}$) multiplied by the equivalent resistance of the human body ($R_{\text{HBM}}$) is the human body model (HBM) ESD passing voltage ($V_{\text{HBM}}$). To make comparisons, the TLP performances of p-GaN power HEMTs with/without the proposed protection scheme have been tested in Fig. 6. For the p-GaN power HEMT without the protection scheme, the forward/reverse TLP failure current ($I_{\text{fail}}$) is less than 0.156 A/0.08 A. However, significant advantages can be observed with the proposed protection scheme,

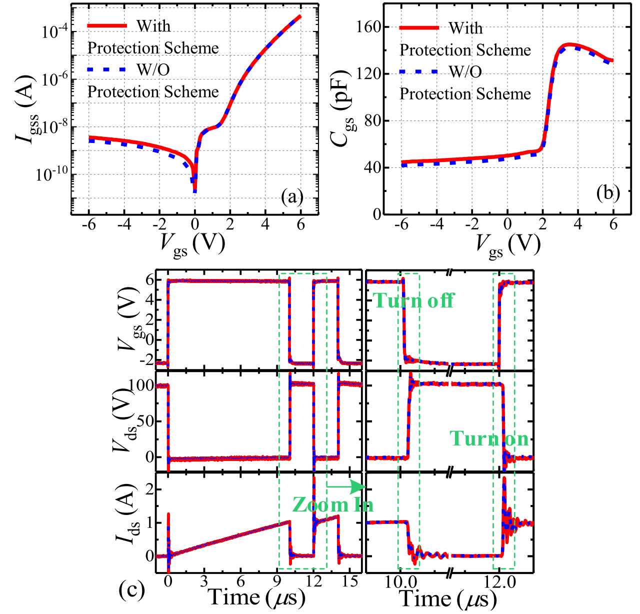


Fig. 7. (a) Gate leakage curves, (b) gate capacitance curves, and (c) switching characteristics of the protected p-GaN power HEMT with and without the proposed protection scheme.

where the forward/reverse $I_{\text{fail}}$ is increased to 1.36 A/5.26 A. And the forward/reverse HBM ESD passing voltage ($V_{\text{HBM}}$) for the p-GaN power HEMT with the proposed protection scheme is increased to ∼2.0 kV/∼7.0 kV form ∼0.8 kV/∼3.0 kV. This indicates that the protection scheme successfully provides bidirectional ESD protection, and the gate ESD reliability of the protected device has been greatly improved, with an 8×/65× forward/reverse improvements. This demonstrates that the protection structure using one DG-HEMT as the discharged transistor successfully provides bidirectional ESD protection, and the gate ESD reliability of the protected device has been greatly improved.

Furthermore, it also can be seen that the TLP current with the protection scheme becomes larger at a TLP voltage of about 9 V. This is due to the fact that the DG-HEMT is turned ON and the turn-ON voltage is equal to the sum of the threshold voltage of the DG-HEMT and the voltage drop of the diode chain. In addition, the asymmetry of the TLP $I$–$V$ curves is mainly due to the inconsistency of the forward and reverse failure voltages and leakage currents of the p-GaN gate.

Then, Fig. 7 shows the gate leakage, gate capacitance, and switching characteristics of the p-GaN power HEMTs with/without the proposed protection scheme. It can be seen that the curves are almost overlapped, which indicates that the electrical performance of the protected device is almost unaffected.

### C. Comparisons of Performances

Two typical bidirectional ESD protection schemes are shown in Fig. 8. Scheme A [13] achieves bidirectional protection through four discharging transistors with the same gate width. Hence, the area of Scheme A is so huge to maintain enough ESD

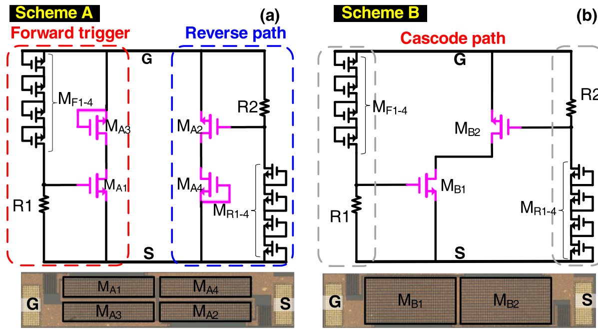


Fig. 8. Prior ESD protection topologies.

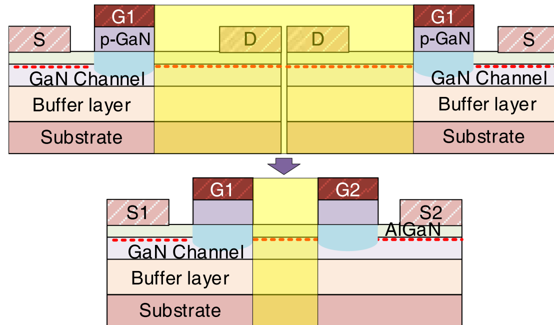


Fig. 9. DG-HEMT effectively saves device area and reduces ON-resistance by sharing gate-to-drain drift region.

capability. Scheme B [14] reduces the numbers of discharging transistors from 4 to 2 by the cascade configuration. However, the two discharging HEMTs are connected in series on the same path, which may lead to about 50% reduction of ESD capability. In the proposed bidirectional ESD protection scheme, only one discharging transistor is required thanks to the bidirectional switching capability of the DG-HEMT. The dual-gate effectively saves device area and reduces ON resistance by sharing the gate-to-drain drift region [16], [17], [18], as shown in Fig. 9. In the traditional ESD protection circuit, the area of discharging transistor is huge. Therefore, by using only one DG-HEMT as the discharging transistor, the area of the ESD protection circuit is effectively saved.

In order to equitably compare the bidirectional gate ESD capability of the proposed scheme, the aforementioned two typical ESD protection schemes are fabricated on the same wafer with the same area. Fig. 10(a) shows the TLP response voltage performances with the same TLP current for different protection schemes. For this proposed work, the clamped TLP voltage is reduced from 14.9 to 12.5 V, which is an average value from 70 to 90 ns. This is attributed to the fact that for the same area, the gate width of the DG-HEMT is larger and the ON-resistance is smaller compared to Schemes A and B. Therefore, the gate of the p-GaN power HEMT with the proposed ESD protection scheme is much less prone to failure. Furthermore, the area of the protection scheme is the sum of the areas of the forward/reverse trigger circuits and the discharging HEMT. The area proportion of discharging HEMT increases with ESD capability; hence, the higher the required ESD withstanding capability is, the higher the efficiency of area usage will be. As shown in Fig. 10(b), to

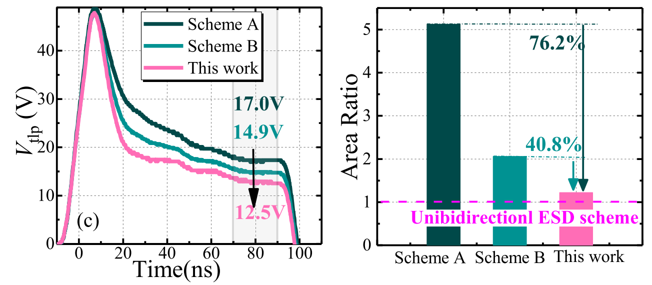


Fig. 10. (a) Transient response curves of different schemes under a 1.2-A TLP current pulse. (b) Comparisons of the area of different bidirectional protection schemes at the same ESD protection level.

| Comparison condition | | Maintaining the same protection scheme area[1] | | | | Maintaining the same ESD protection level[2] | |
|---|---|---|---|---|---|---|---|
| Protection technology | | Forward/ Reverse $I_{fail}$ (A) | $V_{clamp}$ (V) @$I_{tlp}$=1.2A/ @$I_{tlp}$= -1.2A | Parasitic $I_{leak}$(nA) @$V_{gs}$=6V | Parasitic $I_{leak}$(nA) @$V_{gs}$= -6V | Normalized Area | Parasitic $C_g$ (pF) @$V_{gs}$=6V |
| Unidirectional | resistor-based | 0.854/- | 15.0/9.83 | 4.2 | 11060 | 1.0 | 5.5 |
| Bidirectional | Scheme A | 0.152/2.63 | 17.0/16.8 | 3.9 | 6.2 | 5.13 | 12.7 |
| | Scheme B | 0.548/3.72 | 14.9/16.1 | 4.5 | 7.2 | 2.06 | 7.4 |
| | This work | 1.36/5.26 | 12.5/12.2 | 5.0 | 6.4 | 1.22 | 4.0 |

[1] The protection scheme area is 1.2mm×0.28mm. [2] The ESD protection level is about 2kV HBM.

Fig. 11. Detailed comparisons of the parameters of different protection schemes.

achieve 2-kV HBM ESD protection, the proposed ESD circuit area can be reduced by about 76.2% and 40.8% compared to Schemes A and B, respectively.

In general, these phenomena indicate that the ESD capability of the proposed protection scheme is significantly improved with the same area as other schemes, without introducing the drawbacks. Fig. 11 shows the detailed comparative information of those protection schemes. Furthermore, bidirectional switch GaN devices can be used in power converters, matrix converters, motor drives, and battery management systems [19], [20], [21], [22]. This work shows that they can also be used in bidirectional ESD protection field. In short, this technique not only provides an effective solution for bidirectional ESD protection for various unipolar devices, but also shows more promising applications of bidirectional GaN devices.

## IV. Conclusion

In this letter, a monolithically integrated bidirectional gate ESD protection scheme of the p-GaN power HEMT by dual-gate device technology has been proposed. Experimental results demonstrated that the protection scheme achieves excellent ESD capability (forward $V_{\mathrm{HBM}}$ is ~2.0 kV and reverse $V_{\mathrm{HBM}}$ is ~7.0 kV) within the limited area. In the proposed scheme, a dual-gate device can provide a bidirectional switching capability to discharge forward and reverse ESD energy, therefore achieving 40.8% area saving. In conclusion, this technique is strong competitive in the future ESD protection field.

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