# Electrical-Thermal Coupling Modeling of SiC MOSFETs Based on Field-Circuit Coupling and Its Application in Junction Temperature Calculation During Surges

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***Abstract*—Chip temperature is crucial for assessing the surge reliability of silicon carbide metal-oxide-semiconductor-field-effect transistors (SiC MOSFETs). Unlike conventional reliance on virtual junction temperature in normal conditions, evaluating the non-uniform temperature distribution across the chip under surge conditions is essential for robustness and field reliability. This paper proposes a novel field-circuit coupling model for temperature calculation of SiC MOSFETs. The proposed field-circuit coupling model enables the collaborative computation of temperature fields and circuits within circuit simulation platforms, capturing the spatial distribution of electrical and thermal properties across the chip. The validity of the field-circuit coupling calculation model is verified through three different test conditions. The electrical and thermal characteristics of SiC MOSFETs under different surge current amplitudes are analyzed, leading to a prediction of the maximum surge current capacity of the device. The method proposed in this paper extends the traditional field-circuit coupling method, providing a novel perspective for calculating the temperature of power devices under extreme conditions. To enhance understanding, this paper is accompanied by a video demonstrating the computational process of the proposed method.**

***Index Terms*—Field-circuit coupling, junction temperature calculation, proper orthogonal decomposition (POD) algorithm, surge, silicon carbide metal-oxide-semiconductor-field-effect transistors (SiC MOSFETs).**

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## I. Introduction

SILICON carbide metal-oxide-semiconductor-field-effect transistors (SiC MOSFETs) are widely used in various application areas, including sustainable energy and electric transportation, due to advantages such as high switching speed, high breakdown electric field strength, and high thermal conductivity [1], [2]. Their junction temperature is an important operational parameter, which directly affects the field performance, reliability, safe operating area (SOA), and cooling requirements. For example, during the start-up process of a power factor correction or certain fault conditions in a voltage source inverter of the motor-driven load, SiC MOSFETs encounter short-term extreme conditions characterized by high power surges [3]. During surges, self-heating in SiC MOSFETs becomes pronounced, causing temperatures to exceed SOA. Thus, this heat buildup and overtemperature are primary factors leading to device premature failures and performance degradation [4]. Large temperature gradients appear across the chip surface when power devices work in practice and the temperature distribution is nonuniform. The chip manufacturing advancements of SiC MOSFETs lead to further reduction of chip thickness, thus amplifying the temperature gradients and nonuniform distribution. Studies show the center-edge temperature difference can readily surpass 40 °C under rated operation [5] and will be more significant under surge events. This substantial and nonuniform heating introduces reliability challenges. Therefore, accurately modeling temperature distributions across chips is imperative for reliability evaluations of devices like SiC MOSFETs undergoing power surge stresses.

Frequently used methods for acquiring temperature information from power devices can be classified into four categories: 1) the optical method (notably the Infrared method), 2) electrical methods, 3) physical contact methods, and 4) electro-thermal modeling approaches [6], [7]. The optical method, represented by IR cameras, can provide comprehensive temperature data across chip surfaces, with measurement errors generally within 2% [8]. However, most IR cameras' relatively low sampling rate and high cost limit their widespread adoption. Electrical methods offer a high sampling rate and validated accuracy

TABLE I
COMPARISON OF TEMPERATURE ACQUIRING METHODS

| | Optical | Electrical | Physical contact | Electro-thermal coupling model | |
|---|---|---|---|---|---|
| | | | | 1-D | 3-D |
| Temporal Resolution | Millisecond | Microsecond | Millisecond | Optional | Optional |
| Spatial Resolution | Yes | No | No | No | Yes |
| Accuracy | High | Medium | Low | Medium | Medium |
| Hardware Cost | High | Medium/Low | Low | Low | Low |

[6], [9], [10], but only provide average chip temperature. The electrical methods incur some hardware costs, which depend on the selected electrical parameters. The physical contact method places sensors inside the device to measure temperature. While this approach incurs lower hardware costs, the accuracy is compromised because the sensors cannot be positioned directly on the chip. Moreover, the method has a low sampling rate and is unable to capture the temperature distribution across the chip [11]. The electro-thermal coupling model is based on the power loss model and thermal model to obtain the temperature information [12], [13]. Depending on the application scenario, the temporal resolution of the electro-thermal coupling model varies ($\mu$s~s), and its accuracy has been validated [14], [15]. According to the thermal model (one-dimensional (1-D) or 3-D), the electro-thermal coupling model can be classified into 1-D and 3-D models. The 1-D thermal models, such as the Foster and Cauer thermal network model, cannot calculate temperature distribution, whereas 3-D models possess this ability. This article compared the temperature measurement methods, the comparison results are detailed in Table I. Among these, the 3-D electro-thermal model calculation method stands out due to its superior performance and cost-effectiveness.

Within the 3-D electro-thermal coupling model model, the 3-D RC thermal network is the most commonly used thermal model. The 3-D RC thermal network can provide a simplified thermal analysis for the SiC MOSFETs die and its packaging. This thermal model is readily incorporated into circuit simulators such as Pspice and Saber. Ma et al. [16], and Bahman et al. [17], [18] establish a 3-D thermal network model for IGBT modules. The method is to establish a finite element simulation model, set multiple temperature calculation points, after which step power loss is applied to each chip in turn, and use the finite element model to calculate the transient temperature of the calculation points under each condition, and then obtain the 3-D thermal network model parameters by fitting data. Chen et al. [19] and Li et al. [20] described similar processes to build SiC MOSFET thermal networks. These methods are associated with high time costs and significant challenges in parameter identification. Yang et al. [21] and Heng et al. [22] proposed a commendable thermal network modeling method that extracts equivalent thermal paths for IGBT modules using finite element steady-state calculations. This approach eliminates the need for time-consuming transient finite element calculations. However, multiple finite element steady-state calculations and data-fitting processes are still required. Additionally, as the number of temperature calculation points increases, the difficulty of parameter identification also rises.

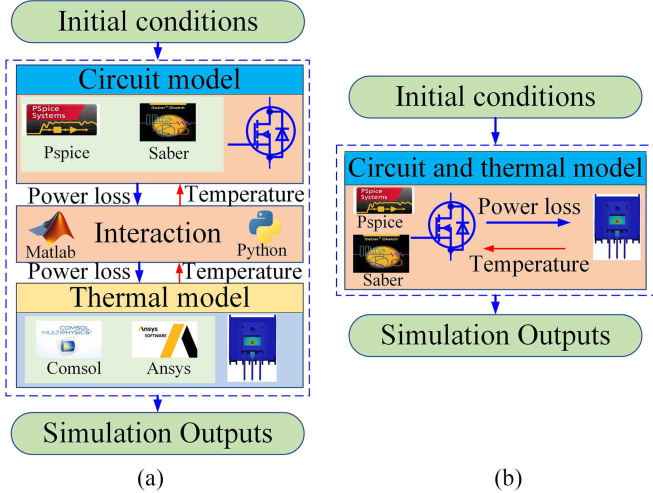



Fig. 1 Structure of field-circuit coupling model. (a) Traditional model. (b) Proposed model.

Different from thermal network models, numerical models such as the finite element method (FEM) provide accurate simulations of temperature distribution in power equipment [23]. However, many FEM simulation tools lack precise circuit models, hampering power loss calculations and suitability for surge condition electro-thermal analysis. To address the FEM limitations, field-circuit coupling models, which integrate FEM with circuit models, have been developed. This enables high-precision calculation of the electrical and thermal characteristics of the power device. The field-circuit coupling model requires a simultaneous solution of power devices' electrical and thermal characteristics, which is not available in most commercial software. The structure of the traditional field-circuit coupling model is shown in Fig. 1(a) [24], [25], [26], where it can be seen that the overall computational process entails not only time-intensive numerical simulations but also intricate data exchanges among multiple platforms, contributing to a slower computation speed.

In summary, the nonuniform temperature distribution on the SiC MOSFET chip poses challenges for the electro-thermal model of SiC MOSFET devices. To better understand device thermal behavior under surges, this article introduces a novel electric-thermal coupling model, the structure is shown in Fig. 1(b). The main contributions of this article are as follows.

1) Multicell electrothermal model. An advanced multicell chip partitioning technique is used for inhomogeneity analysis in the body diode of SiC MOSFET. This approach

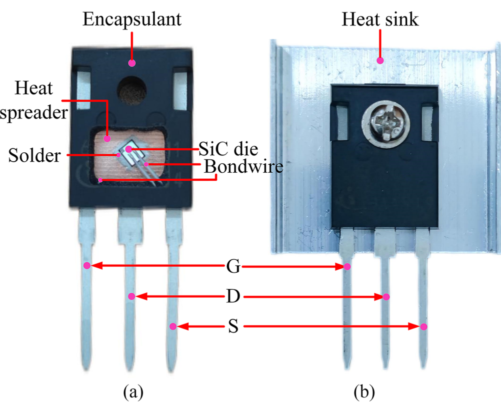



Fig. 2. SiC MOSFET (IMW65R048M1H) (a) in a transfer outline (TO) package; and (b) with a heat sink.

helps in understanding the spatial distribution of electrical and thermal properties across the chip.

2) Increased number of temperature calculation Points. The proposed thermal model enables temperature calculation of nearly any location within the circuit simulation platform, thereby enhancing the analysis of temperature distribution across the device.
3) Accurate temperature calculations. Assessing the nonlinear thermal properties of each cell ensures precise temperature calculations of the device, even under extreme operating conditions.
4) Simplified electrical and thermal coupling process. Based on circuit simulation platforms (e.g., Pspice, Saber) to calculate the device temperature field, the method proposed in this article simplifies the integration of electrical and thermal calculations.

The rest of this article is organized as follows. Section II introduces the device structures addressed in this article. Section III presents the fundamental principles of thermal modeling and the associated computational methods. Section IV describes the modeling and parameter identification methods for the power device circuit model. Section V details the computational procedures of the field-circuit coupling model and validates its capability to compute the power device chip's temperature distribution accurately. In Section VI, the field-circuit coupling model is employed to calculate the temperature of the power device chip under surge conditions. Section VII describes the limitations and discussions. Finaly, Section VIII concludes this article.

## II. SiC MOSFETs Package Structure

The temperature characteristics of SiC MOSFET devices are closely related to their packaging. The Infineon asymmetric-trench SiC MOSFET (part number: IMW65R048M1H) in a TO247 package was selected as a device under test (DUT) and it is rated as 650 V/ 48 mΩ. Its physical diagram of the IMW65R048M1H device is shown in Fig. 2, where Fig. 2(a) shows the physical diagram of the internal structure of the device, and Fig. 2(b) shows the physical diagram of the device mounted on the heat sink by bolts when it is used.

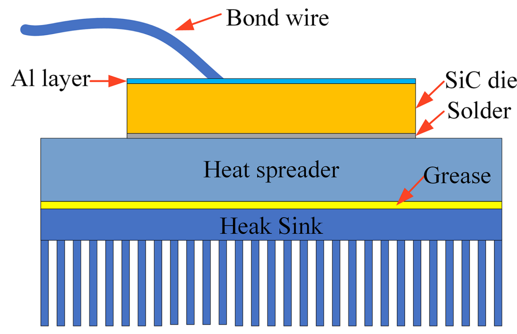



Fig. 3. Cross-sectional view of the SiC MOSFET with a heat sink.

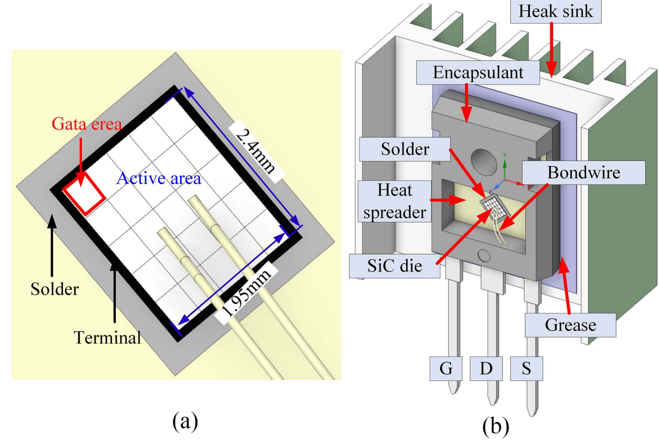



Fig. 4. Three-dimensional model of SiC MOSFET. (a) Chip. (b) Three-dimensional model.

TABLE II
Thickness of Each Component of IMW65R048M1H Device

| Components | Al layer | SiC die | Solder | Heat spreader |
|---|---|---|---|---|
| Thickness(mm) | $5.28\times10^{-3}$ | 0.113 | 0.046 | 2.036 |

The SiC MOSFETs device package with a heat sink is shown in Fig. 3. The device package is mainly composed of a heat spreader and the chip as well as the bond wire and the solder layer. The source surface of the chip is covered with a thin aluminum layer, and the surface of the thin aluminum layer is connected to the electrical terminals (Gate and Source) by ultrasonic bonding technology with bond wires. On the other hand, the chip's drain is affixed to the heat spreader via solder. Finally, the chip is encapsulated for protection from environmental contamination using the epoxy mold compound. In practice, SiC MOSFET devices also require heat sinks to dissipate heat promptly, and to ensure good contact with the heat sink, thermal grease is typically applied between the device case and the heat sink. A 3-D model of the SiC MOSFET device is established, as shown in Fig. 4. The thickness of each part in the SiC MOSFET device was obtained using field emission scanning electron microscopy

(FESEM) and present in Table II. To reduce experimental accidental errors, each component was scanned five times, and the average value was taken as the thickness of that component.

In this article, the chip area is divided into three parts: 1) gate area, 2) terminal area, and 3) active area. The heat within the chip originates within the active area, subsequently being conducted through the solder layer, the heat spreader plate, and the heat-conducting silicone grease, before being dissipated to the surroundings through the heat sink. Considering the relatively minor impact of the thin aluminum layer and gate bonding wire structure atop the chip on the temperature characteristics of power devices, these components have been excluded from the simulation model [18]. Since the SiC MOSFET device is open-capped, the epoxy resin on top of the chip is also removed from the simulation model.

## III. Thermal Modeling of SiC MOSFET

### A. Challenges in SiC Power Device Electro-Thermal Coupling Modeling

SiC materials exhibit a high sensitivity to temperature for both thermal conductivity and specific heat capacity. When developing a thermal model, it is crucial to incorporate the temperature dependence of these material thermal parameters. The thermal conductivity $k_{\mathrm{SiC}}$ (in the unit of W/(m·K)), and specific heat capacity $c_{\mathrm{SiC}}$ (in the unit of (J/(kg·K)) of SiC chips as a function of temperature $T$ (in the unit of K) are given by (1) and (2), respectively [27], [28]

$$k_{\mathrm{SiC}}(T) = \frac{1}{-0.0003 + 1.05 \times 10^{-5} T} \quad (1)$$

$$c_{\mathrm{SiC}}(T) = \frac{5.13 - \frac{1001}{T} + \frac{3.23\times10^{4}}{T^{2}}}{\rho} \quad (2)$$

where $\rho$ (in the unit of (kg·m$^{-3}$)) is the density of SiC chips.

In surge conditions, SiC MOSFET devices experience significant temperature rises. Neglecting the temperature dependency of SiC material thermal parameters can reduce the accuracy of the thermal model. The nonuniform temperature distribution across the SiC MOSFET chip causes variations in thermal parameters across different regions of the chip. Due to thermal coupling effects, the central region of the die tends to experience higher temperatures. As the thermal conductivity of SiC decreases with increasing temperature, this further accelerates the temperature rise in the central region. Additionally, the electrical characteristics of SiC MOSFETs are closely related to temperature, leading to uneven power dissipation across the chip, which further influences the temperature distribution. Overall, the nonuniform temperature distribution on the SiC MOSFETs chip results in inconsistent power dissipation and heat transfer characteristics across different regions, posing challenges for the electrothermal model of SiC MOSFET devices. This article proposes a multicell electrothermal calculation method to address these challenges, more information is given below.

### B. Finite Element Modeling for Temperature Calculations

Based on the Fourier law of heat transfer and the law of energy conservation, the governing equation of the heat transfer problem is shown in

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) + Q = \rho c \frac{\partial T}{\partial t} \quad (3)$$

where $T$ is the transient temperature of the SiC MOSFET; $k_x$, $k_y$, and $k_z$ are the thermal conductivity of the material along the $x$-, $y$-, and $z$-directions, respectively, the unit is W/(m·K); $\rho$ is the material density in kg/m$^3$; $c$ is the specific heat capacity of the material in J/(kg·K); $Q$ is the heat source intensity of the power device, and the unit is W/m$^3$.

Solving the heat transfer equation in (3) necessitates specifying boundary conditions including temperature, heat flux, and convective heat transfer. Power devices usually use air, water, and other media for heat removal via convection. Therefore, this article focuses on analyzing the convection boundary, which is governed by the following equation:

$$k_x \frac{\partial T}{\partial x} n_x + k_y \frac{\partial T}{\partial y} n_y + k_z \frac{\partial T}{\partial z} n_z = h_c \left(T_{\mathrm{a}} - T\right) \quad (4)$$

where $n_x$, $n_y$, $n_z$ are the direction of the boundary, $h_{\mathrm{c}}$ is the convective heat transfer coefficient between the heat sink surface (the green surface in Fig. 4) and the ambient medium, given in the unit of W/(m$^2$·K), and $T_{\mathrm{a}}$ is the ambient temperature.

The finite element discretization format for solving (3) and (4) is as follows:

$$\boldsymbol{C}\frac{d\boldsymbol{T}}{dt} + \boldsymbol{K}\boldsymbol{T} = \boldsymbol{P} + \boldsymbol{F} \quad (5)$$

where $\boldsymbol{T}$ is the temperature of each node in the finite element model, $\boldsymbol{C}$ is the thermal capacitance matrix, $\boldsymbol{K}$ is the thermal stiffness matrix, $\boldsymbol{P}$ is the thermal load matrix related to power loss of the SiC MOSFET chip, $\boldsymbol{F}$ is the thermal load matrix related to the ambient temperature and convective heat transfer coefficient. The matrices $\boldsymbol{C}$, $\boldsymbol{K}$, $\boldsymbol{P}$, and $\boldsymbol{F}$ are sparse matrices formed by assembling the thermal capacitance matrix, thermal stiffness matrix, and thermal load matrix for each element, respectively. The expressions for the thermal capacity matrix, thermal stiffness matrix, and thermal load matrix for each element can be found in [29].

Due to the nonuniform temperature distribution across the SiC MOSFETs chip, the electrical and thermal characteristics vary in different regions. It is feasible to divide the chip into multicells, and the electrical and thermal characteristics of each cell are calculated based on its average temperature within the cell. As shown in Fig. 5(a) for the schematic diagram of chip division, the number of cell divisions is based on the size of the chip. Considering that the chip gate length is approximately 1/5 of the length of the active area length, for convenience, the active area and gate area are collectively divided into 25 cells. Subsequently, the terminal is divided into 24 cells according to the segmentation size of the active and gate areas. In Fig. 5(a), Cell 21 represents the gate area, while Cells 26 to 49 represent the terminal area. Although the number of cells can be improved further for higher accuracy and spatial resolution of the temperature, this will come

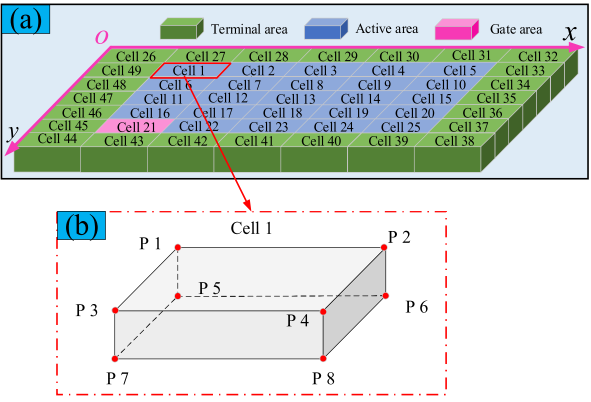



Fig. 5 Schematic diagram of chip division. (a) Chip Cells. (b) Details of the Cell.

at the expense of increased computational load. To account for different power losses in each region, the loss of each cell is treated as a distinct variable, (5) can, thus, be rewritten as

$$\boldsymbol{C}\frac{d\boldsymbol{T}}{dt}+\boldsymbol{K}\boldsymbol{T}=\sum_{i=1}^{49}\boldsymbol{P}_i+\boldsymbol{F} \tag{6}$$

where $\boldsymbol{P}_i$ is the thermal load matrix associated with Cell $i$.

Given the temperature dependence of SiC's thermal properties, both the thermal stiffness matrix and thermal capacity matrix of the FEM must be treated as inherently temperature-dependent. Thus, (6) can be rewritten as

$$\left(\boldsymbol{C}'+\sum_{i=1}^{49}\boldsymbol{C}_i\left(T_{\text{cell}i}\right)\right)\frac{d\boldsymbol{T}}{dt}+\left(\boldsymbol{K}'+\sum_{i=1}^{49}\boldsymbol{K}_i\left(T_{\text{cell}i}\right)\right)$$
$$\boldsymbol{T}=\sum_{i=1}^{49}\boldsymbol{P}_i+\boldsymbol{F} \tag{7}$$

where $\boldsymbol{C}'$ represents the thermal capacitance matrix of the SiC MOSFET device with the chip removed; $\boldsymbol{C}_i$ signifies the thermal capacitance matrix of the Cell $i$ of the SiC MOSFET chip; $\boldsymbol{K}'$ represents the thermal stiffness matrix of the SiC MOSFET device with the chip removed; $\boldsymbol{K}_i$ signifies to the thermal stiffness matrix of the Cell $i$ of the SiC MOSFET chip, and $T_{\text{cell}\ i}$ represents the average temperature of the Cell $i$ of the chip. Taking Cell 1 as an example, its schematic diagram is shown in Fig. 5(b), which shows that Cell 1 region contains eight vertices, and the average temperature of these eight vertices is regarded as the average temperature of Cell 1.

### C. Reduced-Order Model

A reduced-order model primarily involves creating a proper orthogonal decomposition (POD) modal matrix and projecting the high-dimensional finite element matrix into a low-dimensional subspace using this POD modal matrix. The POD modal matrix is essentially composed of a collection of linearly independent and orthogonal basis functions denoted as $\phi_1$, $\phi_2, \ldots, \phi_r$. The temperature at any FEM node can be represented by employing a linear combination of orthogonal basis functions

$$\boldsymbol{T}(t)=a_1(t)\,\phi_1+a_2(t)\,\phi_2+\cdots+a_r(t)\,\phi_r \tag{8}$$

where $\boldsymbol{T}(t)$ is the temperature of FEM and $a_1(t), a_2(t), \ldots, a_r(t)$ are the coefficients of the orthogonal basis. The modal matrix $\Phi = [\phi_1\ \phi_1\ \ldots\ \phi_r]_{M\times r}$ has $M$ rows, representing the number of nodes in the finite element model, and $r$ columns, representing the number of linearly independent orthogonal bases. The matrix $\boldsymbol{a}= [a_1\ a_2\ \ldots\ a_r]^{\text{T}}$ consisting of the coefficients of the bases is called the coefficient matrix. Equation (8) can be represented in matrix form [30]

$$\boldsymbol{T}(t)=\Phi\boldsymbol{a}. \tag{9}$$

This can be obtained by substituting (9) into (7)

$$\left(\boldsymbol{C}'+\sum_{i=1}^{49}\boldsymbol{C}_i\left(T_{\text{cell}i}\right)\right)\Phi\frac{d\boldsymbol{a}}{dt}+\left(\boldsymbol{K}'+\sum_{i=1}^{49}\boldsymbol{K}_i\left(T_{\text{cell}i}\right)\right)$$
$$\Phi\boldsymbol{a}=\sum_{i=1}^{49}\boldsymbol{P}_i+\boldsymbol{F}. \tag{10}$$

Simultaneous multiplication of both sides by $\Phi^{\text{T}}$ can obtain the POD model considering the temperature distribution of the chip and the temperature dependence of the thermal parameters of the SiC material

$$\widehat{\boldsymbol{C}}'\frac{d\boldsymbol{a}}{dt}+\widehat{\boldsymbol{C}}''\frac{\mathrm{d}\boldsymbol{a}}{\mathrm{d}t}+\widehat{\boldsymbol{K}}'\boldsymbol{a}+\widehat{\boldsymbol{K}}''\boldsymbol{a}=\widehat{\boldsymbol{P}}''+\widehat{\boldsymbol{F}} \tag{11}$$

where the matrices $\boldsymbol{C}^{\wedge\prime}{}_{r\times r}$, $\boldsymbol{C}^{\wedge\prime\prime}{}_{r\times r}$, $\boldsymbol{K}^{\wedge\prime}{}_{r\times r}$, $\boldsymbol{K}^{\wedge\prime\prime}{}_{r\times r}$, $\boldsymbol{P}^{\wedge\prime\prime}{}_{r\times 1}$, and $\boldsymbol{F}^{\wedge}{}_{r\times 1}$ are expressed as

$$\begin{aligned}
\widehat{\boldsymbol{C}}' &= \boldsymbol{\Phi}^{\text{T}}\boldsymbol{C}'\boldsymbol{\Phi}\\
\widehat{\boldsymbol{C}}'' &= \boldsymbol{\Phi}^{\text{T}}\left(\sum_{i=1}^{49}\widehat{\boldsymbol{C}}_i\left(T_{\text{cell}i}\right)\right)\boldsymbol{\Phi}\\
\widehat{\boldsymbol{K}}' &= \boldsymbol{\Phi}^{\text{T}}\boldsymbol{K}'\boldsymbol{\Phi}\\
\widehat{\boldsymbol{K}}'' &= \boldsymbol{\Phi}^{\text{T}}\left(\sum_{i=1}^{49}\widehat{\boldsymbol{K}}_i\left(T_{\text{cell}i}\right)\right)\boldsymbol{\Phi}\\
\widehat{\boldsymbol{P}}'' &= \boldsymbol{\Phi}^{\text{T}}\left(\sum_{i=1}^{49}\widehat{\boldsymbol{P}}_i\right)\\
\widehat{\boldsymbol{F}} &= \boldsymbol{\Phi}^{\text{T}}\boldsymbol{F}.
\end{aligned} \tag{12}$$

With this transformation, the problem in (7) is now reformulated into (11), where the dimension of the matrix being sought is $M$ in (7), while in (11), it is reduced to $r$. Given that $M$ is much larger than $r$, this transformation significantly enhances computational efficiency.

### D. Circuit Transformations for Reduced-Order Model

By solving (11), the values of the coefficients $\boldsymbol{a}$ can be determined. Subsequently, the temperature of the SiC MOSFET can be obtained by substituting $\boldsymbol{a}$ into (9). Using the node voltage method, (9) and (11) can be equated to a thermal network model. In this analogy, the variable $\boldsymbol{a}$ is treated as the voltage

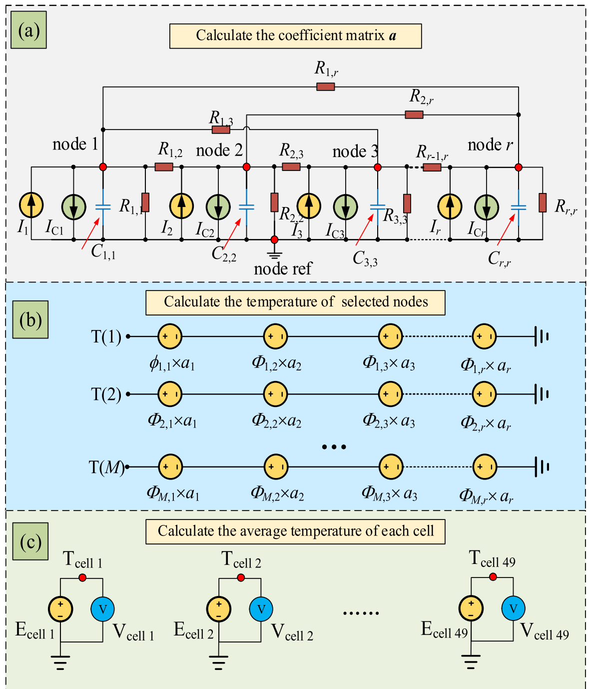



Fig. 6. Proposed thermal network. (a) Calculation of matrix $\boldsymbol{a}$. (b) Calculate the temperature of selected nodes. (c) Calculate the average temperature of each Cell.

at each node of the thermal network model, while the thermal capacity matrix $\hat{\boldsymbol{C}}'$ and $\hat{\boldsymbol{C}}''$, thermal stiffness matrix $\hat{\boldsymbol{K}}'$ and $\hat{\boldsymbol{K}}''$, and thermal load matrix $\hat{\boldsymbol{P}}''$ and $\hat{\boldsymbol{F}}$ correspond to the thermal capacity, thermal resistance, and equivalent current source in the thermal network model, respectively. The thermal network corresponding to (9) and (11) is shown in Fig. 6.

Fig. 6(a) shows the calculation of matrix $\boldsymbol{a}$ based on the power loss from partitioned cells. Here, the equivalent voltage (for temperature difference calculation) between any nodes of node 1, node 2, …, node $r$, and node ref are denoted by the values of $a_1, a_2, \ldots, a_r$, $R_{i,i}$ represents the equivalent thermal resistance between node $i$ and node ref, $R_{i,j}$ ($i{\neq}j$) indicates the equivalent thermal resistance between node $i$ and node $j$, and $C_{i,i}$ signifies the equivalent thermal capacitance between node $i$ and node ref, and the expression for all three is shown in

$$\begin{aligned} R_{i,i} &= \\ &\frac{1}{\left(\hat{k}'_{i,1}+\hat{k}'_{i,2}+\cdots+\hat{k}'_{i,r}\right)+\left(\hat{k}''_{i,1}+\hat{k}''_{i,2}+\cdots+\hat{k}''_{i,r}\right)} \text{ for } i=j \\ R_{i,j} &= -\frac{1}{\hat{k}'_{i,j}+\hat{k}''_{i,j}} \text{ for } \quad i \neq j \\ C_{i,i} &= \hat{c}'_{i,i}+\hat{c}''_{i,i} \end{aligned} \tag{13}$$

where $\hat{k}'_{i,j}$ $(i, j = 12, \ldots, r)$ are the elements of row $i$ and column $j$ of matrix $\hat{\boldsymbol{K}}'$; $\hat{k}''_{i,j}$ $(i, j = 12, \ldots, r)$ are the elements of row $i$ and column $j$ of matrix $\hat{\boldsymbol{K}}''$; $\hat{c}'_{i,j}$ $(i, j = 12, \ldots, r)$ are the elements of row $i$ and column $j$ of matrix $\hat{\boldsymbol{C}}'$, and $\hat{c}''_{i,j}$ $(i, j = 12, \ldots, r)$ are the elements of row $i$ and column $j$ of matrix $\hat{\boldsymbol{C}}''$.

The current source $I_i$ depicted in Fig. 6(a) signifies the injected current flowing from node ref to node $i$. The value of this current source is related to power loss and convective heat transfer, and its specific expression is

$$I_i = \hat{p}''_i + \hat{f}_i \tag{14}$$

where $\hat{p}''_i$ and $\hat{f}_i$ are the elements of the $i$th row of the matrices $\hat{\boldsymbol{P}}''$ and $\hat{\boldsymbol{F}}$, respectively.

The current source $I_{\mathrm{C}i}$ in Fig. 6(a) is the injected current from node $i$ to node ref, which mainly represents the influence of other nodes on node $i$. The specific expression is

$$I_{\mathrm{C}i} = \sum_{j=1}^{r} \hat{c}'_{i,j}\frac{\mathrm{d}a_j}{\mathrm{d}t} + \sum_{j=1}^{r} \hat{c}''_{i,j}\frac{\mathrm{d}a_j}{\mathrm{d}t}\,(i \neq j)\,. \tag{15}$$

Fig. 6(b) demonstrates how to calculate the temperature of the selected nodes, and the selected nodes can be added as needed. As an example, to calculate the temperature of Cell 1, which consists of eight vertices, assume that the node numbers of the eight vertices in the FEM are $\mathrm{P}_1$, $\mathrm{P}_2$, …, $\mathrm{P}_8$, the temperatures of the vertices, $T(\mathrm{P}_1)$, $T(\mathrm{P}_2)$, …, $T(\mathrm{P}_8)$, are shown in

$$\begin{aligned} T(\mathrm{P}_1) &= \phi_{\mathrm{P}_1,1}\cdot a_1+\phi_{\mathrm{P}_1,2}\cdot a_2+\cdots+\phi_{\mathrm{P}_1,r}\cdot a_r \\ T(\mathrm{P}_2) &= \phi_{\mathrm{P}_2,1}\cdot a_1+\phi_{\mathrm{P}_2,2}\cdot a_2+\cdots+\phi_{\mathrm{P}_2,r}\cdot a_r \\ &\cdots \\ T(\mathrm{P}_8) &= \phi_{\mathrm{P}_8,1}\cdot a_1+\phi_{\mathrm{P}_8,2}\cdot a_2+\cdots+\phi_{\mathrm{P}_8,r}\cdot a_r \end{aligned} \tag{16}$$

where $\phi_{\mathrm{P}\,i,j}$ is the elements of the $\mathrm{P}_i$ rows and $j$ columns of the matrix $\Phi$, $a_i$ is the elements of the $i$ rows of the matrix $\boldsymbol{a}$.

Fig. 6(c) calculation of the average temperature of each Cell by its vertex temperature. Taking Cell 1 as an example, its average temperature $T_{\mathrm{cell}\ 1}$ is

$$T_{\mathrm{cell1}} = \frac{T(\mathrm{P}_1)+T(\mathrm{P}_2)+\cdots+T(\mathrm{P}_8)}{8}. \tag{17}$$

Thus, the thermal model of SiC MOSFET is constructed through the following steps. A FEM was built at first to calculate the temperature of SiC MOSFET. The FEM is then converted to a reduced-order model using the POD algorithm. Finally, the reduced-order model is converted into a thermal network, which can efficiently compute the temperature distribution of the SiC MOSFET device through a circuit simulator, enabling convenient coupling with device circuit models. The entire process is summarized by the flowchart illustrated in Fig. 7.

To obtain the thermal network model parameters, the 3-D model of the SiC MOSFET was created using SpaceClaim and meshed in Ansys, as shown in Fig. 8 (The significance of the comparison lines and comparison point in Fig. 8 will be mentioned in Section V). The mesh consists of 100 620 quadratic tetrahedral elements and 165 506 nodes. With the mesh data, a custom MATLAB program was developed to calculate the $\hat{\boldsymbol{C}}'$, $\hat{\boldsymbol{C}}''$, $\hat{\boldsymbol{K}}'$, $\hat{\boldsymbol{K}}''$, $\hat{\boldsymbol{P}}''$, and $\hat{\boldsymbol{F}}$ based on material property parameters shown in Table III [16], [31], [32]. Finally, the matrices $\hat{\boldsymbol{C}}'$, $\hat{\boldsymbol{C}}''$, $\hat{\boldsymbol{K}}'$, $\hat{\boldsymbol{K}}''$, $\hat{\boldsymbol{P}}''$, and $\hat{\boldsymbol{F}}$ are transformed into equivalent circuit models according to (13)–(17).

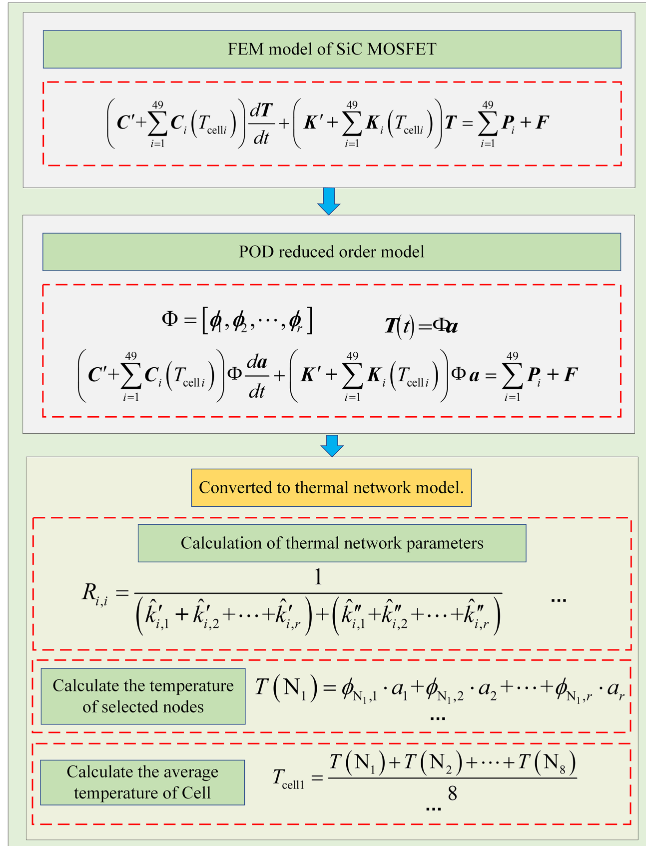



Fig. 7. Flowchart for the thermal model of SiC MOSFET.

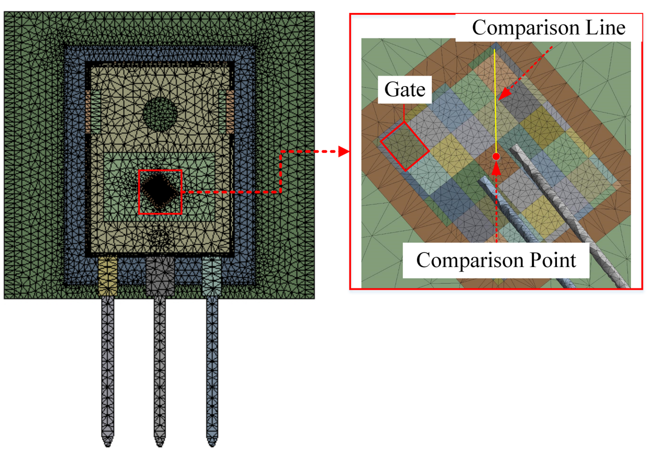



Fig. 8. Mesh for SiC MOSFET thermal modeling.

## IV. Electrical Modeling of SiC MOSFET

SiC MOSFET do not have an independent diode chip, but rather a body diode consisting of different doped regions within the SiC MOSFET chip. The SiC MOSFET surge refers to the process in which the SiC MOSFET body diode flows a high current for a few milliseconds, which in turn causes the SiC MOSFET device temperature to rise. During this process, the SiC MOSFET device temperature depends not only on its thermal characteristics but also on the electrical characteristics of the body diode. Therefore,

TABLE III
Thermal Properties of SiC MOSFETs

| Component/material | Density (kg·m$^{-3}$) | Specific heat (J/(kg·K)) | Thermal conductivity (W/(m·K)) |
|---|---|---|---|
| Chip/ Silicon Carbide | 3216 | (2) | (1) |
| Solder/Sn96.5Ag3.5 | 9000 | 288 | 57 |
| Heatspreader/copper | 8954 | 384 | 391 |
| Leadframe/copper | 8954 | 384 | 391 |
| Encapsulant/epoxy mold compound | 1780 | 800 | 0.7 |
| Grease | 2000 | 300 | 3 |
| Hesksink/Aluminum | 2700 | 900 | 200 |

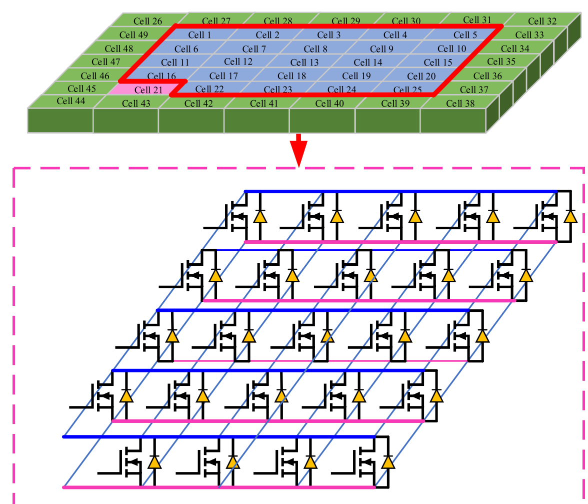


Fig. 9. Division schematic for SiC MOSFET circuit modeling.

it's crucial to understand the electrical behavior of the SiC MOSFET body diode.

### A. Diode Distributed Circuit Model

Similar to the thermal model, in the circuit model, the SiC MOSFET body is equivalently represented as multiple parallel cells, as illustrated in Fig. 9. Notably, in Fig. 9, Cell 21 corresponds to the gate region of the SiC MOSFET, while Cell 26–Cell 49 correspond to the terminal region. Due to the relatively low power loss in the gate and terminal regions, these areas are neglected in this circuit model.

The SiC MOSFET body diode can be equated to a voltage-controlled current source with the expression shown in [33].

$$I_{\text{sd}} = \alpha\,(T) \cdot (V_{\text{sd}} - V_{\text{PN}}\,(T))^{\gamma(T)} \tag{18}$$

where $I_{\text{sd}}$ is the diode current, $T$ is the diode temperature; $\alpha\,(T)$, $V_{\text{PN}}\,(T)$, $\gamma(T)$ are the model fitting parameters, and $V_{\text{sd}}$ is the voltage across the diode.

The values of $\alpha$ (T), $V_{\text{PN}}$ (T), and $\gamma$(T) are closely related to the temperature of the diode, which is approximated through fitting procedures. The specific expressions for these approximations are provided in (19), (20), and (21), respectively, as

TABLE IV
MODEL PARAMETERS OF THE SiC MOSFET BODY DIODE

| Parameters | $a_1$ | $a_2$ | $a_3$ | $v_1$ |
|---|---|---|---|---|
| Value | 0.094 | 0.60 | 4.31 | 89.95 |
| Parameters | $v_2$ | $v_3$ | $g_1$ | $g_2$ |
| Value | -2.56 | 2.18 | 1.81 | 0.00 |

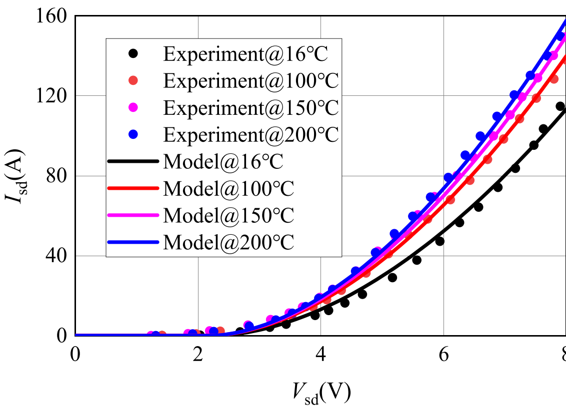



Fig. 10. Forward characteristics of SiC MOSFET body diode at different temperatures.

follows:

$$\alpha(T) = a_1 \cdot T^{a_2} + a_3 \tag{19}$$

$$V_{PN}(T) = v_1 \cdot T^{v_2} + v_3 \tag{20}$$

$$\gamma(T) = g_1 + g_2 \cdot T \tag{21}$$

where $\alpha_1$, $\alpha_2$, $\alpha_3$, $v_1$, $v_2$, $v_3$, $g_1$, $g_2$ are the fitting coefficients.

### B. Diode Model Parameters Extraction

The relevant parameters (18)–(21) can be extracted from the forward characteristics of the SiC MOSFET body diode. Upon obtaining the forward conduction characteristics of DUT at varying temperatures, the model parameters of the body diode can be derived by fitting the pertinent parameters within (18)–(21). These parameters are presented in Table IV after the fitting process. The forward conduction curves of the body diode at different temperatures are shown in Fig. 10. It can be seen that the constructed model aligns with the experiment results and is a good representation of the forward characteristic. The body diode is regarded as a parallel structure of multiple cells, and then the forward conduction model of the body diode in each cell region can be easily obtained.

## V. PRINCIPLES OF FIELD-CIRCUIT COUPLING MODEL CALCULATION AND MODEL VALIDATION

### A. Principle of Field-Circuit Coupling Calculation

The field-circuit coupling model proposed in this article consists of two parts: the circuit model and the thermal model. Both the circuit model and the thermal model are implemented by using Spice programming and calculated by the circuit simulation platform (Twin Builder). The specific concept of the field-circuit coupling model is shown in Fig. 11, which mainly contains the following steps.

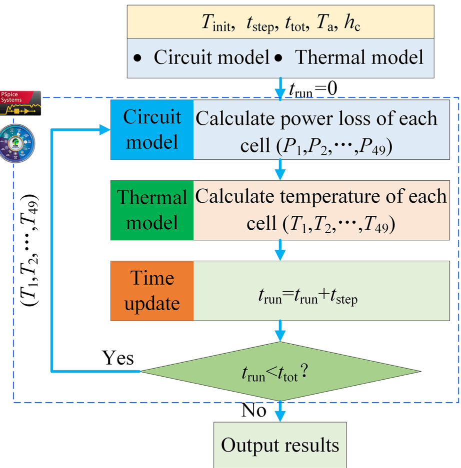
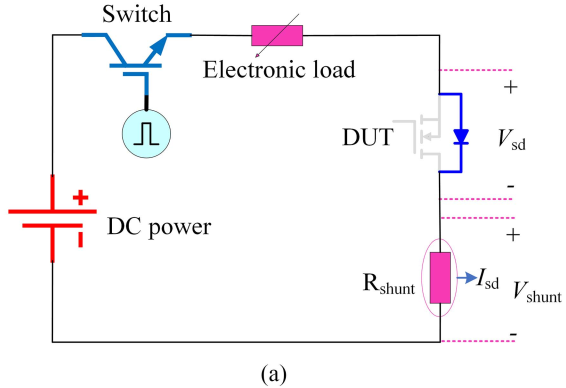



Fig. 11. Principle of field-circuit coupling model.

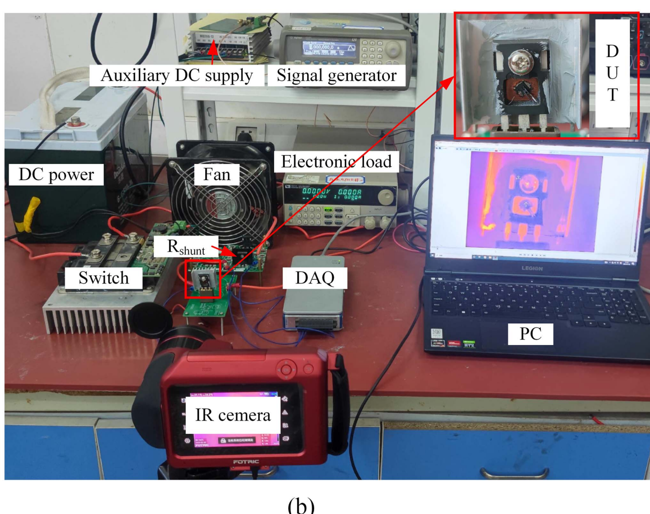
1) The initial temperature $T_{\rm init}$, time step $t_{\rm step}$, and total calculation time $t_{\rm tot}$ are specified for both the circuit and thermal models. The ambient temperature $T_{\rm a}$ and convection heat transfer coefficient $h_c$ are provided for the thermal model. At the start, the current calculation time $t_{\rm run}$ of the field-circuit coupled model is set to 0 s.
2) The circuit model calculates the power loss of each cell within a time step $t_{\rm step}$ based on the temperature of each cell in the SiC MOSFET.
3) The power loss of every cell is substituted into the thermal model to calculate the temperature of every cell within a time step $t_{\rm step}$.
4) Update the current calculation time $t_{\rm run}$ of the field-circuit coupling model.
5) Determine whether the computational procedure meets the termination criterion. The termination criterion is that the current calculation time $t_{\rm run}$ is not less than the total calculation time $t_{\rm tot}$.
6) If the termination criterion is not met, the temperature values of each cell are fed back into the circuit model for the computation of the next time step.
7) If the termination criterion is met, the computation is terminated and the results of the computation (temperature, voltage, and power) are exported.

### B. Experimental Platforms

To facilitate the comparison between the field-circuit coupling model results and experimental measurements, a corresponding experimental setup was initially assembled in this article. The experimental schematic diagram and the established experimental platform are shown in Fig. 12. The experiment utilizes a lead-acid battery as the heating power source, employs an IT8512 electronic load model to regulate the heating current of the DUT, and uses an IGBT module as a switch to manage the heating duration. The driving signal for this IGBT module is supplied by a signal generator, which is modeled with Agilent




(a)




(b)

Fig. 12. Experimental platform. (a) Schematic. (b) Experimental setup.

TABLE V
TEST CONDITIONS

| | Current(A) | Heating time (ms) | $T_a$ (°C) |
|---|---|---|---|
| Test 1 | 10 | 400 | 25 |
| Test 2 | 20 | 400 | 25 |
| Test 3 | 25 | 400 | 25 |

33220A. The current $I_{sd}$ of the DUT is calculated by sampling the voltage across the resistor $R_{shunt}$, where $R_{shunt}$ is selected as a 100 mΩ high precision noninductive resistor. The DUT voltage $V_{sd}$ and current $I_{sd}$ were acquired by a data acquisition system (DAQ). The encapsulant above the chip is removed; after that, the chip is sprayed with black body paint to keep its emissivity at 0.95. In this way, the chip temperature can be measured by the FOTRIC 288 IR camera. The IR image of SiC MOSFET is shown in Fig. 13.

### C. Test Conditions

Based on the field-circuit coupling model, the temperature distribution and power loss distribution of the SiC MOSFET chip under three test conditions are calculated, and the three test conditions are shown in Table V. During the experiment, the SiC MOSFET dissipates heat by forced convection through a fan,

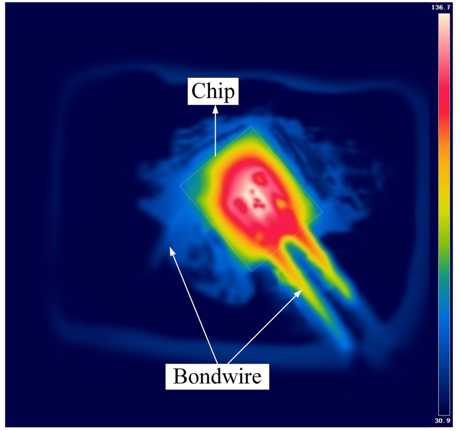



Fig. 13. IR image of SiC MOSFET.

and the heat transfer coefficient of the SiC MOSFET is about 67 W/m$^2$·K based on the cooling curve.

The established field-circuit coupling model can compute the power distribution and temperature distribution of each cell. To fully capture the temperature characteristics of the SiC MOSFET chip, the total calculation time $t_{all}$ is set to 800 ms, and the $t_{step}$ is set to an adaptive step size. At the beginning of the test, the power of each cell is zero, and at 400 ms of operation time, the power distribution of each cell is displayed in Fig. 14. Similarly, the temperature distribution of each cell at the beginning of the test is 25 °C, and at 400 ms of operation time, the temperature distribution of each cell is illustrated in Fig. 15. In Figs. 14 and 15, the values of the $x$-axes and $y$-axes represent the sequence of cells along the $x$-axes and $y$-axes, as shown in Fig. 5. From Figs. 14 and 15, it can be observed that as the chip's power loss increases, the chip's temperature gradually rises. Due to thermal coupling effects, differences in power loss and temperature distribution among cells begin to emerge. The power loss of the cells in the center region of the chip is maximum, and the power loss of the cells in the edge region of the chip is minimum. Analogous to the power loss distribution, it is evident from Fig. 15 that as chip power loss increases, the inhomogeneity of the temperature distribution among the cells gradually increases, with the cells in the center having the highest temperatures and the cells in the edge having lower temperatures. The uneven distribution of chip temperature is a combined outcome arising from the uneven power loss across cells and the synergistic effect of thermal coupling between the cells.

### D. Model Validation

To evaluate the accuracy of the field-circuit coupling model, it is essential to define the model error, which is shown in

$$\varepsilon_{\mathrm{Val}} = \sum_{i=1}^{n} \left( \frac{\left| Val_{\mathrm{model}}^{i} - Val_{\mathrm{ref}}^{i} \right|}{Val_{\mathrm{ref}}^{i}} \right) / n \quad (22)$$

where *Val* refers to the parameter to be evaluated, such as the temperature or power loss, $\varepsilon_{\mathrm{Val}}$ is the error in the calculated value of the field-circuit coupling model, $Val^{i}_{\mathrm{ref}}$ is the value of *Val* at the *i*th moment obtained through experimentation, $Val^{i}_{\mathrm{model}}$ is

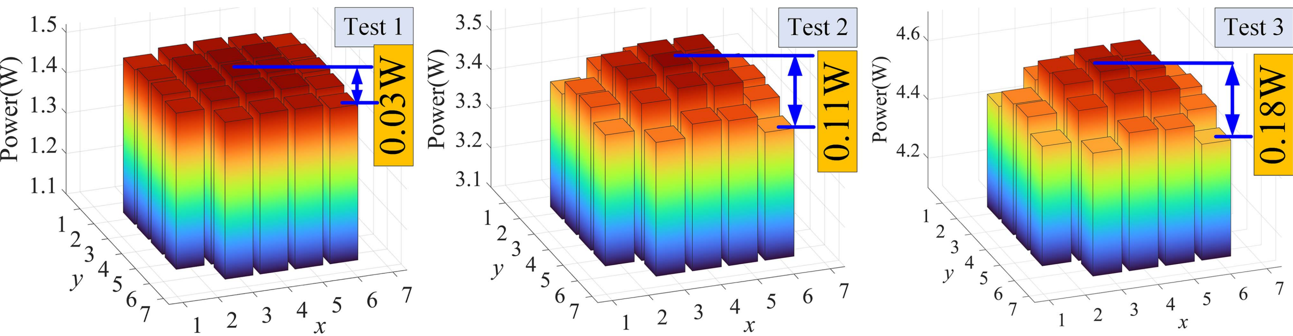



Fig. 14. Simulation results of power loss distribution (time = 400 ms).

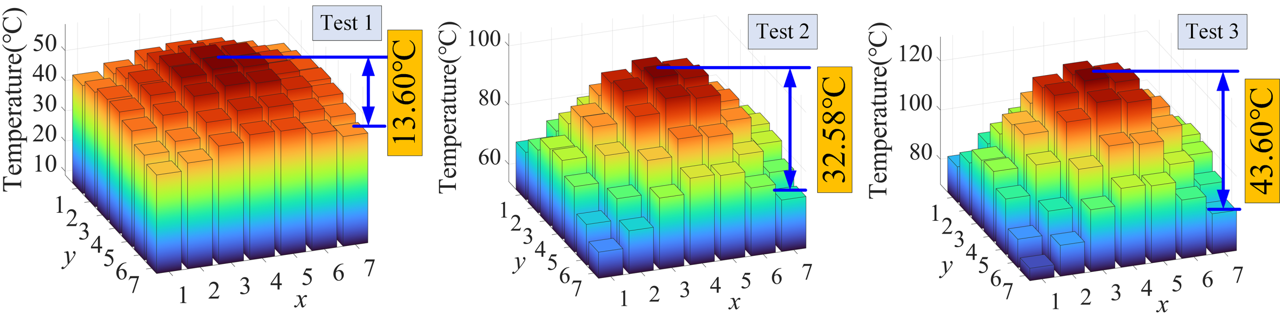



Fig. 15. Simulation results of temperature distribution (time = 400 ms).

TABLE VI
ERROR OF FIELD-CIRCUIT COUPLING MODEL UNDER THE TEST CASE

| | Power | Temperature |
|---|---|---|
| Test 1 | 0.82% | 2.92% |
| Test 2 | 0.21% | 4.25% |
| Test 3 | 0.58% | 3.79% |

the calculated value of the field-circuit coupling model at the same moment as $Val^{i}{}_{\mathrm{ref}}$, and $n$ is the number of samples used for this parameter.

This article validates the proposed model's effectiveness in both time and space dimensions. First, in terms of the time scale, compares the power loss and transient temperature of the chip calculated by the field-circuit coupling model and experimentally measured under different test conditions, where the temperature comparison point is at the center of the chip, as shown in Fig. 8. The results for various test conditions are shown in Fig. 16. From Fig. 16, it can be seen that the power loss and temperature of the chip calculated by the proposed field-circuit coupling model are in good agreement with the experimental results. Then, (22) is employed to quantify the error in the calculated results; the outcomes are presented in Table VI. Notably, the maximum error in the calculated power loss is 0.82%, and the maximum error in the calculated temperature is 4.25%. Both the power loss and temperature exhibit calculation errors below 5%, indicating that the constructed field-circuit coupling model is effective.

In space dimensions, this article calculates the temperature distribution of the chip surface under different test conditions. To facilitate comparison, a line segment between the chip's center point and an edge point is chosen as the temperature comparison line. The position of the temperature comparison line is shown in Fig. 8 and the time of temperature comparison is 0 ms and 400 ms moment. The temperature difference between the chip edge and the chip center point is compared through the line temperature distribution. The temperature of the comparison line is determined by calculating the temperature at each corresponding mesh node along the line. The specific calculation process is illustrated in Fig. 6(b), and the calculation results are shown in Fig. 17. From Fig. 17, it can be seen that the proposed field-circuit coupling model accurately depicts the temperature variation from the chip's edge corner to its center point. The validity of the model is verified in the space dimension.

### *E. Extensibility Analysis*

SiC MOSFETs can be categorized into three structures, which are asymmetric-trench, double-trench, and planar. To demonstrate the universality of the field-circuit coupling method, this article also extends it to double-trench SiC MOSFETs and planar SiC MOSFETs. The double-trench SiC MOSFET (part number: SCT3120AL) is referred to as DUT2, while the planar SiC MOSFET (part number: SCT20N120) is referred to as DUT3. The structural parameters of DUT 2 and DUT 3 were also obtained by FESEM. To facilitate the temperature measurement, DUT2 and DUT3 are also subjected to open-cap processing. Subsequently,

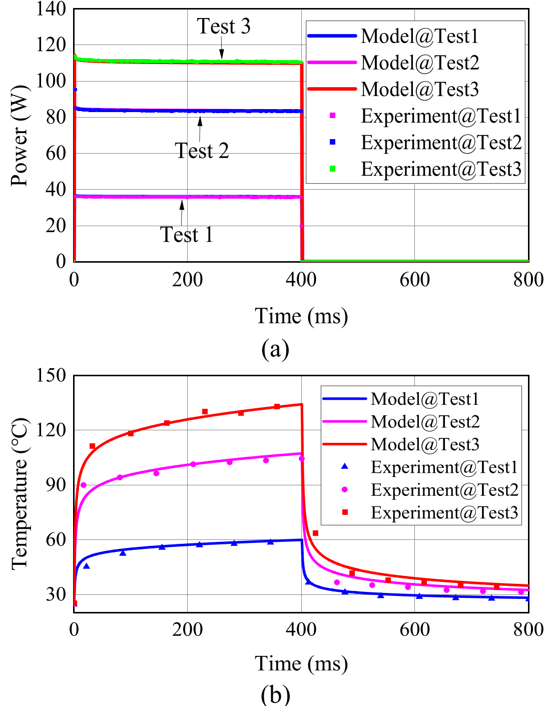



Fig. 16. Comparison of field-circuit coupling modeling and experimental testing on time scales. (a) Power loss. (b) Temperature at the comparison point.

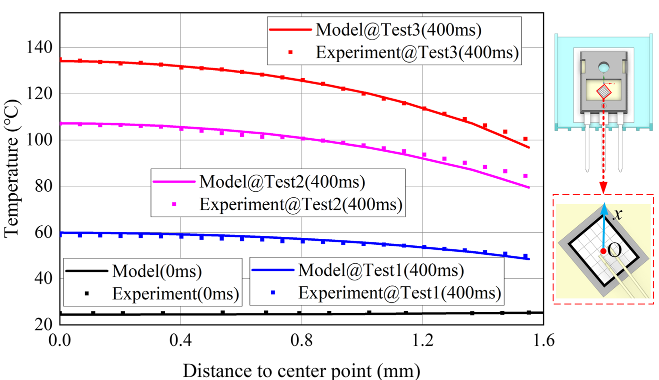



Fig. 17. Comparison of line temperature under different test conditions.

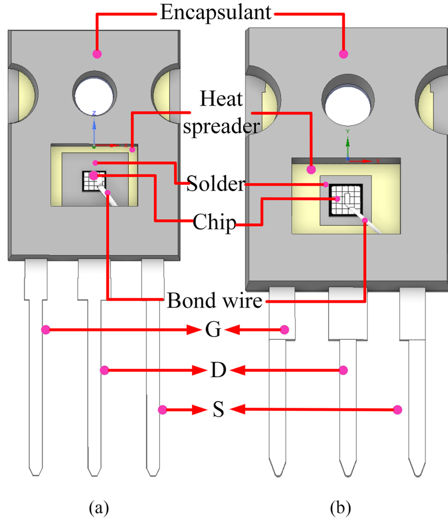



Fig. 18. Three-dimensional models of DUT2 and DUT3. (a) DUT2. (b) DUT3.

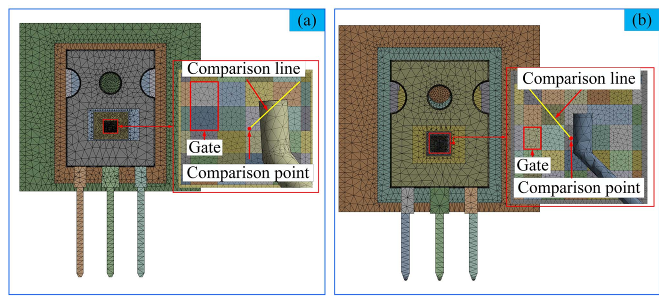



Fig. 19. Mesh of DUT2 and DUT3 thermal modeling. (a) DUT2. (b) DUT3.

TABLE VII
MODEL PARAMETERS OF DUT1 AND DUT2

| | | | | | |
|---|---|---|---|---|---|
| DUT2 | Parameters | $a_1$ | $a_2$ | $a_3$ | $v_1$ |
| | Value | -0.23 | 0.14 | 2.17 | 26.42 |
| | Parameters | $v_2$ | $v_3$ | $g_1$ | $g_2$ |
| | Value | -4.97 | 1.98 | 1.53 | $6.23\times10^{-4}$ |
| DUT3 | Parameters | $a_1$ | $a_2$ | $a_3$ | $v_1$ |
| | Value | 8.29 | -0.71 | 3.69 | 3.27 |
| | Parameters | $v_2$ | $v_3$ | $g_1$ | $g_2$ |
| | Value | -0.34 | 1.77 | 1.63 | $6.64\times10^{-4}$ |

3-D models of the devices are established based on the actual dimensions, as illustrated in Fig. 18.

The active area of the DUT3 chip is similar in size to that of DUT, while the active area of the DUT2 chip is smaller. The active region of DUT2 is divided into 16 cells, and the active region of DUT3 is divided into 25 cells. The thermal models of DUT2 and DUT3 are established based on the method proposed in Section III. The finite element mesh of DUT2 and DUT3, as shown in Fig. 19. Furthermore, based on the method proposed in Section IV, the circuit models of DUT2 and DUT3 are established. When the gate-source voltage $V_{gs}$ is $-5$ V, the circuit parameters of the devices are shown in Table VII, and the forward characteristics of DUT2 and DUT3 at different temperatures are shown in Fig. 20. The validity of the DUT2 and DUT3 field-circuit coupling models was verified by three test conditions, as shown in Table VIII. During the tests, DUT2 and DUT3 dissipate heat through natural convection, and the convective heat transfer coefficient of the heat sink is set to 10 $W/m^2 \cdot K$.

The validity of the field-circuit coupling models of DUT2 and DUT3 is also illustrated through both time and space dimensions. Fig. 19 illustrates the temperature calculation node locations for DUT2 and DUT3, while Fig. 21 presents the results of power loss and temperature calculations under various test conditions for both DUT2 and DUT3. The calculation errors of the devices under different test conditions are computed based on (23), as detailed in Table IX.

From Fig. 21 and Table IX, it can be observed that the device power loss and temperature calculated by the proposed

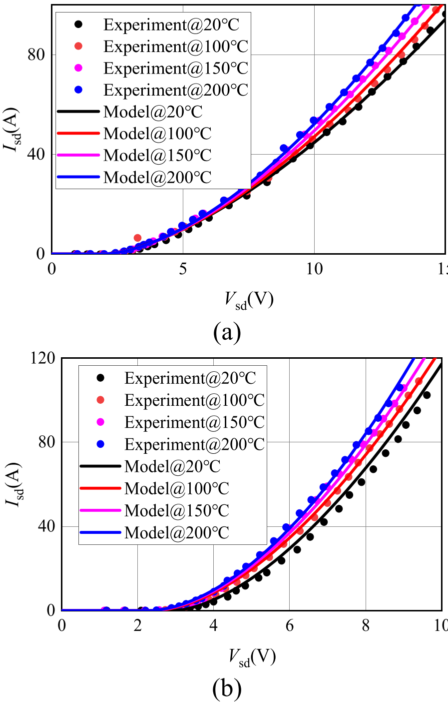



Fig. 20. Forward characteristics of DUT2 and DUT3 at different temperatures. (a) DUT2. (b) DUT3.

TABLE VIII
TEST CONDITIONS OF DUT2 AND DUT3

| | | Current(A) | Heating time (ms) | $T_a$ (°C) |
|---|---|---|---|---|
| DUT2 | Test 1 | 10 | 400 | 18 |
| | Test 2 | 12 | 400 | 18 |
| | Test 3 | 15 | 400 | 18 |
| DUT3 | Test 1 | 6 | 400 | 19 |
| | Test 2 | 12 | 400 | 19 |
| | Test 3 | 18 | 400 | 19 |

TABLE IX
ERROR OF FIELD-CIRCUIT COUPLING MODEL

| | | Power | Temperature |
|---|---|---|---|
| DUT2 | Test 1 | 1.89% | 4.77% |
| | Test 2 | 2.96% | 4.44% |
| | Test 3 | 2.93% | 4.25% |
| DUT3 | Test 1 | 2.08% | 1.24% |
| | Test 2 | 2.63% | 2.82% |
| | Test 3 | 2.30% | 2.36% |

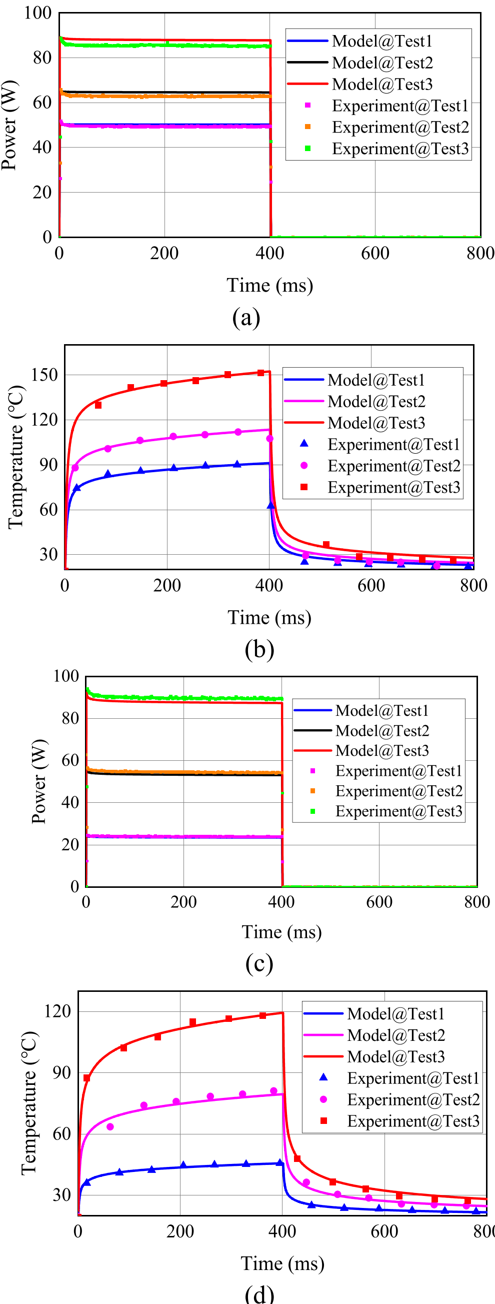



Fig. 21. Comparison of field-circuit coupling modeling and experimental testing on time scales. (a) DUT2 power loss. (b) DUT2 temperature. (c) DUT3 power loss. (d) DUT3 temperature.

field-circuit coupling model are in good agreement with the experimental results. All the calculation errors for power losses and temperatures of each device are below 5%, signifying the effectiveness of the established field-circuit coupling model.

In space dimensions, this article calculates the temperature distribution on the surface of each device under different test conditions. Likewise, the line connecting the center point and the edge point of the chip is designated as the temperature comparison line. The temperature comparison lines for DUT2 and DUT3 are shown in Fig. 19, and the calculation results are shown in Fig. 22. As shown in Fig. 22 the proposed field-circuit coupling model can describe the temperature variation from the edge to the center point of the chip.

## VI. CALCULATION OF JUNCTION TEMPERATURE DURING SURGE PROCESS

This article has successfully established the SiC MOSFET field-circuit coupling model. In this section, the field-circuit coupling model is applied to compute the power loss and temperature distributions of the SiC MOSFET chip during the surge process.

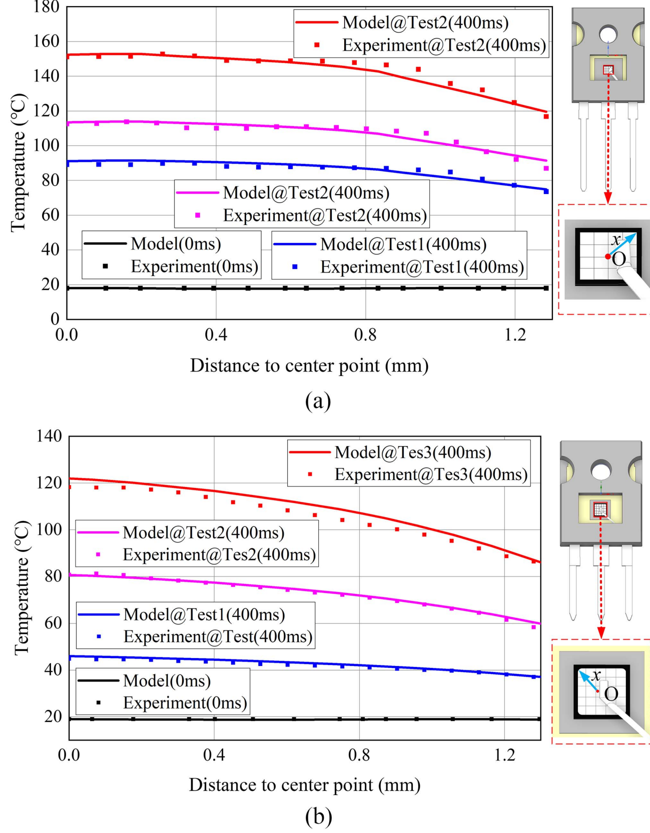



Fig. 22. Comparison of line temperatures under different test conditions. (a) DUT2. (b) DUT3.

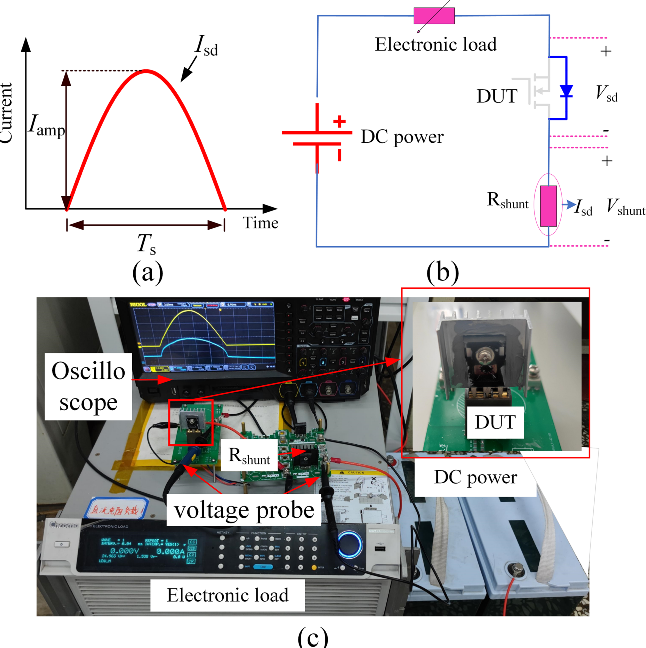



Fig. 23. Experimental platform of surge test. (a) Half-sinusoidal forward current pulse used in surge test. (b) Schematic. (c) Test setup.

TABLE X
SPECIFICATIONS OF THE EXPERIMENTAL PLATFORM

| | Parameter or model |
|---|---|
| Dc source | 24 V |
| Electronic load | Chroma 63212 A |
| $R_{shunt}$ | 100 mΩ |
| DUT | IMW65R048M1H Body Diode |

## A. Experimental Platforms

The surge current is selected as a half-sinusoidal forward current pulse, as shown in Fig. 23(a). The surge current duration is $T_s$ and the amplitude is $I_{amp}$. The schematic diagram of the surge test circuit used in this article is shown in Fig. 23(b), and the physical photograph of the experimental platform is shown in Fig. 23(c). The specifications of the experimental platform are presented in Table X. The surge current for the DUT is applied using the user defined waveform function of the electronic load. At the beginning of the test, the electronic load is triggered to generate a half-sinusoidal forward current. Simultaneously, an oscilloscope and voltage probes were used to record the voltages of the DUT and $R_{shunt}$, which in turn can be used to obtain the current of the DUT.

## B. Calculation Result

In this study, the surge test current amplitudes, $I_{amp}$, are 30 A, 60 A, and 120 A, respectively, with each duration, $T_s$, being 10 ms. After each test, the DUT was cooled for 30 s to return to ambient temperature before proceeding with the next test. The proposed field-circuit coupling model was used to calculate the voltage, current, and temperature of the DUT. The total calculation time $t_{all}$ is set to 10 ms, and the $t_{step}$ is set to an adaptive step size. The calculation results for different surge currents are shown in Fig. 24. Fig. 24(a) displays the voltage and current of the DUT; Fig. 24(b) shows the transient temperature of the comparison point; Fig. 24(c) shows the I-V trajectory of the DUT. The color of the I-V trajectory represents the transient temperature at the comparison point. As shown in Fig. 24(a), the voltage characteristics of the SiC MOSFET devices calculated using the proposed field-circuit coupling model align closely with the experimental values. This alignment serves as validation for the effectiveness of the proposed model. As can be seen in Fig. 24(b), the thermal characteristics of the SiC MOSFET body diode are the same for different amplitudes of surge currents, and the temperature at the comparison point of the chip reaches the maximum value about 6.3 ms after the surge occurs. From Fig. 24(c), it is evident that the I-V trajectories of the SiC MOSFET body diode approximate a crescent shape under various surge currents. This behavior is primarily due to the initial stages of the surge, where the MOSFET's temperature is relatively low. As the surge progresses, the MOSFET's temperature increases, leading to differences in its electrical characteristics.

The power loss and temperature of the SiC MOSFET body diode under the surge condition is higher than that of the conventional condition, which makes the temperature distribution on the chip surface more inhomogeneous. Fig. 25 shows the power loss of each Cell of the SiC MOSFET at the moment of 5 ms after the surge occurs, and Fig. 26 shows the temperature of each Cell of the SiC MOSFET at the moment of 6.3 ms after the surge occurs.

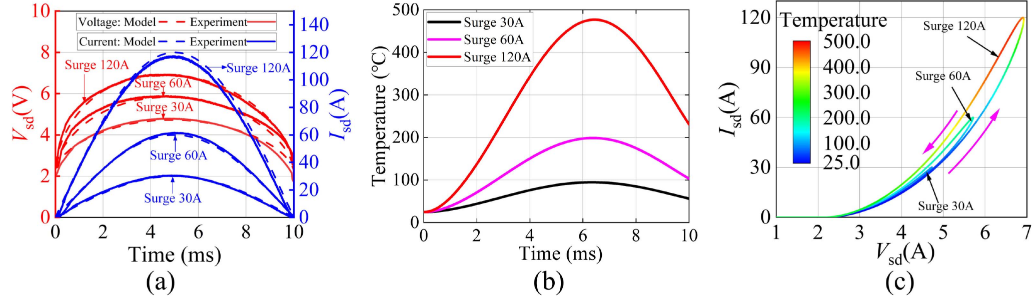



Fig. 24. Results of surge test. (a)$V_{\rm sd}$ and $I_{\rm sd}$. (b) Temperature. (c) *I-V* trajectory.

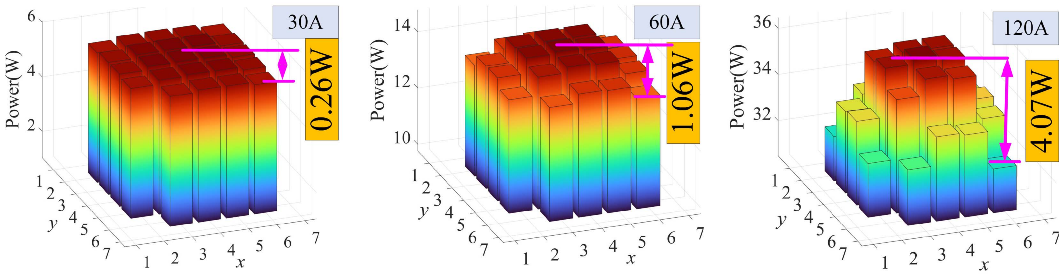



Fig. 25. Power loss distribution of the chip under surge conditions (time = 5 ms).

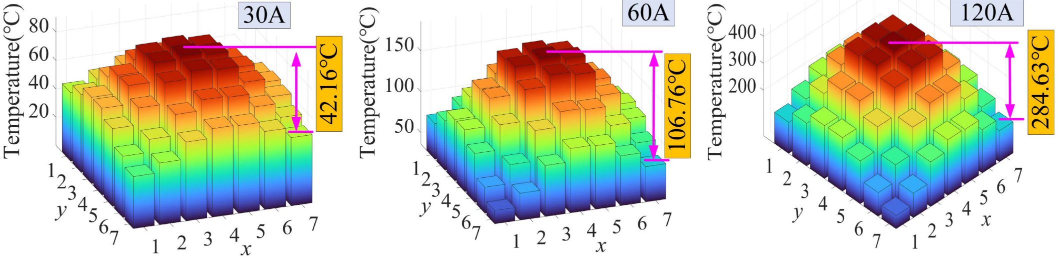



Fig. 26. Temperature distribution of the chip under surge conditions (time = 6.3 ms).

Since Cell 21 corresponds to the gate region of the chip and Cells 26 to 49 correspond to the terminal region, the power loss in these cells can be neglected.

As can be seen in Figs. 25 and 26, the power loss and temperature distribution disparity among each cell of the SiC MOSFET body diode escalate with the surge current amplitude. Thermal coupling effects cause the temperature of the cell in the chip's central region to gradually exceed that of the cell at the edge, even if their initial power losses are identical. This results in the power loss of the central region's cell progressively surpassing that of the edge's cell, consequently accentuating the temperature disparity among each cell. At a surge current of 120 A, the temperature of cell 38, located at the edge of the chip, is 145.44 °C, while cell 13, located in the center region, has a temperature as high as 430.07 °C, indicating a temperature discrepancy of 284.63 °C between these Cells. Neglecting the temperature distribution of the chip would lead to an inaccurate assessment of the chip's surge capability.

### C. Comparison With Thermal Network Models

To substantiate the progress achieved by the electrical-thermal coupling model proposed herein, it is compared with the widely recognized Cauer thermal network model, which is extensively utilized in the industry. Manufacturers generally provide parameters of the power device's Cauer thermal network model. In this article, the device's Cauer thermal network model is coupled with the circuit model and computes device temperatures under varying surge conditions. This article compares the proposed field-circuit coupled model and the Cauer thermal network model under surge current durations, $T_{\rm s}$, of 10 ms and 20 ms. When $T_{\rm s}$ = 10 ms, the calculated results at different surge current amplitudes are shown in Fig. 27. When $T_{\rm s}$ = 20 ms, the calculated results at different surge current amplitudes are shown in Fig. 28

From Figs. 27 and 28, it can be seen that when the surge current is low, the outcomes computed by both models closely

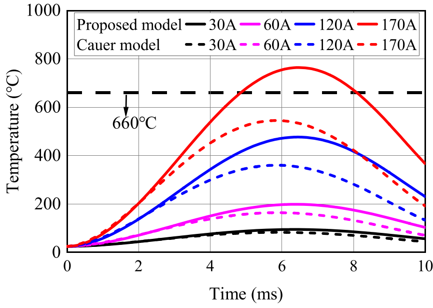



Fig. 27. Calculation results of device temperature under different surge currents at $T_s = 10$ ms. (b) $T_s = 20$ ms.

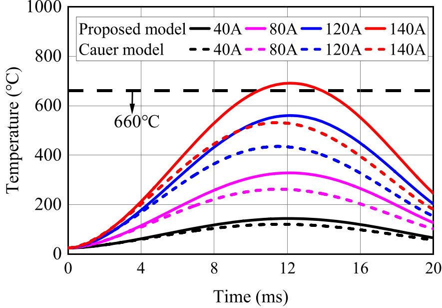



Fig. 28. Calculation results of device temperature under different surge currents at $T_s = 20$ ms.

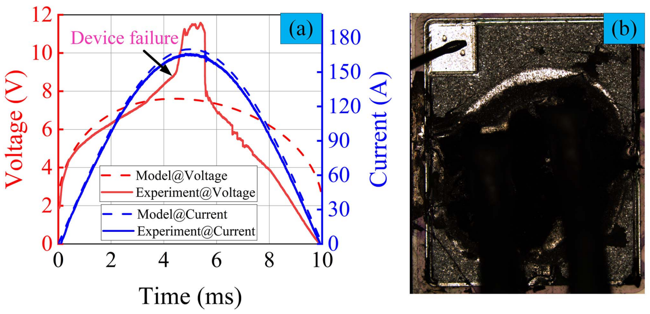



Fig. 29. Results of surge test when $I_{amp} = 170$ A, $T_s = 10$ ms. (a) $V_{sd}$ and $I_{sd}$. (b) Chip surface.

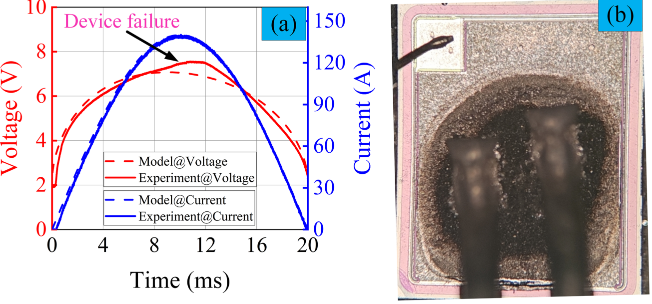



Fig. 30. Results of surge test when $I_{amp} = 140$ A, $T_s = 20$ ms. (a) $V_{sd}$ and $I_{sd}$. (b) Chip surface.

align. However, as the surge current increases, the Cauer thermal network model tends to underestimate the device temperature. When the $I_{amp} = 170$ A and $T_s = 10$ ms, the chip temperature calculated by the Cauer thermal network model is approximately 544 °C, while the model proposed in this article calculated the chip temperature of about 764 °C. This temperature exceeds the melting point of aluminum (660 °C), indicating that under this condition, the device will experience aluminum layer melting. When the $I_{amp} = 140$ A and $T_s = 20$ ms, the chip temperature calculated by the Cauer thermal network model is approximately 531 °C, while the model proposed in this article calculated the chip temperature of about 690 °C. This temperature also exceeds the melting point of aluminum (660 °C).

To validate the effectiveness of the proposed model, tests were conducted on new SiC MOSFET devices using a surge test experimental platform. When $T_s = 10$ ms and $I_{amp} = 170$ A, the device's voltage and current behavior are shown in Fig. 29(a). After the surge test, the device was opened, and the chip surface morphology was photographed using a microscope, as shown in Fig. 29(b). When $T_s = 20$ ms and $I_{amp} = 140$ A, the device's voltage and current behavior are shown in Fig. 30(a), and the chip surface morphology is shown in Fig. 30(b). Figs. 29 and 30 indicate that the device was damaged after the surge test, evidenced by the melting of the chip surface aluminum layer, consistent with the predictions of the proposed model.

### D. Extensibility Analysis

The validity of the field-circuit coupling models for DUT2 and DUT3 was also verified through surge tests. Surge current amplitudes of 20 A, 40 A, 60 A, and 80 A were applied to DUT2, and 20 A, 60 A, 100 A, and 120 A to DUT3, respectively. Specifically, DUT2 was damaged at a surge current of 80 A, and DUT3 was damaged at a surge current of 120 A. Following open-capping, the chip morphologies were examined under a microscope, revealing the melting of the aluminum layers on both DUT2 and DUT3 chips. The temperatures at the center point of DUT2 and DUT3 chip surfaces under different surge currents are shown in Fig. 31.

From Fig. 31, it can be observed that the calculated temperatures by field-circuit coupling models are higher than those calculated by the Cauer thermal network model. Compared to the Cauer model, the field-circuit coupling model proposed in this article successfully predicted the failure of DUT2 and DUT3 under surge current, validating its superiority.

## VII. Limitations and Discussions

When evaluating the surge capability of SiC MOSFETs using the electro-thermal coupling model, it is essential to first identify the failure mechanisms of the device. For asymmetric-trench and planar SiC MOSFETs, the surge current path is through the body diode in the active region, and the failure mechanism is the melting of the chip surface aluminum layer [34]. The model proposed in this article is able to predict the surge reliability of these two types of SiC MOSFETs. For double-trench SiC MOSFETs, a separate discussion is required. When the gate-source voltage $V_{gs}$ is negative, ensuring reliable channel shutdown, the surge current path is through the body diode in the active region, with the failure mechanism being the melting of the chip surface aluminum layer. The model presented in this article can predict surge reliability in this case as well. However, when $V_{gs}$ is 0 V, the

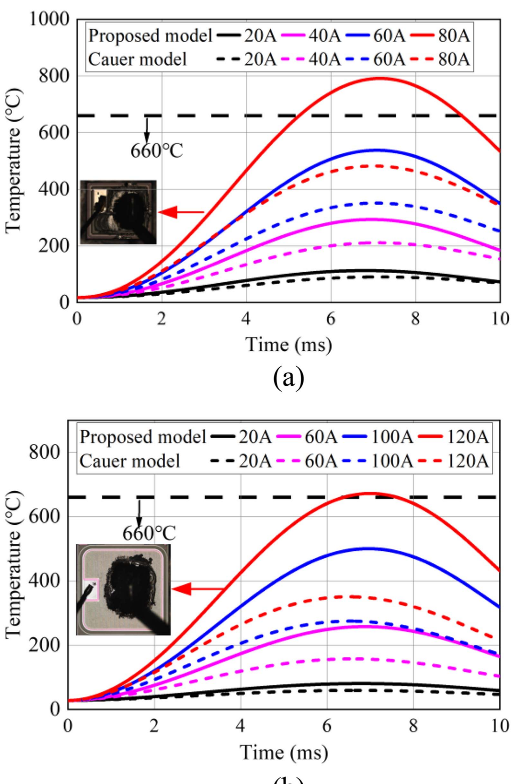



Fig. 31. Temperature of DUT2 and DUT3 under different surge currents. (a) DUT2. (b) DUT3

failure mechanism of dual trench SiC MOSFETs remains unclear [35], [36], which limits the application of the electrothermal model. Research on the failure mechanism of double trench SiC MOSFETs is outside the scope of this article. Nevertheless, as research into the failure mechanisms of double trench SiC MOSFETs progresses, it will be possible to adjust power loss based on their electrothermal characteristics, refine failure criteria, and enhance the applicability of the electrothermal model.

## VIII. Conclusion

This article presents a field-circuit coupling model designed for calculating the junction temperature during the surge process of SiC MOSFET. The model achieves the following: 1) Calculation of chip voltage and power under surge current. 2) Calculation of chip temperature distribution under surge current. The field-circuit coupling model is validated by test conditions and surge conditions. Under the three test conditions, the computational results of the field-circuit coupling model are in high agreement with the experimental results. The computed power loss errors range from 0.21% to 0.82%, while the temperature calculation errors range from 2.92% to 4.25%. Then, a surge test platform for SiC MOSFET is established, and the electrical and thermal characteristics of SiC MOSFET under three surge current amplitudes are computed. The computed voltage drop $V_{\mathrm{sd}}$ of the SiC MOSFET body diode aligns closely with experimental values, reinforcing the effectiveness of the field-circuit coupling model. As surge current amplitude increases, the power loss and temperature distribution inhomogeneity among the cells of the body diode also intensify. Neglecting the chip's temperature distribution under these circumstances would lead to an inaccurate evaluation of its surge capability. Subsequent destructive surge experiments are conducted, and the results show that, compared to the traditional Cauer thermal network model, the model proposed in this article successfully predicted the failure of the SiC MOSFET. The article also extends the field-circuit coupling model to double-trench SiC MOSFETs and planar MOSFETs, verifying the universality of the field-circuit coupling model.

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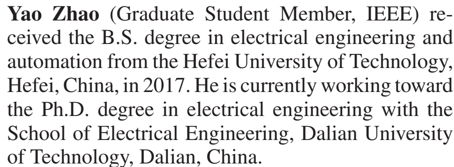

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