Development of a Half-Bridge Cell-Derived All-Inclusive Conducted Emission Noise Model for SiC-Based Single Phase Boost PFC Converter

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***Abstract*—This work presents a novel all-inclusive power electronic converter noise model comprised of both differential-mode (DM) and common-mode (CM) parasitic circuit components. Furthermore, a thorough modeling method and novel experiment-driven methodology to analyze the impact of the DM and CM circuit components on the resultant conducted emission electromagnetic interference in a single-phase power factor correction boost converter rated for 1 kW 120 VAC/400 VDC utilizing silicon-carbide MOSFETs is presented. This is achieved by predicting DM and CM noise corner frequencies and observing DM/CM noise corner frequencies in a novel half-bridge noise cell-based, all-inclusive converter parasitic circuit model. Frequency spectrum results find that eight DM noise corner frequencies are estimated by the proposed all-inclusive noise model with low average error of 6.45%, and the model further successfully identifies lumped CM capacitances present in the power converter system.**

***Index Terms*—Common mode (CM), differential mode (DM), electromagnetic interference (EMI), power factor correction (PFC).**

I. Introduction

FUTURE generation power electronic converter technology is anticipated to be dominated by wide bandgap (WBG) semiconductor devices in most low- and high-voltage, high-power applications areas currently implementing silicon (Si) power MOSFET semiconductor devices [1], [2]. This owes to the fact that GaN and silicone-carbide (SiC) devices exhibit far superior electrical and thermal characteristics over Si MOSFET technology [3], enabling a significant advancement in realizable converter power density and efficiency. However, despite these improvements in electrical and thermal performance, WBG devices do pose a challenge regarding both differential-mode (DM) and common-mode (CM) conducted emission (CE) electromagnetic interference (EMI) stemming from the power converter [4]. This inherent increase in DM and CM noise results in a larger required volume of a passive EMI filter, which could be to the extent that the volumetric reduction in the power conversion stage is nullified [5]. This is especially likely if the filter is oversized for the actual converter CE EMI noise spectrum, and, on the other hand, if the filter is undersized the outcome is then failure to meet CE EMI requirements and delay of product time to market. Thus, it is of utmost importance in the design of a power converter system to adequately model the power stage capacitive C_p and inductive L_p parasitic couplings, and to further understand which L_pC_p combinations most impact DM and CM noise compared to CE EMI standard requirements.

Therefore, the focus of this work is to address the impact of WBG semiconductor devices on CE EMI, for which noise interference within the typical standard 150 kHz–30 MHz frequency band is largely impacted, most prominently within the 1–30 MHz high-frequency band [4], [6], [7], [8], [9]. Across literature in the past few decades, modeling methods have incorporated both time- and frequency-domain calculations and simulations for estimating the DM and CM CE EMI noise spectrum. This is achieved by a variety of methods, such as physics-based calculations and analysis tools, namely partial element equivalent circuit analysis and finite element analysis (FEA) [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. In addition, physical measurements of the converter via a network analyzer, pulsed voltage stimulus, or different short and open circuit tests are commonly performed [19], [20].

In regard to DM CE EMI noise modeling, it has been found that a major noise propagation source is the switched power transfer inductor which may be modeled as an equivalent noise source by fast-Fourier transform of the switched current waveform [10]. However, for a comprehensive modeling of the entire DM noise path, it must be noted that the parasitic circuit elements of the bulk capacitor and the connected converter load itself can also contribute significantly to DM noise [11]. Moreover, for accurate modeling of the DM current noise, the switched inductor current and the effect of its current on the power loop parasitic inductances should additionally be observed, similar to as modeled in [12].

For CM CE EMI noise modeling, the main current propagation paths are through cabling capacitances, switched node capacitance, MOSFET heatsink capacitance, and the capacitance between PCB power/return planes and the conductive test

Received 31 March 2024; revised 23 June 2024 and 21 August 2024; accepted 18 October 2024. Date of publication 23 October 2024; date of current version 18 December 2024. This work was supported by the National Science Foundation under Grant 2236846. Recommended for publication by Associate Editor Z. Chen. *(Corresponding author: Ayan Mallik.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3485035.

Digital Object Identifier 10.1109/TPEL.2024.3485035

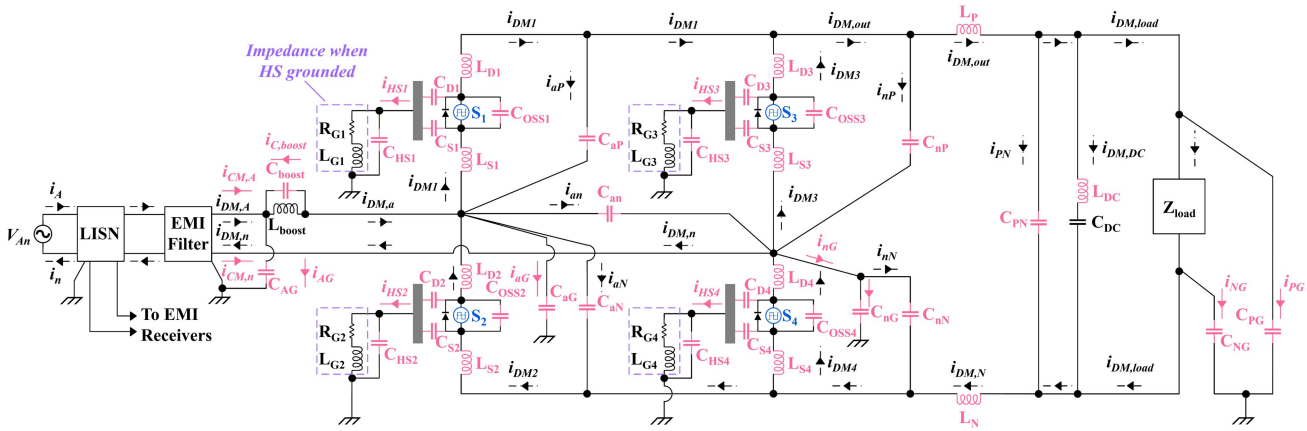

Fig. 1. Single-phase totem pole boost PFC parasitic circuit model.

system protective Earth (PE) plane due to switched voltage transients [11], [12], [14], [15], [16], [18]. Further, it has been found that assuming balanced parasitic circuit components for estimating EMI as a means to derive simplified equivalent circuit models in [13] and [14] results in error for the high frequency 1–30 MHz band, again where WBG devices most impact the noise spectrum. This is because a power electronic converter oftentimes does not have matched parasitic components [9], [15], [21]. Notably for CM CE EMI, the identification of CM capacitances is a challenging task that typically involves iteration of the initial model estimate, done by error minimization in [22] and utilization of a Kalman filter in [23]. Although these works are able to accurately identify CM impedance in unique application scenarios, a universal method for identification of CM capacitances in a power converter does not presently exist.

In consideration of the above-mentioned findings in literature, this article proposes and experimentally validates a heterogeneous noise modeling framework for estimating DM and CM CE EMI in a single-phase totem pole PFC circuit topology utilizing 650 V_{DC} SiC MOSFETs rated for 120 V_{AC}/400 V_{DC} voltage conversion at 1 kW. The goal of this characterization effort is to put forth a widely applicable methodology to estimate parasitic couplings earlier in the power converter design and development process. This is accomplished by physics-based modeling, FEA simulation, and measurement of the DM and CM parasitic components of Fig. 1, excluding the CM capacitances from converter nodes to the test system PE plane. A novel half bridge-cell derived noise source model is next introduced which provides the mixed-DM and CM noise relations of the half-bridge cell and subsequent impact on the neighboring converter circuits. Relevant noise corner frequencies arising from the half bridge-cell noise model interaction with the PFC input/output circuits are then analyzed, and noise corner frequencies internal and external to the boost-cell found. A few works in [5],[24], and[25] have put forth effort in characterization of CE EMI noise corner frequencies, but none have comprehensively investigated both DM- and CM-corner frequencies in a single work along with relative error comparisons between estimated and measured corner frequencies. In [24], only the influence of the self-resonance of the boost inductor in a PFC topology on a few observed DM noise corners, omitting several noise corners observed in the work, is investigated without a detailed error analysis to validate the findings. Further, the work in [25] only provides a theoretical analysis of noise corner frequencies arising from the mathematical derivation of trapezoidal waveforms, however, no experimental validation to the hardware platform is provided and thus the work lacks in providing a practically useful noise corner frequency framework. Finally, the study in [5] only provides estimation for two CM noise corner frequency estimates centered around the MOSFET heatsink capacitance with no comprehensive error analysis, and does not provide insight into several corner frequencies also observed in the noise spectra results.

This work instead aims to characterize all major noise corner frequencies found in both the DM and CM noise spectra of a single-phase totem-pole PFC converter with comprehensive error analysis. The objective of characterizing the DM and CM noise corner frequencies is to aid in the design of EMI filters, both by enabling EMI prediction during converter design before hardware fabrication by use of analytical equations and FEA simulation to construct an all-inclusive parasitic circuit model, and also by experimental measurement during converter prototyping. This allows the designer to anticipate unexpected increases in DM and CM EMI noise magnitudes and avoid an in-compliant DM/CM EMI filter design or an overdesigned filter that detriments the system power density. Furthermore, estimation of noise corner frequencies serves to aid in considering the DM and CM frequency response of both the EMI filter design and power converter, mitigating the risk of poor high frequency filter performance that can be caused by parasitic circuit interaction. Moreover, a novel method to experimentally characterize CM capacitances of a power converter, that is adaptable for other power converter typologies and output load types, is introduced and thoroughly tested allowing for deterministic calculation of ground leakage current. This aids in adhering to touch-current safety standard requirements [26]. The theoretical analysis is then validated via comparison to operational single-phase boost PFC CE EMI noise spectrum measured across four operating points of 1) 120 VAC/400 VDC 1 kW, 2) 120 VAC/400 VDC 500 W, 3) 85 VAC/400 VDC 500 W, and 4) 85 VAC/400 VDC 250 W.

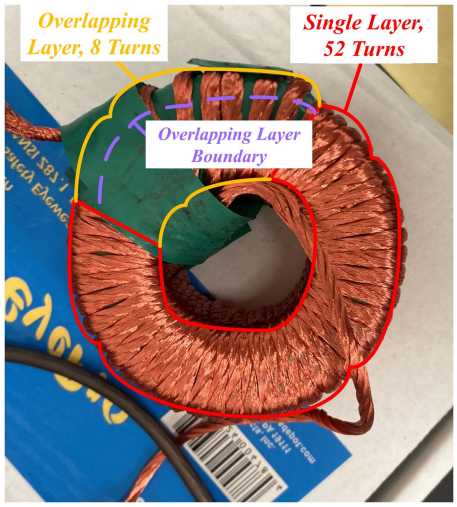

Fig. 2. Single phase totem pole PFC boost inductor.

The key contributions of this work are as follows.

1) Development of a heterogeneous modeling methodology comprised of physics-derived computations and FEA-based simulation for initial estimation of parasitic coupling components in a power converter to enable prehardware prototype EMI prediction.
2) Formulation of a novel half-bridge noise cell derived from parasitic coupling components, and the resultant impact of the parasitics-integrated half-bridge cell on the all-inclusive noise model of a single-phase totem pole PFC converter using superposition of voltage- and current-mode multitone noise sources.
3) A novel, experimentally driven methodology to validate the derived noise circuit model by correlation of noise corner frequencies observed in the measured CE EMI spectrum of a power converter to estimated noise corner frequencies formulated based on possible parasitic L_pC_p couplings as per the all-inclusive noise model.
4) A novel experimental method to characterize the CM capacitance of the power converter by reformulation of the measured CE EMI noise spectrum through insertion of a known-value external capacitance.

II. Modeling of Power Component and PCB Conductive Plane Parasitic Couplings

A. Boost PFC Inductor Model

The boost inductor installed in the single phase boost PFC converter under study is shown in Fig. 2. Equation (1) is considered for analytically determining the inductance L_{boost}, where magnetic core permeability μ_r, cross-sectional area A_c, and effective magnetic path length l_c are found from core datasheet parameters in [27] for 60 turns

$$L_{\text{boost}} = \frac{N^2 \mu_r \mu_0 A_c}{l_c}. \tag{1}$$

Then, for the analytical approximation of the parasitic capacitance C_{boost} it is observed that, of the 60 total turns wound upon the magnetic core in Fig. 2, 52 turns reside on a single nonoverlapped layer while the remaining eight turns reside on a second layer, overlapping the initial eight turns of the first layer. First, the respective turn-to-turn capacitances $C_{\text{tt},1}$, corresponding to $C_{1,2}$–C_{51-52} and C_{43-44}–C_{49-50} in Fig. 3, and $C_{\text{tt},2}$, corresponding to C_{42-43}, C_{1-43}, C_{1-44},..., C_{7-49}, C_{7-50}, and C_{8-50} in Fig. 3, are found by the method of [28]. To facilitate this, the approximate angle of the electric field induced is computed in (2), where d_{w0} and d_w correlate to the core outer and inner diameter, respectively, and ϵ_{r1} is the dielectric constant of the winding coating material. Then, the elementary interturn and airgap capacitances are found in (3) and (4) considering mean length turn (MLT) l_T of a single winding. Here, it must be noted that $\epsilon_{r2} = 1$ for nonoverlapping winding layers, and $\epsilon_{r2} \neq 1$ for overlapping winding layers to account for the green polyvinyl chloride (PVC) tape installed in-between winding layers.

The resultant turn-to-turn capacitances are lastly found as $C_{\text{tt},1}$ for the first winding layer in (5), and as $C_{\text{tt},2}$ for the second winding layer in (6). All inputs to these expressions are found considering the dielectric constant of PVC tape at ambient temperature, approximate winding MLT from the core datasheet in [27] for l_{T1}, which is extended to find l_{T2} considering the geometry of two overlapping winding turns, and the Litz wire datasheet parameters in [29]. Plugging these parameters into (5) and (6) results in a $C_{\text{tt},1} = 6.8321$ pF and $C_{\text{tt},2} = 47.47$ pF, respectively. The equivalent lumped capacitance of the nonoverlapping capacitances is approximated as $3.366C_{\text{tt},1}$, and the equivalent lumped capacitance of overlapping capacitance approximated as $1.83C_{\text{tt},2}$. As the lumped capacitances appear in parallel with one another, the resultant boost inductor parasitic capacitance C_{boost} is computed in (7)

$$\theta = \cos^{-1}\left(1 - \frac{\ln\left(\frac{d_{w0}}{d_w}\right)}{\epsilon_{r1}}\right) \tag{2}$$

$$C_{it} = 2\int_0^{\theta} \frac{\epsilon_{r1}\epsilon_0 l_T}{2\ln\left(\frac{d_{w0}}{d_w}\right)} d\theta \tag{3}$$

$$C_g = 2\int_0^{\frac{\pi}{2}} \frac{\epsilon_{r2}\epsilon_0 l_T}{2\ln 1 - \cos\theta} d\theta \tag{4}$$

$$C_{\text{tt},1} \approx \epsilon_0 l_{T1}\left(\frac{\epsilon_{r1}\theta}{\ln\left(\frac{d_{w0}}{d_w}\right)} + \cot\left(\frac{\theta}{2}\right) - 1\right) \tag{5}$$

$$C_{\text{tt},2} \approx \epsilon_0 l_{T2}\left(\frac{\epsilon_{r1}\theta}{\ln\left(\frac{d_{w0}}{d_w}\right)} + \epsilon_{r2}\cot\left(\frac{\theta}{2}\right) - 1\right) \tag{6}$$

$$C_{\text{boost}} \approx 3.366C_{\text{tt1}} + 1.83C_{\text{tt2}}. \tag{7}$$

B. SiC MOSFET Heatsink Capacitance Model

Generally, the installation of a MOSFET onto the thermal heatsink is as depicted in Fig. 4(a), where the red arrow

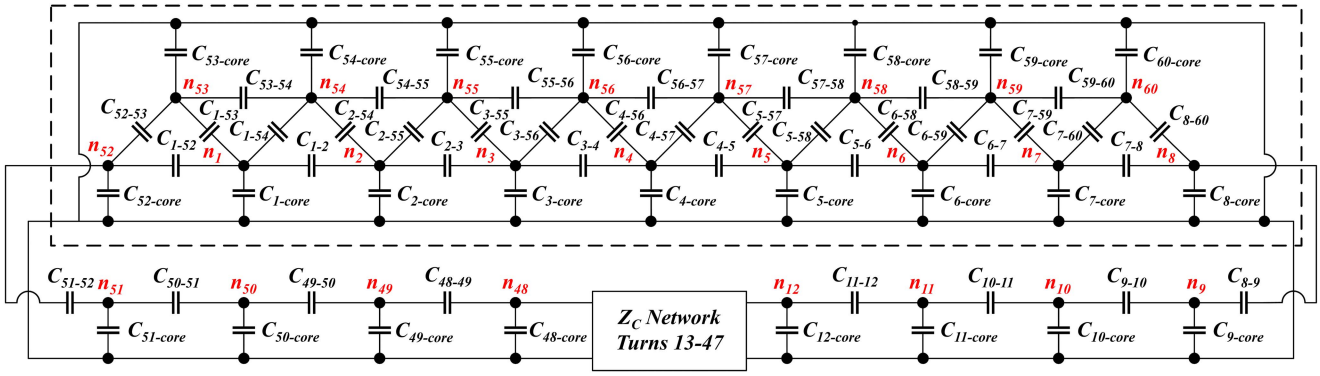

Fig. 3. Magnetic core inductor parasitic capacitance model.

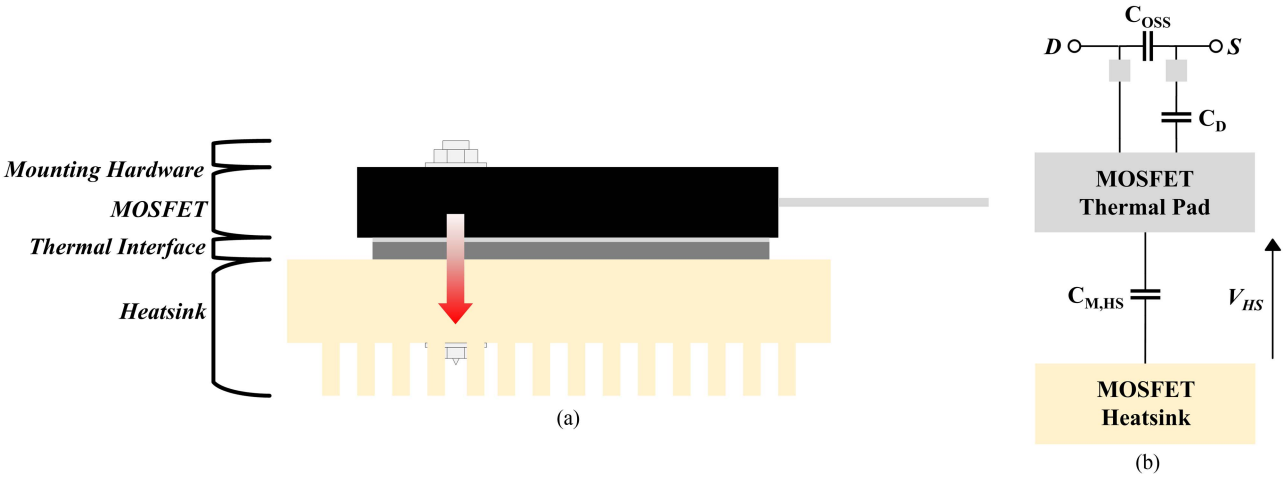

Fig. 4. SiC MOSFET heatsink installation. (a) Physical representation. (b) Equivalent circuit model.

demonstrates the thermal dissipation path. The mounting hardware consists of a screw, nut, and thermal washer which guarantee a flush surface between the MOSFET body thermal pad area, thermal interface material (TIM), and heatsink. The physical representation of the MOSFET-to-heatsink installation correlates to an equivalent circuit model in Fig. 4(b), where C_{OSS} is the C3M0120065PD MOSFET output capacitance, C_S the parasitic capacitance between the MOSFET source terminal and TIM thermal pad, and $C_{M,\text{HS}}$ the parasitic capacitance of the region in-between the TIM thermal pad and MOSFET heatsink. Due to the proximity of these regions, it is assumed that fringing electric field effects are negligible, thus, (8) is then derived considering the overlapping region. Here, $\epsilon_{r,M}$ is the dielectric constant of the TG-A126X-150-150-0.5 TIM pad Si elastomer material, t_M the TIM thickness from, and A_{pad} the MOSFET thermal pad area. As $C_{M,\text{HS}} \gg C_D$, (8) is considered to be the approximate parasitic capacitance of the heatsink, with a resultant value of 8.36 pF per parameters from [30] and [31]

$$C_{M,\text{HS}} = \frac{\epsilon_0 \epsilon_{r,M} A_{\text{pad}}}{t_M}. \tag{8}$$

C. PCB Conductive Plane Capacitance and Inductance Model

In order to determine the mutual-capacitance and self-inductance of PCB conductive planes without physical measurement, FEA simulation is carried out by use of ANSYS Q3D. The suggested PCB interconnect modeling and FEA simulation process is depicted in Fig. 5. Referring to Fig. 1, FEA simulation allows for partially determining all $L_{S,j}$ and $L_{D,j}$ for $j \in [1, 2, 3, 4]$. In addition, interplane capacitances C_{an}, C_{aP}, C_{aN}, C_{nP}, C_{nN}, and C_{PN} of Fig. 1 which naturally arise in the PCB design are further extracted. This is done as, if there were to be significant capacitance between the conductive planes, considerable switched noise current propagation could occur and detriment converter operation.

Equation (9) demonstrates the general expression for computing overlapping plane capacitance considering both parallel plate and fringing field effects which, due to the per-segment capacitances appearing in parallel to one another, is the summation of I number of overlapping areas considering the prepreg material dielectric constants $\epsilon_{r,\text{prp}}$, overlapping area $l_{\text{ol},i} w_{\text{ol},i}$ per segment, height between conductive planes $h_{P,N}$, and the conductive plane thickness t_{cu} [32]. In the single-phase PFC converter under study, the only overlapping plane area is between

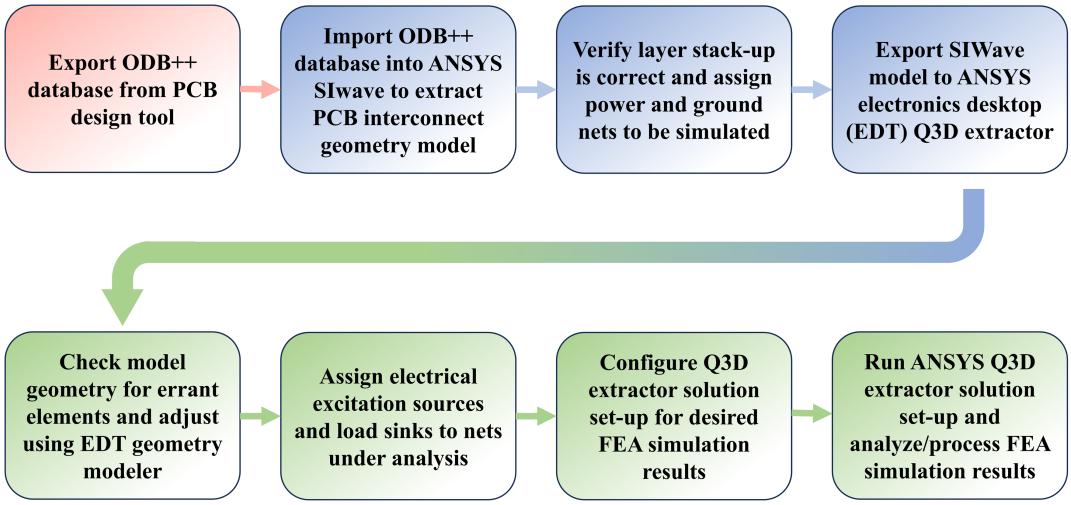

Fig. 5. PCB interconnect modeling and simulation steps.

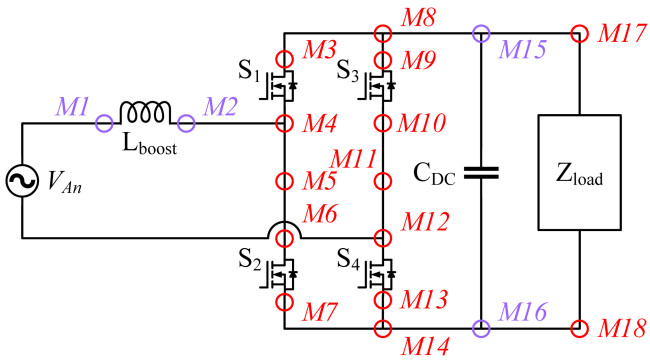

Fig. 6. Single-phase totem pole boost PFC circuit parasitic measurement points.

TABLE I
FEA SIMULATION RESULTS, SINGLE-PHASE TOTEM POLE BOOST PFC INTERCONNECT INDUCTANCES

Measurement point	Simulated inductance
$M4-M5$	L_{S1} = 12.57 nH
$M3-M8$	L_{D1} = 24.96 nH
$M7-M14$	L_{S2} = 17.48 nH
$M5-M6$	L_{D2} 12.66 nH
$M10-M111$	L_{S3} = 12.76 nH
$M8-M9$	L_{D3} = 24.53 nH
$M13-M14$	L_{S4} = 13.26 nH
$M11-M12$	L_{D4} = 12.85 nH
$M8-M15$	L_P = 27.00 nH
$M14-M16$	L_N = 55.66 nH

the primary and neutral conductors, and therefore this expression only applies to $C_{P,N}$ in Fig. 1. From FEA simulation results considering the parasitic PCB capacitance between measurement points M15–M16 in Fig. 6, it is found that $C_{P,N} = 125.70$ pF, which is large enough to be a contributor of CE EMI noise within the 150 kHz–30 MHz frequency band, and is considered in the parasitic circuit model.

For capacitance between adjacent conductive planes in the same PCB layer (10) shown at the bottom of the next page, is considered, where $\epsilon_{r,\text{adj}}$ is the dielectric constant for material medium between conductors, g_c is the gap distance, $l_{\text{adj}} w_{\text{adj}}$ the overlapping area width and length, $h_{c,r}$ the height of the planes to the overall power return plane, and $C_{c,\text{gnd}}$ the capacitance to the return plane which is found considering (9) [32]. For the single phase boost PFC, this applies to capacitances C_{an}, C_{aP}, C_{aN}, C_{nP}, and C_{nN}. From FEA simulation results, it is found that all adjacent plane capacitances are <1 pF. Therefore, these capacitances are considered to be negligible contributors of CE EMI noise, and are omitted in the parasitic circuit model

$$C_{\text{ol}} = \sum_{i}^{I} \epsilon_0 \epsilon_{r,\text{prp}} l_{\text{ol},i} \left(1.15 \left(\frac{w_{\text{ol},i}}{h_{P,N}} \right) + 2.8 \left(\frac{t_{cu}}{h_{P,N}} \right)^{0.222} \right) \tag{9}$$

As for FEA simulation of the PCB interconnect, all electrical excitation sources and load sinks are defined per Fig. 6 and the measurement points listed in the left column of Table I, for which the self-inductance of each segment is found for derivation of parasitic inductances which are partial solutions of $L_{S,j}$ and $L_{D,j}$ for $j \in [1,2,3,4]$ in Fig. 1. In addition to FEA simulation of the PFC PCB interconnect, a step file for the C3M0120065D MOSFET available from Wolfspeed is imported into Q3D to extract the drain and source lead inductance. The results of FEA simulation are presented in the right column of Table I, which accounts for the sum of the PCB interconnect and step file solutions for the overall parasitic MOSFET drain and source inductance estimate

III. PARASITIC MEASUREMENT EXTRACTION OF SINGLE-PHASE BOOST PFC

Parasitic measurements for relevant parameters in Fig. 1 which are measurable by a Bode 100 vector network analyzer (VNA) are performed. Referring to Fig. 6, measurements are made in-between M1 and M2 for determining the boost inductor lumped parasitic capacitance C_{boost}, between various combinations of M3–M11 and M14, M15 to extract the PCB trace inductances and FET source and drain inductances which individually

are partial elements of the $L_{S,j}$ and $L_{D,j}$, $j \in [1,2,3,4]$ parasitics, and between M12 and M13 to extract dc link inductance L_{DC} and capacitance C_{DC} of Fig. 1. For the boost inductor, an impedance adapter is employed with test setup per [33], which enables accurate measurement of magnetic components over a $20\,\text{m}\Omega - 600\,\text{k}\Omega$ impedance range. Fig. 7(a) demonstrates the resultant impedance magnitude over frequency, for which in the low-frequency inductive region the measured boost inductance is extracted by $L_{\text{boost}} = \frac{Z_{L,\text{boost}}}{2\pi f}$. The first resonant mode occurs at $f_{r1} = 566.8$ kHz and therefore the first resonance parasitic capacitance is extracted by $C_{\text{boost}} = \frac{1}{4\pi^2 f_r^2 L_{\text{boost}}}$, yielding 116.64 pF. Therefore, the estimated boost inductor parasitic capacitance value $C_{\text{boost}} = 109.87$ pF found in Section III is in close agreement with –5.8% error.

For the lumped half-bridge inductances $L_{S,j}$ and $L_{D,j}$, $j \in [1,2,3,4]$, the Bode 100 VNA is setup in its shunt-through measurement configuration, suitable for low impedance measurements from $1\,\text{m}\Omega - 100\,\Omega$ [33] with test leads oriented in a kelvin connection to reduce any lead inductance error. For any measurement in which an SiC MOSFET is not directly in the path, the converter is completely de-energized. However, for measurements between M4–M15, M9–M15, M6–M16, and M11–M16, the respective MOSFETs in the path are biased on to ensure the channel is conductive. Example measurement results for both PCB interconnect and MOSFET drain-to-source inductance are presented in Fig. 7(c) and (d). In both cases it is found that a linearly increasing impedance region, which correlates to a predominantly inductive impedance under measurement, begins around a frequency of 100 kHz and lasts until 600–900 kHz owing to the small impedance magnitude of the PCB traces and MOSFET leads. Due to the equivalent inductance being very close to what is expected, these regions alone are considered by taking the average inductance in the linearly increasing impedance region over the valid frequency range. The eventual inductances present at the drain and source terminals, respectively, are determined by assuming that half the measured drain-to-source inductance can be equally distributed between the switch nodes. The distributed drain-to-source inductances are then summed with the measured conductive plane inductances found between measurement points for the final solution of all $L_{S,j}$ and $L_{D,j}$, $j \in [1,2,3,4]$.

For the dc link impedance Z_{DC}, the series-through measurement setup is used, suitable for impedance measurements within $1\,\text{k}\Omega - 1\,\text{M}\Omega$ [33]. The dc link hardware consists of a 1 mF capacitor C_{DC1}, with equivalent series inductance (ESL) L_{DC1}, in parallel with five 22 μF capacitors C_{DC2}, with respective ESL L_{DC2}, for an ideal 1.1 mF capacitance. Equation (11) shown at the bottom of the this page, then presents the equivalent dc link impedance expression, where it is evident that there is a purely capacitive term expressed as the sum of parallel capacitances. The dc link inductances are, however, evidently a more complex solution.

TABLE II
SIMULATED AND EXPERIMENTALLY MEASURED PARASITIC COMPONENTS OF SINGLE-PHASE TOTEM POLE BOOST PFC

Parasitic component	Simulated value	Experimental value	Error
L_{boost}	678.78 μH	676.00 μH	+0.41%
C_{boost}	109.87 pF	116.64 pF	–5.80%
C_{DC}	1.10 mF	994.75 μF	–9.57%
L_{S1}	12.57 nH	15.09 nH	–16.70%
L_{D1}	24.96 nH	16.81 nH	+48.48%
L_{S2}	17.48 nH	13.37 nH	+30.74%
L_{D2}	12.66 nH	15.33 nH	–17.42%
L_{S3}	12.75 nH	16.91 nH	–24.60%
L_{D3}	24.53 nH	16.68 nH	+47.06%
L_{S4}	13.26 nH	17.38 nH	–23.71%
L_{D4}	12.85 nH	17.10 nH	–24.85%
L_P	27.00 nH	26.10 nH	+3.45%
L_N	55.66 nH	55.66 nH	0.00%

From measurement of the installed dc link in Fig. 7(b), it is found that the exact dc link capacitance is 994.75 μF with an approximate lumped ESL of 851.78 nH, for which the average values over the nearly constant inductance and capacitance regions throughout the valid frequency range in the respective plots are considered. These regions are observed due to the inherent resonance of the dc link, where the capacitive impedance is predominant for frequencies $f \ll f_{r,\text{link}}$, whereas inductive impedances are predominant for frequencies $f \gg f_{r,\text{link}}$. These results are within the expected value as the 1 mF capacitor used has a $\pm 20\%$ tolerance and, considering the capacitive term of (11), the remaining capacitors are approximately 22 μF. Finally, the MOSFET heatsink capacitance is measured by the series-through connection, with the network analyzer source connected to the MOSFET drain pin and measurement input to the heatsink bonding pin. From this, a value of $C_{M,\text{HS}} = 26.25$ pF is measured, which is three-times larger than the analytically estimated value of 8.36 pF, indicating that the interfin capacitance in the heatsink structure must additionally be considered for an accurate analytical estimate.

Table II consolidates all comparable analytically derived/simulated and experimentally measured parasitic component values with respective errors shown as appropriate. From the comparison, an average estimation error of 19.44% is found. Therefore, values found herein Section II may be used as a benchmark for checking parasitic circuit values measured by VNA herein Section III. Moreover, the power converter modeling framework developed in Section II can be used to develop an early design phase power converter CE EMI noise model, and

$$C_{\text{adj}} = \epsilon_0 \epsilon_{r,\text{adj}} \frac{g_c l_{\text{adj}}}{h_{c,r}} \left(1.15 \left(\frac{w_{\text{adj}}}{h_{c,r}} \right) + 2.8 \left(\frac{t_{cu}}{h_{c,r}} \right)^{0.222} + 0.03 \left(\frac{w_{\text{adj}}}{h_{c,r}} \right) + 0.83 \left(\frac{t_{cu}}{h_{c,r}} \right) - 0.07 \left(\frac{t_{cu}}{h_{c,r}} \right)^{0.222} \right) + C_{c,\text{gnd}}. \tag{10}$$

$$Z_{\text{DC,eq}}(\omega) = \frac{1 + \omega^4 L_{\text{DC1}} L_{\text{DC2}} C_{\text{DC1}} C_{\text{DC2}} - \omega^2 \left(L_{\text{DC1}} C_{\text{DC1}} + L_{\text{DC2}} C_{\text{DC2}} \right)}{j\omega \left(5 C_{\text{DC2}} + C_{\text{DC1}} \right) - j\omega^3 \left(L_{\text{DC1}} C_{\text{DC1}} C_{\text{DC2}} + L_{\text{DC2}} C_{\text{DC1}} C_{\text{DC2}} \right)}. \tag{11}$$

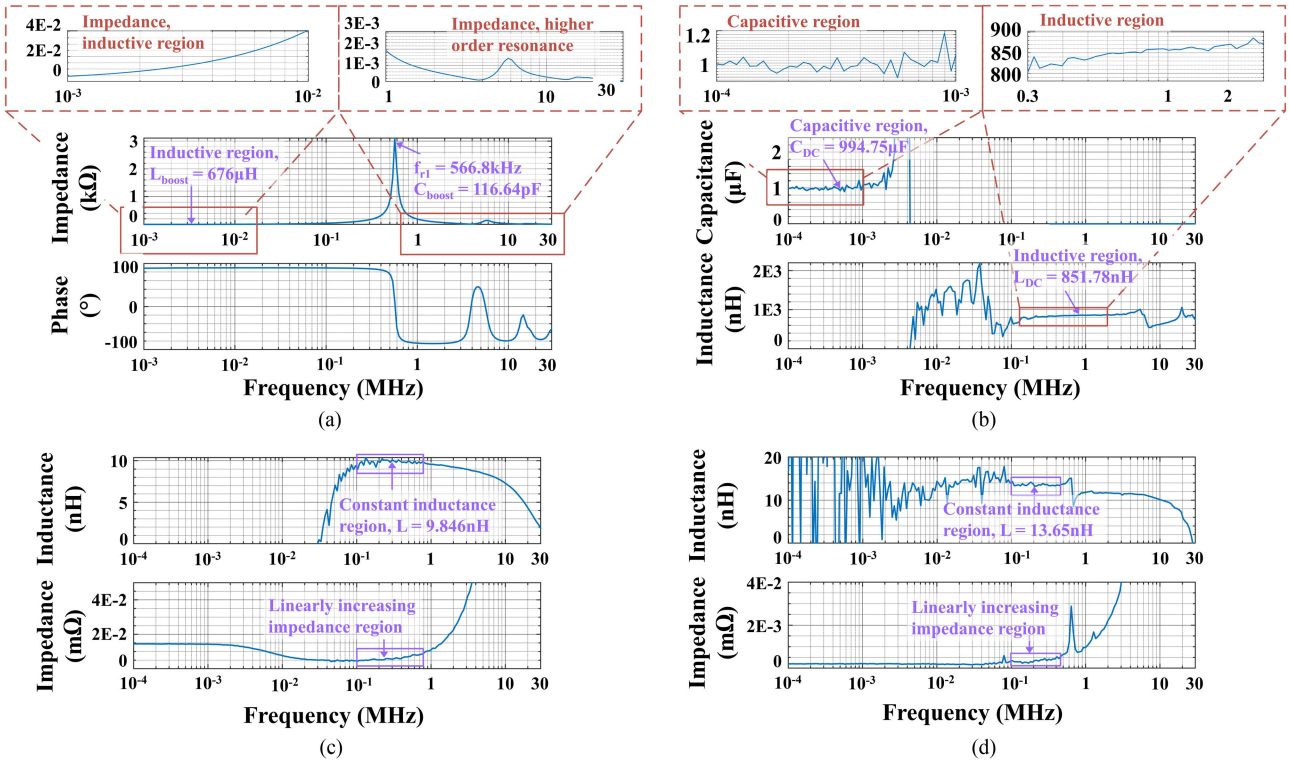

Fig. 7. Bode 100 measurement results for (a) boost inductor, (b) DC link, (c) trace inductance from S3 drain to S5 drain, (d) drain-to-source inductance for S5.

values may be updated posthardware fabrication by use of VNA measurement.

For the remaining parasitic capacitances in the circuit, $C_{PN} = 125.70$ pF found via FEA simulation in Section II is considered, the C3M0120065PD MOSFET device datasheet [30] provides estimated values for $C_{\text{OSS}}(0V) = 700$ pF and $C_{\text{OSS}}(V_{\text{DS}}) = 5.5$ pF, and for the MOSFET heatsinks the VNA is again used, where a measured value of $C_{\text{HS}} = 26.25$ pF is considered. Hence, owing to the close agreement of simulated and experimentally measured values in Table II, estimated stray inductance, magnetic component, and PCB interconnect capacitance parasitic circuit parameters are verified via a combination of device datasheet inspection, FEA simulation, and VNA measurement. In addition, as will be investigated further in Section V, noise corner frequencies observed in the measured CE EMI spectra provide a further validation point of the parasitic circuit parameters found in Table II. For validation of CM capacitances, such as C_{HS}, a novel experimental reconstruction of the CM EMI noise spectrum by insertion of capacitors between the input/output terminals and test system PE plane will be carried out and discussed in detail in Section V.

IV. Equivalent Current-Mode and Voltage-Mode Noise Source Modeling and CE EMI Noise Characterization

Considering the convention for currents $i_{\text{DM},A}$, $i_{\text{DM},n}$, $i_{\text{CM},A}$, and $i_{\text{CM},n}$ in Fig. 1, the overall power converter DM current as seen by the source-side is split per (12) and (13). This allows for analysis of the DM and CM current spectra independently as seen by an EMI test line-impedance stabilizer network (LISN) and EMI receiver termination impedance [21]. From observing these simple current expressions and the current paths of Fig. 1, it is evident that the half-bridge cells performing the boosting function (switches S_1 and S_2, which operate with $f_{\text{sw}} = 100$ kHz) and inductor biasing (switches S_3 and S_4, which operate with $2f_{\text{line}} = 120$ Hz) introduce a sizeable amount of terms to the overall DM and CM current components. Moreover, the CE DM and CM EMI noise is induced from switching instances at the MOSFET drain and source terminals, causing high-frequency oscillation voltages V_D and V_S which then propagate as high-frequency currents throughout the parasitic coupling components. Therefore, a novel half-bridge noise cell model is proposed, consisting of seven total nodes containing both DM and CM current components, as presented in Fig. 8

$$i_{\text{DM}} = \frac{i_{\text{DM},A} - i_{\text{DM},n}}{2} \tag{12}$$

$$i_{\text{CM}} = \frac{i_{\text{CM},A} + i_{\text{CM},n}}{2}. \tag{13}$$

A. Half Bridge-Cell Equivalent Noise Source Model

Fig. 8 demonstrates the model for the half bridge-cell equivalent noise source. Comparing to Fig. 1, this model individually considers the current propagation paths nearby the complementary switch pairs S_1/S_2 and S_3/S_4. As the model is generic and applies to both switching legs in the single-phase PFC converter, Fig. 8 generically denotes the top-switch as S_1 and

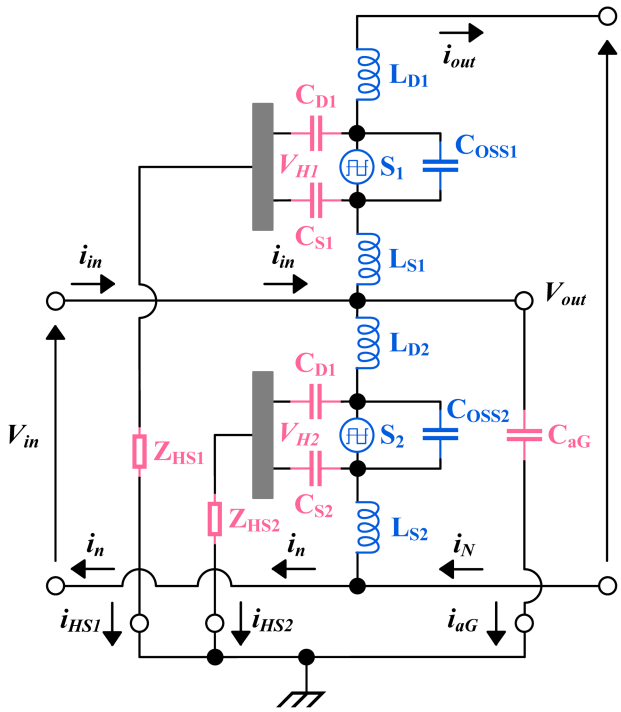

Fig. 8. Half bridge cell noise model.

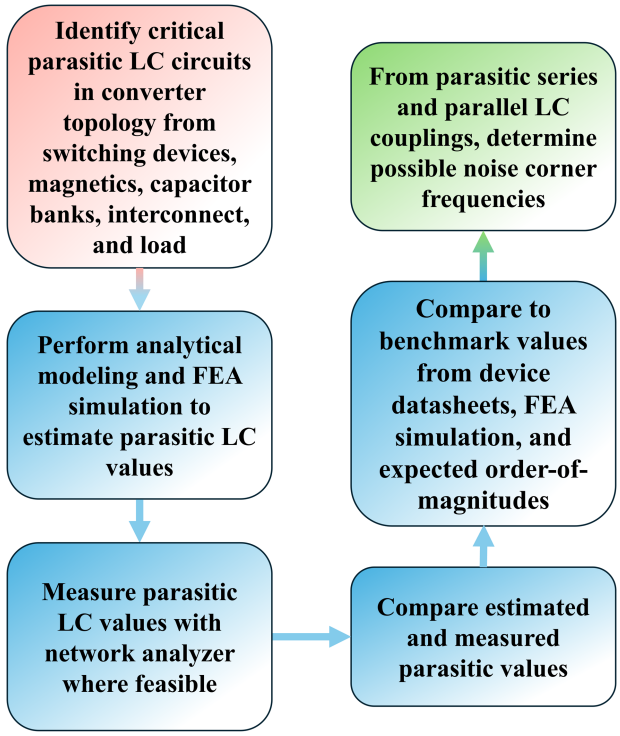

Fig. 9. Power converter parasitic circuit modeling flowchart.

bottom-switch S_2. Node (1) corresponds to the switching node comprised of both DM- and CM-components, node (2) the neutral current and voltage as seen by the power source, and similarly two output nodes (3) and (4) are further defined as the output voltage/current and load-side neutral connection as seen downstream from the half-bridge noise cell. Again, nodes (2), (3), and (4) consist of mixed DM- and CM-components, but nodes (5)–(7) finally represent the current flow from MOSFET heatsinks and switch node capacitance to the PE plane, and therefore are comprised of CM current components only.

Considering these parasitic elements as equivalent voltage- and current-sources by $V_L = L\frac{di_L}{dt}$ and $i_C = C\frac{dV_C}{dt}$ in tandem with switched MOSFET voltages $V_{\text{DS1}}(t)$ and $V_{\text{DS2}}(t)$, all resultant current and voltage expressions are derived in appendix equations (A.1)–(A.6). Moreover, the internal half-bridge cell heatsink voltages are estimated in appendix equation (A.7) for the case of 1) heatsink bonded to power converter PE plane by bond impedance $R_{G,x}$, $L_{G,x}$ in Fig. 1, or 2) without connection of heatsink to PE plane, resulting in a coupling impedance of $C_{\text{HS},x}$. In either case, the eventual impedance is in series with the CM current components arising from the heatsink capacitances. Moreover, the defined model is not only applicable to SiC power devices, and can be applied generally to half bridge circuits employing Si or GaN devices, regardless of whether hard-switching or soft-switching modulation techniques are incorporated. Furthermore, Fig. 9 depicts the generic process for adapting for extending the modeling framework presented herein this work to other power converter topologies, where guidance regarding analytical modeling, FEA simulation, and network analyzer measurement of parasitic circuit components is provided in Section II, and guidance regarding analysis of possible noise corner frequencies elaborated in Sections IV-C and V.

B. Impact of Boost-Cell on Totem Pole Single-Phase PFC EMI

Considering the half bridge-cell noise models, the overall boost PFC parasitic circuit in Fig. 1 is re-arranged and simplified in Fig. 9, where all voltages and currents flowing in/out of the boost-cell equivalent models are as defined in appendix equations (A.1)–(A.7). Subsequently, denoting the respective voltage potentials present at the boost cell parasitic noise models as $V_{\text{in},1}(t)$, $V_{\text{in},2}(t)$, $V_{n,1}(t)$, $V_{n,2}(t)$, $V_{N,1}(t)$, and $V_{N,2}(t)$, along with noise currents flowing in and out as $i_{\text{DM1}}(t)$, $i_{\text{DM2}}(t)$, $i_{\text{DM3}}(t)$, and $i_{\text{DM4}}(t)$, the influence of the intrinsic cell model parasitic components on the DM and CM EMI noise of the interfacing converter circuits may then be expanded in appendix (A.8)–(A.15). As can be seen by considering the combination of currents going into the load, the DM noise components present both in the dc link and load are strongly dependent on the induced DM noise from both equivalent cell noise models. These currents then propagate to the neutral terminal $i_{\text{DM},N}(t)$, which then all recombine with the intrinsic neutral current noise of the line frequency cell model.

For the CM currents, however, each will flow out of the relevant ports from intrinsic cell model heatsink impedances and switch node capacitances, in addition to coupling capacitances to the test system PE plane present at the boost inductor and load terminals. These currents are thereby defined by voltages present at their respective nodes per $i_C(t) = C\frac{V_C(t)}{dt}$. For the currents

TABLE III
ANALYTICALLY ESTIMATED DM NOISE CORNER FREQUENCIES OF SINGLE-PHASE TOTEM POLE BOOST PFC

DM LC parasitic coupling	Noise type	Estimated corner frequency
$L_{\text{boost}}C_{\text{OSS}}(0V)$	DM	231.37 kHz
$L_{\text{boost}}C_{\text{OSS}}(V_{\text{DC}})$	DM	2.61 MHz
$L_{\text{boost}}C_{\text{boost}}$	DM	566.79 kHz
$L_{\text{boost}}C_{\text{HS}}$	CM	1.19 MHz
$2L_{\text{boost}}C_{\text{HS}}$	CM	844.83 kHz
$4L_{\text{boost}}C_{\text{HS}}$	CM	597.38 kHz
$L_{S4}C_{IN}$	DM	2.57 MHz
$L_{D4}C_{IN}$	DM	2.59 MHz
$L_{S3}C_{IN}$	DM	2.61 MHz
$L_{D3}C_{IN}$	DM	2.63 MHz
$L_{N}C_{IN}$	DM	2.75 MHz
$L_{C,DM}C_{DM}$	DM	3.41 MHz
$L_{\text{DC}}C_{\text{OSS}}(0V)$	DM	6.52 MHz

flowing out of the half bridge cell models, the heat-sink capacitance voltage is found per appendix (A.7), and switch-node voltage per appendix (A.1). For the CM current induced by the boost inductor input node, the voltage is defined by appendix (A.8a), and voltages imposed across the primary- and neutral-to PE plane found by considering the voltage drop across the load impedance Z_{load} in appendix (A.12). The overall CM current is then simply found as the summation of all terms in appendix (A.15), where subscript ",1" denotes currents stemming from the switching frequency half bridge cell, and ",2" currents from the line frequency half bridge cell.

C. Noise Corner Frequency Synthesis

In observation of all derived equations, it is evident that there are a significant number of possible parasitic coupling paths. However, certain combinations exist which will not be strongly coupled within the standard CE EMI bandwidth of 150 kHz–30 MHz, and therefore do not significantly contribute to the overall DM or CM EMI spectrum, or exhibit corner frequencies which exceed its maximum bound of 30 MHz. Such parasitic couplings are therefore instead a consideration for RE EMI noise effects where such equivalent circuit models become invalid. It is hypothesized that strong parasitic couplings present in the converter noise model will result in observable noise corner frequencies in the CE EMI frequency spectrum. This is indicated by a change in slope of the measured noise envelope. Further, it is anticipated that a series L_pC_p coupling will result in contribution of a rising noise envelope slope after the respective corner frequency due to the coupling impedance being minimum at resonance, whereas a parallel L_pC_p coupling will result in contribution of a falling noise contour owing to the coupling impedance being maximum at resonance. This hypothesis will be addressed next in Section V.

Table III presents estimated noise corner frequencies from the parasitic component parameter values found in Table II. In the converter under study, there is a 220 nF capacitor C_{DM} installed across the power and neutral conductors, which forms DM filter with the boost inductor. This capacitor is additionally considered as a potential cause of noise corner frequencies in the DM current spectrum, with its ESL measured as $L_{C,\text{DM}} = 9.88$ nH. Aside from the resonance of the dc link impedance, all other potential parasitic couplings to the dc link capacitance C_{DC} are neglected as these equivalent resonant frequencies are $\ll$150 kHz. Further, the estimated corner frequencies for the coupling of $L_{S,j}$ and $L_{D,j}$, $j \in [1,2,3,4]$ and C_{OSS} are disconsidered, as these all present resonant frequencies from 45–50 MHz, and 120–200 MHz for $C_{\text{OSS}}(0V)$ and $C_{\text{OSS}}(V_{\text{DC}})$, respectively. For the possible CM noise corner frequencies only the MOFSET heatsink capacitance $C_{M,\text{HS}}$ is able to be estimated due to the large distance between the PFC converter and PE plane shown in Fig. 9. For possible parasitic couplings, there only exists one that lies within the 150 kHz–30 MHz frequency span, which is the coupling of $L_{\text{boost}}C_{\text{HS}} = 1.19$ MHz. This is because the coupling of L_P, L_N, $L_{S,j}$, and $L_{D,j}$, $j \in [1,2,3,4]$ and C_{HS} result in estimated corner frequencies from 324–355 MHz.

TABLE IV
CE EMI TEST SETUP EQUIPMENT

Test article	Equipment part number
Spectrum analyzer	RSA503A
DM/CM noise splitter	TBLM01
Auxiliary power supply	ODP3033
LISN	LI-125C
BNC cable	S-LMR240
Dc electronic load	IT8514B
1-ϕ ac power source	APT 8520
DAQ/control PC	Dell Optiplex XE3

V. EMI NOISE MEASUREMENTS FOR TOTEM POLE SINGLE-PHASE PFC AND RECONSTRUCTION OF ESTIMATED PARASITICS

A. Experimental Characterization of DM + CM CE Spectrum

CE EMI noise measurements are performed over the frequency span of 150 kHz–30 MHz using the test setup in Fig. 11, with all test equipment utilized listed in Table IV. The single-phase ac power source supplies the $120V_{\text{AC}}$ input voltage to the PFC, the auxiliary power supply provides a $\pm 15V_{\text{DC}}$ voltage to power voltage and current measurement sensors, and the dc electronic load is set to 160 Ω for 1 kW output power, 320 Ω for 500 W output power, and 640 Ω for 250 W output power. For measurement of CE EMI noise, two LISNs are installed in-series with the power source primary and neutral wires and the PFC converter input. The radiofrequency (RF) output ports of the LISNs then connect to a DM/CM noise splitter box via a LI-125C 50 Ω low-loss BNC cable, which then connects to the RF input of the RSA503A real-time spectrum analyzer through another LI-125C BNC cable. Overall, the test system error is expected to be low with the LI-125C cables having a maximum insertion loss of < 0.5 dB [34], the TLBM1 noise splitter an average DM insertion loss of –0.53 dB and CM insertion loss of –0.93 dB over the 30 kHz–30 MHz frequency band [35], and the amplitude accuracy of the RSA503A error being within ± 1.0 dB [36]. For data acquisition of the frequency spectrum measurements, the RSA503A spectrum analyzer utilizes a 14-bit analog-to-digital conversion that executes at 112×10^6 samples per second with ± 0.8 dB amplitude accuracy. Results are then provided through SignalVu-PC software interface. The device is further configured to use a Hanning window with positive-peak

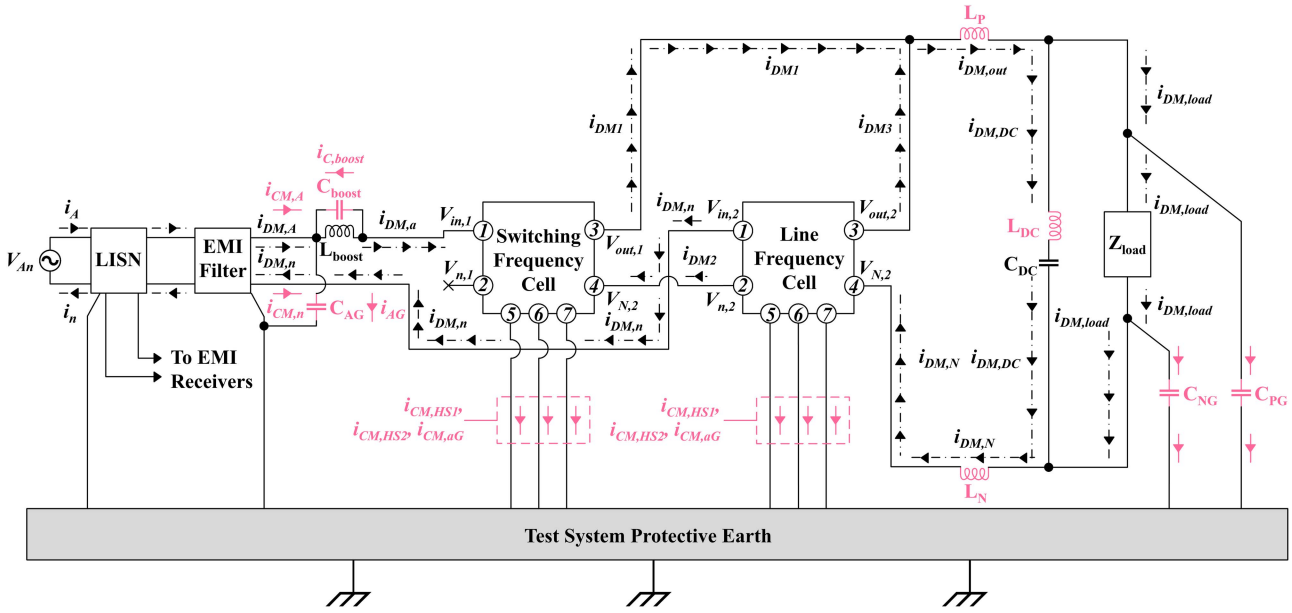

Fig. 10. Single-phase totem pole boost PFC equivalent boost-cell derived all-inclusive noise model.

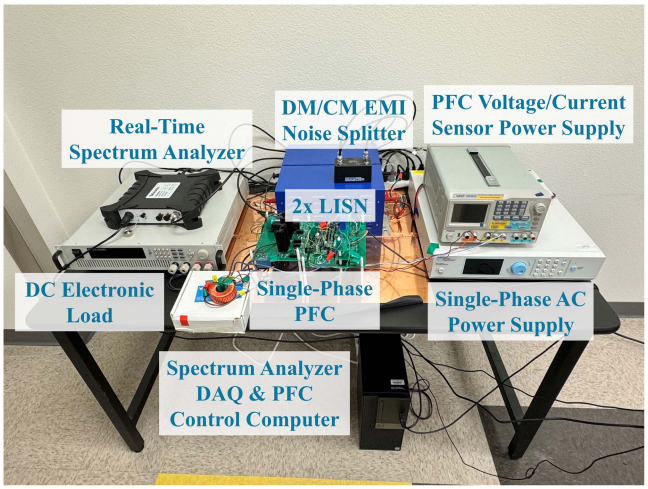

Fig. 11. Experimental test setup.

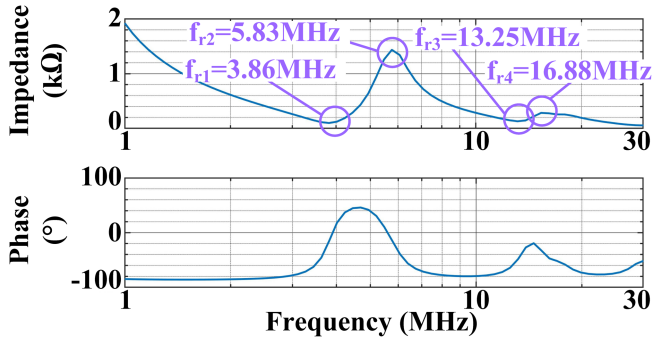

Fig. 12. Boost inductor higher order resonant modes.

detection, where spectrum measurements are processed using an average-of-VRMS function over a 60 Hz acquisition length. Further, the resolution bandwidth is set to 1 kHz with 10 401 total spectrum trace points collected.

Experimental results for the DM and CM EMI noise spectra of the single-phase totem pole PFC converter are presented in Fig. 13, with Fig. 13(a) and (b) demonstrating the 120 VAC/400 VDC, 1 kW DM and CM noise, respectively, Fig. 13(c) and (d) demonstrating the 120 VAC/400 VDC, 500 W DM and CM noise, Fig. 13(e) and (f) the 850 VAC/400 VDC, 500 W DM and CM noise, and Fig. 13(g) and (h) the 85 VAC/400 VDC, 250 W DM and CM noise spectra. Between these results, it is found that the unique noise corner frequencies are consistent between operational voltage/power levels, proving that the noise corner frequencies are dependent upon the unique *LC* coupling components in the PFC converter topology. Now, an attempt is made to match the estimated DM current corner frequencies of Table III to corner frequencies observed from measurement results in Fig. 13. Considering that series L_pC_p coupling components cause a rising noise envelope slope, and parallel L_pC_p components a decreasing noise lower envelope slope, it is found that three such possible parasitic couplings closely match the measured DM EMI frequency spectrum. Specifically, the coupling of $L_{\text{boost}}C_{\text{boost}}$ closely matches $f_{c,\text{DM1}}$ with +11.749% error, $(L_{D2}+L_{S2})C_{\text{DM}}$ closely matches $f_{c,\text{DM2}}$ with 0% error and, $L_{\text{DC}}C_{\text{OSS}}(0V)$ closely matches $f_{c,\text{DM5}}$ with –17.47% error. For the remaining measured noise corner frequencies, the initial estimates in Table III do not yield close matches. Hence, an investigation into other possible parasitic coupling components is performed.

First, by observation of the higher order resonances exhibited by the impedance measurement of the boost inductor in Fig. 12, it is found that the second, $f_{r2} = 3.86$ MHz, and third, $f_{r3} =$

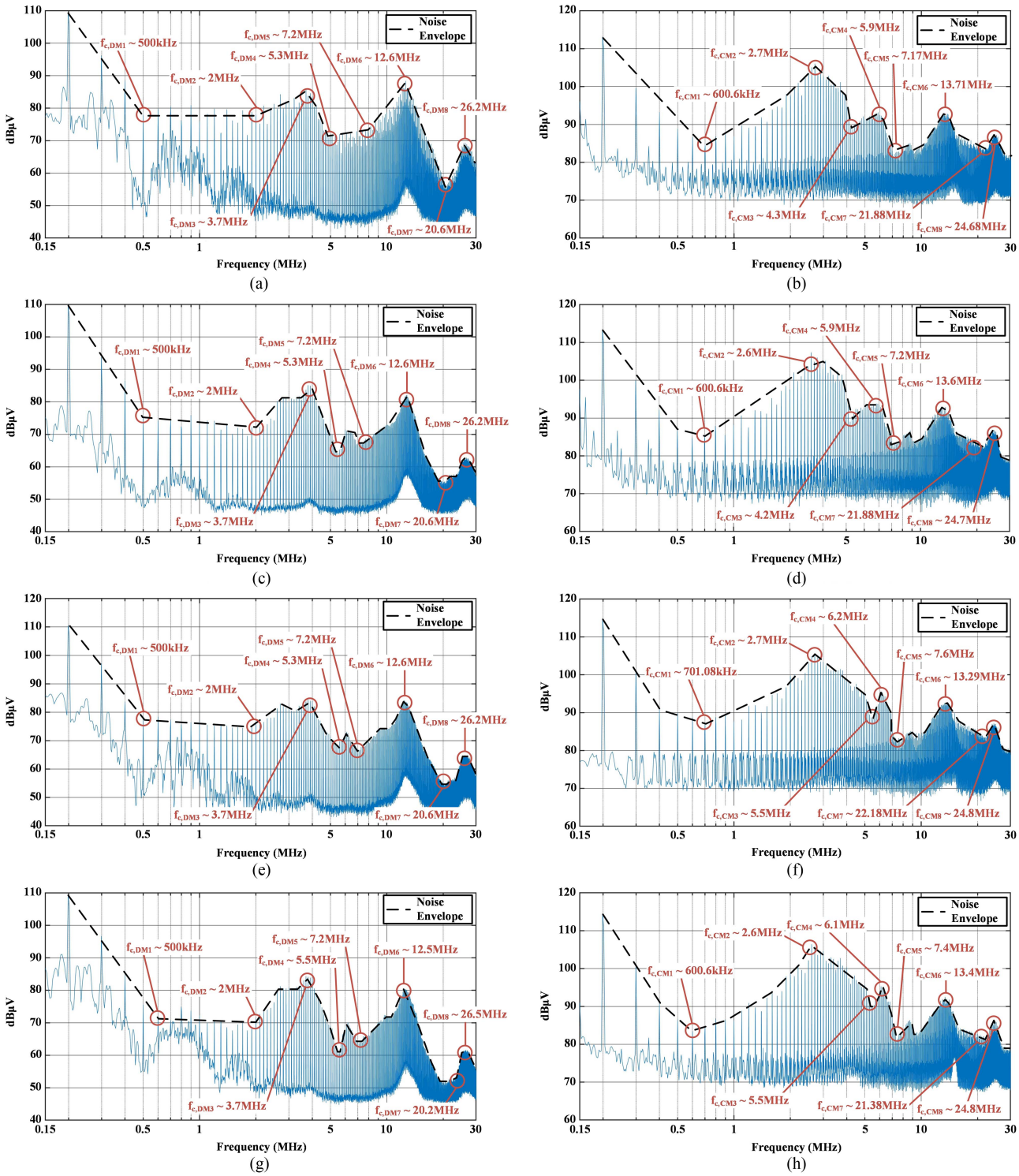

Fig. 13. Powered converter CE EMI 150 kHz–30 MHz frequency spectrum results. (a) 120 VAC/400 VDC 1 kW DM noise. (b) 120 VAC/400 VDC 1 kW CM noise. (c) 120 VAC/400 VDC 500 W DM noise. (d) 120 VAC/400 VDC 500 W CM noise. (e) 85 VAC/400 VDC 500 W DM noise. (f) 85 VAC/400 VDC 500 W CM noise. (g) 85 VAC/400 VDC 250 W DM noise. (h) 85 VAC/400 VDC 250 W CM noise.

5.83 MHz, resonant modes closely match $f_{c,\mathrm{DM2}} = 3.7$ MHz and $f_{c,\mathrm{DM4}} = 5.3$ MHz closely with +4.32% and +10% error, respectively. Moreover, the boost inductor impedance increases after f_{r2} and subsequently decreases after f_{r3}, matching the decreasing noise envelope in the $f_{c,\mathrm{DM2}} < f_{c,\mathrm{DM3}}$ frequency band and increasing noise envelope in the $f_{c,\mathrm{DM4}} < f < f_{c,\mathrm{DM5}}$ frequency band. For the other unknown DM corner frequencies, Fig. 14 represents the parasitic inductance network which may be referred to DM capacitances in unique series and parallel combinations, where $L_{\mathrm{SW1}} = L_{D1} + L_{S1}$, $L_{\mathrm{SW2}} =$

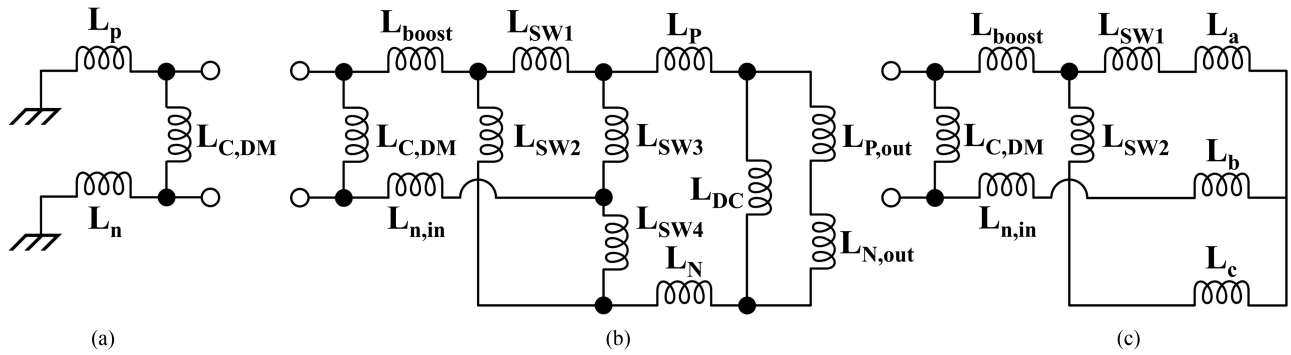

Fig. 14. Parasitic inductance paths. (a) Equivalent PFC input inductance. (b) Equivalent PFC bridge with Δ-equivalent output inductance. (c) Equivalent PFC bridge with *Y*-equivalent output inductance.

$L_{D2}+L_{S2}$, $L_{\mathrm{SW3}}=L_{D3}+L_{S3}$, $L_{\mathrm{SW4}}=L_{D4}+L_{S4}$. The ESL of the DM capacitor installed in the test setup measured as $L_{C,\mathrm{DM}}=9.88$nH by the Bode 100 VNA setup in its series-through measurement configuration. Fig. 14(a) presents the input inductance network, Fig. 14(b) the output inductance network, and Fig. 14(c) the output inductance network after performing $\Delta-Y$ transformation of the output interconnect, where $L_{P,\mathrm{out}}=5.36$ nH and $L_{N,\mathrm{out}}=5.45$ nH are additionally measured by the VNA, included to improve noise corner frequency estimation.

Equation (14) provides the equivalent parallel output inductance of S3, S4, and the Δ-equivalent output interconnect network shown in Fig. 14(b). Considering a parallel coupling with $C_{\mathrm{OSS}}(0V)$, an estimated frequency of 20.96 MHz is found yielding a close match to $f_{c,\mathrm{DM7}}=20.6$ MHz with +1.75% error. Next, considering the connection of S1 and S2 along with S3 and S4 to the Δ-equivalent output interconnect, the output inductance may then be rearranged as a *Y*-equivalent circuit in Fig. 14(c). An exact match to $f_{c,\mathrm{DM6}}=12.6$ MHz is found by the potential coupling of $L_{a,\mathrm{out}}C_{P,N}=12.6$ MHz. Finally, considering the high-frequency switch state when S1 is disconnected from the rest of the PFC interconnect due to S2 and S3 being in the OFF-state, the series coupling of the stray inductance path of $(L_{\mathrm{SW1}}+L_P)C_{\mathrm{OSS}}(0V)=27.64$ MHz yields a close match to $f_{c,\mathrm{DM8}}=26.2$ MHz, reporting only +5.5% error, and moreover it is found that the similar stray inductance path of $L_{\mathrm{SW2}}+L_P$, and similarly $L_{\mathrm{SW3}}+L_N/L_{\mathrm{SW4}}+L_N$ in the neutral conduction path, yield similar results considering a $C_{\mathrm{OSS}}(0V)$ coupling. Table V provides a comparison for the DM noise corner frequencies where, from comparison of analytically derived DM noise corner frequencies and experimentally measured noise corner frequencies, all eight unique DM noise corner frequencies have been estimated with a low average error of +6.45%. However, it has been found that the first-order inductor model must be extended to include the first three resonant modes to account for $f_{c,\mathrm{DM2}}$ and $f_{c,\mathrm{DM4}}$

$$L_{\mathrm{par,out}}=\frac{L_{\mathrm{DC}}(L_{P,\mathrm{out}}+L_{N,\mathrm{out}})}{L_{\mathrm{DC}}+L_{P,\mathrm{out}}+L_{N,\mathrm{out}}} \tag{14}$$

TABLE V
COMPARISON OF ANALYTICAL AND EXPERIMENTAL PARASITIC COUPLINGS CAUSING DM NOISE CORNER FREQUENCIES

LC coupling	Analytical $f_{c,\mathrm{DM}}$	Experimental $f_{c,\mathrm{DM}}$	Error
$L_{\mathrm{boost}\,1}C_{\mathrm{boost}\,1}$	566.79 kHz	500 kHz	+11.79%
$(L_{D2}+L_{S2})\,C_{DM}$	2 MHz	2 MHz	0%
$L_{\mathrm{boost}\,2}C_{\mathrm{boost}\,2}$	3.86 MHz	3.7 MHz	+4.32%
$L_{\mathrm{boost}\,3}C_{\mathrm{boost}\,3}$	5.83 MHz	5.3 MHz	+10%
$L_{DC}C_{\mathrm{OSS}}\,(0V)$	6.52 MHz	7.9 MHz	–17.47%
$L_{a,\mathrm{out}}\,C_{P,N}$	12.6 MHz	12.6 MHz	0%
$L_{\mathrm{eq,out}}C_{\mathrm{OSS}}(0V)$	20.96 MHz	20.6 MHz	+1.75%
$(L_{\mathrm{SW1}}+L_P)C_{\mathrm{OSS}}(0V)$	27.64 MHz	26.2 MHz	+5.5%

$$L_{\mathrm{eq,out1}}=\frac{(L_{\mathrm{SW3}}+L_{\mathrm{SW4}})\,(L_P+L_N+L_{\mathrm{par,out}})}{L_{\mathrm{SW3}}+L_{\mathrm{SW4}}+L_P+L_N+L_{\mathrm{par,out}}} \tag{15}$$

$$L_a=\frac{L_{\mathrm{SW3}}(L_P+L_N+L_{\mathrm{par,out}})}{L_{\mathrm{SW3}}+L_{\mathrm{SW4}}+L_P+L_N+L_{\mathrm{par,out}}} \tag{16}$$

$$L_b=\frac{L_{\mathrm{SW3}}L_{\mathrm{SW4}}}{L_{\mathrm{SW3}}+L_{\mathrm{SW4}}+L_P+L_N+L_{\mathrm{par,out}}} \tag{17}$$

$$L_c=\frac{L_{\mathrm{SW3}}(L_P+L_N+L_{\mathrm{par,out}})}{L_{\mathrm{SW3}}+L_{\mathrm{SW4}}+L_P+L_N+L_{\mathrm{par,out}}}. \tag{18}$$

For the CM noise corner frequencies, the only estimated CM capacitance is the MOSFET heatsink capacitance C_{HS}. The series coupling of the boost inductor's primary inductance L_{boost1} and the parallel four MOSFET heatsink capacitances results in an estimated corner frequency of 597.38 kHz, closely matching $f_{c,\mathrm{CM1}}=600.6$ kHz with a low –0.54% error. In order to characterize the other CM noise corner frequencies, a novel experiment is conducted by inserting 22 nF capacitors between the PFC converter input and output terminals to the PE conductive plane. By doing so, the distributed capacitance seen between these nodes and the PE will be predominantly the 22 nF capacitor term. The insertion of the 22 nF capacitor is expected to thereby cause a shift in the observed noise corner frequencies and effectively reconstruct the CM noise spectrum.

B. Reconstruction of Measured CM EMI Noise Spectrum Through External Capacitor Insertion

In order to identify the unknown lumped equivalent CM capacitances of the PFC, novel experimental method is proposed. Identification of the lumped CM capacitance of the power converter enables an accurate calculation of the inherent ground-leakage current for touch-current safety requirements [26]. Further, this provides an accurate estimate of the CM frequency response for checking the interaction of EMI filter design and power converter parasitic components to ensure adequate filter performance in the high-frequency band. As outlined in Fig. 16, the objective of this experiment is to establish artificially created *LC* networks that cause shifts in the CM EMI noise corner frequencies observed in Fig. 13. The artificial *LC* networks are formed by symmetrically inserting a pair of 22 nF capacitors between the converter input/output positive and neutral nodes and PE plane. Fundamentally, the insertion of the capacitors forces the lumped capacitance at the input/output terminals to be the experimental value, and the noise corner frequencies observed in the CM EMI spectrum will shift. The shifted noise corner frequencies may then be correlated to equivalent lumped stray inductance networks resonating with the inserted capacitors. Then, by knowledge of the shifted noise corner frequency and lumped stray inductance network, lumped CM capacitances at the converter input and output are estimated from the original EMI spectrum. Moreover, installing the 22 nF capacitors between either the input or output terminals and the PE plane will not detriment the expected operation of the PFC, as the resultant phase angle displacement on the input current will not exceed 5°, maintaining a good operational power factor > 0.995.

Fig. 15 demonstrates the measured CM EMI spectra for each test case by following the experimental methodology outlined in Fig. 16, with Fig. 15(a), (c), (d), (e), and (g) depicting the results of inserting a 220 nF capacitor between the converter input terminals and chassis for 120 VAC/400 VDC 1 kW, 120 VAC/400 VDC 500 W, 85 VAC/400 VDC 500 W, and 85 VAC/400 VDC 250 W test cases respectively. Fig. 15(b), (d), (e), (f), and (h) then demonstrate the results of inserting a 22 nF capacitor between the converter output terminals and chassis for 120 VAC/400 VDC 1 kW, 120 VAC/400 VDC 500 W, 85 VAC/400 VDC 500 W, and 85 VAC/400 VDC 250 W test cases, respectively. It is found that the observed CM EMI noise spectra between unique test case results are similar across the different operational voltage and output power scenarios, consistent with the observations of Fig. 13.

First, observing the effect of inserting 22 nF capacitors between the input terminals and PE plane, it is found that $f_{c,\mathrm{CM1}}$ shifts up from 600.6 to 798.7 kHz indicating that the coupling of the four parallel heatsink MOSFET capacitances and boost inductor is influenced by the 22 nF capacitor insertion. Further, $f_{c,\mathrm{CM2}}$ is unchanged, and the third noise corner $f_{c,\mathrm{CM3}}$ then increases from 4.3 to 5.9 MHz. The fourth and fifth noise corner frequency are no longer observed in the spectra, and $f_{c,\mathrm{CM6}}$ shifts from 13.71 to 13 MHz, $f_{c,\mathrm{CM7}}$ from 21.88 to 19 MHz, and $f_{c,\mathrm{CM8}}$ from 24.68 to 25.3 MHz. Next, the impact of inserting 22 nF capacitors between the output terminals and chassis is analyzed. As is found in the insertion of 22 nF capacitors between the input terminals and chassis, $f_{c,\mathrm{CM1}}$ shifts up from 600.6 to 798.7 kHz. However, $f_{c,\mathrm{CM2}}$ uniquely shifts from 2.7 to 3.8 MHz, a result which was not observed when inserting the 22 nF capacitor at the input terminals. The third noise corner is then observed to shift from 4.3 to 6.2 MHz, and the fourth and fifth noise corner frequencies are again no longer observed. The sixth noise corner frequency has not shifted, but the seventh noise corner frequency $f_{c,\mathrm{CM7}}$ has shifted slightly from 21.88 to 20.08 MHz, and $f_{c,\mathrm{CM8}}$ from 24.68 to 25.2 MHz.

TABLE VI
EXPERIMENTALLY OBTAINED PARASITIC INDUCTANCES, INSERTED 22 NF CAPACITANCE AT V_A, V_n INPUT NODES TO PE PLANE

Corner frequency	L
$f_{c,\mathrm{CM3}} = 5.9$ MHz	33.1 nH
$f_{c,\mathrm{CM4}} = 13$ MHz	6.81 nH
$f_{c,\mathrm{CM5}} = 19$ MHz	3.19 nH
$f_{c,\mathrm{CM6}} = 25.3$ MHz	1.8 nH

TABLE VII
EXPERIMENTALLY OBTAINED PARASITIC INDUCTANCES, INSERTED 22 NF CAPACITANCE AT V_P, V_N OUTPUT NODES TO PE PLANE

Corner frequency	L
$f_{c,\mathrm{CM2}} = 3.8$ MHz	79.7 nH
$f_{c,\mathrm{CM3}} = 6.2$ MHz	30 nH
$f_{c,\mathrm{CM4}} = 13.7$ MHz	6.13 nH
$f_{c,\mathrm{CM5}} = 20.1$ MHz	2.81 nH
$f_{c,\mathrm{CM6}} = 25.2$ MHz	1.81 nH

Next, an estimation of the parasitic inductances resonating with the inserted 22 nF CM capacitors is performed by considering the observed shifts in noise corner frequencies, which are considered as $f_{c,\mathrm{CM1}}$ in Fig. 16. It is assumed that, for noise corner frequencies which have uniquely shifted between the two measured cases, the changed corner frequency indicates a resonance of a stray inductance network with the inserted 22 nF capacitors per the second-to-last step outlined in Fig. 16. Tables VI and VII present the experimentally obtained inductance values found by insertion of the 22 nF capacitors between the PFC input and output terminals, respectively, and PE plane. For estimating what parasitic inductances in the PFC converter are resonating, Fig. 14 is used to derive equivalent path inductances, which may couple with the CM capacitances in Fig. 1. Equations (19) and (20) are the equivalent input inductance between the primary- and neutral-to-ground capacitances C_{pG} and C_{nG}, respectively, and (21) the equivalent output inductance observed in series with C_{pG}. These analytically derived inductances, along with L_b and L_c found per equations (17) and (18), result in values close to the experimentally obtained coupling inductances in Tables VI and VII.

Table VIII summarizes the comparison between experimentally and analytically found parasitic inductances according to Fig. 14, yielding an average estimation error of 18.87%. From these results, it is deduced that the CM currents measured in the

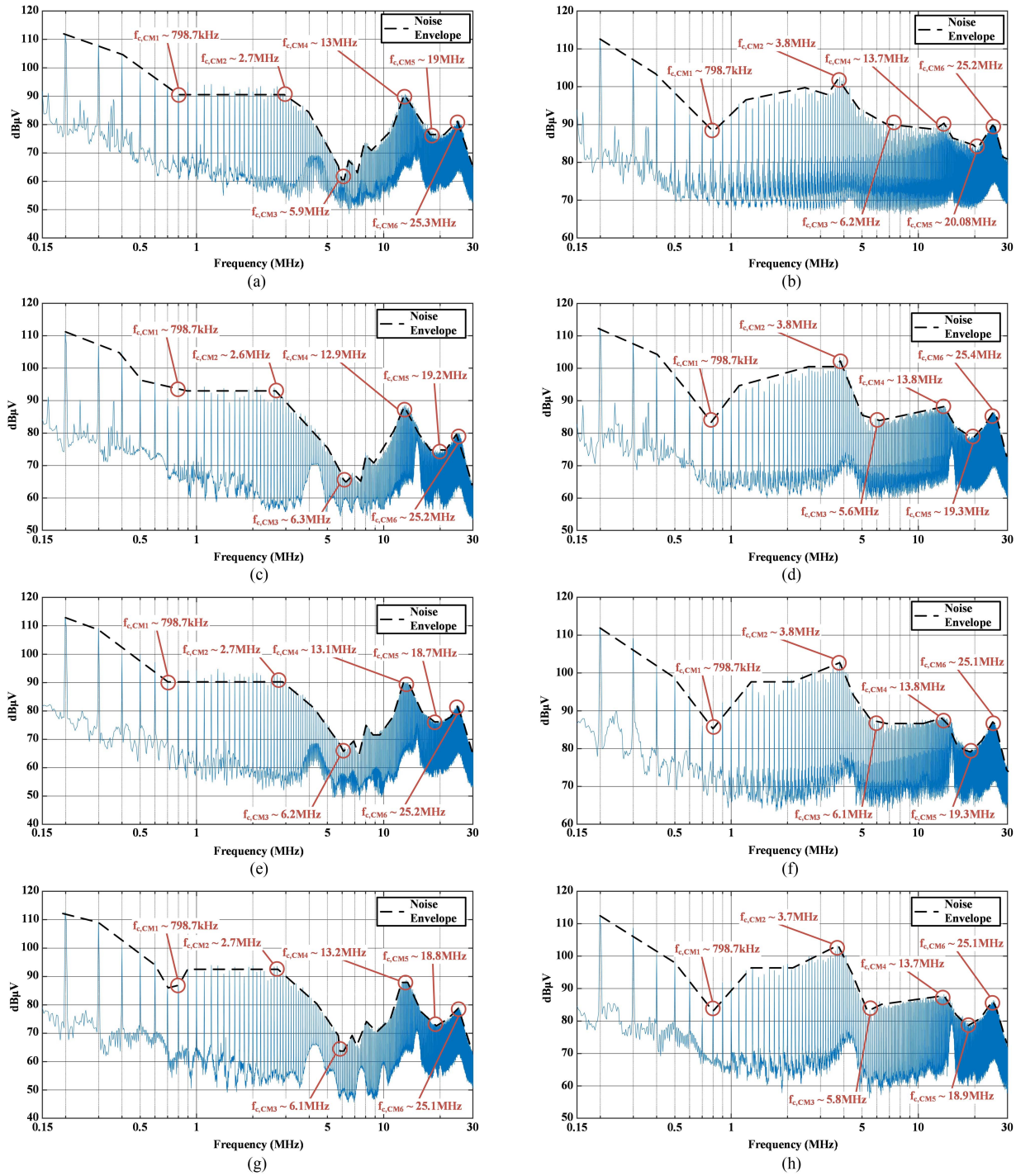

Fig. 15. Reconstructed powered converter CE EMI 150 kHz–30 MHz frequency spectrum results. (a) 120 VAC/400 VDC 1 kW CM noise, 22 nF capacitor inserted at VIN terminals. (b) 120 VAC/400 VDC 1 kW CM noise, 22 nF capacitor inserted at VOUT terminals. (c) 120 VAC/400 VDC 500 W CM noise, 22 nF capacitor inserted at VIN terminals. (d) 120 VAC/400 VDC 500 W CM noise, 22 nF capacitor inserted at VOUT terminals. (e) 85 VAC/400 VDC 500 W CM noise, 22 nF capacitor inserted at VIN terminals. (f) 85 VAC/400 VDC 250 W CM noise, 22 nF capacitor inserted at VOUT terminals. (g) 85 VAC/400 VDC 250 W DM noise, 22 nF capacitor inserted at VIN terminals. (h) 85 VAC/400 VDC 250 W CM noise, 22 nF capacitor inserted at VOUT terminals.

original EMI spectrum are predominantly caused by the coupling of lumped parasitic inductance networks and the lumped parasitic capacitance present in the air medium between the conductive PCB and PE planes. Finally, estimated lumped CM capacitance values present at the converter input and output terminals are found considering the original EMI spectrum results by the final step in Fig. 16 in Table IX, where $f_{c,\mathrm{CM2}}$ is the corner frequency of the original EMI spectrum, and L_{est} is considered from the results in Tables VII and VIII. From the experimentally estimated CM capacitances, it is evident that the CM EMI spectra noise corner frequencies are caused by the lumped equivalent capacitance network comprised of distributed

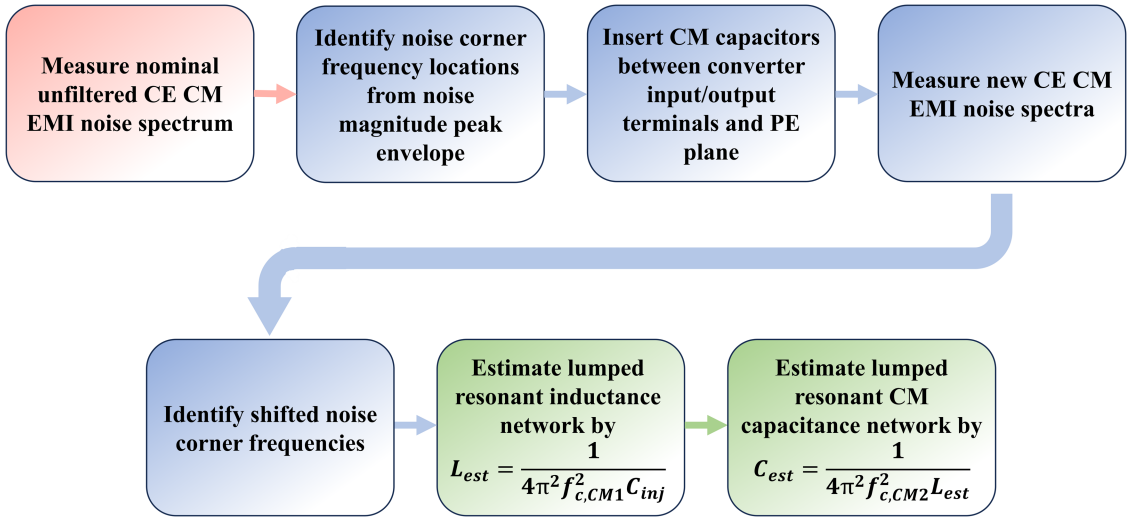

Fig. 16. Power converter CM EMI frequency spectrum reconstruction experiment, methodology flowchart.

TABLE VIII
COMPARISON OF EXPERIMENTAL AND ANALYTICAL PARASITIC CM PATH INDUCTANCES

Experimental L_{IN}	Experimental L_{OUT}	Analytical L	Error
33.1 nH	30 nH	L_c = 32.01 nH	+1.46%
6.81 nH	6.13 nH	$L_{CpG,in}$ = 6.55 nH	–5.26%
3.19 nH	2.81 nH	$L_{CnG,in}$ = 4.09 nH	+36.33%
1.8 nH	1.81 nH	L_b = 1.22 nH	–32.41%

TABLE IX
EXPERIMENTALLY OBTAINED LUMPED PARASITIC CAPACITANCES FROM RECONSTRUCTED CM EMI NOISE SPECTRA

Corner frequency	C_{IN}	C_{OUT}
$f_{c,CM2}$ = 2.6 MHz	N/A	22.01 nF
$f_{c,CM3}$ = 4.2 MHz	43.34 nF	47.87 nF
$f_{c,CM6}$ = 13.6 MHz	20.11 nF	22.34 nF
$f_{c,CM7}$ = 21.88 MHz	16.59 nF	18.83 nF
$f_{c,CM8}$ = 24.7 MHz	23.07 nF	22.94 nF

discrete CM capacitors

$$L_{\text{CPG,in}} = \frac{L_p(L_n + L_{C,\text{DM}})}{L_p + L_n + L_{C,\text{DM}}} \tag{19}$$

$$L_{\text{CNG,in}} = \frac{L_n(L_p + L_{C,\text{DM}})}{L_N + L_P + L_{C,\text{DM}}}. \tag{20}$$

VI. CONCLUSION

A comprehensive heterogeneous parasitic component modeling method consisting of physics-derived modeling, FEA simulation, and measurement for a 1 kW-rated 120 VAC/400 VDC single-phase totem pole boost PFC converter utilizing SiC MOSFET devices has been thoroughly defined, investigated, and experimentally validated. Most derived parasitic component values show a close agreement with respect to measurement results, yielding an average error of 15.06% for the parasitics of the converter boost inductor, dc link capacitor, and switch node self-inductance. Subsequently, a proposed novel all-inclusive noise cell model is experimentally validated by measurement of the CE EMI noise spectrum. It is found that all eight unique noise corner frequencies observed in the DM EMI noise component are accurately estimated by the model, with a low average error of 6.45%. For the CM EMI noise spectrum, one estimated corner frequency caused by the coupling of the PFC boost inductor and analytically estimated SiC MOSFET heatsink capacitance is validated, with –0.54% error. For unknown system CM capacitances, a novel experimental method extracted the lumped CM capacitor components by reconstruction of the CM EMI noise spectrum, and it is found that CM noise currents are caused by the coupling of multiple parasitic inductance components with several distributed CM capacitances.

APPENDIX

Derived equations for the half-bridge noise cell model and all-inclusive noise model are provided here. Equations (A.1)–(A.7) shown at the top of the next page, are all derived considering the half-bridge noise cell model of Fig. 12 in Section IV-A. Specifically, (A.1) and (A.2) represent the switched-node input voltage and current, and (A.3) and (A.4) depict the half-bridge output voltage and current. Equations (A.5) and (A.6) then show the neutral voltage and current, and equation (A.7) shows the heatsink voltage expression.

Equations (A.8)–(A.15) shown at the top of the next page, are all derived considering the all-inclusive noise model of Fig. 13 in Section IV-B. Equations (A.8) and (A.9) correlate to the power line input noise expressions, and (A.10) the switch node voltage of the high-frequency half-bridge cell. Equations (A.11)–(A.14) then depict the dc-link and output-load noise expressions, and (A.15) the total CM noise current expression

$$V_{\mathrm{IN}}(t) = \frac{L_{D2}V_{S1}(t)}{L_{S1}+L_{D2}} + \frac{L_{S1}V_{S2}(t) + L_{S1}L_{D2}\left(C_{S1}\frac{d^2(V_{S1}(t)-V_{H1}(t))}{dt^2} + C_{\mathrm{OSS1}}\frac{d^2(V_{S1}(t)-V_{D1}(t))}{dt^2} - C_{D2}\frac{d^2(V_{D2}(t)-V_{H2}(t))}{dt^2} - C_{\mathrm{OSS2}}\frac{d^2(V_{S2}(t)-V_{D2}(t))}{dt^2}\right)}{L_{S1}+L_{D2}} \tag{A.1}$$

$$i_{\mathrm{IN}}(t) = \frac{1}{L_{S1}}\int V_{\mathrm{IN}}(t) + V_{S1}(t)dt - \frac{1}{L_{D1}}\int V_{D2}(t) - V_{\mathrm{IN}}(t)dt$$
$$= C_{S1}\frac{d(V_{S1}(t)-V_{H1}(t))}{dt} + C_{\mathrm{OSS1}}\frac{d(V_{S1}(t)-V_{D1}(t))}{dt} - C_{\mathrm{OSS2}}\frac{d(V_{S2}(t)-V_{D2}(t))}{dt} - C_{D2}\frac{d(V_{D2}(t)-V_{H2}(t))}{dt} \tag{A.2}$$

$$V_{\mathrm{out}}(t) = V_{D1}(t) - L_{D1}\left(C_{\mathrm{OSS1}}\frac{d^2(V_{S1}(t)-V_{D1}(t))}{dt^2} - C_{D1}\frac{d^2(V_{D1}(t)-V_{H1}(t))}{dt^2}\right) \tag{A.3}$$

$$i_{\mathrm{out}}(t) = C_{\mathrm{OSS1}}\frac{d(V_{S1}(t)-V_{D1}(t))}{dt} - C_{D1}\frac{d(V_{D1}(t)-V_{H1}(t))}{dt} = \frac{1}{L_{D1}}\int V_{D1}(t) - V_{\mathrm{out}}(t)dt \tag{A.4}$$

$$V_N(t) = L_{S1}\left(C_{S2}\frac{d^2(V_{S2}(t)-V_{H2}(t))}{dt^2} + C_{\mathrm{OSS2}}\frac{d^2(V_{S2}(t)-V_{D2}(t))}{dt^2}\right) + V_{S2}(t) \tag{A.5}$$

$$i_n(t) = \frac{1}{L_{S1}}\int V_N(t) - V_{S2}(t)dt = C_{S2}\frac{d(V_{S2}(t)-V_{H2}(t))}{dt} + C_{\mathrm{OSS2}}\frac{d(V_{S2}(t)-V_{D2}(t))}{dt} \tag{A.6}$$

$$V_{H,x}(t) = \begin{cases} R_{G,x}\left(C_{D,x}\frac{d(V_{D,x}(t)-V_{H,x}(t))}{dt} + C_{S,x}\frac{d((V_{S,x}(t)-V_{H,x}(t))}{dt}\right) + L_{G,x}\left(C_{D,x}\frac{d^2(V_{D,x}(t)-V_{H,x}(t))}{dt^2} + C_{S,x}\frac{d(V_{S,x}(t)-V_{H,x}(t))}{dt^2}\right) \\ \frac{C_{D,x}\frac{d^2V_{D,x}(t)}{dt^2} + C_{S,x}\frac{d^2V_{S,x}(t)}{dt^2}}{C_{\mathrm{HG},x}+C_{D,x}+C_{S,x}} \end{cases} \tag{A.7}$$

$$V_A(t) = L_{\mathrm{boost}}\frac{d\left(i_{\mathrm{in1}}(t) + C_{\mathrm{boost}}\frac{d(V_A(t)-V_{\mathrm{in1}}(t))}{dt}\right)}{dt} \tag{A.8a}$$

$$i_{\mathrm{AG}} = C_{\mathrm{AG}}\frac{dV_A(t)}{dt} \tag{A.8b}$$

$$i_a(t) = \frac{1}{L_{\mathrm{boost}}}\left(\int V_{\mathrm{in},1}(t)dt - \frac{1}{C_{\mathrm{AG}}\int V_{C,\mathrm{AG}}(t)dt}\right) - C_{\mathrm{boost}}\frac{d(V_{\mathrm{in},1}(t))}{dt} - \frac{V_{C,\mathrm{AG}}(t)}{C_{\mathrm{AG}}} \tag{A.9}$$

$$V_{\mathrm{in},1}(t) = \frac{1}{C_{\mathrm{AG}}}\int i_{C,\mathrm{AG}}(t)dt - L_{\mathrm{boost}}\frac{di_{L,\mathrm{boost}}(t)}{dt} \tag{A.10}$$

$$V_{C,\mathrm{DC}}(t) = V_{\mathrm{out},2}(t) - L_P\frac{d(i_{\mathrm{DM1}}(t)+i_{\mathrm{DM2}}(t))}{dt} - L_{\mathrm{DC}}\frac{d(i_{\mathrm{DM1}}(t)+i_{\mathrm{DM2}}(t)-i_{\mathrm{DM,load}}(t))}{dt} \tag{A.11a}$$

$$i_{\mathrm{DM,DC}}(t) = C_{\mathrm{DC}}\frac{dV_{C,\mathrm{DC}}(t)}{dt} \tag{A.11b}$$

$$i_{\mathrm{DM,load}}(t) = i_{\mathrm{DM1}}(t) + i_{\mathrm{DM2}}(t) - i_{\mathrm{DM,DC}}(t) \tag{A.12}$$

$$i_{\mathrm{DM},N}(t) = i_{\mathrm{DM,DC}}(t) + i_{\mathrm{DM,load}}(t) \tag{A.13}$$

$$V_{\mathrm{PG}}(t) - V_{\mathrm{NG}}(t) = i_{\mathrm{DM,load}}(t)Z_{\mathrm{load}} \tag{A.14}$$

$$i_{\mathrm{CM}}(t) = i_{\mathrm{CM,AG}} + i_{\mathrm{CM,HS1},1} + i_{\mathrm{CM,HS2},1} + i_{\mathrm{CM,aG},1} + i_{\mathrm{CM,HS1},2} + i_{\mathrm{CM,HS2},2} + i_{\mathrm{CM,aG},2} + i_{\mathrm{CM,PG}} + i_{\mathrm{CM,NG}}. \tag{A.15}$$

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