Design and Control of a Four-Wire MMC-Based Power Conditioning System for the Unbalanced Load Support in a Transformer-Less Asynchronous Microgrid

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***Abstract*—A four-wire modular multilevel converter (MMC) with the split dc-link capacitor topology is a promising solution for a power conditioning system (PCS) of an asynchronous microgrid (ASMG). In an ASMG, the PCS is applied to connect two distribution-level systems with a transformerless structure, which has numerous challenges in the design and control of the MMC. However, in the existing literature, MMCs have been mainly applied in transmission systems with isolation transformers or serve as static compensators in distribution systems. The design and control methods of MMCs for these applications cannot be directly applied to an ASMG. Therefore, in this article, considering the impacts of the unbalanced load, transformerless structure, and different operation modes on the MMC-based PCS, the corresponding control and hardware design are conducted. The proposed MMC-based PCS solution can limit the microgrid (MG) voltage unbalance caused by the load unbalance, eliminate the harmonic zero-sequence current impacts on the main grid, and compensate for the unbalanced load current of local sources in the M. Moreover, a medium voltage testing setup is developed to verify the analysis and demonstrate the proposed control algorithms on a 10 kV SiC MOSFET-based MMC at 13.8 kV ac voltage.**

***Index Terms*—10 kV SiC MOSFET, asynchronous microgrid, modular multi-level converter, transformer-less system, unbalanced system.**

I. Introduction

ASYNCHRONOUS microgrid (ASMG) is a novel microgrid (MG) concept where a back-to-back connected power conditioning system (PCS) serves as the interface between the MG and the main distribution grid. An example ASMG is shown in Fig. 1 [1], [2], where the main grid and MG realize a transformerless connection. The medium voltage (MV) converter-based PCS can be directly connected to the main grid and MG without step-up transformers so that the total loss and size of the PCS can be reduced.

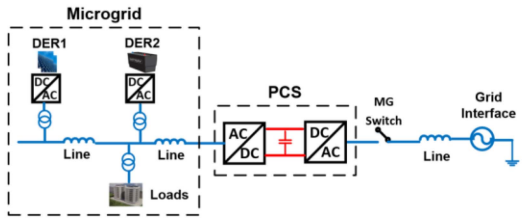

Fig. 1. ASMG architecture.

As a key to an ASMG, the PCS can lead to numerous benefits, including fault isolation [3], better transition performances (grid-connected to island mode and vice-versa) [4], and system stability enhancement [5]. Due to its natural modularity, better scalability, and high-quality output waveforms [6], a modular multilevel converter (MMC) becomes a promising solution for PCS implementation [7].

To establish a transformerless connection between two distribution-level systems (main grid and MG), MMC-based PCS is faced with numerous challenges. First, the unbalanced loads in the MG require a neutral wire to provide a path for zero-sequence (ZS) components. It is more efficient to obtain the neutral directly from the PCS with a four-wire topology than an additionally added neutral-forming transformer. As a result, the corresponding requirements of the system neutral, such as limiting the neutral voltage shift caused by the ZS current and providing a neutral in different operation modes, should also be considered in the PCS implementation.

Second, the PCS serves as the grid-forming mode (GFM) source of the MG in the grid-connected mode. The MMC-based PCS needs to limit its output voltage unbalance caused by the unbalanced load currents. Otherwise, unbalanced voltages will affect the operation of three-phase loads, such as motors [8] and

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equipment insulation [9]. Third, the four-wire transformerless structure can also provide a path for harmonic ZS currents, such as third-order components, which may also affect the operation of PCS and worsen the power quality of the ASMG.

In the existing literature, MMCs are mainly applied in three-wire transmission-level grids [10], [11], such as high voltage direct current (HVDC) for two transmission systems or offshore wind farms, where the system load conditions are usually balanced. In this condition, two line-frequency transformers are applied to link the MMC to two systems, which can decouple the MMC from the two grids [12]. In this application, the impacts of unbalanced load currents and harmonic ZS currents are usually not considered.

In distribution-level systems, MMCs are mainly adopted as static compensators (STATCOMs) [13], [14], [15], [16], [17]. Duarte et al. [13] proposed a control strategy to use the STATCOM to compensate for the network ZS voltage. Pirouz and Bina [14] utilized paralleled four-leg MMCs as an unbalanced compensator to increase reliability. Lin et al. [15] provided the analysis and control of the circulating current for MMC-based four-wire STATCOM with the split capacitor topology. Xu et al. [16] applied the MMC-based STATCOM to compensate for the positive and negative sequence voltages at the point of common coupling of the grid. Shadlu [17] proposed a model predictive control approach for a four-leg MMC-based STATCOM to compensate for the nonlinear and unbalanced load. However, in these papers, MMCs all operate in the grid-following (GFL) mode, and voltages are provided by main grids. The unbalanced load impacts on the output voltage of a GFM controlled MMC have not been considered. Moreover, in all these papers, the harmonic ZS currents and CM currents' impacts on the MMC operation are not discussed.

In recent years, MMCs have started to be used as solid-state transformers, targeting MV dc systems [18], [19]. Nevertheless, the unbalanced load impacts are also not considered in these papers.

To address all the aforementioned issues, in this article, the design and control of a four-wire MMC-based PCS with split dc-link topology is conducted to achieve a transformerless connection of two distribution-level systems. The impacts of the transformerless structure are analyzed first to define the design and control requirements. Then, corresponding hardware and control designs are proposed to address the issues considering different operation modes. Simulations are provided to verify the control and design. A testing setup at 25 kV dc, 13.8 kV ac voltage is developed to test the PCS unbalanced load support in different operation modes. The main contributions of this article are highlighted as follows.

1) MMC's output voltage unbalance caused by the unbalanced load is analyzed and dedicated unbalanced voltage regulation control is proposed.
2) Harmonic ZS current distribution of MMC is analyzed and third-order harmonic ZS current control is proposed.
3) A novel arm inductance design method is proposed to eliminate the high-frequency harmonic ZS currents.
4) Dedicated control strategies are proposed to eliminate the MG's unbalanced load impacts on the main grid.

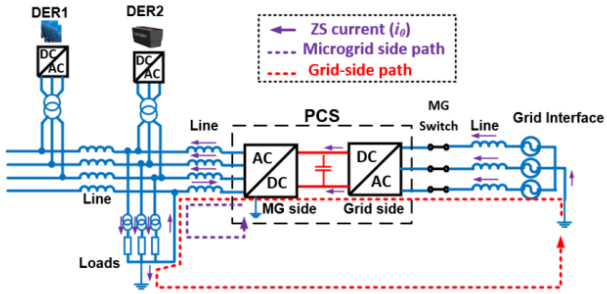

Fig. 2. ZS current distribution.

5) A MV prototype-based testing setup is developed to demonstrate the proposed design and control solutions.

The rest of this article is organized as follows: the challenges of implementing an ASMG with a transformerless structure are discussed in Section II. The MMC operation analysis under unbalanced load conditions is discussed in Section III; the control design is proposed in Section IV. Hardware design is provided in Section V. Simulation verifications are shown in Section VI. Experimental testing is provided in Section VII. Finally, Section VIII conclude this article.

II. ASMG With Transformerless Structure

A. Neutral Forming of the MG

Considering symmetrical components, the unbalanced current can be represented as

$$\begin{cases} i_{mg}^{a} = i_0 + i_1 + i_2 \\ i_{mg}^{b} = i_0 + a^2 i_1 + a i_2 \\ i_{mg}^{c} = i_0 + a i_1 + a^2 i_2 \end{cases} \tag{1}$$

where $a = e^{j2\pi/3}$ and

$$\begin{cases} i_0 = I_0 \sin(\omega t + \theta_{i0}) \\ i_1 = I_1 \sin(\omega t + \theta_{i1}) \\ i_2 = I_2 \sin(\omega t + \theta_{i2}) \end{cases} \tag{2}$$

where i_0, i_1, and i_2 are ZS, PS, and NS components in the current; $\omega = 2\pi f_{\text{line}}$ and f_{line} is the line frequency. The ZS current usually requires a neutral wire to provide the current path. Due to the transformerless structure, the MG is directly connected to the PCS. To support the unbalanced load in the MG, the neutral of the MG is formed by the PCS. As shown in Fig. 2, the grid-side PCS is a three-wire connection, while the MG-side PCS is a four-wire connection.

Considering different operation modes, the PCS serves as the source of the MG to provide load currents in the grid-connected mode. The PCS is sized such that it can support all the load current. In the islanded mode, since the MG is disconnected from the main grid, the voltage and frequency are formed by local distributed energy resource (DERs) in the MG. However, local DERs, especially commercial ones, are usually three-wire sources and have limited unbalanced capability (specifically NS capability). Therefore, in the islanded mode, the neutral of the MG is also formed by the PCS to provide the ZS current path.

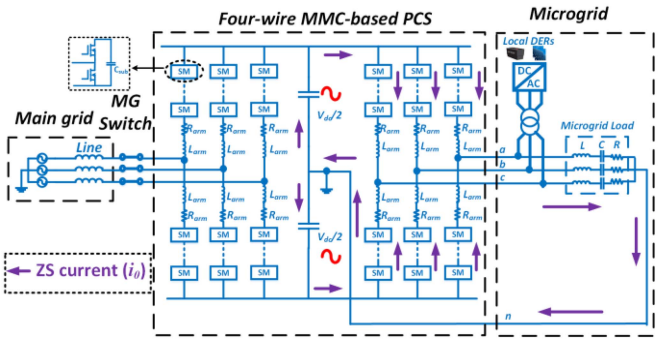

Fig. 3. Four-wire MMC-based PCS.

In the meantime, the PCS will serve as a STATCOM to reduce the NS current of sources.

B. Grid-Side Ground Impacts on ZS Current Paths

According to (1), the ZS current is defined by the summation of three-phase currents. Although the ZS current in an ac grid is mainly comprised of fundamental frequency components, the summation of three-phase currents also includes harmonic currents arising from the load or converter operation. The four-wire transformerless structure will provide paths for both types of currents.

Moreover, the main grid is usually grounded, and the PCS dc link cannot naturally block ZS currents. As a result, there will be a potential path for the ZS current, which is between the load ground and the main grid ground. As shown in Fig. 2, the ZS current will flow through the positive and negative bus of the dc-link to the MG. According to Fig. 2, the ZS currents will flow through the ground line of the main grid and MG in normal operation, which may cause false triggering of ground fault protection. In order to isolate the ZS components from the MG, specific control and design should be conducted, which will be described in Sections IV and V.

III. Unbalanced Load Impacts on MMC-Based PCS Operation

The unbalanced load is supported by the four-wire MG-side PCS. In this section, the analysis focuses on the MG-side PCS, and the analyses of the second-order circulating current and third-order harmonic ZS currents are also valid for the grid-side PCS.

A. Impacts on MG Voltage Unbalance

A four-wire MMC-based PCS is shown in Fig. 3. Based on the discussion in Section II-A, the ZS current path will be provided by the MG-side PCS. The ZS current flows into the dc-link midpoint and flows through the dc link upper and lower capacitors. The ZS current will cause a dc-link fundamental frequency voltage ripple, which can be described as follows

$$\Delta v_{\rm dc} = \Delta V_{\rm dc} \sin\left(\omega t + \theta_r\right) \tag{3}$$

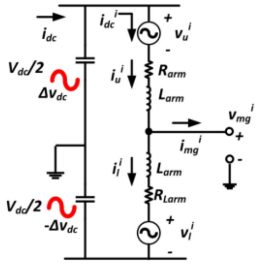

Fig. 4. Equivalent circuit of one phase leg.

where $\Delta V_{\rm dc} = \frac{I_0}{2\omega C_{\rm dc}}$ is the dc-link voltage ripple amplitude that is determined by the maximum ZS current and dc-link capacitance value [20]; the definition of ω is the same as it is in (2). In the equivalent circuit of one phase leg shown in Fig. 4, the voltage produced by the submodules is modeled by a controlled voltage source. The dc-link voltage ripples on the upper and lower half dc links have identical amplitude and in opposite directions. The upper and lower arm voltage in Fig. 4 can be described as

$$\begin{cases} v_u^i = \frac{V_{\rm dc}}{2} - v_{mg}^i - i_u^i R_{\rm arm} - L_{\rm arm}\frac{di_u^i}{dt} + \Delta v_{\rm dc} \\ v_l^i = \frac{V_{\rm dc}}{2} + v_{mg}^i - i_l^i R_{\rm arm} - L_{\rm arm}\frac{di_l^i}{dt} - \Delta v_{\rm dc} \end{cases} \tag{4}$$

where v_{mg}^i and i_{mg}^i are the voltage and current of phase i of the MG. Thus, MG phase voltage in Fig. 4 can be described as

$$v_{mg}^i = \frac{v_l^i - v_u^i}{2} + R_{\rm arm}\frac{i_l^i - i_u^i}{2} + \frac{L_{\rm arm}}{2}\frac{d\left(i_l^i - i_u^i\right)}{dt} + \Delta v_{\rm dc}. \tag{5}$$

In the grid-connected mode, the MG voltage is established by the PCS. If no unbalanced control is applied, the voltages generated by three phase legs in (5) ($\frac{v_l^a - v_u^a}{2}$, $\frac{v_l^b - v_u^b}{2}$, $\frac{v_l^c - v_u^c}{2}$) are balanced. The load currents are unbalanced, resulting in unbalanced upper and lower arm currents. From (1), the unbalanced arm currents will introduce NS and ZS voltage drops on arm inductors to cause voltage unbalance. Moreover, from (5), the dc-link voltage ripple $\Delta v_{\rm dc}$ in Fig. 4 and (5) occurs in all three phases, meaning that it is a ZS component. From the ZS perspective, it can be viewed as a voltage drop caused by the ZS current flowing through the impedance of the ZS current path (dc capacitance). According to (5), the dc-link voltage ripple will add an additional ZS voltage to the output three-phase voltage, which further increases the voltage unbalance of the whole MG.

In the islanded mode, the MG voltage is formed by local DERs. However, since the PCS provides the neutral wire and the only ZS current path for the load ZS current, the PCS will partially provide PS and NS currents and all the ZS current. The ZS voltage will be determined by the PCS control and the PCS ZS impedance. If no unbalance control is applied, the ZS current flowing into the PCS will cause ZS voltage drops on both arm inductors and dc capacitors ($\Delta v_{\rm dc}$) to result in the ZS voltage of the MG. Meanwhile, the NS current flowing into the GFM-controlled DER will result in NS voltage, worsening the MG voltage unbalance. Therefore, using the PCS to serve as a NS

current compensator will not only reduce the DER unbalanced current but also limit the voltage unbalance.

B. Harmonic ZS Current Analysis

According to Fig. 4 and [21], considering the second-order circulating current, using phase *a* as an example, the upper and lower arm currents are described as

$$\begin{cases} i_u^a = i_{\text{dc}}^a + \frac{i_{mg}^a}{2} + i_{\text{cir}}^a \\ i_l^a = i_{\text{dc}}^a - \frac{i_{mg}^a}{2} + i_{\text{cir}}^a \end{cases} \tag{6}$$

where the circulating current can be described as

$$\begin{aligned} i_{\text{cir}}^a = {} & I_0^c \sin(2\omega t + \theta_{c0}) \\ & + I_1^c \sin(2\omega t + \theta_{c1}) + I_2^c \sin(2\omega t + \theta_{c2}). \end{aligned} \tag{7}$$

Subscripts 0, 1, and 2 represent ZS, PS, and ZS components in the circulating current, respectively. According to [6], [16], and [21], if no unbalance control is applied, the average switching function of the upper and lower arms are

$$\begin{cases} S_u^a = \frac{1}{2}\left[1 - M\sin(\omega t)\right] \\ S_l^a = \frac{1}{2}\left[1 + M\sin(\omega t)\right] \end{cases} \tag{8}$$

where *M* is the modulation index. The capacitor charging current of the upper and lower arms can be written as

$$\begin{cases} i_{ua}^{ch} = S_u^a\, i_u^a = i_{\text{dc}}^a + i_{1f}^a + i_{2f}^a + i_{3f}^a \\ i_{la}^{ch} = S_l^a\, i_l^a = i_{\text{dc}}^a - i_{1f}^a + i_{2f}^a - i_{3f}^a \end{cases} \tag{9}$$

where

$$i_{\text{dc}}^a = \frac{1}{2}\, i_{\text{dc}}^a - \frac{1}{8} M \left(I_0 \cos\theta_{i0} + I_1 \cos\theta_{i1} + I_2 \cos\theta_{i2}\right) \tag{10}$$

$$\begin{aligned} i_{f1}^a = {} & \frac{1}{4}\, i_{mg} - \frac{1}{2} M I_{\text{dc}}^a \sin(\omega t) - \frac{1}{4} M I_0^c \cos(\omega t + \theta_{c0}) \\ & - \frac{1}{4} M I_1^c \cos(\omega t + \theta_{c1}) - \frac{1}{4} M I_1^c \cos(\omega t + \theta_{c1}) \end{aligned} \tag{11}$$

$$\begin{aligned} i_{f2}^a = {} & \frac{1}{2}\, i_{\text{cir}}^a + \frac{1}{8} M I_0 \cos(2\omega t + \theta_{i0}) \\ & + \frac{1}{8} M I_1 \cos(2\omega t + \theta_{i1}) + \frac{1}{8} M I_2 \cos(2\omega t + \theta_{i2}) \end{aligned} \tag{12}$$

$$\begin{aligned} i_{f3}^a = {} & \frac{1}{4}\, M I_0^c \cos(3\omega t + \theta_{c0}) \\ & \frac{1}{4} M I_1^c \cos(3\omega t + \theta_{c1}) + \frac{1}{4} M I_2^c \cos(3\omega t + \theta_{c2}). \end{aligned} \tag{13}$$

According to (12), the dc component of phase *a* can be solved

$$i_{\text{dc}}^a = \frac{1}{4}\, M \left(I_0 \cos\theta_{i0} + I_1 \cos\theta_{i1} + I_2 \cos\theta_{i2}\right). \tag{14}$$

The dc currents of the other two phases can be derived similarly, which will be impacted by the PS, NS, and ZS current amplitude as well as phase angles. Thus, the three-phase dc currents are not equal. Also, from (8)–(13), the submodule capacitor ripples can be derived as

$$\begin{cases} v_{\text{sub}}^{ua} = \frac{1}{j\omega C_{\text{sub}}}\, i_{f1}^a + \frac{1}{j2\omega C_{\text{sub}}} i_{f2}^a + \frac{1}{j3\omega C_{\text{sub}}} i_{f3}^a \\ v_{\text{sub}}^{la} = -\frac{1}{j\omega C_{\text{sub}}} i_{f1}^a + \frac{1}{j2\omega C_{\text{sub}}} i_{f2}^a - \frac{1}{j3\omega C_{\text{sub}}} i_{f3}^a \end{cases}. \tag{15}$$

The submodule voltage will contain the first, second, and third orders components. For the upper and lower arms, the odd number of harmonic ripples have the opposite direction, which may result in corresponding order currents in the output currents. The even-order ripples have the same direction, leading to the internal circulating current. Based on this analysis, since the MG-side PCS is a four-wire topology that can provide a path for the third-order harmonics, the upper and lower arm current in Fig. 4 can be updated as

$$\begin{cases} i_u^a = i_{\text{dc}}^a + \frac{i_{mg}^a}{2} + i_{\text{cir}}^a + \frac{i_{3f}}{2} \\ i_l^a = i_{\text{dc}}^a - \frac{i_{mg}^a}{2} + i_{\text{cir}}^a - \frac{i_{3f}}{2} \end{cases}. \tag{16}$$

Furthermore, if arm currents are updated from (6) to (16), the capacitor charging and discharging current can have fourth-order components and will introduce fifth-order ripples. Therefore, in general, the MMC upper and lower arm currents can be written as

$$\begin{cases} i_u^a = \sum_{k=0}^{n} i_{(2k)f}^a + \sum_{k=0}^{n} i_{(2k+1)f}^a \\ i_l^a = \sum_{k=0}^{n} i_{(2k)f}^a - \sum_{k=0}^{n} i_{(2k+1)f}^a \end{cases}. \tag{17}$$

The odd-order components will flow out of the converter, and even-order components will circulate within the converter. For the harmonic ZS current, the odd-order components (180 Hz, 540 Hz, etc.) will flow out of the MMC through the neutral wire, and the even-order components will not impact the MG.

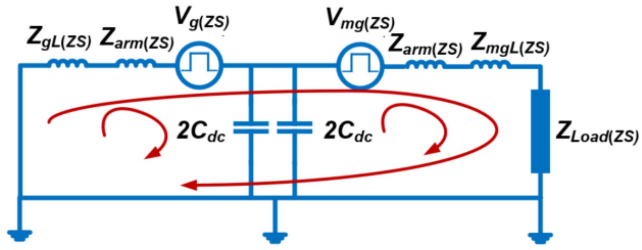

Fig. 5. Equivalent CM circuit of the PCS.

C. Harmonic ZS Current Impacts

The transformerless structure provides a path for the harmonic ZS current, which will cause more harmonics in the PCS currents. The equivalent ZS circuit of the ASMG is shown in Fig. 5. There are three paths for the ZS currents. Besides the ZS current paths in Fig. 2, there will be another path for harmonic ZS currents, which is between the grounding of the main grid and dc-link midpoint. The ZS currents are affected by ZS impedances of lines, arm inductors, dc capacitors and loads. The harmonic ZS currents will affect the power quality of the PCS output currents. To limit the harmonic ZS current, both control and hardware solutions are considered.

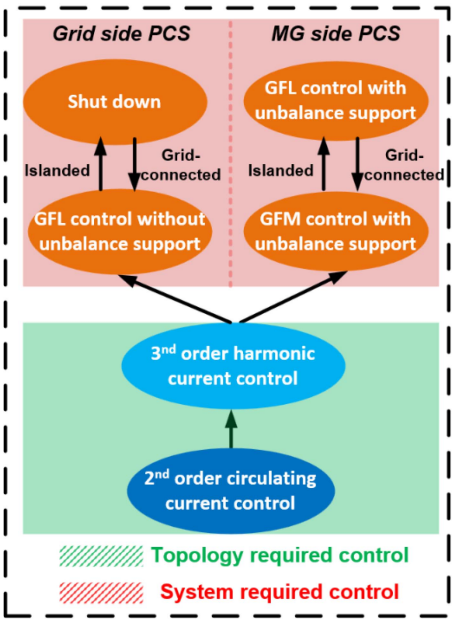

Fig. 6. PCS overall control structure.

From the perspective of control, the PCS controller can regulate the low-frequency ZS current (third-order) to zero. As for the high-frequency ZS current, the hardware design approach will be applied. According to Fig. 5, increasing the arm inductance is a direct way because the arm inductance is placed in all three paths of ZS currents. The design of the arm inductance will be provided in Section V.

IV. Control Design and Impact Analysis

The overall PCS control structure is shown in Fig. 6, including the converter topology required control functions and the ASMG operation required control functions. In this section, the control algorithms of the MMC are proposed. The corresponding impacts of the proposed algorithms on the MMC operation are also analyzed.

A. Topology Required Control Functions

1) Second-Order Circulating Current Control: Second-order circulating current has been analyzed in the literature [22]. In this article, a direct second-order current control is applied, as shown in Fig. 7, where a nonideal proportional resonant (PR) controller with 120 Hz resonant frequency is applied to regulate the second-order current to be zero in each arm [23]. After the control is applied, the second-order term in (6) can be regulated to be zero. Also, since the second-order control is applied, the second components in the arm current can be viewed as zero, while the average switching functions in (8) need to consider the second-order components, which are

$$\begin{cases} i^a_{u(2nd)} = i^a_{\rm dc} + \frac{i^a_{mg}}{2} \\ i^a_{l(2nd)} = i^a_{\rm dc} - \frac{i^a_{mg}}{2} \end{cases} \tag{18}$$

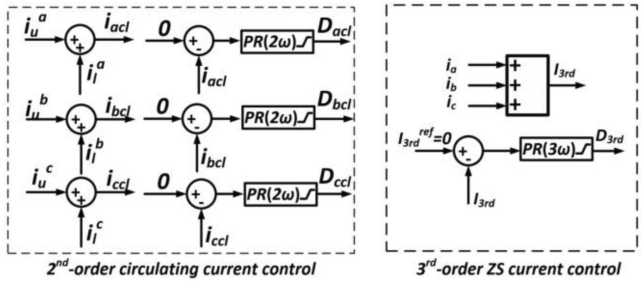

Fig. 7. Topology required control functions.

$$\begin{cases} S^a_{u(2nd)} = \frac{1}{2}\left[1 - M\sin(\omega t) + M_{(2nd)}\sin(2\omega t + \theta_{2nd})\right] \\ S^a_{l(2nd)} = \frac{1}{2}\left[1 + M\sin(\omega t) + M_{(2nd)}\sin(2\omega t + \theta_{2nd})\right] \end{cases}. \tag{19}$$

Therefore, the updated submodule capacitor charging current can be written as

$$\begin{cases} i^{ch}_{ua(upd)} = i^a_{dc(upd)} + i^a_{1f(upd)} + i^a_{3f(upd)} \\ i^{ch}_{la(upd)} = i^a_{dc(upd)} - i^a_{1f(upd)} - i^a_{3f(upd)} \end{cases} \tag{20}$$

where the dc components are the same as (14), the second-order components are regulated to be zero. The fundamental and third-order components in (20) are

$$\begin{aligned} i^a_{f1} = {} & \frac{1}{4} i_{mg} - \frac{1}{2} M i^a_{\rm dc}\sin(\omega t) \\ & + \frac{1}{8} M_{(2nd)} I_0 \cos(\omega t + \theta_{(2nd)} - \theta_{i0}) \\ & + \frac{1}{8} M_{(2nd)} I_1 \cos(\omega t + \theta_{(2nd)} - \theta_{i1}) \\ & + \frac{1}{8} M_{(2nd)} I_2 \cos(\omega t + \theta_{(2nd)} - \theta_{i2}) \end{aligned} \tag{21}$$

$$\begin{aligned} i^a_{f3} = {} & -\frac{1}{8} M_{(2nd)} I_0 \cos\left(3\omega t + \theta_{(2nd)} + \theta_{i0}\right) \\ & - \frac{1}{8} M_{(2nd)} I_1 \cos\left(3\omega t + \theta_{(2nd)} + \theta_{i1}\right) \\ & - \frac{1}{8} M_{(2nd)} I_2 \cos\left(3\omega t + \theta_{(2nd)} + \theta_{i2}\right). \end{aligned} \tag{22}$$

Therefore, although the second-order current is regulated to be zero, the third-order current can still be generated by the added circulating current control.

2) Third-Order Harmonic Current Control: According to the aforementioned analysis, the MMC topology will generate a third-order harmonic current in the output current which negatively impacts the grid and MG current power quality. To avoid this impact of the third-order harmonic current, a third-order harmonic current controller is applied for both grid and MG-side PCS. The nonideal PR controller with 180 Hz resonant frequency is utilized to eliminate the third-order harmonic ZS current. As shown in Fig. 7, instead of regulating the third-order current in each phase, the control is applied to regulate the third-order harmonic current in the summation of the three-phase

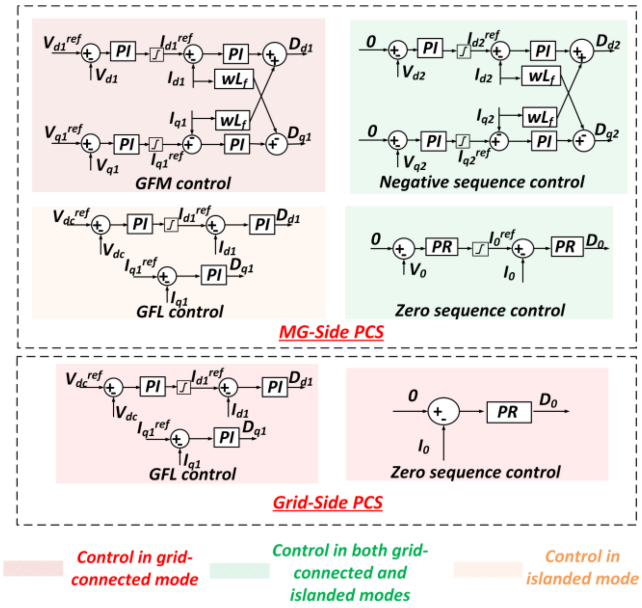

Fig. 8. Detailed control algorithm of the PCS.

currents to eliminate the flowing path of the third-order harmonic current.

Moreover, the added third-order current control will result in third-order components in (19) to further introduce fourth and higher-order components. Therefore, when control is applied, the harmonic analysis in (17) is still valid.

B. System Required Control Functions

1) MG-Side PCS Control Functions: The control diagram of the MG-side PCS is shown in Fig. 8, including control algorithms in both grid-connected and islanded modes. In the grid-connected mode, the MG-side PCS serves in the GFM mode to regulate the MG voltage and frequency. The local DERs in the MG usually operate in the GFL mode to regulate output power. For the unbalanced load support, the NS and ZS voltages of the PCS are controlled to be zero so that the PCS can provide a balanced output voltage for the MG. In addition, since the NS and ZS voltages are zero, the equivalent output NS and ZS impedances of the MG-side PCS can be viewed as zero. The ZS voltage caused by the dc-link voltage ripple can also be compensated. The unbalanced load current will be provided by the PCS to reduce the load unbalance impacts on the local DERs in the MG.

In the islanded mode, local DERs will change the operation mode to GFM mode to provide the MG with voltage and frequency. The PCS operates in the GFL mode to regulate the MV dc-link voltage and provide reactive power to the MG. The unbalance control is the same as the grid-connected mode. From the ZS perspective, the ZS voltage in the MG is determined by the load ZS current, line impedances, and the PCS ZS impedance. The MG usually has small line impedances, so the PCS ZS voltage is the main reason for the MG ZS voltage. Regulating the PCS ZS voltage to zero can limit the ZS voltage in the MG to meet the voltage unbalance requirement in [8]. From the NS perspective, the NS current will flow into the GFM-controlled DERs and the PCS. By controlling the PCS NS voltage to zero, the impedance of the NS current of the PCS will be small or even zero if line impedances are neglected. Load NS currents will be compensated by the PCS. Therefore, the NS current of the local DERs will be reduced, and the NS voltage requirement in [24] can be met.

2) Grid-Side PCS Control Functions: The control diagram of the grid-side PCS is shown in Fig. 8. The grid-side PCS is shut down in the islanded mode. In the grid-connected mode, the grid-side PCS serves in the GFL mode to regulate MV dc-link voltage and output reactive power to the main grid. According to the analysis in Section II, the transformerless PCS topology will result in one additional fundamental-frequency ZS current path. In order to decouple the MG-side load unbalance impacts on the main grid, a ZS current control is applied to the grid-side PCS. By regulating the ZS current to be zero, the grid-side PCS can eliminate the grid-side ZS current path. All the ZS current in the MG flows through the MG-side path in Fig. 2.

C. Stability Analysis

For the proposed control algorithms in *dq* coordinates, the stability analysis has been conducted in the existing literature [25]. In this section, the stability of the fundamental frequency ZS control and the third-order harmonic ZS current control are conducted. For these two controllers, the control parameters need to ensure a sufficient phase margin of the compensated loop gain so that the converter is stable.

For the fundamental frequency ZS control, a PR controller with a 60 Hz resonant frequency is applied. To design a stable PR controller, the average model of a MMC in [26] is applied, and the digital delay (1.5 switching cycle) is considered [27]. The controller's bode plots and the compensated open-loop gain are shown in Fig. 9(a), where the PR parameters are $k_p = 0.013$, $k_r = 1.2$. The MMC's parameters are 25 kV dc voltage, 13.8 kV ac voltage, 100 kVA power, 90 mH arm inductance, and 10 kHz control frequency. The transfer function of the compensated open-loop gain (with delay considered) is

$$G_{\mathrm{op}(60)}^{\mathrm{com}} = \frac{325s^2 + 1.905 \times 10^5 s + 4.619 \times 10^7}{0.09s^3 + 0.6055s^2 + 1.279 \times 10^4 s + 5685} \times e^{-1.5\times10^{-4}s}. \quad (23)$$

From Fig. 9(a), the designed control parameters can ensure a 49.5-degree phase margin, meaning that the controller stability is realized. For the third-order harmonic ZS current controller, the bode plots are shown in Fig. 9(b), where the PR parameters are $k_p = 0.0129$, $k_r = 1.18$. The transfer function of the compensated open-loop gain for the third-order harmonic ZS current controller is

$$G_{\mathrm{op}(180)}^{\mathrm{com}} = \frac{325s^2 + 1.905 \times 10^5 s + 4.157 \times 10^8}{0.09s^3 + 0.6055s^2 + 1.151 \times 10^5 s + 5.116 \times 10^4} \times e^{-1.5\times10^{-4}s}. \quad (24)$$

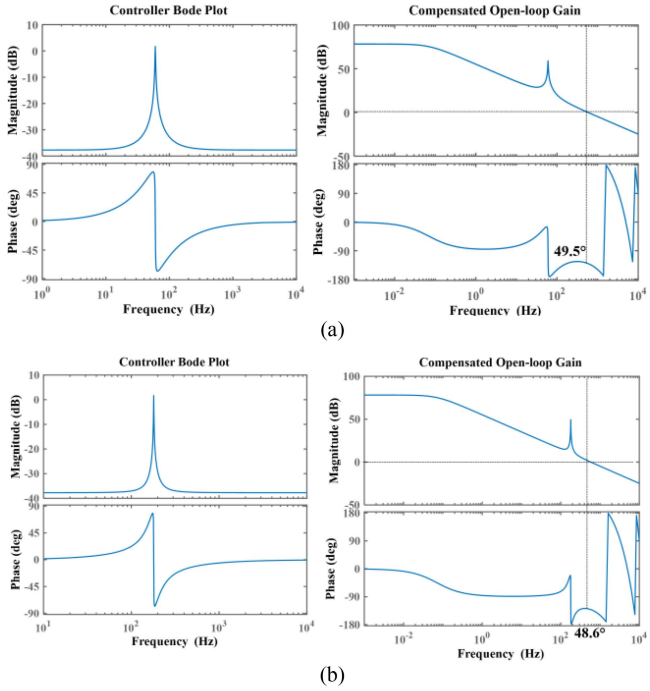

Fig. 9. Stable controller design. (a) Fundamental ZS controller. (b) Third-order harmonic ZS controller.

From the bode plot, a 48.6° phase margin for the compensated open-loop gain is realized.

V. Unbalanced Load and Transformerless Structure Impacts on the Hardware Design

According to the aforementioned analyses, the transformerless structure will result in ZS current, harmonic ZS currents and voltage unbalance, which will affect the design of dc-link capacitors and arm inductors of a MMC-based PCS.

A. Dc-Link Capacitor Design

In a four-wire MMC with a split dc-link capacitor topology, the dc-link capacitors are used only for the ZS current path. Therefore, the dc-link voltage ripples are caused by the ZS currents. Note that a three-phase MMC is composed of three phase legs, and the second-order power ripples of each phase leg are provided by the submodule capacitors. The second-order dc-link voltage ripples are limited by the circulating current control. According to (HYPERLINK 2), the dc-link voltage ripple is written as [20]

$$\Delta V_{\rm dc} = \frac{1}{2C}\int_{-\frac{\theta_{i0}}{\omega}}^{-\frac{\pi-\theta_{i0}}{\omega}} I_0 \sin\left(\omega t + \theta_{i0}\right) dt = \frac{I_0}{\omega C} \tag{25}$$

where C is the total capacitance of dc link. Therefore, the capacitance design requirement is

$$C \geq \frac{I_{0m}}{2\omega \Delta V_{\rm dc}^m} \tag{26}$$

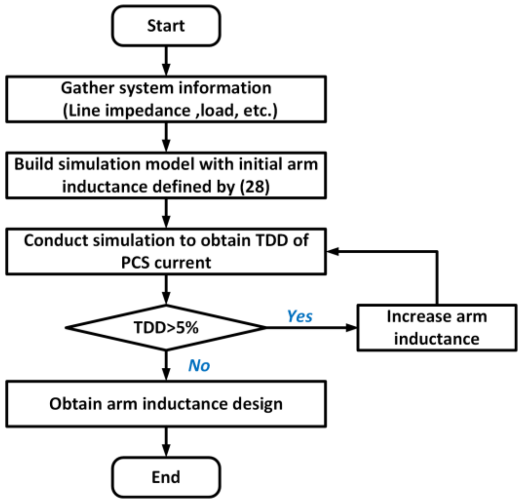

Fig. 10. Arm inductor design methodology considering TDD requirement.

where I_{0m} is the peak value of the maximum ZS current and $\Delta V_{\rm dc}^m$ is the maximum allowed dc-link voltage variation, which is determined by the voltage level of ac MG and dc link. Since the MG side is four-wire, third-order harmonic injection modulation strategies cannot be applied. The maximum modulation index is 1. The dc-link ripple requirement is defined as:

$$\frac{V_{\rm dc}}{2} - \Delta V_{\rm dc}^m \geq V_p \tag{27}$$

where V_p is the peak value of the phase voltage.

B. Arm Inductor Design

In the literature, when the second-order circulating current control is applied, the arm inductor design has considered the current ripple impacts [28], which is described as

$$L_{\rm arm} \geq \frac{NT_s}{8\omega C_{\rm sub} I_{pp}^{\rm max}} \sqrt{\frac{9}{16} I_{ac}^2 + \frac{1}{9} I_{\rm dc}^2 - \frac{1}{2} I_{ac} I_{\rm dc}} \tag{28}$$

where $C_{\rm sub}$ is the submodule capacitance; $I_{pp}^{\rm max}$ is the maximum peak-to-peak current; N is the submodule number; and T_s is the switching time. The design in [28] is for a three-wire MMC. The calculated arm inductance from (28) may not be sufficient for a four-wire transformerless structure because the odd-order ZS harmonic currents also have paths.

For the arm inductor design, a total demand distortion (TDD) related requirement is considered. From the grid power quality requirement, the low-frequency harmonics (up to 50th-order harmonics) need to be less than 5%, according to [29]. Therefore, the arm inductor design methodology is summarized in Fig. 10. ASMG information is gathered first. The simulation model is built with control functions in grid-connected mode. Note that in the design simulation, the full load condition is simulated to consider the worst scenario. The initial arm inductance is selected based on (28), which can meet the current ripple requirement. In the simulation, the arm inductance is increased from the initial arm inductance [obtained from (28)] until the PCS current TDD

TABLE I
SIMULATION SETUP PARAMETERS

	Items	Information
MMC	MG voltage rating	13.8 kV
	MG power rating	100 kVA
	Switching frequency	10 kHz
	Submodule number	4
	Submodule topology	Half bridge
	Arm inductance	90 mH
	MV dc capacitance	12.5 μF
	Submodule capacitance	8.75 μF
BESS	BESS inverter voltage	480 V
	BESS inverter power	100 kVA
	BESS transformer impedance	5%
	BESS transformer connection	Δ (MV)-Yg (LV)
Load	Load resistance	R_a=R_b=R_c= 246 Ω
	Load capacitance	C_a=C_b=1.25 μF, C_c=12.5 μF

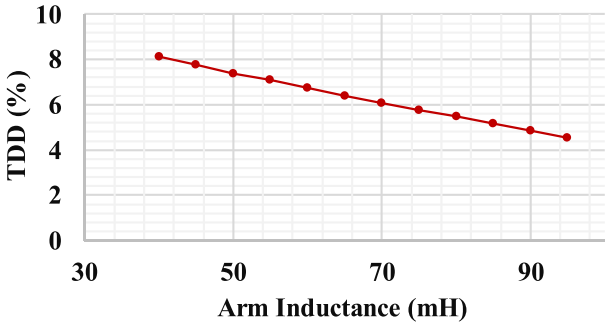

Fig. 11. Arm inductance design.

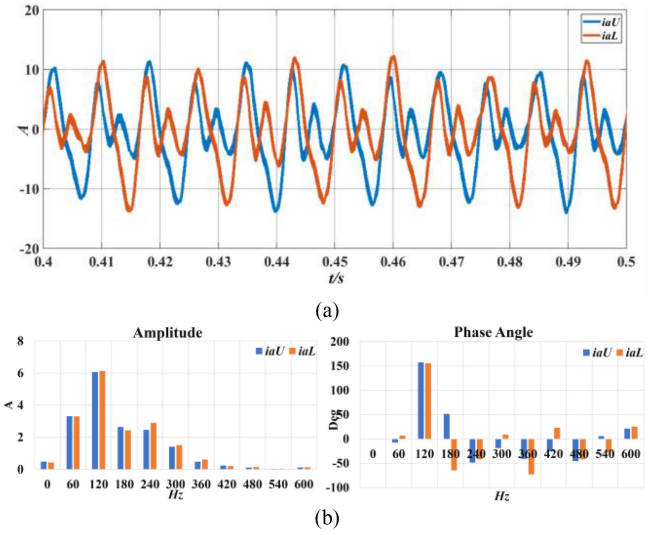

Fig. 12. Upper and lower arm current of grid-side PCS without topology-related control. (a) Waveforms. (b) Frequency spectra.

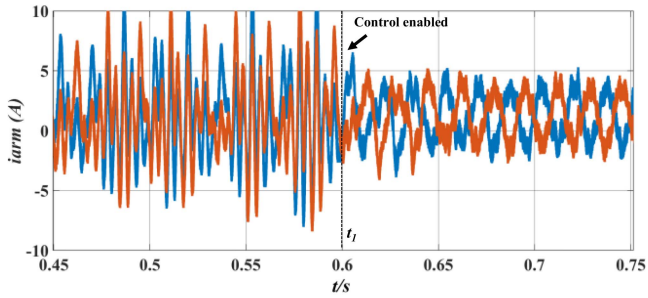

Fig. 13. Second-order circulating current control verification.

requirement can be met, and the minimum arm inductance that can meet the requirement is selected.

VI. SIMULATION VERIFICATION

The simulation follows the setup in Fig. 3, where a battery energy storage system (BESS) with a three-wire inverter is applied as the local DER. The adopted modulation is nearest-level pulsewidth modulation [30], and the detailed parameters are given in Table I.

The dc capacitance is selected with a 5% (peak-to-peak) dc-link ripple requirement. The arm inductance is designed based on the methodology in Fig. 10. As shown in Fig. 11, when the total TDD of the PCS output current is 5%, the arm inductance is ∼90 mH. The simulation is applied to verify the topology-related control as well as the system-related control.

A. Topology-Related Control

1) Arm Current Harmonic Current Analysis: In the simulation, the arm current of the grid-side PCS is used for harmonic analysis. The simulation results are shown in Fig. 12, where no topology-related control is applied. The arm currents in Fig. 12(a) are rich in harmonics. The frequency spectrums up to ten-order components are shown in Fig. 12(b), including both the amplitude and phase angle of each component. The results show that the amplitude of odd-order components of the upper and lower arms are close while phase angles are in opposition to each other. As for even-order components, both the amplitude and phase are close. The simulation results verify the analysis in (17).

2) Second-Order Circulating Current Control: The simulation results of the PCS arm current (phase *a* of MG-side PCS in the grid-connected mode) are shown in Fig. 13. The second-order control was enabled at time t_1. After the control was enabled, the second-order components in upper and lower arm currents were eliminated. With the circulating current control, the second-order circulating current can be eliminated under the unbalanced load condition.

3) Third-Order Harmonic Current Control: The simulation results of the grid-side PCS current are shown in Fig. 14. The third-order harmonic current control was applied at time t_1. When the third-order harmonic current control was not applied, third-order harmonic current flows into the main grid, which verifies the four-wire MMC analysis in Sections III and IV. After the third-order control was applied, the third-order harmonic current can be eliminated.

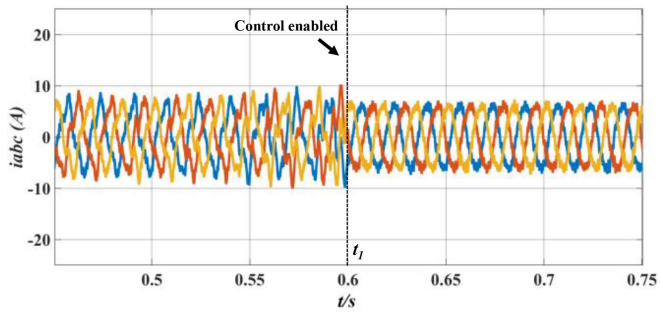

Fig. 14. Third-order harmonic current control verification.

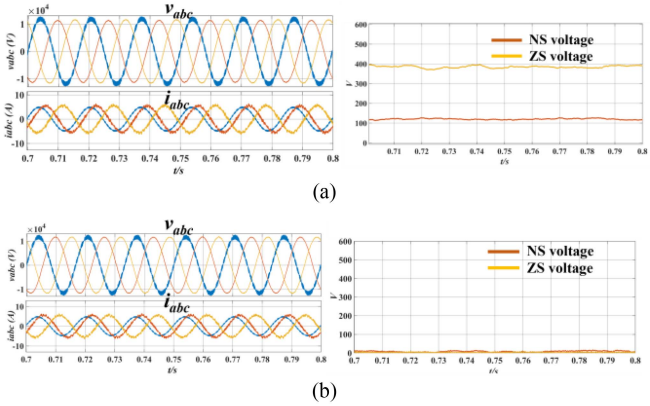

Fig. 15. Voltage unbalance regulation in the grid-connected mode. (a) Without proposed control. (b) With proposed control.

B. System-Related Control

1) Voltage Unbalance Control in the Grid-Connected Mode: In the grid-connected mode, the proposed unbalance control is compared to the conventional output voltage control in *dq* coordinates without considering unbalance regulation. The simulation is shown in Fig. 15(a). The arm inductor voltage drops, and dc-link voltage ripples result in the voltage unbalance, which can potentially impact the load operation and equipment safety in the MG. When the proposed voltage unbalance control is applied as shown in Fig. 15(b), the arm inductor voltage drops, and the dc-link voltage ripple can be compensated. The MG voltage is regulated to be balanced.

2) Load Unbalance Distribution in the Grid-Connected Mode: In this grid-connected mode, the PCS should decouple the MG-side load unbalance impacts on the main grid. The PCS only transfers active power between the main grid and MG. The simulation results are shown in Fig. 16. Before t_1, the MG-side DER output 6 kW active power and 1 kW reactive power, and the grid-side PCS did not enable the proposed ZS current control in Fig. 8. Therefore, there were two ZS current paths. The load ZS current flowed to the grid side and back to the MG through the PCS. Also, the dc current contained ZS currents. The ZS current control of the grid-side PCS was enabled at t_1 to eliminate the ZS current path of the grid side. The grid-side PCS current became balanced and no ZS components were on the dc-link current. The active power of the local DER was increased to 40 kW at time t_2, and the grid-side PCS current was increased accordingly. The reactive power of the local DER increased to 30 kW at time

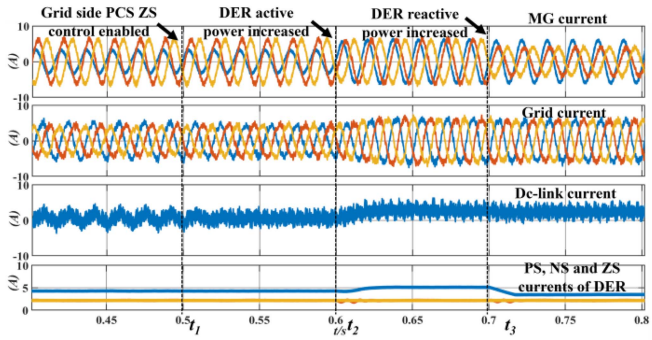

Fig. 16. Load unbalance distribution in the grid-connected mode.

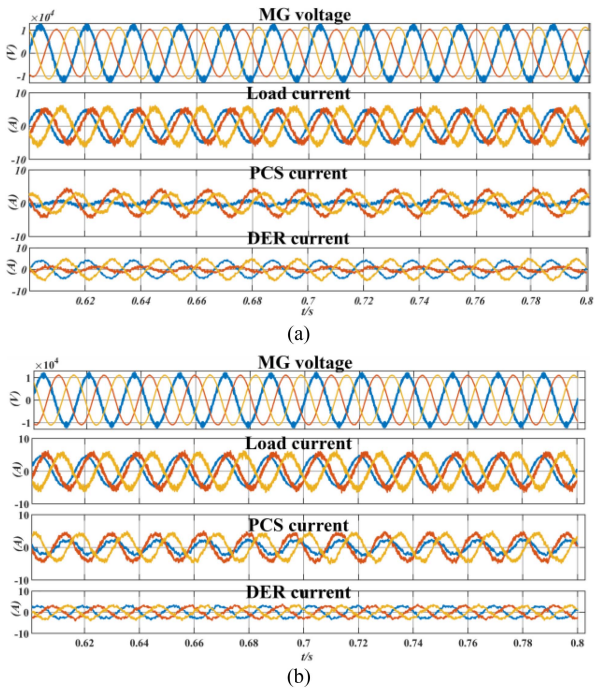

Fig. 17. PCS unbalanced load support in the islanded mode. (a) Without unbalance control. (b) With unbalance control.

t_3, while the grid-side PCS current did not change. From the sequence perspective, when the active or reactive power of the DER was changed, only the PS component of the MG-side PCS current was changed. The NS and ZS components of the DER were not changed, meaning that, with the proposed control, the MG PCS provided all the unbalanced currents of the MG load.

3) Load Unbalance Compensation in the Islanded Mode: In the islanded mode, the MG-side PCS serves as a compensator and NFT to compensate NS current and provide a ZS current path. The simulation results are shown in Fig. 17. When the proposed unbalance control is not applied, the PCS will also provide the ZS current path. However, as shown in Fig. 17(a), the PCS arm inductance and dc-link capacitance will result in NS and ZS voltage drop to cause voltage unbalance of the MG. By applying the proposed unbalance control, the MG voltage unbalance can be eliminated. In the meantime, when the unbalance control is not enabled, since the DER is the GFM source of the MG, the load NS current will flow into both the PCS

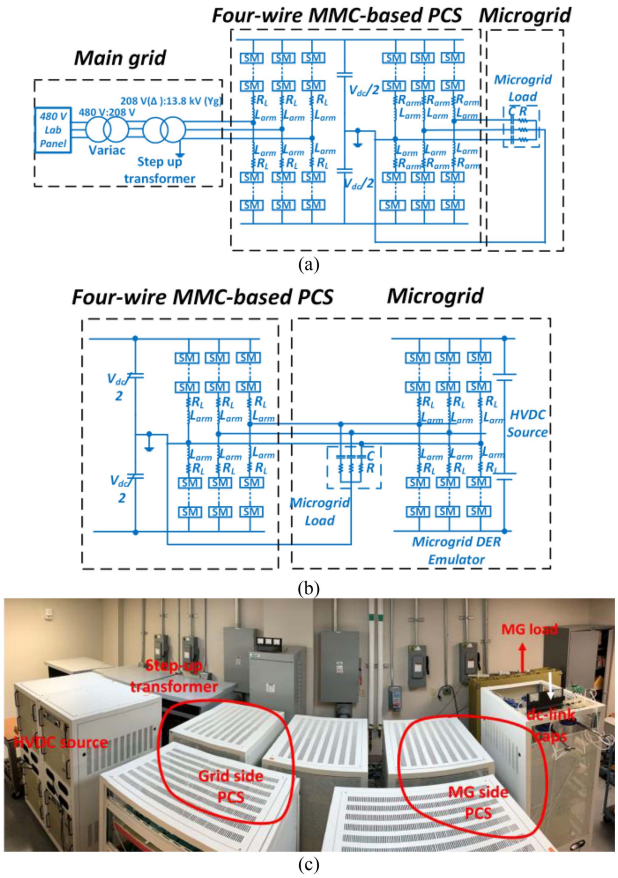

Fig. 18. Experimental setup. (a) Grid-connected mode. (b) Islanded mode. (c) Hardware setup.

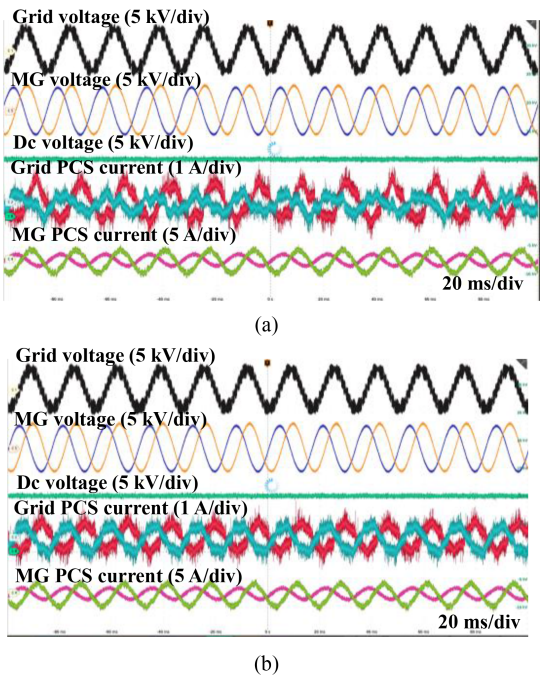

Fig. 19. Third-order current and ZS current control verification. (a) Without proposed in grid-side PCS. (b) With proposed control in grid-side PCS.

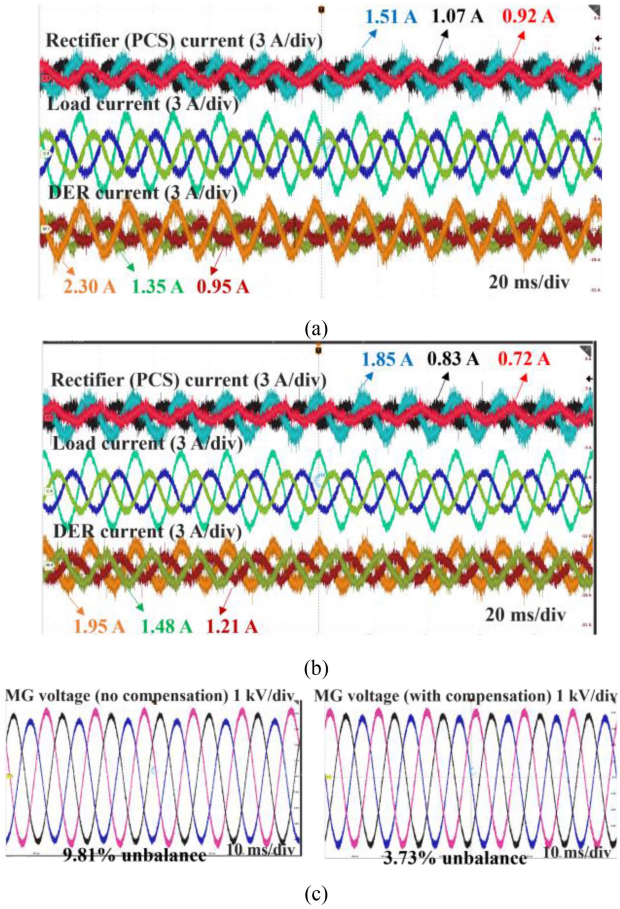

Fig. 20. Unbalance compensation testing in the islanded mode. (a) Current distribution without unbalance control. (b) Current distribution with unbalance control. (c) Voltage unbalance comparison.

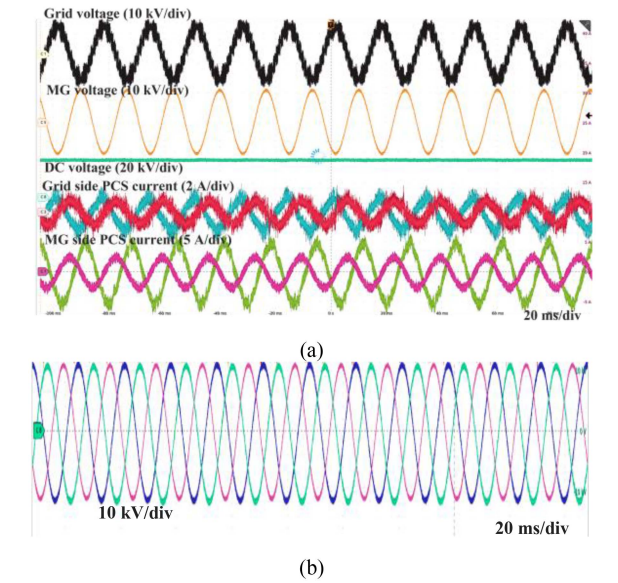

Fig. 21. Full voltage testing in the grid-connected mode. (a) Overall waveforms. (b) MG voltage waveforms.

TABLE II
LOAD AND DC CAPACITANCE UNDER DIFFERENT TESTING CONDITIONS

	Dc Capacitance	Load Condition
PCS unbalance compensation in the islanded mode	C_{dc}=4.25 μF	R_a=R_b=R_c= 246 Ω C_a=C_b=1.25 μF, C_c=2.5 μF
Other Cases	C_{dc}=19 μF	R_a=R_b=R_c= 246 Ω C_a=C_b=1.25 μF, C_c=0.625 μF

TABLE III
SUMMARY OF THE CONTROL PERFORMANCE DEMONSTRATION

	Without proposed control	With proposed control
Third-order harmonic current	0.38 A	0.11 A
ZS current of grid-side PCS	0.41A	0.07 A
PCS current (peak) in islanded mode	I_a= 0.92 A I_b= 1.07 A I_c= 1.51 A	I_a= 0.72 A I_b= 0.83 A I_c= 1.85 A
DER current (peak) in islanded mode	I_a= 1.35 A I_b= 0.95 A I_c= 2.30 A	I_a= 1.48 A I_b= 1.21 A I_c= 1.95 A
Voltage unbalance	NS voltage: 3.05% ZS voltage: 6.76%	NS voltage: 1.04% ZS voltage: 2.69%

and the local DER. The NS current distribution is determined by the NS impedance of the DER inverter as well as the PCS. After the unbalance control is enabled, the PCS regulated the NS voltage to be zero to provide a low impedance path for the NS current. Therefore, the DER current became balanced. The proposed control can reduce the current unbalance of local DERs in the MG.

VII. EXPERIMENTAL DEMONSTRATION

A. Experiment Setup

A back-to-back connected MMC-based PCS is realized. Except for the dc-link capacitance, the rest of the parameters are the same as the parameters in Table I. Due to the availability of the capacitor product in the MV application, the dc-link capacitance in the PCS is selected to be 19 μF, which can also meet the requirement in (26). The 10 kV SiC MOSFET is applied for the half-bridge submodule. The load condition follows in Table I.

The testing setup is shown in Fig. 18. In the grid-connected mode shown in Fig. 18(a), to realize a 13.8 kV grid in the laboratory, two transformers are utilized. The 480 V (line-to-line voltage) lab panel is connected to a variac to output 208 V. The variac output is connected to a step-up transformer with a Δ-Yg connection to boost the voltage to 13.8 kV. The local DER only provides balanced output power in the grid-connected mode, which will not impact the unbalanced load support of the PCS. Therefore, the local DER is not emulated in the grid-connected mode. As shown in Fig. 18(b), in the islanded mode, the MG voltage is provided by the local DER. Therefore, the DER emulator needs to be emulated. Since the grid-side PCS is shut down in the islanded mode, it is utilized to emulate the local DER in the MG. The MG-side PCS serves as a rectifier in the islanded mode. The hardware implementation is shown in Fig. 18(c).

B. Testing for Control Demonstration

To verify the analysis of load unbalance impacts on the MMC-based PCS, the control functions will be demonstrated by comparing the results with and without the proposed control algorithms. The comparison will be conducted at 10 kV dc-link voltage first. Then the testing results at the full voltage (25 kV dc) with all proposed control functions will be provided. To support the algorithm testing, the load and dc capacitances are changed, which are given in Table II. The MG load mainly consumes reactive power. This is because the step-up transformer ratio is large and the power panel in the laboratory has limited active power capability. Reactive power-dominated load will be supported by the MG-side PCS to reduce the current of the laboratory power panel. The grid-side PCS will provide the small active power drawn by the load resistors.

1) Third-Order Harmonic Current Control and Grid-Side ZS Current Elimination in the Grid-Connected Mode: In the grid-connected mode, the MG-side load is unbalanced. When the third-order and fundamental frequency ZS current control algorithms are not implemented in the grid-side PCS, the testing results are shown in Fig. 19(a). Due to the third-order harmonic components, the grid-side PCS current is distorted, which can verify the PCS harmonic current analysis. Meanwhile, without the ZS current control, the MG load ZS current flow into the grid-side PCS to cause current unbalance. When the control is implemented as shown in Fig. 19(b), the grid-side PCS current distortion is eliminated, and the PCS current becomes balanced. The detailed data are given in Table III. With the proposed control algorithms, the PCS can realize the unbalanced load decoupling. As a result, the unbalanced load in the MG will not affect the main grid, which also demonstrates the benefit of the ASMG configuration.

2) Unbalance Compensation in the Islanded Mode: To verify the voltage unbalance analysis and demonstrate the proposed unbalanced voltage control, as given in Table II, the dc-link capacitance is reduced from 19 to 4.25 μF and the load unbalance is increased to create a worse unbalance condition. As shown in Fig. 20(a), when the control is not applied, the PCS and local DER share the unbalanced current. Note that the peak values of the PCS current and DER current are labeled. Due to the PCS and DER impedances, the MG voltage is unbalanced (3.05% NS and 6.76% ZS), which cannot meet the voltage unbalance requirement. When the proposed unbalance control is utilized, the testing results are shown in Fig. 20(b). After the unbalance control is applied, the PCS will provide a more unbalanced current to reduce the unbalance of the DER current. As shown in Fig. 20(c), the unbalance of MG voltage is reduced to 1.04% NS and 2.69% ZS to meet the voltage unbalance requirement in [8] and [24]. The detailed data are also summarized in Table III. With the proposed control algorithm, the PCS will compensate for the unbalanced load in the MG so that the unbalanced current requirements of DERs can be reduced.

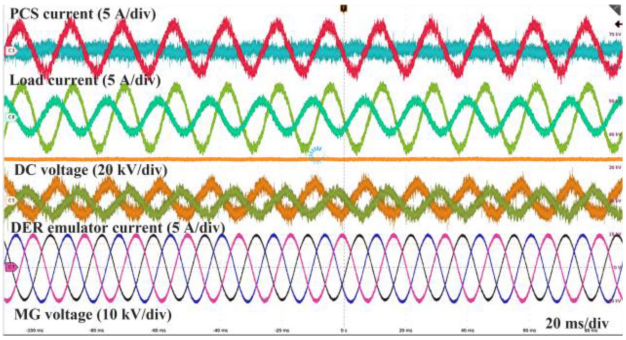

Fig. 22. Full voltage testing in the islanded mode.

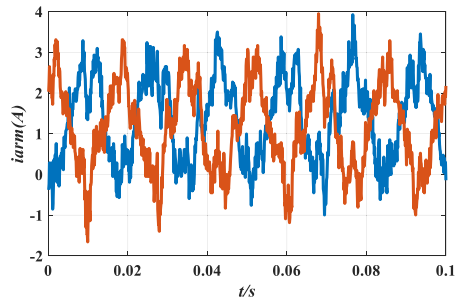

Fig. 23. Arm currents of phase *a* (MG-side PCS).

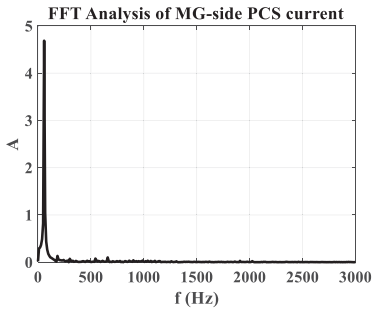

Fig. 24. FFT analysis of MG-side PCS current (phase *a*) up to 50th-order harmonic current.

C. Full Voltage Testing

The PCS unbalanced load support capability is demonstrated under full dc-link voltage (25 kV) to support a 13.8 kV ac MG. The full voltage testing includes the grid-connected mode and islanded mode. With the proposed control functions, as shown in Fig. 21(a), the PCS can support the unbalanced load in the MG and eliminate the third-order and fundamental ZS currents in the grid-side PCS in the grid-connected mode. Due to the limitation of the number of scope channels, the MG voltage is measured separately. As shown in Fig. 21(b), the MG voltage can also be regulated to be balanced.

The testing results of the islanded mode are shown in Fig. 22. The waveforms show that the PCS can provide ZS current path and serve as a compensator to reduce the DER unbalanced current. The DER voltage is also compensated to be balanced.

The arm currents of phase *a* in MG-side PCS are shown in Fig. 23. Due to the MV operation, the arm current within the converter cabinet cannot be directly measured by probes. The waveforms are the measurement feedback of arm currents in the PCS controller. The waveforms show that under unbalanced load conditions, the circulating current control can still eliminate the second-order components in the arm current.

Fast Fourier transform (FFT) analysis up to 50th-order harmonic currents of MG-side PCS current in the grid-connected mode is conducted. The FFT results are shown in Fig. 24. The TDD of MG-side PCS current is 4.91%, which meets the TDD requirement in [29].

VIII. Conclusion

A four-wire MMC-based PCS can form a transformerless structure for an ASMG, leading to numerous challenges for the design and control of the MMC. Based on the analysis, the challenges are summarized as follows.

1) The PCS needs to provide the MG with a neutral in both grid-connected and islanded mode.
2) The transformerless PCS cannot block ZS current path, so the fundamental and harmonic ZS currents will flow into the grounding line of the main grid to affect the protection.
3) The dc-link voltage ripples and arm inductance voltage drop will cause output voltage unbalance of the PCS.
4) The odd-order harmonic ZS currents of MMC will flow into the grid and MG.

In order to solve the challenges, the control and design methods are proposed for the MMC-based PCS. From the design perspective, the dc-link capacitors are designed to provide the neutral of the MG. The arm inductance is designed to eliminate the high-order harmonic ZS currents to meet the TDD requirement.

From the control perspective, a third-order harmonic current controller is proposed to eliminate the low-order harmonic ZS currents for the grid-side PCS and MG-side PCS. A fundamental ZS current control is proposed for the grid-side PCS to limit the avoid the ZS current flowing to the grounding line of the main grid. An NS and ZS voltage control is applied to the MG-side PCS to compensate for the voltage unbalance in the grid-connected mode and compensate for the unbalanced currents of DERs in the islanded mode.

Moreover, a MV MMC-based PCS is developed to demonstrate the hardware design and the proposed control strategies up to 13.8 kV ac voltage.

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