Degradation Dependency Analysis and Modeling of 1700 V Planar-Gate SiC MOSFETs Under Gate Switching Instability

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***Abstract*—Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are becoming increasingly prevalent in various power electronic applications. However, their widespread adoption is hindered by significant reliability issues related to the gate oxide. The threshold voltage drift under alternating gate bias, commonly referred to as gate switching instability (GSI), presents a substantial challenge to reliability. Given the widespread use of SiC MOSFETs in power converters, researching GSI is of practical significance compared to conventional bias temperature instability. This study systematically investigated the dependence of 1700 V planar-gate SiC MOSFETs on factors, such as gate bias, temperature, and switching time, and also provided the form of acceleration factor based on the physical explanation. Based on this, an accelerated degradation model was developed to quantify the impact of stresses on GSI for the first time. This research enhances the understanding of GSI and establishes a foundational framework for modeling and predicting the degradation of SiC MOSFETs under GSI.**

***Index Terms*—Degradation dependency analysis, degradation modeling, gate switching instability (GSI), reliability, silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs).**

I. Introduction

As a representative of the new generation of semiconductor materials, silicon carbide (SiC) exhibits a wider bandgap, superior thermal conductivity, and higher electron mobility compared to silicon (Si) [1], [2]. These performances have prompted the adoption of SiC in many power electronic devices as a replacement for Si, including SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) [3], [4]. Due to the wider bandgap of SiC MOSFETs, their breakdown electric field is ten times higher than that of Si MOSFETs to achieve a high breakdown voltage [5]. In addition, SiC MOSFETs can operate at extremely high temperatures while maintaining good stability in electrical parameters [6]. These characteristics have contributed to the widespread adoption of SiC MOSFETs in the design of high-voltage, high-frequency, and high-power-density power electronic applications [7].

Despite the evident performance benefits offered by SiC MOSFETs, their utilization is constrained by pronounced reliability challenges [8], [9], [10], [11]. The densities of interface and oxide defects in SiC MOSFETs are approximately two orders of magnitude greater than those observed in Si MOSFETs, leading to a variety of reliability concerns regarding gate oxide. Among these, the most common issue is the occurrence of threshold voltage drift under gate bias, commonly referred to as bias temperature instability (BTI). It is typically categorized into positive and negative BTI (PBTI and NBTI) based on the polarity of the gate bias [12], [13]. An increase in the threshold voltage under PBTI leads to elevated ON-state resistance, consequently causing higher power loss. Conversely, a decrease in the threshold voltage under NBTI can result in increased leakage current, potentially leading to unintended conduction [12], [13].

The use of SiC MOSFETs in power converters results in the gate bias of SiC MOSFETs not being polarity-invariant. Instead, it alternates based on signals generated by pulsewidth modulation (PWM). Under such alternating gate bias, the drift pattern of the threshold voltage exhibits complex behavior, referred to as gate switching instability (GSI) [14]. There is a growing interest in understanding and predicting the degradation under GSI [15], [16], [17]. However, due to the different physics of failure, models used for predicting the degradation under BTI may not be directly applicable to GSI [18].

Up to now, research on the accelerated degradation modeling of SiC MOSFETs under GSI is limited [14], [19], [20], [21]. Current models do not consider the impact of stresses such as temperature and gate bias on the degradation process of GSI. Consequently, the ability to predict the degradation of SiC MOSFETs in practical scenarios is limited when they are operated under particular temperatures and gate bias conditions.

This article conducted an examination of the dependency of GSI on stresses and established an accelerated degradation

Received 4 June 2024; revised 21 September 2024; accepted 27 October 2024. Date of publication 1 November 2024; date of current version 18 December 2024. Recommended for publication by Associate Editor K. Ngo. *(Corresponding author: Zicheng Wang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3490172.

Digital Object Identifier 10.1109/TPEL.2024.3490172

model for a commercial 1700 V planar-gate SiC MOSFET. Section II described the distinct characteristics of GSI as well as the physics of failure behind it. Section III introduced the equipment for all accelerated degradation tests (ADTs) and the testing procedures involved in this study. Section IV evaluated the dependency of GSI on various stresses, such as switching frequency, gate bias, temperature, switching time, and duty cycle, to identify the factors that have a significant impact and utilize them as accelerating stresses. Finally, an accelerated degradation model for SiC MOSFETs under GSI was established in Section V. This model incorporates acceleration factors related to temperature, negative bias voltage, and switching-ON time. The ability of the model to describe and predict degradation under particular stress conditions was also verified.

II. Characteristics and Mechanism

The primary distinction between GSI and BTI lies in the utilization of alternating gate bias on the gate, which is aligned with common application scenarios for SiC MOSFETs such as power converters. GSI presents unique phenomena and guidelines separate from BTI, thereby expanding the scope of reliability investigations concerning SiC gate oxides.

This section provides the characteristics and physics of failure of GSI to support dependency analysis in Section IV and to provide physics information for the development of the accelerated degradation model in Section V.

A. Characteristics of GSI

The unique characteristics of GSI are primarily manifested in the following aspects:

1) Without Counteracting Under Alternating Gate Bias: The most notable characteristic of GSI is that the threshold voltage drift does not counteract itself, even though the gate bias alternates between positive and negative. This contradicts the habitual thinking derived from BTI. The overwhelming majority of research findings suggest that GSI induces a positive drift in threshold voltage, demonstrating a significantly higher rate and extent compared to BTI [14], [21].

2) Dependency on Switching Events: GSI is considered a degradation process related to switching events, rather than duration-dependent like BTI [22]. In fact, some research teams use a simple power law model to summarize the drift of threshold voltage caused by GSI, as shown follows:

$$\Delta V_{\text{th}} = A \times (N_{\text{cycle}})^n \tag{1}$$

where ΔV_{th} represents the drift in the threshold voltage, N_{cycle} denotes the number of switching events, and A and n are fitting coefficients.

Nevertheless, this model does not function as an accelerated degradation model. While it effectively illustrates the dependency of GSI on switching events, it lacks consideration for additional acceleration factors of stresses such as temperature and gate bias voltage. Consequently, the model is not directly applicable for predicting degradation under particular temperatures and gate bias voltages. This limitation serves as a significant motivation for developing an accelerated degradation model in this research.

3) Permanent Degradation: The drift in threshold voltage under the influence of gate bias voltage can be categorized into two components: permanent and transient. In GSI, it is important to highlight that a significant portion of the threshold voltage drift is permanent. After the gate voltage is removed, this type of drift will not reverse unless the temperatures exceed the standard operating conditions significantly higher [22]. The following discussion will outline the differences between permanent and transient drift to prevent potential misconceptions.

The transient drift, also referred to as threshold voltage hysteresis [23]. In the context of GSI, the threshold voltage drifts during each cycle under positive and negative gate bias voltages. This behavior is attributed to the presence of defects in SiC MOSFETs located at the interface. These defects have the ability to capture or release charges (electrons or holes) depending on the polarity of the gate bias voltage. The accumulation of these transient charges results in the creation of an electric field denoted as E_{Local}. The electric field E_{Driven} induced by the gate bias voltage, combined with E_{Local}, influences the electric field within the channel, denoted as E_{Channel}, as shown follows:

$$E_{\text{Channel}} = E_{\text{Driven}} + E_{\text{Local}}. \tag{2}$$

The intensity of E_{Channel} plays a crucial role in the transition from accumulation to inversion within the channel, thereby influencing the threshold voltage. When a positive gate voltage is applied, electrons occupy interface defects, leading to a negative E_{Local}. A higher E_{Driven} is needed to achieve the same intensity of E_{Channel} leading to a positive drift in the threshold voltage. Conversely, a negative gate voltage causes interface defects to be filled with holes (or release electrons), creating a positive E_{Local} that requires a lower E_{Driven} to invert the channel, leading to a negative drift in the threshold voltage.

However, upon the removal of the gate bias voltage, a significant release of charges back into the channel occurs, leading to the recovery of both E_{Local} and E_{Channel}. Therefore, the threshold voltage hysteresis is not indicative of structural damage but rather a reversible phenomenon arising from the bias-induced capture and release of charges within defects [13], [24]. Some studies have shown that the threshold voltage hysteresis does not exhibit significant changes after GSI occurs, and its impact on reliability is weak [25], [26]. In other words, the threshold voltage hysteresis is a transient phenomenon rather than long-term structural degradation.

From the perspective of long-term reliability, the permanent drift in the threshold voltage is of more concern [27], [28]. Therefore, the purpose of the accelerated degradation model established in this study is to describe the permanent damage caused by GSI, rather than threshold voltage hysteresis. In the following sections, the main focus is primarily on the permanent drift of the threshold voltage under GSI.

B. Physics of Failure of GSI

Compared to BTI, there is no prolonged unipolar gate bias due to the continuous alternation of gate bias polarity in GSI.

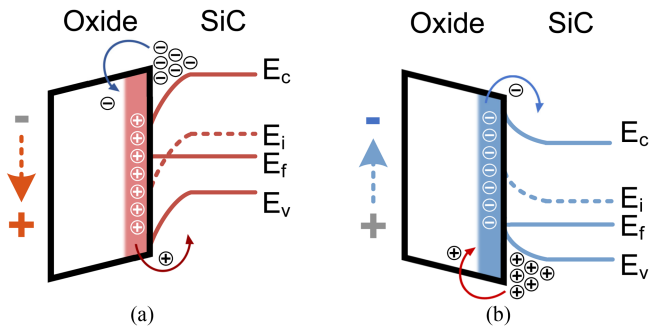

Fig. 1. During switching events, the charges trapped by the gate bias voltage from the previous half-cycle are unable to complete the capture and emission processes in time. This results in their polarity aligning with the gate bias voltage of the current half-cycle, which reinforces the electric field within the channel. (a) The moment of switching-ON. (b) The moment of switching-OFF.

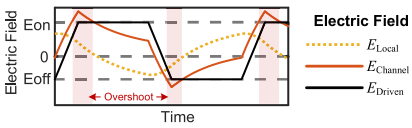

Fig. 2. Due to E_{Local} and E_{Driven} maintain the same polarity during switching events, overshoots occur in $E_{Channel}$.

This suggests that the permanent drift in threshold voltage is not caused by sustained gate bias voltage. While numerous explanations exist for BTI, the unique phenomena of GSI preclude a direct application of the physics of failure of BTI. This section presented two potentially conflicting models that can explain the unique phenomenon of GSI, based on enhanced local electric field [20], [29] and recombination-enhanced defect reactions (REDRs) [15], [30], respectively.

From the perspective of the enhanced local electric field, the polarity of the gate bias switches rapidly, typically within 300 ns. However, the capture and emission of charges from traps back to the channel occurs at a much slower rate, lagging behind the polarity switching of gate bias. This results in the charge in traps induced by the bias voltage of the previous half cycle not being emitted back to the channel in time, as shown in Fig. 1. At this time, E_{Local} is of the same polarity as E_{Driven}, leading to overshoots of $E_{Channel}$ during each switching event, as shown in Fig. 2. Overshoots of $E_{Channel}$ cause additional charges to be captured by traps with initially higher activation energy. Due to their higher emission activation energy, these additional captured charges are difficult to emit back into the channel, resulting in a permanent drift in the threshold voltage.

Therefore, GSI is always induced by switching events, instead of being counteracted by the gate bias that alternates between positive and negative polarities.

Another perspective of the REDRs expands on this premise. Due to the same reason, when the polarity of the gate bias voltage switches rapidly, it becomes difficult to promptly release a significant amount of trapped charges back to the channel. At this time, the newly arrived gate bias voltage induces new charges to enter the defects, leading to a recombination of electrons and holes, as shown in Fig. 1. The energy released from the recombination excites local vibration modes of the defects, activating additional acceptor-like interface defects. These defects, which are difficult to recover, exhibit negative charge states by capturing electrons during threshold voltage extraction, resulting in a permanent positive drift of the threshold voltage.

In the vast majority of cases, overshoots of $E_{Channel}$ are more likely to occur at the rising edge, resulting in an increase in threshold voltage rather than a decrease. This is because, at the falling edge, the emission time constant of electrons in traps is smaller than that of holes, enabling them to emit to the channel with the switching of the gate bias voltage. This leads to smaller E_{Local} and negative overshoots. Furthermore, since the positive bias voltage is often greater than the negative one in practice, the $E_{Channel}$ during the positive half cycle is relatively higher, amplifying the effect of overshoots.

The two theories present contradictory perspectives on the nature of damage. Both the additional charges resulting from the enhanced local electric field and the acceptor-type interface states induced by REDRs can contribute to a drift in the threshold voltage. Each theory has the potential to clarify the underlying physics of failure. Currently, the results of some photon emission and capacitance testing point toward the REDRs theory appearing more convincing [15], [23], [31]. Nevertheless, the predominant mechanism behind the GSI in SiC MOSFETs with different gate types and voltage levels remains intricate and uncertain [20], necessitating further investigation. The forthcoming analysis will rely on the currently agreed-upon principles to elucidate the observed phenomena.

TABLE I
SPECIFICATION OF DUTS

Type	WM1A045170L
Maximum positive gate voltage, V_{Gmax}	20 V
Maximum negative gate voltage, V_{Gmin}	–10 V
Standard threshold voltage value, V_{TH0}	2.6 V
Reference current of the threshold voltage, I_{REF}	18 mA

III. TEST SETUP

A commercial 1700 V planar-gate SiC MOSFET with a typical threshold voltage of 2.6 V, ON-state resistance of 45 mΩ and housed in a TO-247-4 package was chosen as the device under test (DUT), as shown in Table I. To meet the demand for accurate and precise measurements for a large number of DUTs and to facilitate the adjustment of stress levels, stress loading equipment, measurement equipment, and measurement sequences have been developed.

A. Stress Loading Equipment

The experimental setup for inducing GSI in DUTs consists of two components: electrical and temperature loading equipment, as shown in Fig. 3.

1) Electrical Loading Equipment: The electrical loading equipment is designed to provide a variable gate bias voltage for DUTs to induce GSI, as shown in Fig. 4. It includes dc–dc

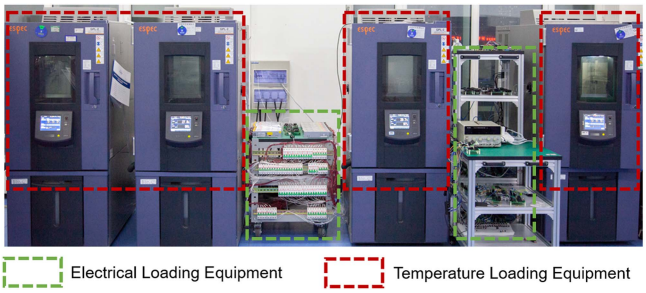

Fig. 3. Stress loading equipment.

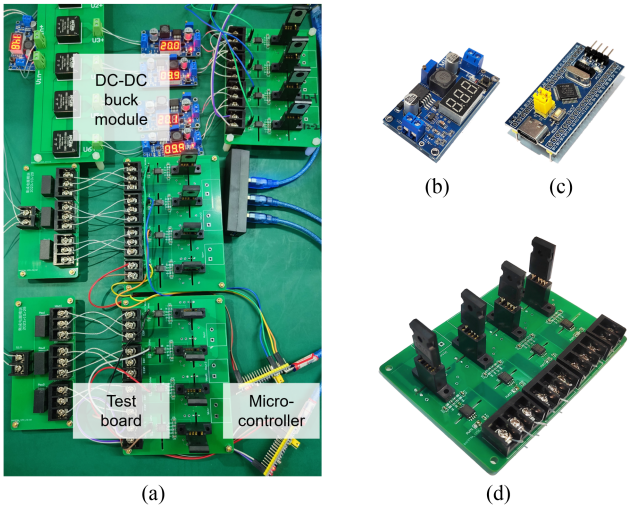

Fig. 4. Electrical loading equipment. (a) Total equipment. (b) DC–DC buck module. (c) Microcontroller. (d) Test board.

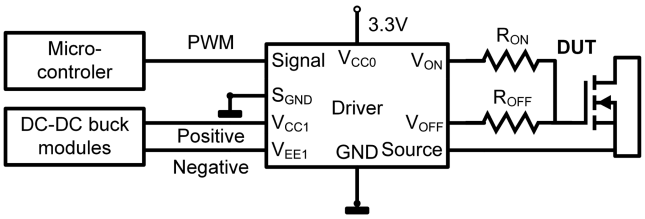

Fig. 5. Circuit of testing boards for each DUT.

buck modules, microcontrollers, and testing boards. The driver chip used on the test board is the 1ED3121MU12H.

Various factors affecting GSI can be adjusted, including gate bias voltages, switching frequency, switching times, and duty cycle. The dc–dc buck modules provide both positive and negative voltage inputs to the drivers, enabling gate bias voltage adjustments from −10 to 30 V. The switching frequency and duty cycle can be adjusted by programming the microcontroller. Furthermore, by modifying the drive resistors R_{ON} and R_{OFF} on test boards shown in Fig. 5, it is available to control the switching-ON and switching-OFF times of the DUTs, which can range from 100 to 200 ns.

2) Temperature Loading Equipment: To maintain a consistent and suitable long-term temperature for GSI, and to separate

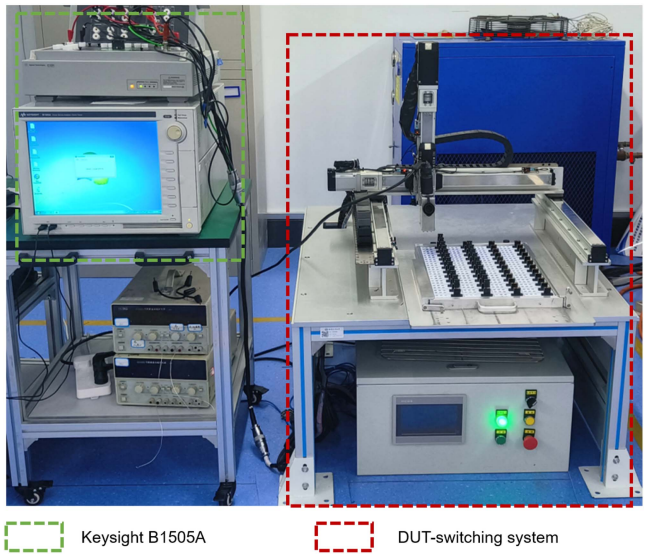

Fig. 6. Measurement equipment.

the dependency of temperature on GSI from other variables while protecting the gate oxide layer from external factors, the decision was made to employ passive heating instead of self-heating. The drain and source of DUTs are connected in a short-circuited configuration because previous studies indicate that the degradation of gate oxide due to load current is insignificant [32]. The DUTs housed on testing boards rely on constant temperature chambers capable of maintaining temperatures within the range of 25–120 °C. This temperature range aligns with the typical operational temperature spectrum for SiC MOSFETs.

B. Measurement Equipment

The primary equipment used to periodically extract the threshold voltage of the DUTs under GSI after prolonged stress is the Keysight B1505A. Furthermore, to effectively measure a large quantity of DUTs effectively, a DUT-switching system has been developed, which is controlled by a programmable logic controller. This system can extract the threshold voltage of 48 DUTs within 15 min, with a maximum error in repeated measurements of 2%, as shown in Fig. 6.

C. Measurement Sequence

From the perspective of long-term reliability, the accelerated degradation model established in this study aims to describe the permanent degradation caused by GSI. To eliminate the threshold voltage hysteresis, a novel measuring sequence was applied, which can be divided into four stages, as shown in Fig. 7.

1) Stress Stage: Attach stress as needed in ADTs. After the stress is removed, there is a noticeable hysteresis in the threshold voltage caused by the emission of charges from traps, which must be eliminated in the next stage.

2) Cooling Stage: Ensure the complete discharge of charges over a 4-h period to effectively eliminate the threshold voltage hysteresis. During this stage, the cooling period of up to 4 h

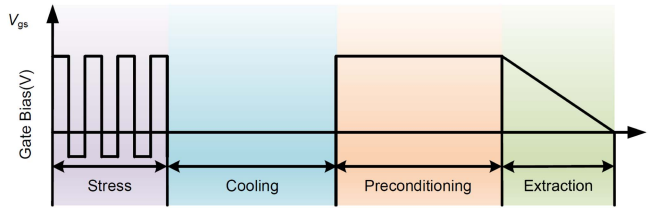

Fig. 7. Measurement sequence.

allows the temperature to stabilize at room temperature and provides ample time for the charges in traps to emit back into the channel.

3) Preconditioning Stage: Implement a 20 V positive gate bias for 30 s to perform a preconditioning procedure. This step ensures a uniform charge-filled state in all DUTs before extracting the threshold voltage [33].

4) Extract Stage: Perform the threshold voltage measurement in 10 s after the preconditioning stage using the Keysight B1505A.

This measurement sequence ensures the standardization of the charge-filled state in traps across all DUTs, eliminates the threshold voltage hysteresis to minimize residual effects following the stress stage, particularly the hysteresis associated with different stresses, and establishes a consistent baseline for all DUTs.

IV. Acceleration Factors and Degradation Dependency Analysis

Previous research has presented different conclusions on the relationship dependency of GSI on stresses [14], [19], [20], [21], [22], [34], [35], [36]. These discrepancies do not necessarily imply conflicting viewpoints or inaccurate findings because different conclusions may arise from variations in testing methodologies, gate types, and voltage levels of SiC MOSFETs. However, limited research exists on the dependency of GSI on stresses in 1700 V planar-gate SiC MOSFETs.

Therefore, to avoid over-complicating the degradation model with excessive stresses, the dependency of GSI on stresses was evaluated through ADTs. These stresses include switching frequency, gate bias voltage, temperature, switching-ON time, switching-OFF time, and duty cycle. The study also assessed the range within which the dependency remains accurate to identify potential scenarios suitable for the application of the accelerated degradation model. In addition, mechanistic insights were provided to assist in determining the structures of stress acceleration factors and to guide the development of accelerated degradation models in Section V.

Controlling for variables was used to facilitate a single-factor analysis. The standard stress conditions include a switching frequency of 50 kHz, a temperature of 75 °C, a duty cycle of 50%, a positive gate bias of 20 V, a negative gate bias of −5 V, and switching-ON and switching-OFF times of 100 ns each. When examining the dependence of GSI on a specific stress, only that stress is altered, while other stresses are maintained at a constant level as mentioned above or are minimally influenced.

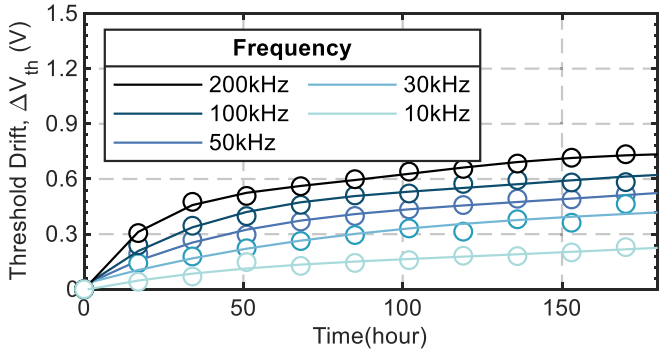

Fig. 8. Degradation trajectories of DUTs at different frequencies.

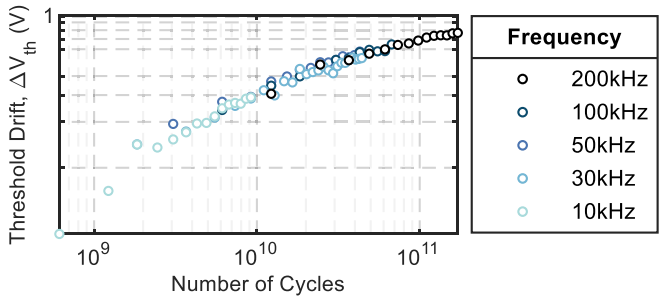

Fig. 9. Degradation trajectories of DUTs at different frequencies (measured in numbers of cycles).

In each set of ADT, three DUTs are allocated for each stress level, and their average degradation is documented daily to ensure that the conclusions drawn are not coincidental. It is reasonable to conduct data collection once a day, as frequent extraction of threshold voltage for a large number of DUTs can be time-consuming.

A. Dependency on Switching Frequency

It has been shown in (1) that the dependency of GSI on switching frequency has been transformed into the dependency on switching events, but this conclusion is provisional. Some teams have pointed out that when the switching frequency is either too high or too low, the parameter "*n*" of the power-law model in (1) will change [34], [36]. The accelerated degradation model established in this study is expected to be applicable within the switching frequency range of 10–200 kHz, which is common in applications. Therefore, to develop a coefficient-stable accelerated degradation model based on the power law model in (1), it is essential to investigate whether the parameter "n" remains stable within the switching frequency range of 10–200 kHz.

All DUTs were divided into five groups at various switching frequencies: 10 kHz, 30 kHz, 50 kHz, 100 kHz, and 200 kHz.

At first glance, GSI appears to increase significantly with a rising switching frequency, indicating a strong dependency, as shown in Fig. 8. However, a different conclusion in Fig. 9 emerges when calculating the number of cycles of switching events at various frequencies and using it as the horizontal axis.

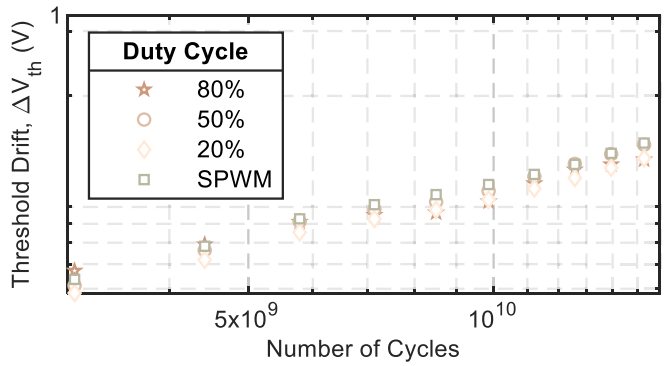

Fig. 10. Degradation trajectories of DUTs at different duty cycle.

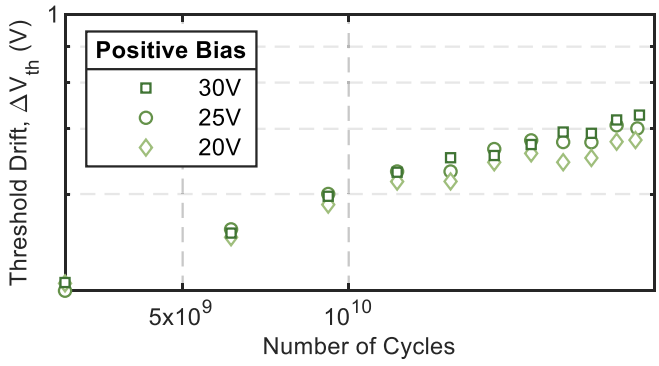

Fig. 11. Degradation trajectories of DUTs under different positive gate biases.

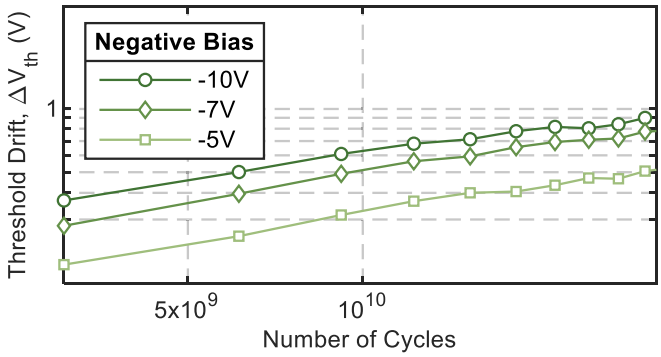

Fig. 12. Degradation trajectories of DUTs under different negative gate biases.

The number of switching events can be quickly calculated by multiplying time by the switching frequency as follows:

$$N_{\text{cycle}} = t \times f \tag{3}$$

where N_{cycle} is the number of switching events, t is the duration of degradation, and f is the switching frequency.

It is evident that when the number of cycles of switching events (logarithmic scale) is used as the horizontal axis, GSI exhibits a broadly consistent trend across different frequency ranges from 10 to 200 kHz. This implies that as long as the same number of switching events is reached, varying the switching frequency does not significantly affect the outcome. This finding aligns with the critical significance of switching events themselves in GSI [22], as mentioned in Section II. Unless specified otherwise, all results in this section will use the number of switching events as the horizontal axis for analysis.

The results above suggest that the fundamental power law model described in (1) is valid for the 1700 V planar-gate SiC MOSFETs used in this study when the switching frequency falls between 10 and 200 kHz. Even in the early stages of degradation, a few data points may exhibit different characteristics. However, from the perspective of long-term reliability, this does not affect the description of degradation using (1) [22].

B. Dependency on Duty Cycle

The ADT was designed to explore the dependency of GSI on duty cycle. The duty cycles in four test groups were set at 20%, 50%, 80%, and a duty cycle with sinusoidal pulsewidth modulation (SPWM) determined by a fundamental frequency of 330 Hz and a modulation index of 0.8. These settings encompass the most common configurations found in dc–dc converters and inverters.

Different from previous records, the analysis of the dependency of the duty cycle generated by SPWM is published for the first time. This corresponds to the operating state of SiC MOSFETs in inverters. It is expected that the accelerated degradation model established in Section V can also be applied to inverters.

It is observed that GSI does not exhibit significant differences across various duty cycles, as shown in Fig. 10. Despite the fact that 20% and 80% duty cycles are complete inverses, and the duty cycle in the SPWM test group is constantly changing, all test results showed no significant variation. These findings serve to complement the earlier research outcomes [14], [22].

Altering the duty cycle does not change the number of switches or the waveform within a single period. Therefore, it does not have a significant impact on GSI. This proves that GSI is essentially independent on the duty cycle, further affirming the close relationship between GSI and the switching events themselves, rather than the duration of the gate bias.

C. Dependency on Gate Bias

DUTs in different test groups were exposed to various levels of gate bias. Notably, all gate biases remained within the maximum gate voltage limit of DUTs which ranged from −10 to 30 V. This was done to prevent direct breakdown caused by excessive voltage or the initiation of new mechanisms. It also aimed to align the stress conditions more closely with typical applications. Small changes in the switching-ON and switching-OFF times may occur when adjusting the gate bias voltage, but they are not significant and will not affect the single-factor analysis in the dependency analysis of this study.

With the negative gate bias consistently set at −5 V, three groups were set up with positive gate biases of 20, 25, and 30 V in ADT, resulting in the degradation illustrated in Fig. 11. Similarly, while keeping the positive gate bias constant at 20 V, three groups were set up with negative gate biases of −5, −7, and −10 V, respectively. The degradation results corresponding to Fig. 12 were obtained.

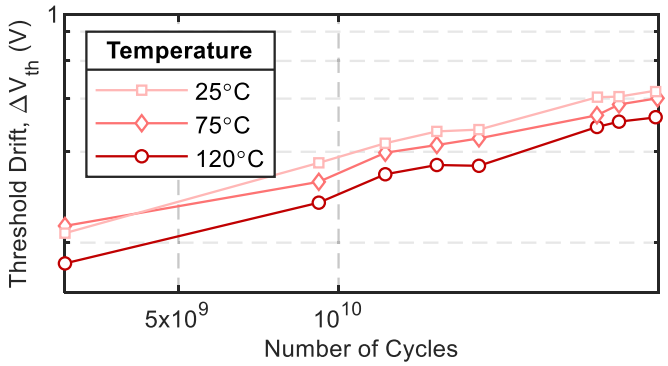

Fig. 13. Degradation trajectories of DUTs at different temperature.

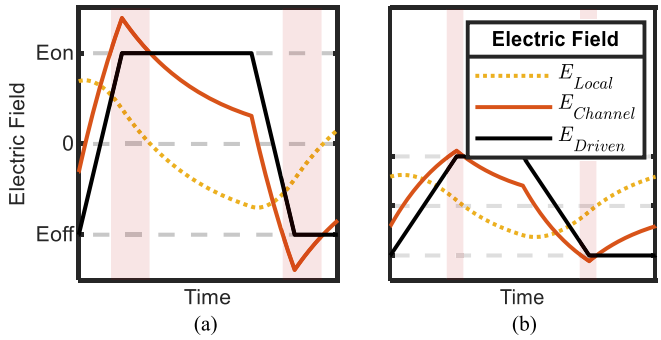

Fig. 14. When the temperature rises, the time constants for trap capture or release of charges decrease, significantly reducing the overshoot in the electric field of channel. (a) Lower temperature. (b) Higher temperature.

The results indicate that for 1700 V planar-gate SiC MOSFETs, negative gate bias has a more significant impact on GSI than positive gate bias. According to the theory presented in Section II, this occurs because a heightened negative bias fills a greater number of holes in the defects before the rising edge, thereby amplifying the enhanced local electric field or REDRs. Conversely, a similar process driven by positive voltage does not significantly affect GSI, as electrons in traps quickly re-emit back into the channel, as discussed in Section II. Therefore, the model in this study will account for the accelerating effect of negative gate bias, and neglect the impact of positive gate bias.

From the perspective of failure mechanisms, the electric field E_{Driven} that drives the capture or release of charges is generated by the negative gate bias V_{N} through the following:

$$E_{\text{Driven}} = \frac{V_{\text{N}}}{t_{\text{OX}}} \tag{4}$$

where t_{OX} is the thickness of the gate oxide layer.

Based on this understanding, first-order kinetics have been used to explain charge capture and simple bond-breaking reactions [37]. The acceleration factor of GSI due to the negative gate bias voltage can be expressed by the following:

$$\Delta V_{\text{th}} \propto V_{\text{N}}^{\beta} (N_{\text{cycle}})^{n} \tag{5}$$

where β is the coefficient that need to be fitted.

D. Dependency on Temperature

To explore the dependency of GSI on temperature, three temperatures (25 °C, 75 °C, and 120 °C) were set for ADTs.

The results shown in Fig. 13 indicate that higher temperatures resulted in less degradation, which is counter-intuitive. This phenomenon can be attributed to the accelerated charge capture and release processes at elevated temperatures. As mentioned in Section II, both the capture and release of charges take time that follows a specific time constant [38], which is inversely related to temperature by the following:

$$\tau_2 = \tau_0 \cdot \left(\frac{\tau_1}{\tau_0}\right)^{\frac{T_1}{T_2}} \tag{6}$$

where τ_0 denotes the capture/emission time constant for infinite temperature, τ_1 and τ_2 represent the capture/emission time constants at temperatures T_1 and T_2, respectively.

According to (6), higher temperatures lead to smaller time constants, accelerating the capture, and release of charges. The duration during which E_{Local} maintains the same polarity as E_{Driven} is significantly reduced, thereby decreasing the overshoot or REDRs, as shown in Fig. 14.

The actual patterns of capture and release are far more complex. For the purpose of analysis, a simplified expression has been used in (6). In reality, the time constants for the capture and release of charges in interface traps are significantly smaller than those in oxide layer traps. Moreover, the capture and release behavior of traps is a collective action involving a large number of charges, exhibiting distinct distribution characteristics [24].

The temperature dependency of the underlying processes of charge tunneling and bond rupture can be well described by the Arrhenius law, proven to have good accuracy and correspondence to physical processes [37]. Reflected in the key parameter of activation energy E_a in (7). Based on the above results, E_a will be negative, which is significantly different from BTI.

$$\Delta V_{\text{th}} \propto \exp\left(-\frac{E_{\text{a}}}{k(T+273)}\right)(N_{\text{cycle}})^{n} \tag{7}$$

where k is the Boltzmann constant (k = 8.62905625*10^{-5} eV/K), and T is the junction temperature.

E. Dependency on the Switching-ON Time and Switching-OFF Time

In practical applications, the switching-ON and switching-OFF times of SiC MOSFETs can be flexibly adjusted by drive resistors. Therefore, exploring the dependency of GSI on the switching-ON and switching-OFF times is also of practical significance. In this study, the drivers on test boards provide separate pins for positive gate bias voltage and negative gate bias voltage for SiC MOSFETs. By adjusting the drive resistor, either the switching-ON time or switching-OFF time can be changed independently without any interference.

While keeping the switching-OFF time constant at 100 ns, switching-ON times of 100, 150, and 200 ns were set in different

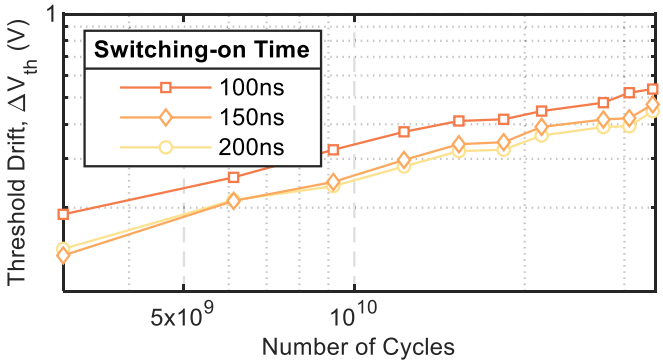

Fig. 15. Degradation trajectories of DUTs at different switching-ON time.

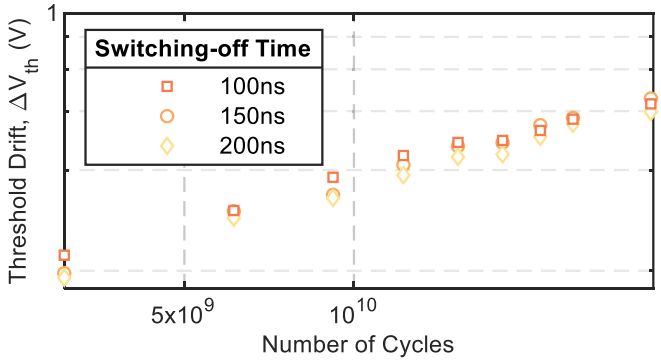

Fig. 16. Degradation trajectories of DUTs at different switching-OFF time.

test groups. Similarly, with a constant switching-ON time of 100 ns, switching-OFF times of 100, 150, and 200 ns were set in separate ADTs. The results are illustrated in Figs. 15 and 16, respectively. The proximity of the two curves in Fig. 15 may be attributed to minor variations in the sensitivity of distinct DUTs to GSI. When analyzing the combined outcomes of all three curves, it is clear that this proximity is unlikely to significantly affect the ability to draw overarching conclusions.

It is evident that longer switching-ON and switching-OFF times result in less degradation. The fundamental physical mechanisms and the influence of temperature on GSI exhibit similarities. This time, the capture and emission time constants of charges remain unchanged. The reduced switching speed provides an extended period for more sufficient charge emission processes. This indicates that prior to the degradation process, a portion of the holes or electrons that would have contributed to degradation are instead emitted back into the channel. E_{Local} has more time to synchronize with E_{Driven}, leading to a reduction in overshoots of E_{Channel}, as shown in Fig. 17. Also, a more sufficient release of charges leads to fewer hole-electron recombinations, thereby weakening REDRs.

In addition, certain studies suggest that the switching-ON time and switching-OFF time have different effects on GSI due to different gate-types and structures [15], [19]. For the 1700 V planar-gate SiC MOSFETs used in this study, the dependency of GSI on switching-ON time is evidently greater than that on switching-OFF time, which is different from the conclusions

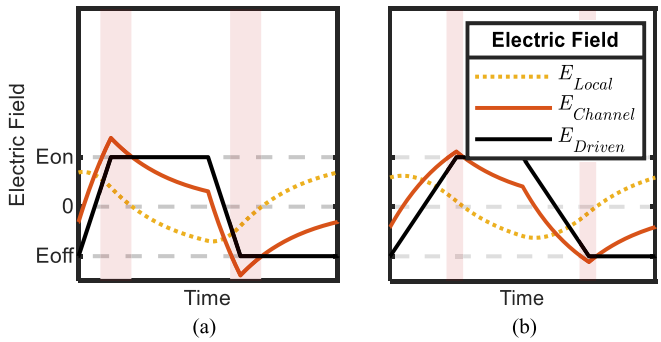

Fig. 17. As the switching-ON and switching-OFF time increase, the charges in the traps have more time to be captured or released, effectively reducing the overshoot in the electric field of channel. (a) Shorter switching-ON and switching-OFF time. (b) Longer switching-ON and switching-OFF time.

drawn for 1200 V planar-gate SiC MOSFETs in [20]. Hence, the model considered the accelerating effect of the switching-ON time, while disregarding the impact of the switching-OFF Time.

According to the physics of failure of GSI, the degradation originates from switching events. Hence, the stress duration is determined by the switching time, not the gate bias duration. The dependency on duration for bond-breaking reactions is commonly quantified using a power law formulation, as represented follows:

$$\Delta V_{\text{th}} \propto t_{\text{on}}^{r}(N_{\text{cycle}})^{n} \tag{8}$$

where r is the coefficient that need to be fitted, and t_{on} is the switching-ON time.

In summary, before proceeding to modeling, a thorough discussion on the dependency of GSI on various stresses has been conducted. For 1700 V planar-gate SiC MOSFETs, temperature, negative gate bias, and switching-ON time had the most significant impact on GSI. Conversely, factors such as switching frequency and duty cycle did not show a significant influence on GSI. Furthermore, a stress range that is capable of applying the accelerated degradation model has been identified. This enables us to determine the specific scenarios in which the accelerated degradation model is suitable for application.

V. Accelerated Degradation Modeling and Validation

A. Model Establishment

Some reports have established simple power-law models, such as (1). However, this model is obviously inadequate because all acceleration factors in (1) are implied in the parameter "A" and common stresses such as temperature and voltage, which accelerate the degradation of GSI, are not described. Hence, existing models are unable to predict the degradation of SiC MOSFETs under particular stress conditions.

Based on the results of the dependency of GSI on stresses, to describe and predict the permanent drift of the threshold voltage of SiC MOSFETs under long-term GSI, an accelerated degradation model in (9) was developed based on the form of the acceleration factor shown in Fig. 18. The accelerated degradation model is expected to be applied to SiC MOSFETs in

TABLE II
SETTING OF STRESSES

Test groups	Junction Temperature, T(°C)	Negative gate bias, V_N(V)	Switching-ON time,t_{on}(ns)	Other stresses
a (Fitting)	25	-5	100	
b (Fitting)	25	-5	150	
c (Fitting)	25	-5	200	Duty cycle = SPWM
d (Fitting)	75	-5	100	Switching frequency = 30kHz
e (Fitting)	120	-5	100	Positive gate bias = 20V
f (Fitting)	25	-8	100	switching-off time = 100ns
g (Fitting)	25	-10	100	
h (Validation)	105	-6	125	

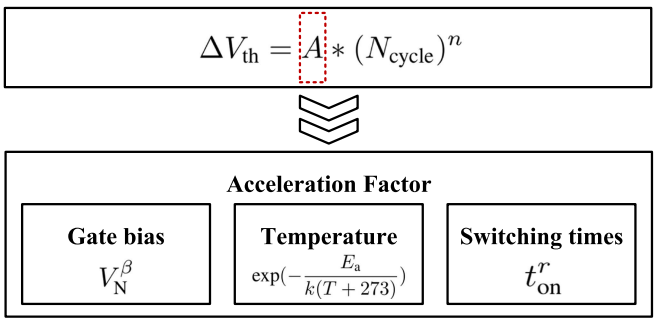

Fig. 18. Acceleration factor of gate bias, temperature, and switching times on GSI.

TABLE III
FITTING RESULTS

Number	Parameters	Value
1	A	$A \sim \mathcal{N}(2.702 * 10^{-5}, (2.106 * 10^{-6})^2)$
2	β	0.6853
3	E_a	-0.02695
4	r	-0.2861
5	n	0.3658

dc–dcconverters (under PWM) or inverters (under SPWM) with switching frequencies ranging from 10 to 200 kHz, positive gate bias voltage ranging from 20 to 30 V, negative gate bias voltage ranging from −10 to −5 V, and switching-ON and switching-OFF times ranging from 100 to 200 ns

$$\Delta V_{th} = A V_N^{\beta} \exp\left(-\frac{E_a}{k(T+273)}\right) t_{on}^{r} (N_{cycle})^n. \quad (9)$$

B. Accelerated Degradation Tests

ADTs were conducted under multiple stress dimensions to gather the data required for modeling. Seven combinations of stress levels were established. Following the analysis of the dependency of GSI on various stresses in Section IV, the three most sensitive stresses were selected: junction temperature T, negative gate bias V_N, and switching-ON time t_{on}. The combination of these three stresses is presented in Table II. Other stresses that have a minor impact on GSI, as mentioned in Section IV, were kept constant: duty cycle generated by SPWM with a fundamental frequency of 330 Hz, a switching frequency of 30 kHz, and a modulation index of 0.8. The positive gate bias is set at 20 V, and the switching-OFF time is configured to 100 ns. The threshold voltage of DUTs was collected once a day.

Even when subjected to identical stress, different DUTs of the same type can exhibit varying degradation trends. These discrepancies in degradation trends necessitate the incorporation of coefficients with distribution characteristics within the accelerated degradation model. Furthermore, it is essential to arrange as many DUTs as possible within the same set of stresses to improve the accuracy of the model. Under each combination, 10 DUTs were set up, totaling 70 DUTs. The results of ADTs are shown in Fig. 19.

C. Fitting

Fitting is performed on all degraded data according to the specified model form in (9). The fitted parameters are recorded in Table III. To account for the introduced errors, the parameter A in the accelerated degradation model follows a normal distribution.

As demonstrated by both the results of the initial degradation data from 70 DUTs and the accelerated degradation model shown in Fig. 19, the accelerated degradation model effectively captures the degradation patterns across different stress levels. Furthermore, the dotted line represents the boundary set by the 90% confidence interval, covering most of the degradation data points. This suggests that the distribution properties inherent in the accelerated degradation model's A factor can effectively address discrepancies in the degradation data.

To quantitatively evaluate the ability of the newly fitted accelerated degradation model to describe the degradation behavior of SiC MOSFET under GSI, two commonly used statistical indicators for assessing the goodness of fit were calculated: the coefficient of determination R^2 and the mean relative error (MRE). The coefficient of determination R^2 was calculated to be 0.9971, and the MRE was 5.60%, indicating that the model's ability to describe the degradation is significant.

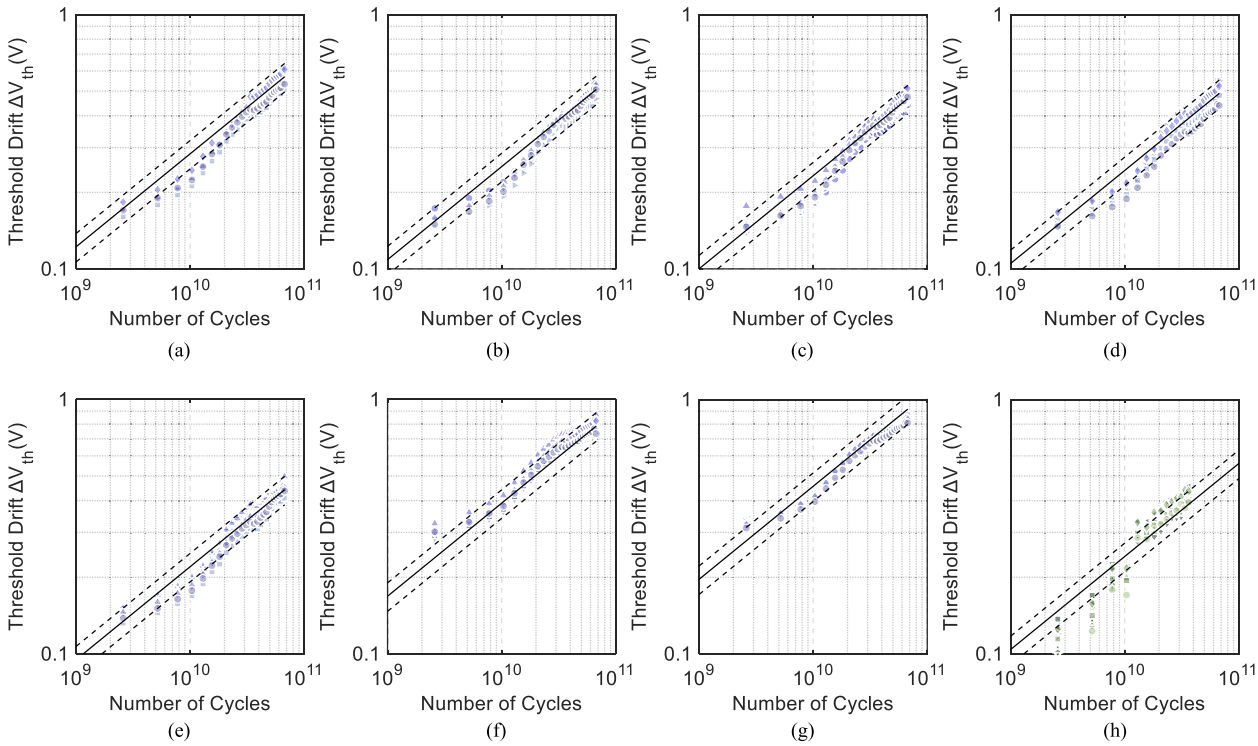

Fig. 19. Degradation trend of DUTs. The solid line represents the established accelerated degradation model, while the dashed line represents the envelope formed by the 90% confidence interval. Distinct shapes of the symbols represent the degradation trajectories of different DUTs subjected to identical stress conditions. (a)–(g) Degradation data used for fitting, (h) Degradation data used for validation.

D. Validation

To validate the predictive capability of the newly developed accelerated degradation model, an additional ADT was designed, with specific stress levels detailed in Table II, which differed from those used in the ADTs during the modeling process. This ADT involved a total of 20 DUTs.

By inputting the stress levels of this ADT into (9), the model generated the degradation trajectory. This trajectory, along with the actual degradation trajectory, was plotted in Fig. 19(h).

The results show that the model accurately predicted the degradation trend of the DUTs. To quantitatively assess the model's ability to describe and predict degradation, two commonly used goodness-of-fit indicators are introduced: the coefficient of determination R^2 in (10) and the MRE in (11).

$$R^2 = 1 - \frac{\sum_{i=1}^{n}(y_i - \widehat{y}_i)^2}{\sum_{i=1}^{n}(y_i - \overline{y}_i)^2} \tag{10}$$

$$\text{MRE} = \frac{1}{n}\sum_{i=1}^{n}\left|\frac{y_i - \widehat{y}_i}{y_i}\right| \tag{11}$$

where n represents the number of DUTs, y_i represents the degradation of a specific sample, $\widehat{y}_i$ represents the degradation predicted by the model, and $\overline{y}_i$ represents the average degradation of the samples.

Generally, a larger R^2 and a smaller MRE indicate higher accuracy of the model. Within a 90% confidence interval, the model accounted for errors. The coefficient of determination R^2 of the model is 0.9957, and the MRE between the model prediction and the actual degradation was only 11.40%, confirming that the accelerated degradation model developed in this article effectively predicts the degradation trends of SiC MOSFETs under prolonged GSI within a certain confidence interval. It is noted that the model's errors are mainly concentrated on the early degraded data. As reported in other studies [22], early locally degraded data may exhibit deviations from the overall degradation trend. Nevertheless, for the purpose of long-term reliability assessment, it is crucial to prioritize aligning the model with the extended-term degradation data. The minor errors caused by early degraded data will not impact the utilization of accelerated degradation models for long-term degradation prediction tasks. Moreover, after defining the failure threshold for ΔV_{th} in DUTs, this model can also be directly converted into a lifetime prediction model. In other words, by solving (9) in reverse, the lifetime of DUTs can be determined.

The accelerated degradation model presented in this study focused on the influence of physical factors on GSI. The accelerating impact of temperature, voltage, and other stresses on GSI were quantified, aiding in the prediction of degradation. The proposed model structure is expected to be applicable to 1700 V planar-gate SiC MOSFETs, as there is limited evidence regarding the different degradation patterns among different series of 1700 V planar-gate SiC MOSFETs under GSI. However, the degradation patterns of SiC MOSFETs with different gate types and voltage levels may differ, indicating that the fundamental structure of the model may require modification. Nevertheless,

the dependency analysis, modeling, and verification processes, along with the framework presented in this article, can still be effectively utilized to derive the basic form of the model.

Furthermore, real-world stress conditions are often complex, requiring the consideration of multiple influencing variables and the application of cumulative damage theory to address evolving environmental stresses. Further advancements are required to enhance this study, with the hope that it can provide guidance for future research endeavors.

VI. Conclusion

This article investigated the dependency of GSI on stresses, leading to the development of an accelerated degradation model for a 1700 V planar-gate SiC MOSFET. This model demonstrated its ability to accurately predict threshold voltage drift under GSI.

GSI exhibits distinctive properties compared to BTI, most notably its close correlation with switching events, often leading to more permanent damage. Two potentially physical explanations (Enhanced local electric field and REDRs) are provided, offering a theoretical foundation for the entire study.

A stress-loading equipment capable of providing long-term, stable stress was established, along with measurement equipment for efficiently and swiftly extracting the threshold voltage of a large number of DUTs. Through meticulous design of the measurement sequence, the permanent component of the threshold voltage drift was successfully extracted.

The dependency of GSI on various stresses has been evaluated before modeling, including switching frequency, gate bias, temperature, switching-ON and switching-OFF times, and duty cycle. The dependency on switching time exhibited a different behavior compared to that in previous studies. In addition, GSI was firstly proven to remain unaffected by the duty cycle produced during SPWM. Several ADTs identified negative gate bias, temperature, and switching-ON time as the stresses sensitive to degradation in the subject of this research and evaluated the range of stresses that exhibit this dependency. These analyses avoid including an excessive number of variables to prevent the degradation model from becoming overly complex.

An accelerated degradation model for SiC MOSFETs under GSI has been established using multiple ADTs. The model demonstrates good predictive capability within a 90% confidence interval. An additional set of ADTs validated the model's predictive accuracy and its resilience to errors. It quantified the accelerating impact of temperature, gate bias, and other stresses on GSI, which contributed to a deeper understanding and the development of models for SiC MOSFETs under GSI to describe and predict degradation.

References

[1] J. Cooper, M. Melloch, R. Singh, A. Agarwal, and J. Palmour, "Status and prospects for SiC power MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 658–664, Apr. 2002.

[2] J. A. Cooper and A. Agarwal, "SiC power-switching devices-the second electronics revolution?," *Proc. IEEE*, vol. 90, no. 6, pp. 956–968, Jun. 2002.

[3] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[4] J. Fabre, P. Ladoux, and M. Piton, "Characterization and implementation of dual-SiC MOSFET modules for future use in traction converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4079–4090, Aug. 2015.

[5] D. Ball et al., "Effects of breakdown voltage on single-event burnout tolerance of high-voltage SiC power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 7, pp. 1430–1435, Jul. 2021.

[6] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[7] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014.

[8] J. Wei, S. Liu, J. Tong, X. Zhang, W. Sun, and A. Q. Huang, "Understanding short-circuit failure mechanism of double-trench SiC power MOSFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5593–5599, Dec. 2020.

[9] J. Hu, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. A. Mawby, "The effect of electrothermal nonuniformities on parallel connected SiC power devices under unclamped and clamped inductive switching," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4526–4535, Jun. 2015.

[10] Z. Chbili et al., "Modeling early breakdown failures of gate oxide in SiC power MOSFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3605–3613, Sep. 2016.

[11] J. Lutz and J. Franke, "Reliability and reliability investigation of wide-bandgap power devices," *Microelectron. Reliab.*, vol. 88, pp. 550–556, 2018.

[12] T. Aichinger, G. Rescher, and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectron. Reliab.*, vol. 80, pp. 68–78, 2018.

[13] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015.

[14] X. Zhong et al., "Bias temperature instability of silicon carbide power MOSFET under AC gate stresses," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1998–2008, Feb. 2022.

[15] M. W. Feil et al., "Towards understanding the physics of gate switching instability in silicon carbide MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*. IEEE, 2023, pp. 1–10.

[16] A. Ghosh et al., "Studies of bias temperature instabilities in 4H-SiC DMOSFETs," pp. 1–4, 2020.

[17] M. W. Feil et al., "Gate switching instability in silicon carbide MOSFETs—part I: Experimental," *IEEE Trans. Electron Devices*, vol. 71, no. 7, pp. 4210–4217, Jul. 2024.

[18] R. Green, A. Lelis, and D. Habersat, "Threshold-voltage bias-temperature instability in commercially-available SiC MOSFETs," *Jpn. J. Appl. Phys.*, vol. 55, no. 4S, 2016, Art. no. 04EA03.

[19] H. Jiang, X. Zhong, G. Qiu, L. Tang, X. Qi, and L. Ran, "Dynamic gate stress induced threshold voltage drift of silicon carbide MOSFET," *IEEE Electron Device Lett.*, vol. 41, no. 9, pp. 1284–1287, Sep. 2020.

[20] H. Jiang et al., "A physical explanation of threshold voltage drift of SiC MOSFET induced by gate switching," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 8830–8834, Aug. 2022.

[21] X. Zhong, H. Jiang, L. Tang, X. Qi, P. Jiang, and L. Ran, "Gate stress polarity dependence of AC bias temperature instability in silicon carbide MOSFETs," *IEEE Trans. Electron Devices*, vol. 69, no. 6, pp. 3328–3333, Jun. 2022.

[22] D. B. Habersat and A. J. Lelis, "AC-stress degradation and its anneal in SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 69, no. 9, pp. 5068–5073, Sep. 2022.

[23] Y. Cai et al., "Effect of threshold voltage hysteresis on switching characteristics of silicon carbide MOSFETs," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 5014–5021, Oct. 2021.

[24] K. Puschkarsky, H. Reisinger, T. Aichinger, W. Gustin, and T. Grasser, "Understanding BTI in SiC MOSFETs and its impact on circuit operation," *IEEE Trans. Device Mater. Reliab.*, vol. 18, no. 2, pp. 144–153, Jun. 2018.

[25] B. Asllani, A. Castellazzi, O. A. Salvado, A. Fayyaz, H. Morel, and D. Planson, "Vth-hysteresis and interface states characterisation in SiC power MOSFETs with planar and trench gate," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2019, pp. 1–6.

[26] A. J. Lelis, R. Green, and D. B. Habersat, "SiC MOSFET threshold-stability issues," *Mat. Sci. Semicon. Proc.*, vol. 78, pp. 32–37, 2018.

[27] X. Zhong et al., "Bias temperature instability of silicon carbide power MOSFET under AC gate stresses," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1998–2008, Feb. 2021.
[28] D. B. Habersat, R. Green, and A. J. Lelis, "Evaluations of threshold voltage stability on cots SiC DMOSFETs using fast measurements," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2016, pp. CD–4–1–CD–4–5.
[29] D. Scholten, J. Baringhaus, D. Krebs, and S. Noll, "Hypothesis to explain threshold drift due to dynamic bipolar gate stress," in *Materials Science Forum*, vol. 1090. Trans Tech Publ, 2023, pp. 159–164.
[30] T. Aichinger, M. W. Feil, and P. Salmen, "Assessing, controlling and understanding parameter variations of SiC power MOSFETs in switching operation," *Key Eng. Mater.*, vol. 947, pp. 69–75, 2023.
[31] Y. Cai et al., "Characterization of gate-oxide degradation location for SiC MOSFETs based on the split C–V method under bias temperature instability conditions," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6081–6093, May 2023.
[32] P. Salmen et al., "Gate-switching-stress test: Electrical parameter stability of SiC MOSFETs in switching operation," *Microelectron. Reliab.*, vol. 135, 2022, Art. no. 114575.
[33] Y. Chen et al., "Investigation of threshold voltage instability of SiC MOSFETs under different gate voltage sequences," *IEEE Trans. Electron Devices*, vol. 71, no. 4, pp. 2536–2542, Apr. 2024.
[34] M. W. Feil et al., "On the frequency dependence of the gate switching instability in silicon carbide MOSFETs," in *Materials Science Forum*, vol. 1092. Trans Tech Publ, 2023, pp. 109–117.
[35] A. J. Lelis, D. B. Habersat, R. Green, and N. Goldsman, "Temperature-dependence of SiC MOSFET threshold-voltage instability," in *Materials Sci. Forum*, vol. 600. Trans Tech Publ, 2009, pp. 807–810.
[36] A. K. Ghosh, O. O. Awadelkarim, J. Hao, S. Suliman, and X. Wang, "Comparison of AC and DC BTI in SiC power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2022.
[37] M. Feil, K. Puschkarsky, W. Gustin, H. Reisinger, and T. Grasser, "On the physical meaning of single-value activation energies for BTI in si and SiC MOSFET devices," *IEEE Trans. Electron Devices*, vol. 68, no. 1, pp. 236–243, 2020.
[38] G. Pobegen, T. Aichinger, M. Nelhiebel, and T. Grasser, "Understanding temperature acceleration for NBTI," in *Proc. Int. Electron Devices Meeting*. IEEE, 2011, pp. 27–3.

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