Letters

An Accurate Power Loop Stray Inductance Extraction Method for SiC MOSFETs Based on Forced Resonance With Decoupling Capacitor

Da Zhou, *Student Member, IEEE*, Zhiqiang Wang, *Senior Member, IEEE*, Guoqing Xin, *Member, IEEE*, Xiaojie Shi, *Senior Member, IEEE*, and Yong Kang, *Fellow, IEEE*

***Abstract*—To better instruct the optimal operation of silicon carbide MOSFETs in converters, accurate estimation of the power loop stray inductance is essential, preventing unacceptable voltage overshoots and EMI noises during switching transients. This letter presents a stray inductance extraction method based on forced low-frequency resonance of the target stray inductance and the dc-link decoupling capacitance, which can be skillfully triggered by applying a switch in the dc bus. An ideal resonant tank can be created by selecting a Class I ceramic capacitor as the stable decoupling capacitor, enabling the precise result to be calculated. The extraction accuracy of this proposed method is verified through experiments, showing a relative error of 2.9% compared with the measurement using a professional impedance analyzer E4990A. Furthermore, unlike existing methods relying on high-frequency resonance with device junction capacitance at the fast-switching ringing stage, this method only requires low bandwidth test equipment, making it attractive for applications limited by costly measuring probes.**

***Index Terms*—Decoupling capacitor, low-frequency resonance, resonant tank, SiC MOSFETs, stray inductance extraction.**

I. Introduction

SILICON carbide (SiC) power MOSFETs have shown superior switching performance compared to their silicon counterparts. However, their switching speed is always limited by the voltage overshoots and EMI noises during switching transients induced by the power loop stray inductance [1], [2]. For SiC power converters, to fully utilize the fast-switching potential and ensure system's safe operation, precise extraction of the power loop stray inductance is becoming crucial [3], [4].

Previous research works on the extraction methods can be classified into three different categories: 1) numerical calculation, 2) instrument measurement, and 3) experimental test.

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The authors are with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: zhouda@hust.edu.cn; zhiqiangwang@hust.edu.cn; guoqingxin@hust.edu.cn; xiaojie_shi@hust.edu.cn; ykang@hust.edu.cn).

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The numerical calculation methods mainly utilize the finite element analysis (FEA) simulation, which relies on accurate three-dimensional (3-D) modeling and material characteristics. They have the potential to achieve high extraction accuracy with only a computer and some requisite domain knowledge [5]. However, in many cases, details of the packaged power module's internal structure are unavailable to design engineers, limiting the practical application of the methods.

The instrument measurement methods extract the target stray inductance utilizing professional equipment, such as the impedance analyzer, vector network analyzer, and *LCR* meter. They can provide an accurate result, at the cost of expensive instruments and time-consuming calibration work [6], [7].

The experimental test methods can be categorized into time-domain method (TDM) and frequency-domain method (FDM). In general, the TDM extracts the stray inductance by measuring the voltage overshoot V_o and current slope di/dt during switching transients [8]. The stray inductance L_p is calculated with the formula $V_o = L_p$ (di/dt), where the accuracy can be easily affected by the precision and synchronization of the voltage and current test probes. An improved TDM based on current integration formulas has been proposed in [9], which effectively reduces the equipment measuring noises.

However, due to the internal package inductance of power devices, the actual voltage V_{ds} during switching processes is hard to measure, making the TDM unsuitable for accurate extraction of the SiC MOSFETs' power loop stray inductance.

To overcome the limitations of the conventional TDM, the FDM has been studied [10], [11], [12]. Generally, the FDM extracts the stray inductance by analyzing the high-frequency ringing oscillation characteristics of the turn-OFF switching transients. In essence, it utilizes the resonance of the stray inductance L_p and the device's output capacitance C_{oss}, which introduces errors in several aspects. First, the C_{oss} is not a stable resonant capacitor due to its nonlinearity. Second, the known value of the C_{oss} could be inaccurate if obtained from the datasheet because of the device dispersion. Third, the C_{oss} can be easily influenced by all kinds of parasitic capacitance distributed in the direct bond copper (DBC) substrate and heatsinks.

To improve the extraction accuracy, the FDM putting a pretested auxiliary capacitor C_0 and the C_{oss} in parallel is proposed in [11] and [12]. However, this method still requires

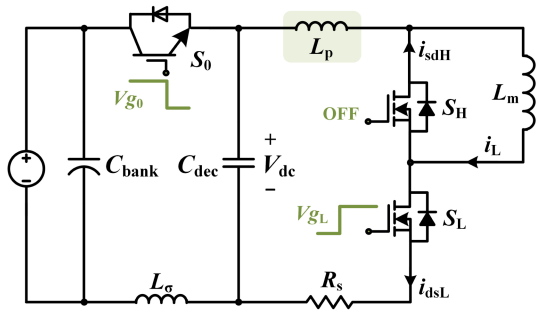


Fig. 1. Proposed power loop stray inductance L_p extraction platform.

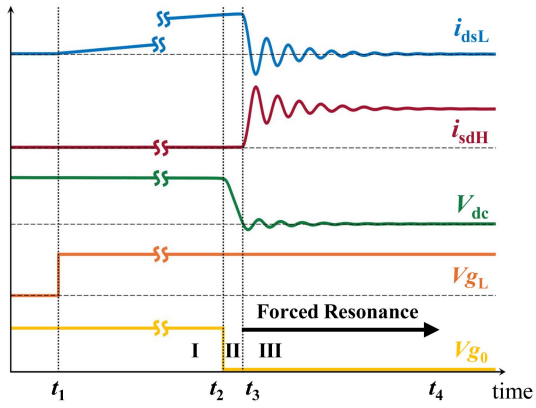


Fig. 2. Waveforms of key parameters during a complete extraction process.

high-bandwidth probes and may face challenges when dealing with power modules, where the capacitor C_0 is tough to add.

Nowadays, the decoupling capacitor has been widely used in the SiC power converts to minimize the stray inductance [8]. To address the challenges mentioned above, this letter presents an accurate FDM utilizing the forced low-frequency resonance of the stray inductance and the decoupling capacitance, which can be useful for SiC converters with dc-link decoupling capacitors. Its effect is validated through experimental results on the power loop formed by a typical SiC MOSFET half-bridge.

II. Proposed Method of Extraction

In this proposed method, an additional auxiliary switch S_0 is incorporated in the dc bus between the bulky bank capacitor $C_{\rm bank}$ and the decoupling capacitor $C_{\rm dec}$, based on the traditional pluses test circuit. This configuration is illustrated in Fig. 1. The target of our extraction is the power loop stray inductance $L_{\rm p}$ impeding the current commutation between switches and free-wheeling diodes (FWD) during the hard switching transients. By coordinating the gate drive signals of the auxiliary switch S_0, the active switch $S_{\rm L}$, and the passive switch $S_{\rm H}$, a desirable resonant tank, which involves the inductance $L_{\rm p}$ and the capacitance $C_{\rm dec}$ can be built. In this created resonant tank, an ideal *RLC* zero-input response is triggered automatically, resulting in a forced *LC* resonance. With the known capacitance $C_{\rm dec}$, accurate value of the inductance $L_{\rm p}$ can get calculated by analyzing the oscillation characteristics.

The entire inductance extraction process can be elucidated with Figs. 2 and 3. There are four necessary steps to elicit the forced $L_{\rm p}$-$C_{\rm dec}$ resonance.

1) *Step 1 (before t_1):* Set the initial state. Keep both the switch $S_{\rm H}$ and switch $S_{\rm L}$ OFF-state. Turn ON the auxiliary switch S_0. Make sure there is no initial current in the power loop.
2) *Step 2 (stage I: $t_1 \sim t_2$):* Enter the current rising stage. Turn ON the active switch $S_{\rm L}$ and keep the auxiliary switch S_0 ON-state. The dc bank capacitor $C_{\rm bank}$ discharges to the load inductor $L_{\rm m}$, resulting in a constant rate of rise in load current due to the negligible capacitor voltage variation.
3) *Step 3 (stage II: $t_2 \sim t_3$):* Enter the voltage dropping stage. Once the load current reaches a sufficient value, turn off the auxiliary switch S_0 and keep the active switch $S_{\rm L}$ ON-state. The load current path shifts from the bank capacitor $C_{\rm bank}$ to the decoupling capacitor $C_{\rm dec}$, which carries on the discharge. Given the considerable load current and the relatively small capacitance $C_{\rm dec}$, the voltage $V_{\rm dc}$ declines rapidly. During this brief interval, the load current could be considered unchanged, resulting in a constant rate of decrease in $V_{\rm dc}$.
4) *Step 4 (stage III: $t_3 \sim t_4$):* Enter forced resonance stage. The decoupling capacitor voltage $V_{\rm dc}$ decreases from the dc bus to a negative value due to the discharge with an inductive load current. Once the reverse voltage applied to the passive switch $S_{\rm H}$ exceeds the FWD's forward threshold, this diode is activated, providing a low-impedance current path for the load inductor $L_{\rm m}$. Driven by the voltage $V_{\rm dc}$ and hindered by the inductance $L_{\rm p}$, the load current shifts from the switch $S_{\rm L}$ to the FWD. Subsequently, the resonant tank consisting of the inductance $L_{\rm p}$ and the capacitance $C_{\rm dec}$ is formed, resulting in a forced *LC* resonance. During this resonant process, the load inductor $L_{\rm m}$ functions as a constant current source, providing a dc bias current for the parallel FWD and not participating

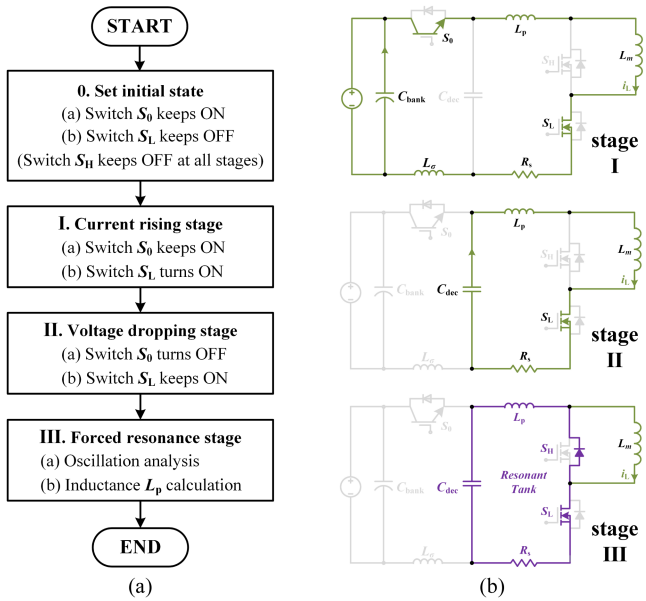


Fig. 3. Detailed information of the proposed extraction method. (a) Flowchart. (b) Current flowing condition at different stages.

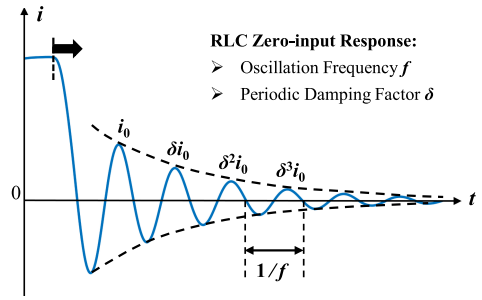


Fig. 4. Sinusoidal damped oscillation waveform of the *RLC* response.

in any resonance. The forward current offset enables the FWD to remain ON-state, consequently allowing the resonant tank's ac current to flow through it. This leads to a complete *RLC* zero-input response in the power loop, with the initial status of no voltage on capacitor $C_{\rm dec}$ and some current on inductor $L_{\rm p}$.

For a practical value of $C_{\rm dec}$, the *RLC* resonant tank can be regarded as an underdamped second-order system whose zero-input response is a sinusoidal damped oscillation, in which the amplitudes of loop current and capacitor voltage exponentially decay with a constant rate while their oscillation frequency f remains unchanged. The parameter δ is defined in reference to the periodic damping factor, which equals to the ratio of two contiguous periods' oscillation amplitudes, as shown in Fig. 4.

Mathematically, this *RLC* underdamped response's characteristic parameters, including the oscillation frequency f and periodic damping factor δ, are given by

$$f = \frac{\sqrt{1-\zeta^2}}{2\pi\sqrt{L_{\rm p}C_{\rm dec}}} \tag{1}$$

$$\delta = e \wedge \left(\frac{-2\pi\zeta}{\sqrt{1-\zeta^2}}\right) \tag{2}$$

where $L_{\rm p}$ is the target power loop stray inductance, $C_{\rm dec}$ is the decoupling capacitance, and ζ is the circuit damping ratio.

By selecting a Class I ceramic capacitor as the decoupling capacitor (e.g., in C0G dielectric) whose capacitance is able to keep constant under different bias voltages and temperatures, an accurate value of the target inductance $L_{\rm p}$ can be calculated with the known quantities and Formulas (1) and (2).

III. Experimental Verification

A. Inductance Measurement With Impedance Analyzer

To estimate the extraction accuracy of this proposed method, a power loop with two discrete SiC MOSFETs is designed for experimental verification, as shown in Fig. 5. This target loop under test consists of a decoupling capacitor and a half-bridge circuit. Without additional anti-parallel diodes, the body diode of the passive SiC MOSFET functions as the FWD, making it convenient to measure the stray inductance.

The baseline stray inductance is first established utilizing an impedance analyzer (IA) Keysight E4990A. According to [13], the one-port impedance characterization technique (e.g., using an impedance analyzer) may bring significant extraction errors due to some potential coupling effects. To ensure the accuracy of this extracted baseline inductance, some crucial details for test are given below. The test method is presented in Fig. 6.

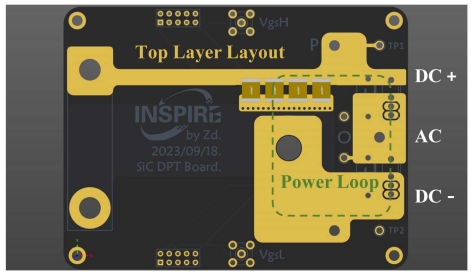


Fig. 5. PCB layout of the designed test power loop for experiment.

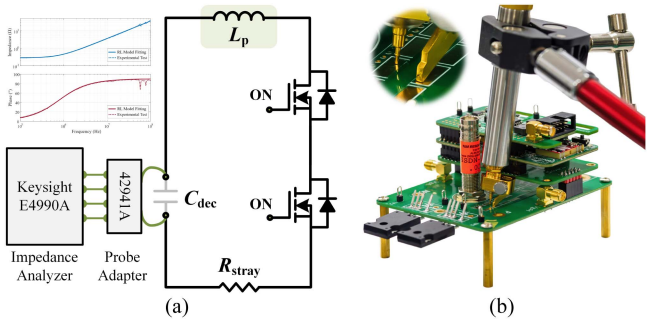


Fig. 6. Inductance $L_{\rm p}$ measurement with an impedance analyzer. (a) Test schematic. (b) Test setup with the probe adapter keysight 42941A.

First, keep both the active and passive switch ON-state with isolated gate drivers, avoiding any floating gate terminals. The impedance of the devices' G-S and G-D parts can be bypassed by the D-S ON resistance at the same time. Second, to reduce the ground parasitic capacitance, a floating battery is used to provide a power supply for the gate drivers. Finally, the power loop is connected to the IA through a probe adapter Keysight 42941 A, with the probe tips touching the capacitor's soldering pads. The target loop's impedance can be measured through a frequency sweep test (100 KHz $\sim$ 100 MHz).

Fitting the measurement results to an ideal RL series model, the target inductance is extracted to be 57.5 nH, not including the equivalent series inductance (ESL) of $C_{\rm dec}$.

The decoupling capacitor's ESL is then obtained using the capacitor characteristic analysis tool "K-SIM3" provided by KEMET [14]. According to this official tool, the used ceramic capacitor in C2220 package exhibits 0.7 nH ESL under 1 MHz frequency. Therefore, 58.2 nH can be regarded as the baseline for this test power loop's stray inductance $L_{\rm p}$.

B. Inductance Extraction With Proposed FDM

The experimental setup for the proposed power loop stray inductance extraction FDM is shown in Fig. 7. In this hardware platform, a 650 V/100 nF ceramic capacitor in C0G dielectric (CKC21C104JWGACAUTO from KEMET) is chosen as the dc-link decoupling capacitor, and two 750 V/26 mΩ SiC MOSFETs (SCT4026DR from ROHM) are used for the active switch $S_{\rm L}$

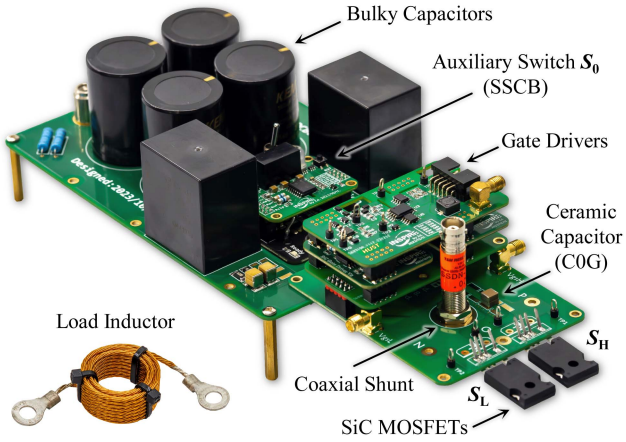


Fig. 7. Experimental setup for the proposed inductance extraction method.

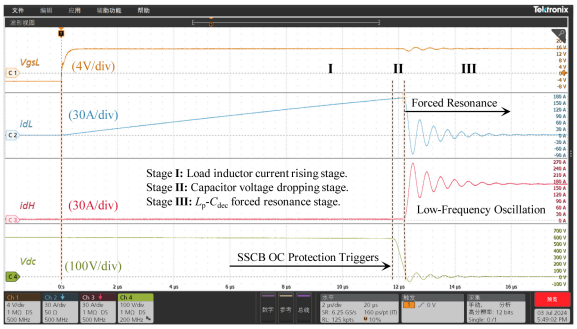


Fig. 8. Experimental waveforms of the proposed FDM.

and passive switch S_H. A solid-state circuit breaker is utilized as the auxiliary switch S_0, which operates like a normally-ON device but is able to turn OFF automatically when the flowing current exceeds its setting threshold.

The experimental waveforms are presented in Fig. 8. After the decoupling capacitor's voltage decreases to zero, an ideal *RLC* zero-input response is triggered. Consequently, a low-frequency sinusoidal damped oscillation can be observed in both the S_L switch's current waveform and the C_{dec} capacitor's voltage waveform, exhibiting identical oscillation frequency and amplitude decay rate. Except for 90° phase difference, the above two waveforms have the same response characteristics. Therefore, for practical applications, measuring one of them is sufficient to finish the extraction.

The extracted key parameters at the forced resonance stage are displayed in Fig. 9, including the oscillation frequency and the periodic damping factor. By utilizing a digital multimeter, the accurate capacitance C_{dec} can be obtained. Subsequently, the target solution can be calculated with (1), (2) and the known quantities. As a result, the extracted target stray inductance is 59.9 nH, with 1.7 nH higher than the baseline.

C. Comparison With Traditional FDM

The traditional FDM relies on the high-frequency ringing oscillation between the power loop stray inductance L_p and the device's output capacitance C_{oss} during the turn-OFF switching transient. In general, the known quantity C_{oss} is obtained from

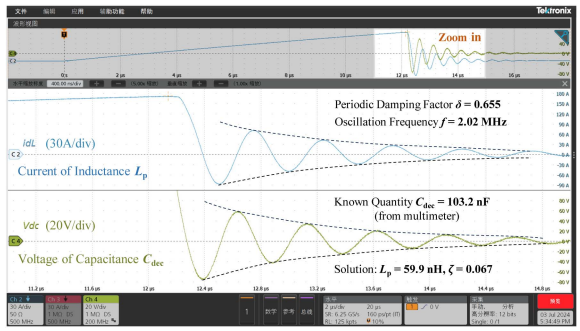


Fig. 9. Zoom-in experimental waveform of the proposed FDM.

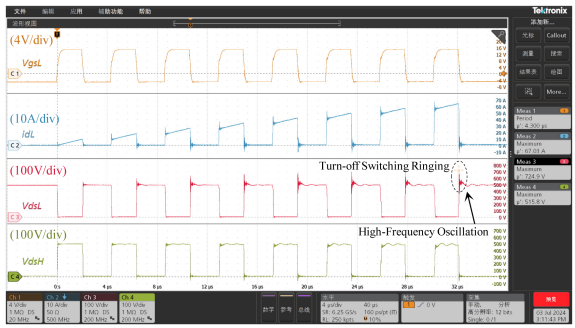


Fig. 10. Experimental waveforms of the traditional FDM.

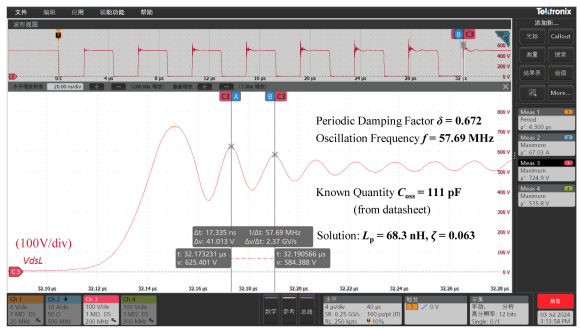


Fig. 11. Zoom-in experimental waveform of the traditional FDM.

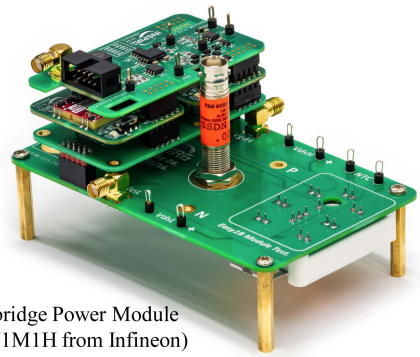
the datasheet, inevitably introducing some errors due to C_{oss}'s nonlinearity and device dispersion. Furthermore, the C_{oss} can be easily influenced by all kinds of parasitic capacitance distributed in the DBC substrate and heatsinks, making the accurate stray inductance extraction challenging.

Based on the previous experimental setup, a conventional pluses test is performed to verify the accuracy of traditional FDM, as shown in Fig. 10. Under the switching condition of 500 V dc voltage and 67 A load current, the active switch's turn-OFF voltage waveform is shown in Fig. 11. During the switching ringing stage, the voltage oscillation frequency is over 50 MHz, which is much higher than the former forced resonance frequency and makes a request for the bandwidth of test probes. By replacing C_{dec} with C_{oss} in Formula (1), the power loop stray inductance L_p is solved to be 68.3 nH, with 10.1 nH higher than the baseline.

According to the experimental results, extraction accuracy of different FDMs is compared in Table I. It is found that the

TABLE I
INDUCTANCE EXTRACTION RESULTS COMPARISON 1

Methods	L_p Extraction	Relative Error	Requirement
IA Measurement	58.2 nH	0%	Professional Instrument
Traditional FDM	68.3 nH	17.4%	High Bandwidth Test Probe
Proposed FDM	59.9 nH	2.9%	Low Bandwidth Test Probe



● SiC Half-bridge Power Module
(FF17MR12W1M1H from Infineon)

Fig. 12. Experimental setup of low-inductance power loop under test.

TABLE II
INDUCTANCE EXTRACTION RESULTS COMPARISON 2

Methods	L_p Extraction	Relative Error	Requirement
IA Measurement	15.2 nH	0%	Professional Instrument
Traditional FDM	17.3 nH	13.8%	High Bandwidth Test Probe
Proposed FDM	15.4 nH	1.3%	Low Bandwidth Test Probe

traditional FDM shows a low extraction accuracy with over 15% relative error, while the proposed FDM holds a much higher extraction accuracy with less than 3% relative error.

This is mainly due to replacing the target stray inductance's resonant object from the nonlinear junction capacitor $C_{\rm oss}$ with small capacitance to the stable decoupling capacitor $C_{\rm dec}$ with large capacitance. It not only improves the ideal *LC* sinusoidal resonance waveforms, but also reduces the measured oscillation frequency significantly. Hence, with this novel FDM, a precise result could be obtained with just low-cost probes.

To verify the extraction accuracy of this method for power loop with low stray inductance, the half-bridge composed of a commercial SiC power module is tested, as shown in Fig. 12. The experimental results are presented in Table II. For this setup, the proposed FDM still exhibits high accuracy, with 12.5% relative error reduction compared to traditional FDM. In theory, the oscillation frequency gets higher in *RLC* circuit with smaller inductance, where the method requiring lower measuring bandwidth could show a greater advantage.

IV. EXTRACTION ACCURACY IMPROVEMENT

To ensure the extraction accuracy of this proposed FDM, some noteworthy suggestions are given below.

Select an appropriate test load current. The load current, which determines the initial state of the *RLC* resonant tank, directly affects the oscillating amplitudes of created zero-input response. Considering that the pulses test is safe, its value is feasibly set higher than the power device's rated current to guarantee a significant amplitude of oscillation, reducing the errors caused by oscilloscope and probes. Meanwhile, it is also expected not to excel three times the rated current, which may make the used SiC MOSFETs operate into the desaturation region and result in a changeful circuit damping ratio ζ.

Choose a suitable decoupling capacitor. For practical SiC applications, the multilayer ceramic capacitor (MLCC) with extremely low ESL is usually preferred. It is recommended to select an MLCC in C0G dielectric, which can provide a stable and constant capacitance. Its capacitance value must be low enough to make the created *RLC* resonant tank an underdamped second-order system ($\zeta < 1$). Otherwise, the result of triggered zero-input response will not be the desired sinusoidal damped oscillation. At the same time, this value should be as large as possible to reduce the oscillation frequency (preferably below 10 MHz), reducing the bandwidth requirement for test probes.

Acquire an accurate $C_{\rm dec}$ capacitance value. The capacitance of the used C0G MLCC in this letter shows a tolerance of 5%, which can directly affect the accuracy of the extraction result. Therefore, it is advisable to measure this capacitance with a commercial digital multimeter for accuracy improvement. Take the used multimeter Fluke 15B+ for example. It is able to measure the capacitance under 200 KHz frequency, providing both 0.1 nF resolution and 2% accuracy for test capacitance below 400 nF, effectively reducing the extraction errors.

V. CONCLUSION

In this letter, a novel power loop stray inductance extraction method is proposed based on forced low-frequency resonance of the stray inductance and the stable decoupling capacitance. By skillfully changing the resonant object from the device junction capacitor to the dc-link decoupling capacitor, this method has two advantages over existing methods. First, it exhibits much higher extraction accuracy, with over 10% less relative error than the traditional FDM. Second, it shows a significantly reduced bandwidth requirement for measuring equipment, making it attractive for applications limited by costly high-bandwidth test probes. The advantages are verified through experimental results both on the SiC MOSFET power module and discrete devices.

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