A Digital Pulse Frequency Modulation Technique for a Series Resonant Converter-Based LED Driver

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***Abstract*—Pulse frequency modulation (PFM)-based controllers are frequently employed for resonant converter-based light-emitting diode (LED) driver applications. Most of the PFM controllers rely on multiple sensors/control loops and exploit multiple proportional integral (PI) controllers. Thus, straightforward digital implementation of these controllers will not be simple and cost-effective. This article proposes a simple digital PFM control scheme for the series resonant converter (SRC)-based LED driver. The slope of the frequency change of the proposed PFM scheme is implemented using a hysteresis current regulator. The hysteresis current regulator utilizes an envelope signal and the rising and falling of the envelope signal are controlled by a hysteresis band. A sawtooth wave is compared with the envelope signal to produce variable frequency pulses. Thus, the proposed scheme can implement PFM without using any PI controller. Furthermore, the proposed technique exploits only one sensor and one control loop. Therefore, the proposed scheme is simple, cost-effective, and does not impose a huge computational burden on the digital platform. Guidelines for designing different components of the proposed control scheme are presented. Moreover, considering current output, the gain of the whole SRC LED system is derived and the design steps of the output filter are discussed. A 170W SRC LED driver prototype is developed and the proposed scheme is validated using a field-programmable gate array (FPGA)-based digital platform. The proposed digital control scheme can be extended further for other resonant converter-based LED drivers.**

***Index Terms*—Digital control, light-emitting diode (LED) driver, pulse frequency modulation (PFM), sampling, series resonant converter (SRC).**

I. Introduction

THE light-emitting diodes (LEDs) find widespread application due to their high efficiency, low maintenance cost, long life, etc [1], [2]. To achieve desired brightness and luminous efficacy, LEDs are driven by current controlled switch-mode drivers [2].

The resonant converters are widely used in many applications where high efficiency is the major concern for a wide range of input supply [3], [4], [5] as well as wide range of output load variation [3], [6]. Furthermore, the inherent soft-switching of these converters enables the designers to operate at a very high switching frequency to achieve high power density without compromising efficiency [5]. The resonant converters are broadly classified under three major categories: series resonant converter (SRC), parallel resonant converter (PRC), and notch resonant converter (NRC) [7]. For LED drivers and related applications, both isolated and non-isolated versions of the SRC are usually preferred [7]. Based on the configuration of the primary switching network, the SRC LED drivers are available in a variety of topologies, such as half-bridge (HB-SRC) [8], full-bridge (FB-SRC), buck–boost half-bridge (BB-HBSRC), and buck–boost full bridge (BB-FBSRC) [9]. Various other topologies were also presented to handle a wide range of input voltage variations [6], [10], [11] and output voltage variations [3], [6].

Modulation techniques, such as phase shift modulation (PSM), pulsewidth modulation (PWM), pulse frequency modulation (PFM), and self-oscillation control (SOC) were reported for LED driver circuits [6], [9], [12]. PSM-based techniques monitor the duty ratio and phase-shift to regulate the power flow. However, these controllers cause excessive energy loss in the switching devices due to asymmetrical current sharing in the H-bridge [13]. PWM-based controllers can achieve zero-voltage-switching (ZVS). However, their voltage gain range is limited [14] and they are preferred for light load conditions [15]. To meet the requirements of LED loads for a wide load variation, application of traditional PFM and hybrid PFM stands necessary for the resonant converters [16], [17], [18], [19], [20], [21]. In [18], a single loop proportional integral (PI) compensator-based current mode PFM controller was utilized for a 100 W boost integrated power factor corrector (PFC-LLC) streetlight LED driver. To maintain better efficiency in PFC-LLC with universal input, a hybrid PFM is combined with asymmetric pulse width modulation (APWM) [19], [20]. To exploit the benefits of PFM and PWM controllers, mode transition from PWM to PFM and vice-versa was reported for active-matrix organic light emitting diode (AMOLED) display applications [21]. In [22] and [23], both PSM and PWM were mixed with the conventional PFM scheme to address circulating current related challenges.

Recently, digital controllers have gained immense popularity in the power management industry for several benefits, such as reprogrammability and real-time tuning capability, etc [24]. However, digital implementation of the well-established analog PFM/hybrid-PFM controllers is not easy [16], [17], [18], [19], [20], [21]. This is due to the computational speed and resource limitations of the digital platforms [25]. Realization of closed-loop PFM or hybrid PFM controllers for a resonant converter needs multiple building blocks, such as a PI or similar compensator block, PLL block, ePWM block, dead-time block, delay block, register units, and counters, and each of

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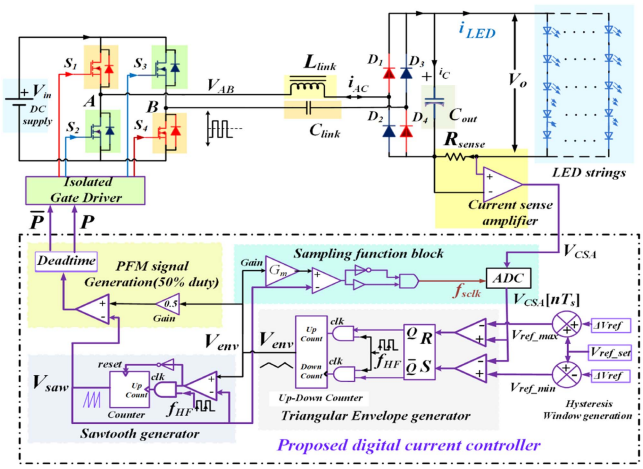

Fig. 1. Schematic diagram of the SRC LED driver governed by the proposed control scheme.

these blocks incorporates elementary microcircuits, such as look-up-table (LUT), D flip-flop (DFF), static random-access memory (SRAM), dynamic random-access memory (DRAM), and digital signal processor (DSP) [26], [27], [28] [29]. Among these blocks, the PI controller alone exploits most of the LUTs, DFFs, and DSPs. To address the abovementioned issues, a single-loop PI controller-free fully digital PFM control scheme is proposed for the SRC LED driver. The proposed PFM scheme's frequency change is managed by a hysteretic current regulator. This regulator uses an envelope signal, with its rise and fall controlled by a hysteresis band. A sawtooth wave is then compared with the envelope signal to generate variable frequency pulses. To capture switching noise-free samples of the LED current, a variable frequency sampling clock is produced in sync with the converter switching frequency. Detailed analysis and design guidelines for the different components of the proposed control scheme are presented. Furthermore, considering the current output, the gain of the whole SRC LED system is derived. The proposed control technique can be easily extended for other resonant converter-based LED drivers.

The rest of this article is organized as follows. The proposed controller and relevant analysis and design are presented in Sections II and III. The design of SRC power stage is discussed in Section IV. Section V provides detailed discussions on analytical estimation of the control slope and thermal effects on the proposed controller. The experimental validation of the proposed scheme is provided in Section VI. Finally, Section VII concludes this article.

II. Proposed PFM-Based SRC System

Fig. 1 presents a schematic diagram of a SRC-based LED driver governed by the proposed digital control scheme. V_{in} is the applied dc voltage input to the H-bridge network consisting of four MOSFETs S_1, S_2, S_3, and S_4. The inductor L_{link} and capacitor C_{link} form a series resonant tank circuit to serve as an AC-link between the input side H-bridge switching network and the output side full bridge rectifier. The rectifier comprises four Schottky diodes D_1, D_2, D_3, and D_4 and it is connected to a filter capacitor C_{out}. Output voltage v_o is developed across the capacitor C_{out}, which contains a peak-to-peak ripple ΔV_{pp} over the dc average value V_o. Therefore, the relation between v_o and V_o can be expressed as, $v_o = V_o \pm (0.5 * \Delta V_{\text{pp}})$. The LED load, which consists of multiple LED strings, is arranged

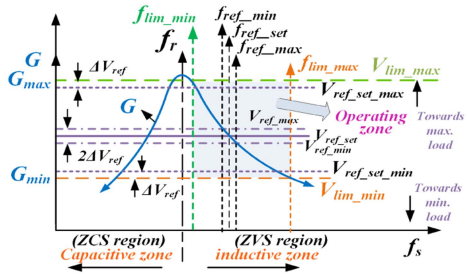

Fig. 2. Transfer characteristics of the SRC.

in parallel with C_{out}. Each string has a few high brightness high-power LEDs connected in series. The total LED current i_{LED} passes through the current sense resistor (CSR) R_{sense} and the voltage drop across it is sensed by the current sense amplifier (CSA). The CSA produces an equivalent voltage V_{CSA}, which is fed to the analog-to-digital converter (ADC) of the proposed digital current controller.

The ADC samples the incoming signal V_{CSA} using a variable frequency sampling mechanism and the controller performs digital signal processing based on the proposed algorithm. Pulse frequency modulated complimentary signals P and $\bar{P}$ with a fixed duty ratio of 50% are generated. Suitable deadtime is introduced with these signals (P and $\bar{P}$) to prevent shoot-through of the high-side and low-side field effect transistors (FETs). The H-bridge legs are operated alternately with these high-frequency gate pulses and the generated pole-to-pole bipolar voltage V_{AB} is fed to the tank circuit. For power transfer, the AC-link current i_{ac} continuously changes its amplitude and frequency as per the control action imposed by the proposed controller. Fig. 2 illustrates the generalized SRC transfer characteristics and highlights the working range of the proposed controller. f_r represents the resonant frequency of the converter. If the switching frequency of the converter f_s is below f_r, the converter will operate in the ZCS region. f_s above f_r leads to the ZVS region where the SRC will operate. Thus, the objective is to regulate the switching frequency above f_r. Symbol $V_{\text{ref\_set}}$ refers to the voltage equivalent to the average demand LED current I_{LED}. A small voltage deviation ΔV_{ref} forms a hysteresis control band around $V_{\text{ref\_set}}$ having the $V_{\text{ref\_max}}$ as the upper limit and $V_{\text{ref\_min}}$ as the lower limit, respectively. This ΔV_{ref} stands equivalent to the allowed peak ripple current Δi_{LED} and the equation can be expressed as follows:

$$\Delta V_{\text{ref}} = G_{\text{CSA}}\, \Delta i_{\text{LED}}. \tag{1}$$

The $2\Delta V_{\text{ref}}$ regulation window around the set reference $V_{\text{ref\_set}}$ represents the voltage equivalent to the allowable peak-to-peak current ripple present in the total LED current i_{LED}. $V_{\text{ref\_max}}$ line intersects the gain curve G at a frequency $f_{\text{ref\_min}}$ and $V_{\text{ref\_min}}$ line intersects the gain curve at a frequency $f_{\text{ref\_max}}$. It is imperative that the selection of Δi_{LED} impacts on the switching frequency f_s and causes its deviation from $f_{\text{ref\_min}}$ to $f_{\text{ref\_max}}$ while maintaining a mean operating frequency $f_{\text{ref\_set}}$ (see Fig. 2). A designer can choose the Δi_{LED} such that it can be small enough under the lowest load output from the converter. A standard choice is around 10% to 30% of the full load current [30], [31], [32], [33].

In conventional controllers for applications like the LED drivers, two-loop control is generally employed. The two-loop scheme exploits a voltage-mode (slow) outer loop and a current-mode (fast) inner loop. One of the features of this outer voltage-loop is to protect the LEDs from over-voltage

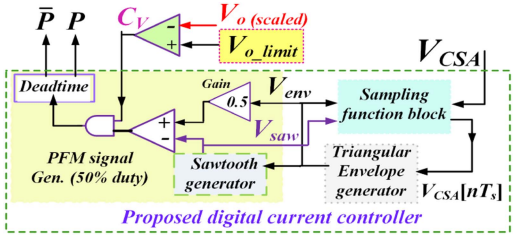

Fig. 3. Illustrative safety feature of the proposed controller.

events. However, application of a single control loop has also been reported in commercial applications [34], [35] and research papers [18], [30], [36], [37]. It avoids the cost of extra sensors or other mixed-signal components and simplifies the control circuitry. Due to these advantages, the authors consider single-loop implementation. However, an additional layer of safety can be incorporated in the proposed controller by sensing the scaled output voltage $V_{o(\text{scaled})}$ as shown in Fig. 3. The scaled output voltage, $V_{o(\text{scaled})}$ can be obtained from a resistor voltage-divider network, connected across the output dc bus. The voltage-divider resistor pairs are to be chosen carefully so that $V_{o(\text{scaled})}$ stays lower than a preset maximum voltage $V_{\text{o\_limit}}$ for normal operating conditions. An external comparator C_v compares $V_{o(\text{scaled})}$ with the preset maximum voltage ($V_{\text{o\_limit}}$). The output of C_v is AND-ed with the proposed PFM output. The switching signals P and $\bar{P}$ will be produced only if $V_{o(\text{scaled})} < V_{\text{o\_limit}}$. Thus, without using any ADC or PI controller, the safety feature can be easily incorporated. The forward voltage, dc "on-resistance," and small-signal impedance of the LED vary with temperature. However, for the present application, the temperature variation would be between 25 °C and 100 °C. Within this range, the variations of the abovementioned parameters are insignificant [38]. Thus, the overvoltage protection loop and controller will work properly.

III. Proposed Control Technique

A. Method of Operation

In Fig. 2, the $V_{\text{lim\_min}}$ represents the minimum voltage limit equivalent to the minimum LED current (for minimum gain G_{min}) when the demand reference is set at $V_{\text{ref\_set\_min}}$. Therefore, the $V_{\text{lim\_min}}$ corresponds to the highest operating frequency $f_{\text{lim\_max}}$. The choice of $f_{\text{lim\_max}}$ helps retaining a tradeoff between the system efficiency and minimum output loading. $V_{\text{lim\_max}}$ refers to the maximum voltage equivalent to the maximum demand current (for maximum gain G_{max}) when the reference is set at $V_{\text{ref\_set\_max}}$ and corresponds to the lowest allowable frequency $f_{\text{lim\_min}}$(slightly higher than the system resonant frequency f_r). Therefore, based on the demand LED current, the converter's switching frequency $f_s(=1/T_s)$ can vary inside the entire range of frequencies from $f_{\text{lim\_min}}$ to $f_{\text{lim\_max}}$. The block diagram of the proposed digital current-controller is portrayed in Fig. 1 and its illustrative waveforms are shown in Fig. 4. The ADC takes this variable frequency sampling clock f_{sclk} to obtain voltage samples $V_{\text{CSA}}[nT_s]$ from the sensed voltage V_{CSA}. Only one sample per switching cycle is obtained as shown in Fig. 4 and the sampled value is compared with the hysteresis band ($2\Delta V_{\text{ref}}$ as shown in Figs. 2 and 4). The outputs of the comparators are passed to a latch as shown in Fig. 1. Whenever $V_{\text{CSA}}[nT_s]$ crosses on or below $V_{\text{ref\_min}}$, the latch is set by the lower comparator's output S and if $V_{\text{CSA}}[nT_s]$ crosses on or above $V_{\text{ref\_max}}$, the latch is reset by the upper comparator's output R. The latch outputs

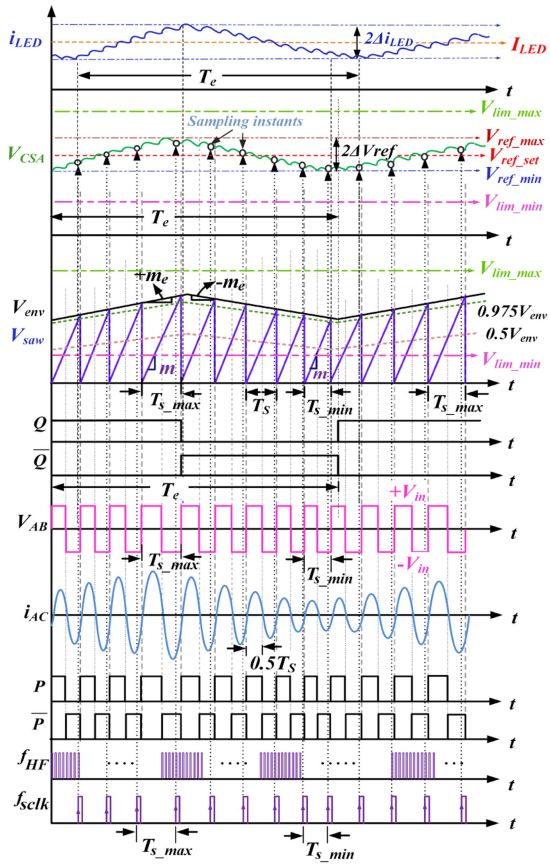

Fig. 4. Illustrative waveforms of the proposed control method.

Q and $\bar{Q}$ both are used to feed high-frequency master clock f_{HF} to the up–down counter module as shown in Fig. 1. If Q is logic high, the counter starts count-up otherwise it starts count-down to develop a triangular envelope waveform V_{env} as shown in Fig. 4. While the counter is in up-count mode, the envelope starts rising with a constant slope $+m_e$ and when the counter is in down-count mode, the envelope starts falling with a constant slope $-m_e$. The frequency of signals Q and $\bar{Q}$ is same as the frequency of this triangular envelope V_{env} (see Fig. 4). The time period of V_{env} is $T_e = 1/f_e$ and T_e depends on the time duration taken by V_{CSA} to reach either of the hysteresis band-limits, from $V_{\text{ref\_min}}$ to $V_{\text{ref\_max}}$ and vice-versa (see Fig. 4). The V_{env} is fed to the sawtooth generator block, sampling function block, and PFM signal generation block.

In sawtooth generator block, a comparator compares the counter module output V_{saw} with envelope signal V_{env}. Initially, V_{saw} is less than V_{env}, and at every $+ve$ edge of high-frequency clock f_{HF}, the counter keeps updating itself till it reaches V_{env}. An automatic reset occurs as V_{saw} crosses V_{env}. This leads to the generation of sawtooth wave V_{saw} with slope m (see Fig. 4). Since the slope m is much higher than the slope m_e, a series of sawtooth cycles appear with continuously varying time periods T_s. At any stable operating condition, T_s increases from a minimum value $T_{\text{s\_min}}$ to a maximum value $T_{\text{s\_max}}$ with the rising slope $+m_e$, and also decreases from $T_{\text{s\_max}}$ to $T_{\text{s\_min}}$ with the falling slope $-m_e$. Clearly, the variation in the sawtooth wave time period T_s occurs in guidance with the control envelope (V_{env}). The hysteresis control-band ($2\ \Delta V_{\text{ref}}$) and the envelope slope m_e are to be chosen such that any abrupt change in switching time-period T_s

can be avoided and the maximum switching frequency can be restricted to a certain allowable value ($f_{\text{lim\_max}}$).

In the PFM signal generation block, V_{env} is made 0.5 times and compared with V_{saw} to produce a PFM signal of 50% duty (see Figs. 1 and 4). The PFM output is passed through the deadtime block to produce complimentary signals P and $\bar{P}$ with an adequate dead time. These complimentary signals are fed to the isolated gate driver. In the sampling function block module, V_{env} is scaled down by passing through a gain block G_m. A typical range of G_m will be between 0.9 and 0.98. The scaled V_{env} is compared with the variable frequency sawtooth wave V_{env} (see Fig. 1) and the output of the comparator is delayed for a few high-frequency clock (f_{HF}) cycles. The same comparator output is also inverted and both the delayed and inverted signals are AND-ed to generate a variable frequency sampling clock f_{sclk} in sync with the converter switching frequency (f_s). The positive edge of the sampling clock (f_{sclk}) can be adjusted with a suitable value of G_m such that the presence of the switching noise can be effectively avoided at the sampling instants of the captured voltage samples ($V_{\text{CSA}}[nT_s]$). Therefore, switching noise-free samples can be obtained even with a variable frequency scheme.

B. Analysis and Digital Implementation of Control Stage

The LED load current i_{LED} consists of an average dc component I_{LED} and peak-to-peak current ripple of $2\Delta i_{\text{LED}}$ (see Fig. 4). The LED current is sensed using a CSA of gain G_{CSA}. Thus, the equivalent voltage reference $V_{\text{ref\_set}}$ can be set for a particular load demand

$$V_{\text{ref\_set}} = I_{\text{LED}}\, G_{\text{CSA}}. \tag{2}$$

Around this $V_{\text{ref\_set}}$, the hysteresis band $2\Delta V_{\text{ref}}$ is applied. This band has a maximum value of $V_{\text{ref\_max}}$ and a minimum value of $V_{\text{ref\_min}}$. Within this limit, the instantaneous LED current will vary around the set reference. As discussed in Section II and illustrated in Fig. 2, the $V_{\text{ref\_set}}$ can take $V_{\text{ref\_set\_max}}$ for the maximum average LED current. For minimum average LED current, it can take $V_{\text{ref\_set\_min}}$. Using (2), these two limits can be expressed in terms of LED current and CSA gain as follows:

$$V_{\text{ref\_set\_max}} = I_{\text{LED(max)}}\, G_{\text{CSA}} \tag{3}$$

$$V_{\text{ref\_set\_min}} = I_{\text{LED(min)}}\, G_{\text{CSA}}. \tag{4}$$

The sawtooth wave V_{saw} achieves the lowest frequency ($f_{\text{lim\_min}}$) when the peak of V_{env} signal reaches $V_{\text{lim\_max}}$ and V_{saw} hits at the peak of V_{env} [see Fig. 5(a)]. Thus, $T_{\text{lim\_max}}$ is the maximum time period that corresponds to the lowest possible frequency $f_{\text{lim\_min}}$. A single cycle of the sawtooth wave is shown in Fig. 5(b) for mathematical analysis. From triangle ΔABC, the slope m of the sawtooth wave can be expressed as follows:

$$m = \tan\theta = {}^{AB}/_{BC}. \tag{5}$$

Now, $AB = (V_{\text{lim\_min}} + x)$ and $BC = T_{\text{s\_min}}$. Thus, the slope m_e can be derived from (5) as follows:

$$m_e = m - {}^{V_{lim\_min}}/_{T_{s\_\min}}. \tag{6}$$

Considering the highest load case, the slope m_e can be extrapolated up to the maximum equivalent limit $V_{\text{lim\_max}}$ as shown in Fig. 5(a). The corresponding time period is $T_{\text{lim\_max}}$. Therefore, m can be written as follows:

$$m = \frac{V_{\text{lim\_max}}}{T_{\text{lim\_max}}} = V_{\text{lim\_max}} f_{\text{lim\_min}}. \tag{7}$$

For digital implementation, both the envelope V_{env} and sawtooth V_{saw} are produced using counters. The V_{env} up–down counter's step-size is k and it increments or decrements its value at every rising edge of f_{HF}. For V_{saw}, a counter operates only in up-count mode with a step increment d at every rising edge of f_{HF}. The counter resets to zero when $V_{\text{saw}} > V_{\text{env}}$. For the sawtooth wave V_{saw}, d needs to be kept fixed such that the slope m can be generated. The slope m_e is also generated for the envelope wave V_{env}, as shown in Fig. 5(c) where the value of k needs to be calculated based on slope m_e. The relation between the step size d and slope m can be derived as follows:

$$m = d/T_{\text{HF}} \quad or, \quad d = m/f_{\text{HF}}. \tag{8}$$

Similarly, for slope m_e, it can be written as follows:

$$m_e = k/T_{\text{HF}} \quad or, \quad k = {}^{m_e}/_{f_{HF}}. \tag{9}$$

Further, (8) can be simplified using (7) as follows:

$$d = V_{\text{lim\_max}} f_{\text{lim\_min}} f_{\text{HF}}^{-1}. \tag{10}$$

The high-frequency clock f_{HF} is readily available with any digital platform. Expressions for $f_{\text{lim\_min}}$ and f_e are derived in Section IV. Afterward, an expression for m_e is estimated. Finally, the choice of $V_{\text{lim\_max}}$ depends on the input voltage limit of the ADC.

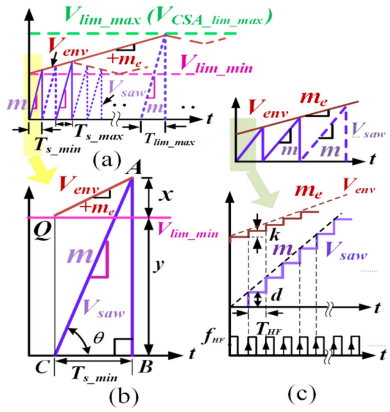

Fig. 5. Diagrams for the calculation of the slope m_e: (a) Sectional representation of the proposed scheme with extrapolated envelope. (b) Close-up view of a cycle indicating minimum switching period. (c) Illustrative diagram for the digital synthesis of slopes m and m_e.

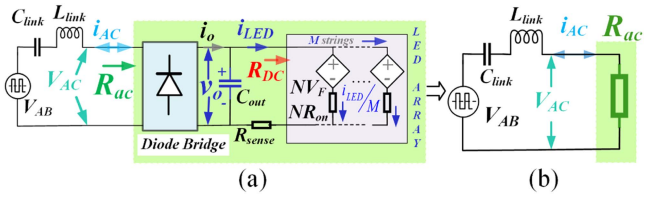

Fig. 6. Illustrative diagram of the LED driver: (a) Switching network is replaced with a square-wave AC source V_{AB} and the output LED load is represented as dependent voltage sources with series resistors. (b) Effective resistive load R_{ac} to the tank circuit.

IV. Design of the Power Stage

A. Determination of R_{ac}

Let us assume that the LED load in Fig. 1 has M number of strings and each string has N number of LED units in series, as shown in Fig. 6(a).

If each unit has a dc "on-resistance" R_{ON} and forward voltage V_F, the average voltage V_o at the dc bus can be expressed as

follows:

$$V_o = NV_F + I_{\text{LED}} R_{\text{ON}} \left({}^{N}/_{M} \right). \tag{11}$$

The dc output power P_o of the LED can be written as follows:

$$P_o = V_o I_{\text{LED}} = \left(NV_F + I_{\text{LED}} R_{\text{ON}} \left({}^{N}/_{M} \right) \right) I_{\text{LED}}. \tag{12}$$

The LED current cannot be negative. Thus, from (12), the following expression of I_{LED} can be derived:

$$I_{\text{LED}} = \frac{-NV_F + \sqrt{\left(NV_F\right)^2 + 4P_o R_{\text{ON}} \left({}^{N}/_{M} \right)}}{2R_{\text{ON}} \left({}^{N}/_{M} \right)}. \tag{13}$$

The equivalent LED load can be represented as resistor R_{DC}, which can be expressed as follows:

$$R_{\text{DC}} = {}^{V_o}/_{I_{\text{LED}}}. \tag{14}$$

Using (11) in (14), the following expression of R_{DC} can be obtained:

$$R_{\text{DC}} = \frac{NV_F}{I_{\text{LED}}} + \left({}^{N}/_{M} \right) R_{\text{ON}}. \tag{15}$$

Now, applying the power balance concept with first harmonic approximation (FHA) [39] and using (13) and (15), the final expression of R_{ac} can be derived as follows:

$$R_{\text{ac}} = \frac{8}{\pi^2} \left({}^{N}/_{M} \right) R_{\text{on}} \left[\frac{1 + \sqrt{1 + \frac{(4R_{\text{on}} P_o)}{(MNV_F{}^2)}}}{-1 + \sqrt{1 + \frac{(4R_{\text{on}} P_o)}{(MNV_F{}^2)}}} \right]. \tag{16}$$

B. Derivation and Analysis of Current Transfer Ratio (G)

Analyzing the waveforms V_{AB} and V_{AC} in Fig. 6 using FHA, the RMS values of the respective fundamental components $V_{AB(01)}$ and $V_{AC(01)}$ are found to be

$$V_{AB(01)} = \frac{2\sqrt{2}V_{in}}{\pi} \quad \text{and,} \quad V_{AC(01)} = \frac{2\sqrt{2}V_o}{\pi}. \tag{17}$$

The voltage transfer ratio $|G_v|$ of the converter is

$$|G_v| = \frac{1}{\sqrt{1 + Q^2 \left(\frac{f_s}{f_r} - \frac{f_r}{f_s} \right)^2}}. \tag{18}$$

Finally, using (17) and (18), the current transfer gain, $|G|$ can be formulated as follows:

$$|G| = \frac{I_{\text{LED}}}{V_{\text{in}}} = \frac{8}{\pi^2} \frac{1}{R_{\text{ac}}} \frac{1}{\sqrt{1 + Q^2 \left(\frac{f_s}{f_r} - \frac{f_r}{f_s} \right)^2}} \tag{19}$$

where Q is the quality factor, f_s is the converter switching frequency, and f_r is the resonant frequency of the converter. The expression (19) represents the generalized transfer function of the SRC LED driver. For different Q values, a family of characteristic curves is plotted using MATLAB (see Fig. 7). Here, x denotes the normalized frequency given by, $x = f_s/f_r$ and it can be varied from 0 to 2. A suitable value for $Q(= Q_{\text{set}})$ needs to be chosen as Q_{max} from the family of curves in the inductive ($x > 1$) zone for maximum loading condition [shown in Fig. 7(a)]. For instance, $Q_{\text{set}} = 4.2$, which stands as the chosen Q_{max} for the system at maximum loading ($R_{\text{ac}} = R_{\text{ac(min)}} = 5\Omega$). The specific curve corresponding to Q_{max}, intersects the rated maximum gain $|G|_{\text{max}} (= 0.109)$ at $x = 1.089$. This value can be treated as x_{min}. Now, from the design perspective, the L_{link} and C_{link} are fixed. Then, Q can be shown varying inversely with R_{ac} as follows:

$$QR_{\text{ac}} = Q_{\text{set}} R_{\text{ac(min)}} = Z = \text{constant} \tag{20}$$

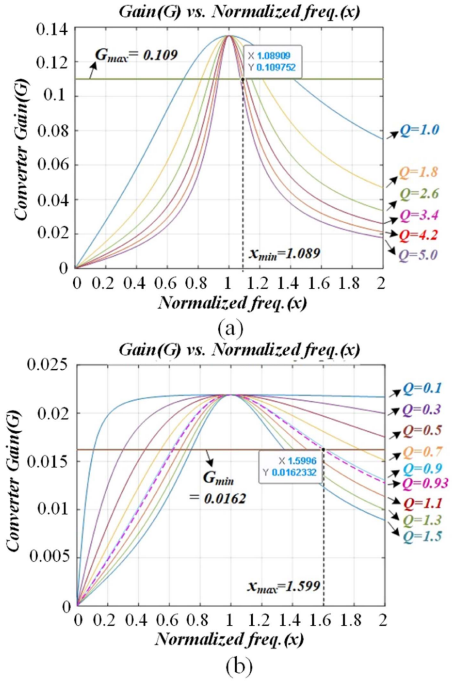

Fig. 7. Family of current transfer characteristics curves: (a) For maximum loading condition ($R_{\text{ac(min)}} = 5\Omega$). (b) For minimum loading condition ($R_{\text{ac(max)}} = 22.5\Omega$).

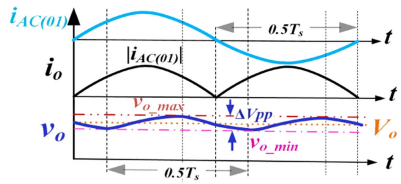

Fig. 8. Illustrative waveforms of different voltages and currents for output circuit. Bus voltage, v_o is developed across C_{out} when the fundamental component $i_{\text{AC(01)}}$ is rectified to obtain current output i_o.

where Z represents the characteristic impedance of the tank circuit. Using (20), the minimum value of $Q(= Q_{\text{min}} = 0.93)$ is obtained with $R_{\text{ac(max)}} = 22.5\,\Omega$ for minimum output loading. In Fig. 7(b), the value of $x_{\text{max}} = 1.599$ is obtained from the point of intersection of the dotted curve (corresponding to Q_{min}) with the minimum expected gain $|G|_{\text{min}} (= 0.0162)$. The $f_{\text{lim\_max}}$ is a fixed parameter, which is to be decided based on the hardware constraints during experimental validation. Hence, the expressions for f_r and $f_{\text{lim\_min}}$ can be written as follows:

$$f_r = \left(x_{\text{max}} \right)^{-1} f_{\text{lim\_max}} \tag{21}$$

$$f_{\text{lim\_min}} = x_{\text{min}} f_r. \tag{22}$$

C. Design of Output Filter C_{out}

The tank circuit effectively filters out the higher-order current harmonics and it is more sensitive to the fundamental component of ac-link current ($i_{\text{AC(01)}}$). This $i_{\text{AC(01)}}$ is rectified by the diode bridge to produce i_o, as shown in Fig. 8.

The ripple in i_o will be filtered out by the output capacitor C_{out}. The design guidelines reported in the literature are based on the allowable ripple current or ripple voltage at the output [40], [41]. When the ripple voltage criterion is considered, the expression

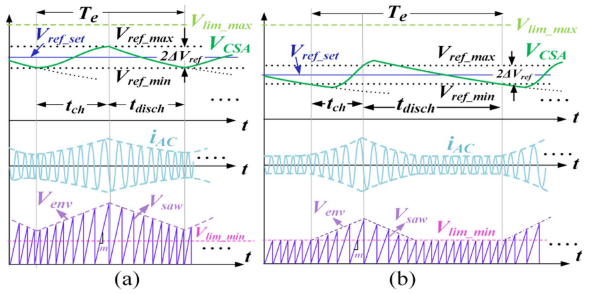

Fig. 9. Illustrative waveforms of V_{CSA} (green), i_{AC} (cyan), and V_{env} (purple) presenting the timing diagram. Effect of $2f_s$ ripple content in the sensed input V_{CSA} is ignored and the characteristic waveforms are portrayed: (a) At rated load or similar output condition ($t_{\text{ch}} \approx t_{\text{disch}}$). (b) At light load condition ($t_{\text{ch}} \neq t_{\text{disch}}$).

of C_{out} can be written as follows:

$$C_{\text{out}} = \frac{I_{\text{LED(max)}}\,(1-d)}{f_s \Delta V_{\text{pp}}}. \tag{23}$$

Considering the PFM control, the maximum value of C_{out} can be obtained with duty ratio, $d = 0.5$ and $f_s = f_{\text{lim\_min}}$.

V. Envelope Frequency and Control Slope Derivations and Thermal Effects Analysis

A. Determination of Envelope Frequency and Control Slope

The output filter capacitor C_{out} with the LED load (R_{DC}), can be approximated as a parallel RC network [see Fig. 6(a)]. In the presence of the bulk output capacitor C_{out}, the capacitive time constant outweighs the inductive time constant of the system and the first-order dynamics is effectively governed by the parallel RC circuit. Let the charging and discharging subintervals be t_{ch} and t_{disch}, respectively (see Fig. 9). Thus, the time period and frequency of V_{env} signal are given as follows:

$$T_e = t_{\text{ch}} + t_{\text{disch}} \quad \Rightarrow f_e = (t_{\text{ch}} + t_{\text{disch}})^{-1}. \tag{24}$$

During both charging and discharging, the LED current rises and falls exponentially and V_{CSA} follows the same profile within the hysteretic control band $2\Delta V_{\text{ref}}$. Thus, an expression related to the discharging subinterval can be established as follows:

$$V_{\text{ref\_min}} = V_{\text{ref\_max}} e^{-t_{\text{disch}}/\tau}. \tag{25}$$

Using (1) and (2), it can be simplified further as follows:

$$t_{\text{disch}} = \tau \ln\left\{\frac{I_{\text{LED}} + \Delta i_{\text{LED}}}{I_{\text{LED}} - \Delta i_{\text{LED}}}\right\}. \tag{26}$$

The above expression holds good throughout the entire load range of the proposed system irrespective of the input voltage V_{in}. At rated load and similar conditions, the ripple content ($2\Delta i_{\text{LED}}$) is small compared with the demand current I_{LED}. Since the V_{env} control signal plays well within the limits ($V_{\text{lim\_min}}$ and $V_{\text{lim\_max}}$), the rising and falling slopes of the envelope are almost the same. This implies that at rated load or similar output, the charging and discharging intervals are almost the same ($t_{\text{ch}} \approx t_{\text{disch}}$). Therefore, f_e can be approximated as follows:

$$f_e \approx 0.5\, t_{\text{disch}}^{-1}. \tag{27}$$

Now, based on the operating conditions (I_{LED} and V_{in}), the boundary frequencies $f_{\text{ref\_min}}$ and $f_{\text{ref\_max}}$ can be derived for the desired output load. Using (11) and (19), the following expressions for $f_{\text{ref\_min}}$ and $f_{\text{ref\_max}}$ can be obtained:

$$f_{\text{ref\_min}} = 0.5 f_r \left(A + \sqrt{A^2+4}\right) \tag{28}$$

$$f_{\text{ref\_max}} = 0.5 f_r \left(B + \sqrt{B^2+4}\right) \tag{29}$$

where the terms A and B represent the following:

$$A = \frac{8}{\pi^2}\frac{V_o}{(I_{\text{LED}} + \Delta i_{\text{LED}})}\sqrt{\frac{C_{\text{link}}}{L_{\text{link}}}\left\{\left(\frac{V_{\text{in}}}{V_o}\right)^2 - 1\right\}} \tag{30}$$

$$B = \frac{8}{\pi^2}\frac{V_o}{(I_{\text{LED}} - \Delta i_{\text{LED}})}\sqrt{\frac{C_{\text{link}}}{L_{\text{link}}}\left\{\left(\frac{V_{\text{in}}}{V_o}\right)^2 - 1\right\}}. \tag{31}$$

The value of slope m is known from (7) as discussed in Section III-B. Thus, from the symmetry consideration ($t_{\text{ch}} \approx t_{\text{disch}}$), the control slope m_e can be expressed as follows:

$$m_e = 2m f_e \left(f_{\text{ref\_min}}^{-1} - f_{\text{ref\_max}}^{-1}\right). \tag{32}$$

The above approximation is based on rated load or similar output conditions to estimate the worst-case value of m_e. However, at light load conditions, t_{ch} is not equal to t_{disch} and t_{ch} can be calculated using the limit $V_{\text{lim\_min}}$. It is observed that, at lightly loaded condition [see Fig. 9(b)], the control envelope V_{env} eventually hits the $V_{\text{lim\_min}}$ limit and the apparent symmetry in charging and discharging subintervals is lost. V_{env} gets limited at $V_{\text{lim\_min}}$ while falling with slope $-m_e$ and remains there till V_{CSA} hits $V_{\text{ref\_min}}$ to initiate the next cycle [see V_{CSA} and V_{env} traces of Fig. 9(b)]. Afterward, the envelope signal rises again (with slope $+m_e$) and the LED current (i_{LED}) increases while V_{CSA} reaches the $V_{\text{ref\_max}}$. The LED current still rises for some time as the excessive inductive energy (stored in L_{link}) freewheels through the output load and finally, V_{CSA} starts decaying exponentially. The phenomena are also observed while V_{CSA} hits $V_{\text{ref\_min}}$. V_{CSA} shortly dips below $V_{\text{ref\_min}}$ before it starts rising again as L_{link} stores inductive energy to deliver for the subsequent switching cycles in the upcoming subinterval t_{ch}. Thus, the peak-to-peak ripple increases in the LED current. However, the proposed controller is able to regulate the LED current at the desired demand value, even at light loads. For such conditions, the charging time (t_{ch}) is approximated by the following relation:

$$t_{ch} = \frac{V_{\text{lim\_min}}}{m_e}\left(\frac{f_{\text{lim\_max}} - f_{\text{ref\_min}}}{f_{\text{ref\_min}}}\right). \tag{33}$$

Now, expression of the discharging subperiod t_{disch} is already available from (26). Therefore, for light load conditions, f_e can be computed from (24) using (33) and (26).

Characteristics of the proposed envelope control scheme are portrayed in Fig. 10. Within the proposed operating frequency range (367–540 kHz), Fig. 10(a) illustrates the variation in the switching frequency f_s with the change in demand LED current I_{LED} and the input voltage V_{in}. The switching frequency f_s decreases with an increase in the output load current. However, at a fixed load demand, f_s increases with an increase in the input voltage V_{in}. Fig. 10(b) depicts the variation of envelope time period T_e with the demand current and input voltage at highly loaded conditions. It is observed that the variation in T_e with the change in V_{in} and load is insignificant.

B. Analysis of Thermal Effects

The LED parameters, such as the forward voltage V_F and the "on-resistance" R_{ON} are sensitive to junction temperature (T_j).

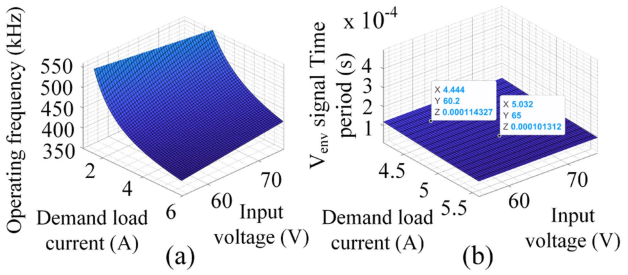

Fig. 10. Characteristic plots obtained at different LED demand current (I_{LED}) and input voltage (V_{in}): (a) Variation in operating frequency (f_s). (b) Variation in time period (T_e) of V_{env} envelope control signal at highly loaded conditions.

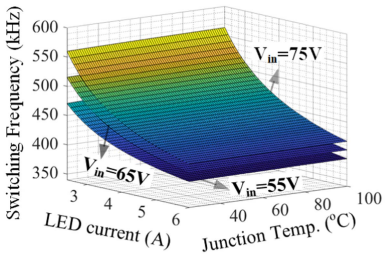

Fig. 11. Variation in switching frequency due to LED junction temperature variation.

From the LED datasheet [38], the expression of V_F for positive temperature change can be approximated as follows:

$$V_F\left(T_j\right) = V_F|_{(25^{\circ}\text{C})} + \Delta V_F\left(T_j\right). \tag{34}$$

The expression of $R_{\text{ac}}(T_j)$ can be written using (15) and (34) as follows:

$$R_{\text{ac}}\left(T_j\right) = \frac{8N}{\pi^2 M}\left[\frac{\left(V_F|_{(25^{\circ}\text{C})} + \Delta V_F\left(T_j\right)\right)}{I_F} + R_{\text{ON}}\left(T_j\right)\right]. \tag{35}$$

Thus, R_{ac} varies with temperature. To nullify the effect of this variation, the controller has to vary the frequency to maintain a constant LED current. Using (19), the switching frequency f_s can be expressed as follows:

$$f_s\left(T_j\right) = 0.5 f_r\left[A\left(T_j\right) + \sqrt{A(T_j)^2 + 4}\right] \tag{36}$$

where

$$A\left(T_j\right) = \frac{8}{\pi^2 Z}\left[\frac{1}{|G\left(T_j\right)|^2} - 1.522 R_{\text{ac}}(T_j)^2\right]. \tag{37}$$

Using (35) and (36), characteristics of the proposed scheme with varying junction temperature (from 25°C to 100°C) are demonstrated in Fig. 11 for different input voltages and LED currents. The plot shows that the switching frequency increases as the temperature increases. However, the change in switching frequency is around 2 kHz. Thus, from the gain plots in Fig. 7, it can be said that the controller can effectively regulate the LED current even with a change in electrical parameters due to a change in junction temperature.

VI. Experimental Validation

A. Hardware Setup

To validate the proposed control scheme experimentally, a 170 W-rated SRC LED driver prototype [see Fig. 12(a) and (b)] is designed with the parameter set given in Table I. An LED load board is also designed [see Fig. 12(c)], which includes 32 high-brightness white HB-LEDs. These are connected in eight parallel strings each having four units in series. The complete test-setup is shown in Fig. 12(d). A variable dc supply is used to deliver different input dc voltages to the SRC LED driver within the specified supply range (given in Table I). The dc supply emulates the double power frequency ripple voltage with peak-to-peak deviation ($\Delta V_{\text{in\_(pp)}}$) appearing over the base average dc voltage (V_{in}). This $\Delta V_{\text{in\_(pp)}}$ is adjusted to be within 10% of V_{in}.

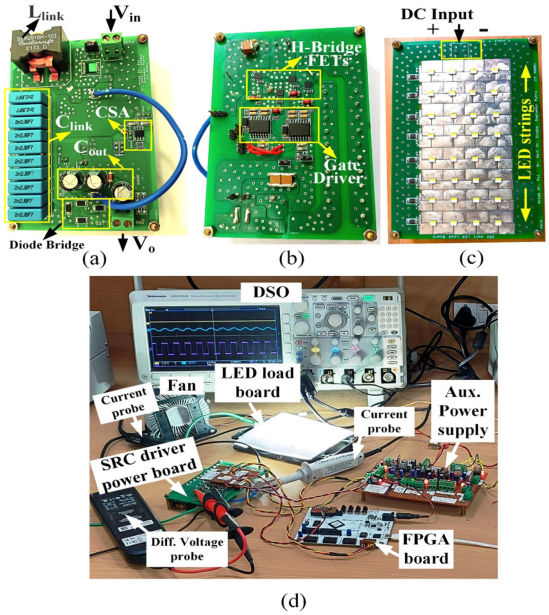

Fig. 12. SRC LED driver: (a) Top view of the SRC PCB board. (b) Bottom side view of the SRC PCB board. (c) LED load board. (d) Experimental test-setup of the SRC LED driver system.

TABLE I
Design Parameters

Parameters	Values
DC input voltage, V_{in}	55–75 V
Max output power, $P_{o(\text{max})}$	170 W
Max. LED current, $I_{\text{LED}(\text{max})}$	5.5 A
Operating frequency, f_s	367–540 kHz
Resonant frequency, f_r	338 kHz
Resonant inductor, L_{link}	10 μH
Resonant capacitor, C_{link}	22 nF
Output filter capacitor, C_{out}	660 μF
Devices	**Part no.**
MOSFETs	BSZ146N10LS5
Schottky diodes	VSS8D5M10
Current sensor	AD8429ARZ-R7
Current sense resistor, R_{sense}	22 mΩ
HBLEDs	KW3 CGLNM3.TK

The proposed control scheme is implemented using a Spartan 7 field-programmable gate array (FPGA) embedded on a development board from Digilent (ARTY S-7). The LED current is sensed using a CSR and an instrumentation amplifier (AD8429 series from Analog Devices) and an equivalent voltage V_{CSA} is produced. The in-built ADC of Spartan 7 is used to sample the sensed voltage V_{CSA}. The ADC samples at the rate of the switching frequency. However, to capture noise-free samples, a variable frequency sampling clock f_{sclk} is employed.

B. Calculation for Hardware Parameters

The ADC samples the signal V_{CSA}. As per the datasheet of the ADC, the peak input of 1 V can be applied. For safe operation, around 20% derating on the maximum input limit is considered here. Therefore, the ADC peak input limit, $V_{\text{CSA\_lim\_max}}$ can be same as $V_{\text{lim\_max}}$, shown in Fig. 5(a) as follows:

$$V_{\text{CSA\_lim\_max}} = V_{\text{lim\_max}} = 0.8V \tag{38}$$

where

$$V_{\text{lim\_max}} = V_{\text{ref\_set\_max}} + \Delta V_{\text{ref}}. \tag{39}$$

Now, (39) can be expressed in terms of known parameters $I_{\text{LED(max)}}$ and Δi_{LED} as follows:

$$V_{\text{lim\_max}} = 0.8 = (I_{\text{LED(max)}} + \Delta i_{\text{LED}})G_{\text{CSA}}. \tag{40}$$

The maximum average LED current and LED current ripple are chosen as 5.5 and 0.04 A, respectively. Using (40), the value of CSA gain G_{CSA} is obtained as 0.158. The hysteresis control-band regulates the envelope frequency f_e and the control slope m_e is adjusted to prevent any abrupt variation in switching frequency (f_s). Thus, the operating frequency can be restricted to a certain maximum limit ($f_{\text{lim\_max}}$) to reduce the converter losses and protect the proposed controller from EMI issues. Using (29) and (31), $f_{\text{lim\_max}} = 680$ kHz is calculated. However, considering the factors related to the system efficiency and the EMI signature, the maximum operating frequency is limited to around 540 kHz. Therefore, using (21) and (22), $f_{\text{lim\_min}}$ =368 kHz is obtained. From the ARTY S-7 board datasheet, the high-frequency clock is, f_{HF} =100 MHz. Thus, substituting (38) in (10), the value of d can be calculated as, $d = 0.0029$.

The switching frequency (f_s) can be calculated based on (19). Using (26) and (27), the value of envelope control frequency f_e is obtained as 9.17 kHz at $V_{\text{in}} = 65$ V and $I_{\text{LED}} = 5$ A. At the same operating condition, the experimental result of Fig. 13(b) shows that $f_e \approx$ 9.5 kHz. Therefore, the experimental V_{env} frequency shows good agreement with the calculation and can be confirmed from the envelope time period T_e obtained in the plot of Fig. 10(b). For hardware implementation, the value of m_e is obtained as 1580 from (32) and $f_{\text{ref\_min}} = 382.7$ kHz and $f_{\text{ref\_max}}$ = 415.8 kHz are calculated based on (28) and (29). Experimental results in Fig. 13(c) and (d) provide $f_{\text{ref\_max}}$ = 410 kHz and $f_{\text{ref\_min}}$ = 373.2 kHz, which are in close agreement with the values calculated from (28) and (29). This minor difference is present due to the discretization effect in the V_{env} and V_{saw}.

C. Hardware Results

The effectiveness of the proposed control technique is tested with the in-house prototype boards under different input voltages and loads. Fig. 14 shows the steady-state behavior of the SRC LED driver governed by the proposed control scheme at $V_{\text{in}} = 60$ V. Fig. 14(a) and (b) present zoomed views of the lowest and highest frequency portions, respectively, under the LED load current of 4.4 A. The blue trace shows the LED current i_{LED}, the magenta trace presents the pole-to-pole voltage V_{AB}, and the cyan trace depicts the ac link current i_{AC}. It is evident that the controller tracks the reference current accurately and maintains ZVS. Based on the instantaneous value of i_{LED}, the proposed PFM controller shifts i_{AC} from low to high frequency and vice versa. The envelope frequency f_e (for test case of Fig. 14) is measured to be around 8.6 kHz and it closely matches the corresponding value of $T_e = 114.3\,\mu$s, obtained from the

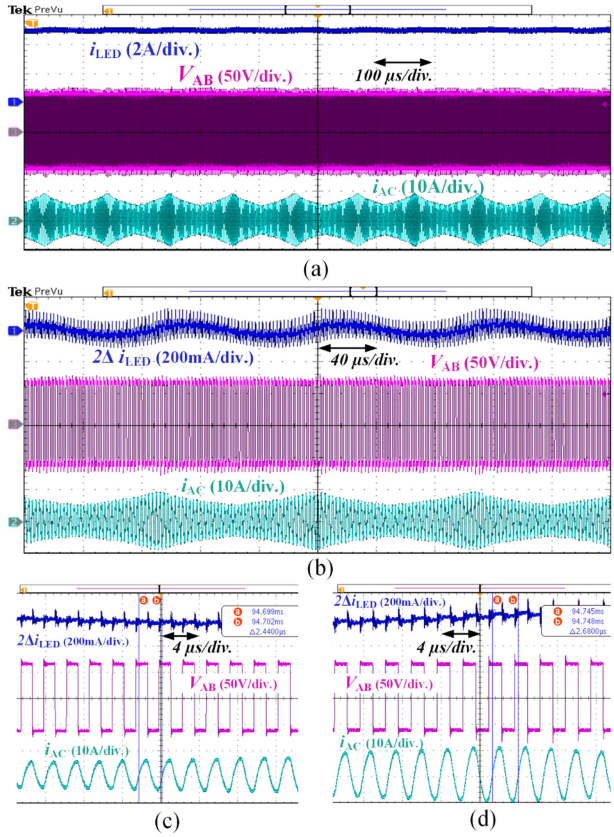

Fig. 13. Experimental test waveforms : (a) Steady-state performance of the proposed controller at $V_{\text{in}} = 65\ V$ and $I_{\text{LED}} = 5$ A. Time scale: 100 μs/div. Blue trace (2 A/div.) shows the LED current i_{LED}, the magenta trace (50 V/div.) presents the pole-to-pole voltage V_{AB}, and the cyan trace (10 A/div.) depicts the AC link current i_{AC}. (b) AC-coupled waveform of the LED current (blue trace, 200 mA/div.) illustrates the ripple content $2\Delta i_{\text{LED}}$. (c) Sectional view of a switching cycle with the minimum time period (representing $f_{\text{ref\_max}}$). (d) Sectional view of a switching cycle with the maximum time period (indicating $f_{\text{ref\_min}}$).

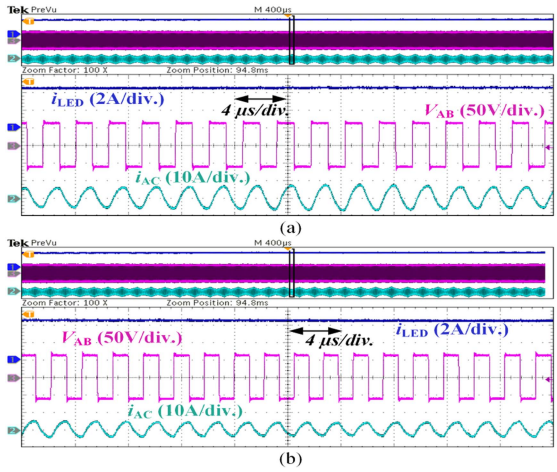

Fig. 14. Experimental waveforms at $V_{\text{in}} = 60\,V$ and $I_{\text{LED}} = 4.4$ A. Time scale: 4 μs/div. Blue trace (2 A/div.) shows the LED current, the magenta trace (50 V/div.) presents the pole-to-pole voltage V_{AB}, and the cyan trace (10 A/div.) depicts the AC link current i_{AC}. (a) Zoomed view of low-frequency region. (b) Zoomed view of high-frequency region.

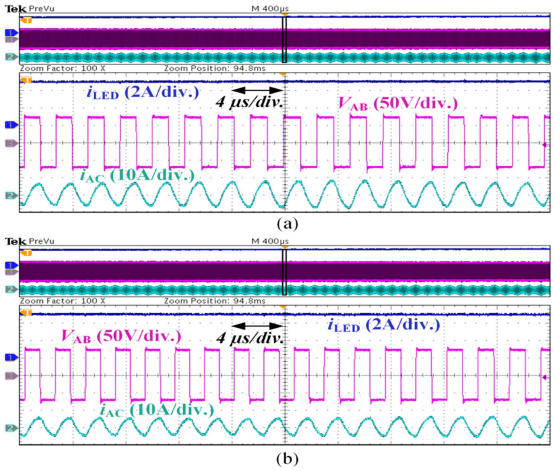

Fig. 15. Experimental waveforms at $V_{in} = 72\,V$ and $I_{LED} = 5$ A. Time scale: 4 μs/div. Blue trace (2 A/div.) shows the LED current, the magenta trace (50 V/div.) presents the pole-to-pole voltage V_{AB}, and the cyan trace (10 A/div.) depicts the AC link current i_{AC}. (a) Zoomed view of low-frequency region. (b) Zoomed view of high-frequency region.

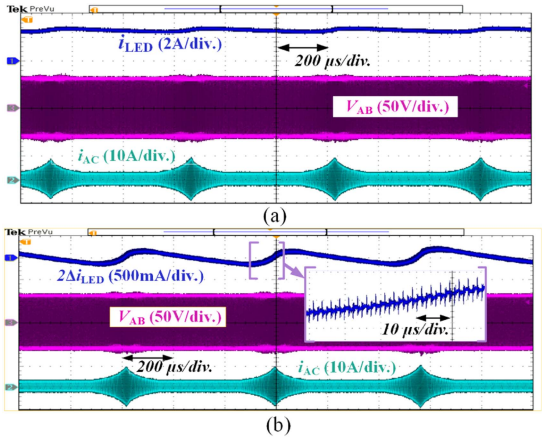

Fig. 16. Performance of the proposed controller under lightly loaded condition at $V_{in} = 60$ V and $I_{LED} = 2.4$ A. Time scale: 200 μs/div. Magenta trace (50 V/div.) shows pole-to-pole voltage V_{AB}, and the cyan trace (10A/div.) portrays AC link current i_{AC}. (a) Steady-state waveforms. Blue trace represents I_{LED} at 2 A/div. (b) AC-coupled LED ripple current (blue trace, 500 mA/div.). Close-up view of i_{LED} shown in inset (at timescale: 10 μs/div.).

plot of Fig. 10(b) under the same operating point. Thus, the experimental data is closely consistent with the calculated value. A similar kind of behavior is also observed in Fig. 15 with $V_{in} = 72$ V and $I_{LED} = 5$ A. Comparing Fig. 15 with Fig. 13(c) and (d), the frequency f_s has increased due to an increase in the input voltage. This is consistent with the plot presented in Fig. 10(a).

Fig. 16(a) illustrates the performance of the proposed scheme under light load condition at $V_{in} = 60\,V$ and $I_{LED} = 2.4\,A$. The ac-coupled LED current waveform under the same operating condition is shown in Fig. 16(b), which exhibits a peak-to-peak ripple $2\Delta i_{LED}$ of 0.32A (see blue trace, 500 mA/div.). The proposed envelope takes control action when V_{CSA} (sensed i_{LED} current) crosses the hysteretic limits of $2\Delta V_{ref}$ band. However, the Δi_{LED} ripple under light load condition appears to be higher than the preset limit of 0.04 A. This can be explained using the dynamics of V_{CSA} and V_{env} as illustrated in Fig. 9(b). The discharge duration t_{disch} is significantly higher than heavy load

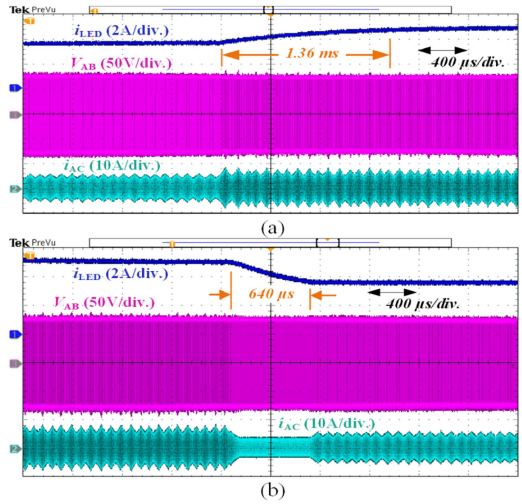

Fig. 17. Load transient performance of the proposed controller (from 3.8 to 5.5 A and vice versa) at $V_{in} = 75$ V. Time scale: 400 μs/div. Blue trace (2 A/div.) shows the LED current, the magenta trace (50 V/div.) presents the pole-to-pole voltage V_{AB}, and the cyan trace (10 A/div.) depicts the AC link current i_{AC}. (a) Load step-up transient. (b) Load step-down transient.

conditions, which causes V_{env} to hit the lower limit V_{lim_min}. At V_{lim_min}, due to very high switching frequency, the energy transfer from the input is negligible and the tank energy decreases exponentially. As the V_{CSA} hits the lower limit of the hysteresis band, the switching frequency starts increasing slowly. However, during this time, the energy supplied from the source is still less than the energy demand, which causes a further dip in LED current, as shown in Fig. 9(b). A similar phenomenon is also observed at the end of charging duration t_{ch} where the energy supplied from the source is more than the demand, which causes V_{CSA} to go beyond the upper limit of the hysteresis band. Due to these phenomena under light load conditions, the peak ripple is increased to 6.6%, whereas, at heavy load condition, it is just 1.4%. However, it is to be noted that the peak ripple current (Δi_{LED}) stays within the acceptable limits of around 10%–30% [30], [31], [32], [33].

The rising and falling of the envelope signal V_{env} will introduce a ripple in the LED current under both heavy and light load conditions. The frequency of this ripple under heavy load condition is around 10 kHz [see Fig. 13(b)] and under light load condition is around 2 kHz [see Fig. 16(b)]. Both these frequencies are beyond the human visual persistence range. Thus, this variation will not cause any flickering issue [42].

To assess the load transient performance of the proposed control scheme, the SRC LED driver is tested with a step change in reference current command from 3.8 to 5.5 A and vice-versa. Fig. 17(a) shows the load step-up transient performance of the proposed scheme. The LED current reaches to steady state at around 1.36 ms. Also, it can be observed that as the reference load command changes, the controller changes the pattern of frequency variation (see cyan trace i_{AC} of Fig. 17). Fig. 17(b) shows the load step-down transient performance of the proposed scheme. The LED current reaches to steady state after 640 μs. Similar to the load step-up transient, the controller changes the envelope control frequency [see cyan trace i_{AC} of Fig. 17(b)].

Using the extended describing function-based approach [43], the control-to-output characteristics of the SRC can be obtained

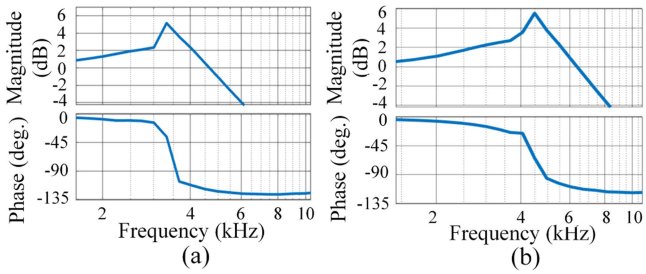

Fig. 18. Frequency response of the proposed PFM-based control system. (a) $V_{in} = 75$ V, $I_{LED} = 3.8$ A. (b) $V_{in} = 75$ V, $I_{LED} = 5.5$ A.

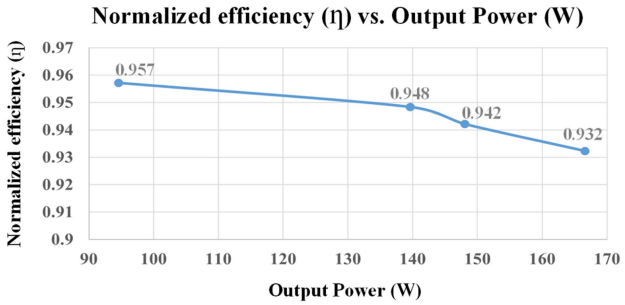

Fig. 19. Efficiency of the SRC LED driver governed by the proposed control scheme.

as a third-order transfer function. However, due to the incorporation of a hysteretic controller, the system's behavior near gain crossover frequency can be approximated as a first-order system [44]. Using the MATLAB Model Linearizer toolbox, the frequency response of the SRC along with the proposed controller is obtained in simulation at $V_{in} = 75$ V, with two different LED currents $i_{LED} = 3.8$ A and $i_{LED} = 5.5$ A and the responses are shown in Fig. 18. In low load current ($i_{LED} = 3.8$ A) condition, the bandwidth is around 4 kHz, and the bandwidth increases to 6 kHz when the LED current increases to 5.5 A. However, in both these cases, the impact of tank dynamics is insignificant as the system's behavior can be approximated to a first-order system near the gain crossover frequency. Similar phenomena are observed in the load transient response of the experimental set-up shown in Fig. 17.

The efficiency of the SRC LED driver under the proposed control scheme is also measured and plotted in Fig. 19. A maximum efficiency of 95.72% is obtained at around 95 W and 93.2% efficiency is achieved for about 167 W output.

D. Comparison With State-of-the-Art Techniques

The features of the proposed PFM-based controller are compared with the existing LED drivers and the comparison data are provided in Table II. It is evident that the reported methods ([6], [30], [32], and [37]) involved digital implementation of single loop current-mode control and utilized at least one PI compensator in the loop. The digital implementation of closed-loop control in a resonant converter needs different blocks, such as a PI or similar controller block, PWM block, dead-time block, PFM block, etc. An FPGA-based implementation of these different components utilizes LUT, DFF, and DSP [26], [27], [28], [29]. Among these blocks, the PI controller exploits most of the LUTs, DFFs, and DSPs. A standard PI controller when discretized using the backward Euler technique

TABLE II
COMPARATIVE OVERVIEW IN TERMS OF RESOURCES

Parameters	Proposed	[6]	[30]	[32]	[37]
Type of power topology used	FBSRC	AHB-SRC	Boost+ HB-SRC	SC-HB	Boost+ HB-SRC
Type of control	Digital	Digital	Digital	Digital	Digital
No. of control loops	1	1	1	1	1
No. of ADCs used	1	1	1	1	1
No. of sensor(s)	1	1	1	2	1
Sensed parameter(s)	o/p DC load current	o/p DC bus current	o/p DC load current	o/p DC load current	o/p DC bus current
No. of PI controllers	0 (zero)	1	1	1	1
Modulation Technique	PFM	PSM	PWM	VFC	VFC

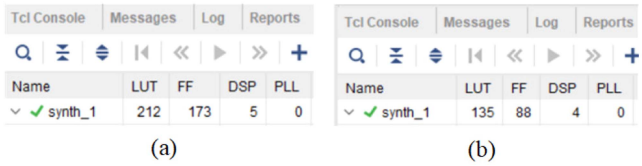

Fig. 20. Digital resource utilization data shown in Xilinx Vivado ISE: (a) Resources utilized by a single PI controller implemented using the backward Euler algorithm on FPGA. (b) Resources utilized by the whole closed-loop code of the proposed PFM controller implemented on FPGA.

TABLE III
PERFORMANCE COMPARISON WITH THE PROPOSED SYSTEM

Parameters	Proposed	[30]	[31]	[33]
Peak LED current ripple (At full load)	1.4 %	26 %	20 %	10 %
Max. o/p power (W)	170	100	145	102.96
Switching frequency (kHz)	367–540	47	100	65–200
Peak efficiency(%)	95.7	92	94.96	93.1

needs 212 LUTs, 173 DFFs, and 5 DSPs [see Fig. 20(a)], whereas, the closed loop code for the proposed PFM controller exploits fewer digital resources [shown in Fig. 20(b)]). Similarly, in a microcontroller-based implementation, a PI controller uses a significant amount of digital resources. In [45], two simple PI controllers were used for average current mode control implementation in a microcontroller (TMS320F28335 from Texas Instruments) and these two controllers used 50% of the total memory used by the whole closed-loop code. Thus, it is evident that the proposed digital controller can save a significant amount of digital resources by not using any PI controller. This enables the designer to implement this controller in a low-cost FPGA/microcontroller, which can significantly reduce the closed-loop controller implementation cost.

Table III compares the performance of the proposed controller with the other LED drivers of similar power ratings [30], [31], [33]. At rated full load, the proposed controller exhibits the lowest peak ripple (1.4%) compared with the other controllers. Furthermore, the proposed controller delivers the highest peak efficiency (95.7%) among the four controllers.

The load transient performance of the proposed controller is compared with the controller reported in [10] and the comparison study is presented in Table IV. During load step-up and load step-down of 1.7 A, the proposed controller exhibits settling times of 1.36 and 0.64 ms, respectively [see Fig. 17(a) and b)]. Clearly, the proposed controller outperforms the dynamics of the reported controller.

Table V compares the load transient performance of the proposed controller with [32]. Due to the constraints in component ratings, the proposed controller is rather simulated using

TABLE IV
PERFORMANCE COMPARISON WITH [10]

Controller	L_{link} (μH)	C_{link} (nF)	f_s (kHz)	Load step (A)	Settling time (ms)	
					Step up	Step down
PWM [10]	23.5	27	200	0.8	1	NP*
Proposed	10	22	367–540	1.7	1.36	0.64

(NP* : Not Provided.)

TABLE V
PERFORMANCE COMPARISON AT $V_{\text{IN}} = 24\text{V}$ AND $V_o = 6\text{V}$

Controller	L_{link} (μH)	C_{link} (nF)	f_s (kHz)	Load step (A)	Settling time (ms)	
					Step up	Step down
VFCCC [32]	22	47	50	3	1	1
Proposed	10	22	367–540	3	0.45	0.5

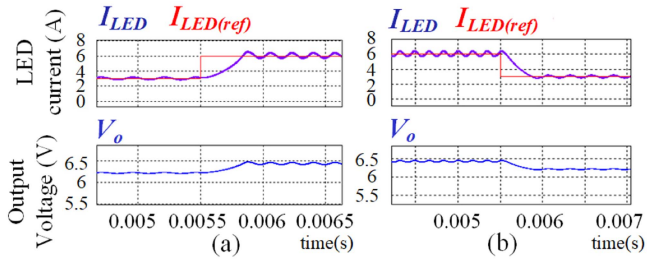

Fig. 21. Load transient performance of the proposed controller in simulation environment with the operating condition of [32]: (a) For load step up. (b) For load step down.

TABLE VI
PERFORMANCE COMPARISON AT $37V \leq V_{\text{IN}} \leq 48V$, $V_o = 22.5V$, AND $I_o = 1A$

Controller	L_{link} (μH)	C_{link} (nF)	f_s (kHz)	i/p volt. step (V)	Settling time (ms)	
					Step up	Step down
APWM [9]	88	10	200	11	40	40
Proposed	16	13.5	367–540	11	0.5	0.5

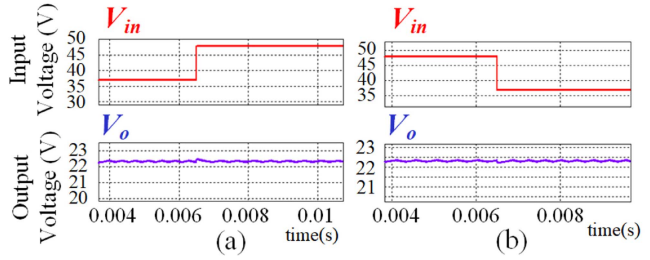

Fig. 22. Input voltage transient performance of the proposed controller in simulation environment with the operating condition of [9]. (a) Input voltage step up. (b) Input voltage step down.

PSIM software under the specific test conditions ($v_{\text{in}} = 24V$ and $V_o = 6V$) mentioned in [32]. For a 3 A load step up/down, the proposed controller exhibits settling times of 0.45 and 0.5 ms, respectively [see Fig. 21(a) and (b)]. Evidently, the proposed controller demonstrates a better transient performance.

The proposed controller is further tested on PSIM software under a step change in input voltage as reported in [9]. The comparison shows that [given in Table VI and Fig. 22(c) and (d)] the proposed controller exhibits a significantly improved transient performance.

Thus, the experimental and simulation results establish the improvements achieved using the proposed controller.

VII. CONCLUSION

This article has proposed a fully digital PFM technique for the SRC-based LED driver. The proposed PFM scheme's frequency change is managed by a hysteretic current regulator using an envelope signal controlled by a hysteresis band. A sawtooth wave is compared with the envelope signal to generate variable frequency pulses. The proposed scheme senses only the LED load current for closed-loop implementation. Moreover, it functions well without requiring the assistance of any PI controller. Therefore, the proposed scheme is simple, cost-effective, and utilizes less digital resources. Furthermore, the proposed scheme can handle a wide range of variations in load as well as in input voltage without losing ZVS. The design of different components of the proposed digital controller and power stage has been discussed thoroughly. The accuracy of the proposed scheme in tracking the reference current has been demonstrated using in-house SRC and LED load boards. The proposed control scheme can be easily extended for other resonant converters used in LED or similar applications.

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