The Active Gate Driver Based on Hardware Closed-Loop Control for Crosstalk Suppression of SiC MOSFETs With Kelvin-Source Connection

Mingkai Cui, Lei Chen, Yulong Pei, and Feng Chai, *Member, IEEE*

***Abstract*—Silicon carbide (SiC) MOSFETs with Kelvin-source connection are widely used in power converters based on a bridge configuration circuit, but crosstalk significantly impacts reliability and limits their application potential. For this problem, this article presents an active gate driver (AGD) based on hardware closed-loop control. A simple hardware closed-loop controller is designed to regulate the gate-source voltage of SiC MOSFETs. For aspect one, the closed-loop structure can reduce the peak voltage of crosstalk online. For aspect two, since the closed-loop structure can ensure the convergence of the gate-source voltage, a higher drive voltage is then permitted to shorten switching time and power loss. Compared with conventional methods, the proposed AGD can suppress crosstalk without adding switching loss. Experimental results verify the superiority of the proposed AGD for the SiC MOSFET-based bridge configuration circuit.**

***Index Terms*—Active gate driver (AGD), crosstalk suppression, SiC MOSFET, switching loss, switching transients.**

I. Introduction

THE rapid advancement in wide-bandgap power devices has facilitated high-frequency operation, which is poised to reshape next-generation power electronics converters. Among them, silicon carbide (SiC) MOSFETs stand out with their exceptional features such as fast switching speed, high power density, and low switching loss. These attributes draw significant attention from both academic and industrial domains [1], [2], [3], [4]. However, in SiC MOSFET based bridge configuration, the rapid voltage changes (*dv*/*dt*) during the fast switching transients of one SiC MOSFET can influence its complementary SiC MOSFET. This interaction between two switches is known as crosstalk [5]. The presence of crosstalk in the SiC MOSFET bridge configuration can lead to spurious turn-ON, increased switching loss, and reduced device lifetime. Thus, crosstalk is a critical element for the power converters based on SiC MOSFETs. Several strategies for crosstalk suppression have been proposed, categorized into three groups based on their principles: decreasing the *dv*/*dt*, applying negative turn-OFF gate voltage, and decreasing the gate-source drive path impedance [6].

In the first category, reducing the *dv/dt* can lower the current through Miller capacitor of SiC MOSFET, thereby suppressing crosstalk. However, reducing the *dv/dt* by slowing down the switching process hinders the full utilization of SiC MOSFET and increases switching loss [7], [8]. An active gate driver (AGD) for improving SiC MOSFET switching trajectory is proposed to reduce *dv*/*dt* without sacrificing switching loss [9]. However, the AGD is an open-loop control system and its control strategy is based on the data measured offline. The control performance may vary when temperature or working condition changes. Considering that the switching time for SiC MOSFET is as short as tens of nanoseconds, the closed-loop control in the switching transition based on a digital processor for SiC MOSFET is difficult to realize. The digital processor needs to operate at a high sampling rate and processing speed [10]. A high-performance FPGA is used to sample the switching transient of SiC MOSFET, and a gate driver can change the output voltage in different switching stages to reduce *dv*/*dt* [11]. However, this method requires the digital processor to sample at a very high speed, increasing costs greatly. Soft-switching can realize zero-voltage switching, resulting in *dv/dt* reduction [12], [13]. However, soft-switching is not suitable for applications with changing operating conditions such as motor control.

For the second category, imposing negative turn-OFF gate-source voltage can reduce the risk of spurious turn-ON at the moment of positive crosstalk. However, due to the low minimum allowable gate-source voltage, imposing negative turn-OFF gate-source voltage cannot fully suppress positive crosstalk and may result in overstress of the negative gate-source voltage of SiC MOSFET when negative crosstalk occurs. Even in a short period of time, the overstress could cause an increase in ON-state resistance and a reduction in the lifetime of SiC MOSFET [14], [15]. A level shifter is proposed to generate negative turn-OFF gate-source voltage in [16] and [17]. However, the required negative voltage may exceed the minimum allowable gate-source voltage of SiC MOSFET. Moreover, it is difficult to select the value of negative turn-OFF gate-source voltage due to oscillation caused by parasitic parameters [18], [19].

For the third category, decreasing the impedance of the gate-source drive path can reduce the amplitude of crosstalk.

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The authors are with the School of Electricarical Engineering and Automation, Harbin Institute of Technology, Harbin 150001, China (e-mail: 22b906011@stu.hit.edu.cn; hitchenlei@hit.edu.cn; peiyulong@hit.edu.cn; chaifeng@hit.edu.cn).

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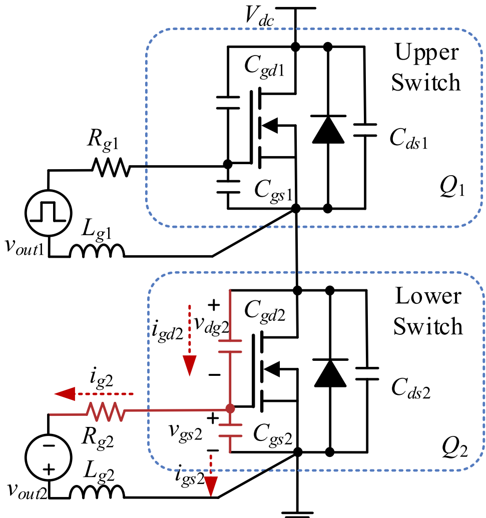

Fig. 1. Structure of conventional SiC MOSFET gate driver.

In [5], additional transistors are used between the gate-source terminals to short the Miller current when the amplitude of crosstalk exceeds the clamping threshold. However, the induced gate-source voltage needs to be predicted and detected. Also, the topology is complex, resulting in decreased reliability. Miller clamping can be employed to suppress the positive crosstalk. However, the negative spikes of gate-source voltage may be introduced during the process of Miller clamping which may result in the overstress of the negative gate-source voltage of SiC MOSFET [20]. In addition, adding auxiliary capacitors at the gate-source of SiC MOSFET can effectively suppress crosstalk, but this method delays the switching speed, as well as increases the switching loss [21].

Therefore, it is still challenging to suppress the crosstalk without sacrificing other performance of SiC MOSFET or introducing complex topology. For SiC MOSFET, Kelvin-source-based connection is commonly utilized in power converters [22]. To suppress the crosstalk of this structure, an AGD based on hardware closed-loop control is proposed. The contribution of this article lies in the following aspects.

1) Positive and negative crosstalk is effectively suppressed, which can prevent spurious turn-ON and improve lifetime of SiC MOSFET.
2) Higher voltage power supply is utilized, combined with the control effect of AGD, resulting in a reduction in switching loss of SiC MOSFET.

II. Defects of Conventional Gate Driver With Auxiliary Capacitors

A. Mechanism of Crosstalk Generation

The typical structure of bridge configuration based on SiC MOSFETs with conventional gate drivers (CGDs) is shown in Fig. 1. Q_1 and Q_2 represent the upper and lower SiC MOSFETs respectively. C_{gdn}, C_{gsn}, and C_{dsn} represent the junction capacitances of SiC MOSFETs, R_{gn} represents drive resistance, and L_{gn} represents parasitic inductance in the drive loop (where $n = 1, 2$. "1" represents the upper and "2" represents the lower). $V_{\rm dc}$ represents the voltage of dc-link.

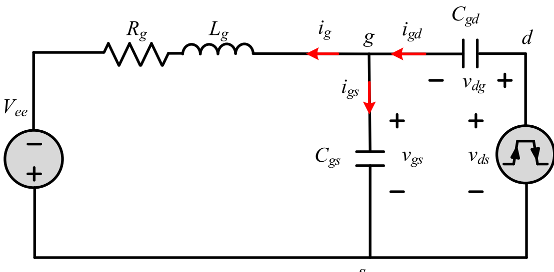

Fig. 2. Equivalent circuit of SiC MOSFET gate driver.

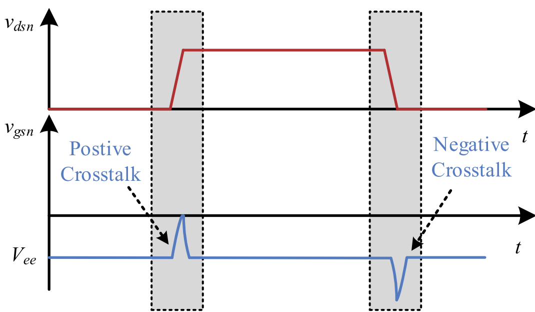

Fig. 3. Schematic waveforms showing crosstalk generation.

The equivalent circuit of the CGD, when crosstalk occurs, is shown in Fig. 2. The relationship between gate driver output voltage $v_{\rm out}$ and gate-source voltage of SiC MOSFET v_{gs} can be expressed as

$$v_{\rm out}\,(t) = R_g i_g(t) + L_g \frac{di_g(t)}{dt} + v_{gs}(t) \tag{1}$$

where i_g represents the output current of SiC MOSFET gate driver and $v_{\rm out}$ is numerically equal to the turn-OFF voltage V_{ee}.

By applying the Kirchhoff's voltage and current law, drain-source voltage v_{ds} and Miller current i_{gd} can be expressed as

$$v_{ds}(t) = v_{dg}(t) + v_{gs}(t) \tag{2}$$

$$i_{gd}(t) = i_g(t) + i_{gs}(t) \tag{3}$$

where i_{gs} represents the gate-source current of SiC MOSFET.

Miller current i_{gd} and gate-source current i_{gs} can be expressed as

$$i_{gd}(t) = C_{gd} \frac{dv_{dg}(t)}{dt} \tag{4}$$

$$i_{gs}(t) = C_{gs} \frac{dv_{gs}(t)}{dt}. \tag{5}$$

Substituting (2), (3), (4), and (5) into (1), the expression of crosstalk voltage can be calculated as

$$\Delta v_{gs}(t) + R_g C_{iss} \frac{d\Delta v_{gs}(t)}{dt} + L_g C_{iss} \frac{d^2 \Delta v_{gs}(t)}{dt^2} = R_g C_{gd} \frac{dv_{ds}(t)}{dt} + L_g C_{gd} \frac{d^2 v_{ds}(t)}{dt^2} \tag{6}$$

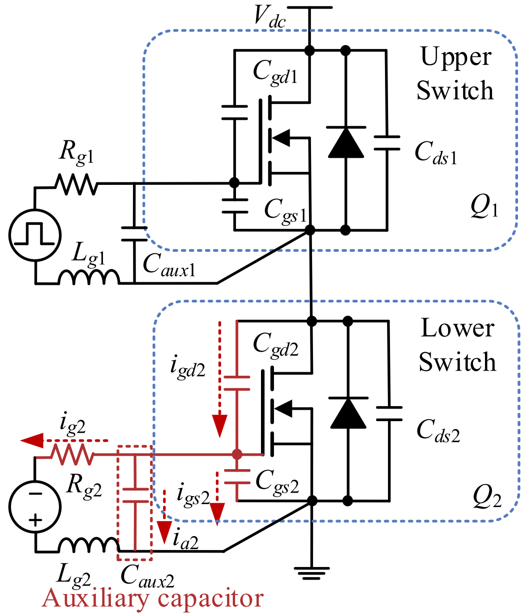

Fig. 4. Structure of conventional gate driver with auxiliary capacitors.

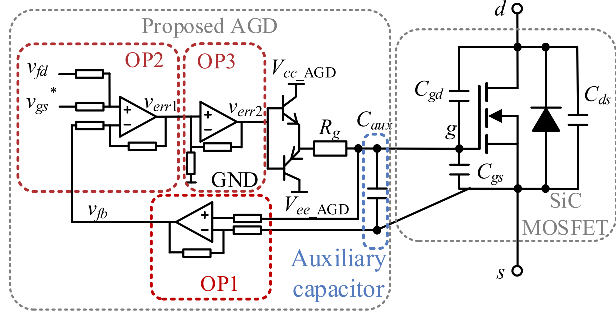

Fig. 5. Overall structure of proposed AGD.

where Δv_{gs} is the change amplitude of gate-source voltage affected by crosstalk and C_{iss} is the input capacitance, which can be expressed respectively as

$$\Delta v_{gs} = V_{ee} - v_{gs}$$
$$C_{iss} = C_{gd} + C_{gs}.$$

It can be observed from (6) and Fig. 2 that Δv_{gs} is primarily determined by the rate of change of drain-source voltage, dv_{ds}/dt as shown in Fig. 3. During the turn-ON process of SiC MOSFET, the rising drain-source voltage results in positive Miller current flowing through the Miller capacitance and gate resistance of the complementary SiC MOSFET, leading to a positive spike in gate-source voltage of the complementary SiC MOSFET. If the positive spike voltage exceeds the threshold voltage of SiC MOSFET, it may cause spurious turn-ON of SiC MOSFET. Similarly, during the turn-OFF process of SiC MOSFET, there will be a negative spike in gate-source voltage of complementary SiC MOSFET. If the negative spike is lower than the minimum allowable gate-source voltage of SiC MOSFET, it may cause a lifetime reduction of SiC MOSFET.

B. Analysis on Energy Loss of Conventional Gate Driver With Auxiliary Capacitors

Conventional gate driver with auxiliary capacitors (CGDACs) can effectively suppress crosstalk [23]. The addition of auxiliary capacitors between the gate and source of the SiC MOSFET, as shown in Fig. 4, results in diversion of Miller current through the auxiliary capacitors. Consequently, this leads to a reduction in crosstalk amplitude.

The turn-ON process of SiC MOSFET with CGDAC is typically divided into four stages, including turn-ON delay stage, current rising stage, voltage falling stage, and gate remaining charging stage. During the turn-ON transient, the switching loss of SiC MOSFET mainly occurs in current rising stage and voltage failing stage. This can be expressed as [24]

$$E_{\text{on_}di_l/dt} = \frac{1}{2} \cdot I_L \cdot V_{\text{dc}} \cdot \frac{I_L}{|di_{ds}/dt|} \tag{7}$$

$$E_{\text{on_}dv/dt} = \frac{1}{2} \cdot I_L \cdot V_{\text{dc}} \cdot \frac{V_{\text{dc}}}{|dv_{ds}/dt|} \tag{8}$$

$$E_{\text{on}} = E_{\text{on_}dI_L/dt} + E_{\text{on_}dv/dt} \tag{9}$$

where $E_{\text{on_}di_l/dt}$ is the energy loss in current rising stage, $E_{\text{on_}dv/dt}$ is the energy loss in voltage falling stage, E_{on} is total loss of turn-ON transient, and I_L is load current of SiC MOSFET.

The current slope and voltage slope can be calculated as [25]

$$|di_{ds}/dt| = \frac{V_{cc} - (0.5I_L/g_m + V_{th})}{R_g C_t/g_m + L_g} \tag{10}$$

$$|dv_{ds}/dt| = \frac{V_{cc} - V_{\text{miller}}}{C_{gd} R_g} \tag{11}$$

where V_{cc} is the positive power supply voltage of SiC MOSFET gate driver, V_{th} is the threshold voltage of SiC MOSFET, g_m is the transconductance of the SiC MOSFET, and C_t is the total gate-source capacitor which can be expressed as

$$C_t = C_{gs} + C_{gd} + C_{\text{aux}}.$$

By substituting (10) into (7), and substituting (11) into (8), the losses in the current rising stage and voltage falling stage can be respectively calculated as

$$E_{\text{on_}di_l/dt} = \frac{1}{2} \cdot I_L \cdot V_{\text{dc}} \cdot \frac{I_L R_g C_t/g_m + L_g}{V_{cc} - (0.5I_L/g_m + V_{th})} \tag{12}$$

$$E_{\text{on_}dv/dt} = \frac{1}{2} \cdot I_L \cdot V_{\text{dc}} \cdot \frac{V_{\text{dc}} C_{gd} R_g}{V_{cc} - V_{\text{miller}}}. \tag{13}$$

It can be seen from (9) and (12) that the addition of auxiliary capacitors increases the loss in the turn-ON process. Similarly, it also increases energy loss in the turn-OFF process. Therefore, CGDAC is incapable of attaining the optimal balance between switching loss and crosstalk suppression.

III. Proposed AGD and Operation Mechanism

The AGD based on hardware closed-loop control is proposed in response to the problems analyzed in Section II, as shown in

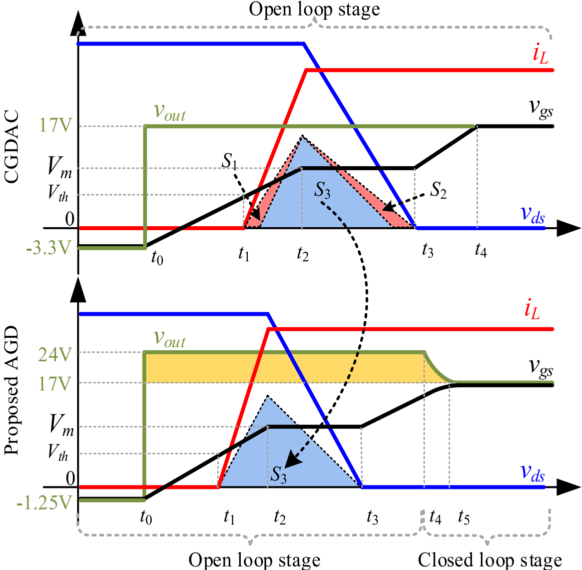

Fig. 6. Turn-ON waveforms of SiC MOSFET with proposed AGD.

Fig. 5. The proposed AGD can effectively enhance two aspects of performance by the hardware closed-loop structure.

1) Higher voltage power supply is utilized, combined with voltage regulation mechanism of the closed-loop controller, resulting in a reduction of switching loss.
2) Crosstalk is suppressed which can prevent spurious turn-ON and improve lifetime of SiC MOSFET.

The proposed AGD consists of two main paths: a feedback path and a feedforward path. In the feedback path, operational amplifier 1 (OP1) converts the gate-source voltage of SiC MOSFET into a feedback signal, v_{fb}. OP2 subtracts the given signal v_{gs}^* from the feedback signal v_{fb} to derive an error signal v_{err1}. OP3 amplifies the error signal v_{err1} to v_{err2}. In the feedforward path, the feedforward signal v_{fd} is introduced to realize the comprehensive suppression of crosstalk, the selection and design of this feedforward signal will be described in Section III-B.

A. Switching Loss Reduction Mechanism of Proposed AGD

For aspect 1, it can be seen from (12) and (13), the switching loss of SiC MOSFET with CGDAC can be reduced by increasing power supply voltage, V_{cc}. However, due to the low maximum allowable gate-source voltage of SiC MOSFET, increasing the power supply voltage may result in a reduction of its lifetime or potential damage. Moreover, since there is no closed-loop control in CGDAC, the output voltage in the switching process cannot be adjusted. Thus, the output voltage in the whole process needs to be set lower than the maximum allowable gate-source voltage of SiC MOSFET. In the proposed AGD, the output voltage can be dynamically adjusted through closed-loop control, which break the limit of maximum allowable gate-source voltage in the opening process and improve the switching speed. It can be seen from Fig. 6 that from moment t_0 to moment t_4, the power supply of proposed AGD, V_{cc_AGD}, is set higher than the power supply of CGD and CGDAC to accelerate the switching speed. After moment t_4, the closed-loop controller adjusts the output accordingly to ensure a suitable gate-source voltage. Subsequently, the specific switching process based on AGD will be analyzed.

The turn-ON process of SiC MOSFET based on the proposed AGD can be divided into five stages, as illustrated in Fig. 6. including turn-ON delay stage (t_0-t_1), current rising stage (t_1-t_2), voltage falling stage (t_2-t_3), gate-source remaining charging stage (t_3-t_4) and gate-source voltage closed loop stage (t_4 to next turn-OFF process). In Fig. 6, the areas of regions S_1, S_2, and S_3, respectively, represent the loss reduction of SiC MOSFET with AGD during the current rising stage, the loss reduction of SiC MOSFET with AGD during the voltage falling stage, and the total loss of SiC MOSFET with AGD during the turn-ON process. The sum of the areas of S_1, S_2, and S_3 is equal to the total loss of SiC MOSFET with CGDAC during the turn-ON process.

1) Turn-On Delay Stage (t$_0$-t$_1$)*:* At t_0, the voltage of gate-source v_{gs} is gate-source turn-OFF voltage of AGD, $v^*_{gs(\text{turn-off})}$, and the amplified error is shown as

$$k_{\text{err}} \cdot v_{\text{err1}} = k_{\text{err}} \cdot (v^*_{gs(\text{turn-on})} - v^*_{gs(\text{turn-off})}) \tag{14}$$

where k_{err} is gate-source voltage error amplifier coefficient and $v^*_{gs(\text{turn-on})}$ is gate-source turn-ON voltage of AGD.

The k_{err} is designed to satisfy

$$k_{\text{err}} \cdot (v^*_{gs(\text{turn-on})} - v^*_{gs(\text{turn-off})}) > V_{cc_\text{AGD}} \tag{15}$$

where V_{cc_AGD} is the positive power supply voltage of the AGD.

The amplified error is larger than the positive power supply voltage of operational amplifiers OP2 and OP3, causing saturation in these two operational amplifiers. Thus, the output of OP3 v_{out} is

$$v_{\text{out}}(t) = V_{cc_\text{AGD}}. \tag{16}$$

In this stage, the gate-source voltage is in open-loop state due to the saturation of the operational amplifiers OP2 and OP3. Thus, the gate-source circuit of SiC MOSFET is a typical second-order system, $v_{gs}(t)$ can be calculated as

$$v_{gs}(t) + R_g C_t \frac{dv_{gs}(t)}{dt} + L_g C_t \frac{d^2 v_{gs}(t)}{dt^2} = V_{cc_\text{AGD}}. \tag{17}$$

According to (23), the $v_{gs}(s)$ in frequency domain can be obtained by Laplace transformation, which is shown as

$$v_{gs}(s) = \frac{V_{cc_\text{AGD}} \cdot \frac{1}{s} + v_{gs}(t_0)(L_g C_t s + R_g C_t) + L_g C_t v'_{gs}(t_0)}{L_g C_t s^2 + R_g C_t s + 1} \tag{18}$$

where $v_{gs}(t_0)$ is the gate-source voltage at t_0, and $v'_{gs}(t_0)$ is value of the derivative of v_{gs} at moment t_0.

2) Current Rising Stage (t$_1$-t$_2$)*:* When the gate-source voltage of SiC MOSFET reaches the threshold voltage, V_{th}, at t_1, the amplified error is still higher than V_{cc_AGD} and the output voltage of gate driver is V_{cc_AGD}. Thus, $v_{gs}(s)$ can be calculated as

$$v_{gs}(s) = \frac{V_{cc_\text{AGD}} \cdot \frac{1}{s} + v_{gs}(t_1)(L_g C_t s + R_g C_t) + L_g C_t v'_{gs}(t_1)}{L_g C_t s^2 + R_g C_t s + 1} \tag{19}$$

where $v_{gs}(t_1)$ is the gate-source voltage at t_1, and $v'_{gs}(t_1)$ is value of the derivative of v_{gs} at moment t_0.

In this stage, the drain-source current, i_{ds}, begins to rise. The slope of i_{ds} during this process is shown as

$$|di_{ds}/dt| = \frac{V_{cc_AGD} - (0.5I_L/g_m + V_{th})}{R_g C_t/g_m}. \quad (20)$$

3) Voltage Falling Stage (t$_2$-t$_3$)*:* When the gate-source voltage of SiC MOSFET reaches the Miller stage voltage, the drain-source voltage, v_{ds}, begins to drop, the slope of v_{ds} can be calculated as

$$|dv_{ds}/dt| = \frac{V_{cc_AGD} - V_{\text{miller}}}{C_{gd} R_g} \quad (21)$$

where V_{miller} is the Miller stage voltage and it can be expressed as

$$V_{\text{miller}} = \frac{I_L}{g_m} + V_{th}.$$

4) Gate Remaining Charging Stage (t$_3$-t$_4$)*:* After t_3, the v_{ds} drops to 0 V. The Miller stage ends and v_{gs} starts to rise again. The amplified error is still higher than $V_{\text{cc_AGD}}$. Thus, the output voltage of gate driver is $V_{\text{cc_AGD}}$. Thus, $v_{gs}(s)$ can be calculated as

$$v_{gs}(s) = \frac{V_{cc_AGD} \cdot \frac{1}{s} + v_{gs}(t_3)\,(L_g C_t s + R_g C_t) + L_g C_t v'_{gs}(t_3)}{L_g C_t s^2 + R_g C_t s + 1} \quad (22)$$

where $v_{gs}(t_3)$ is the gate-source voltage at t_3, and $v'_{gs}(t_3)$ is value of the derivative of v_{gs} at moment t_3.

5) Gate-Source Voltage-Closed Loop Stage (t$_4$ *to Next Turn-off Process*)*:* At t_4, the gate-source voltage satisfies

$$v^*_{gs(\text{turn-on})} - v_{gs}(t) \le (V_{cc_AGD}/k_{\text{err}}). \quad (23)$$

Thus, operational amplifiers OP2 and OP3 enter the linear region. The closed loop of v_{gs} and v^*_{gs} is established. At this stage, the relationship between v^*_{gs} and v_{gs} can be calculated as

$$L_g C_t \frac{d^2 v_{gs}(t)}{dt^2} + R_g C_t \frac{dv_{gs}(t)}{dt} + (1 + k_{\text{err}})\, v_{gs}(t) = k_{\text{err}} v^*_{gs}. \quad (24)$$

According to (24), the relationship between v^*_{gs} and v_{gs} in frequency domain can be obtained by Laplace transformation, which is shown as

$$v_{gs}(s) = \frac{k_{\text{err}} v^*_{gs} \frac{1}{s} + L_g C_t s v_{gs}(t_4) + R_g C_t v_{gs}(t_4) + L_g C_t v'_{gs}(t_4)}{L_g C_t s^2 + R_g C_t s + (1 + k_{\text{err}})} \quad (25)$$

where $v_{gs}(t_4)$ is the gate-source voltage at t_4.

The steady-state value of v_{gs} can be calculated as

$$\lim_{t\to+\infty} v_{gs}(t) = \lim_{s\to0} s v_{gs}(s). \quad (26)$$

By substituting (25) into (26), the steady-state value of v_{gs} can be calculated as

$$\lim_{s\to0} s v_{gs}(s) = \lim_{s\to0} s \frac{k_{err} v^*_{gs} \frac{1}{s} + L_g C_t s v_{gs}(t_4) + R_g C_t v_{gs}(t_4) + L_g C_t v'_{gs}(t_4)}{L_g C_t s^2 + R_g C_t s + (1 + k_{\text{err}})} = \frac{k_{\text{err}}}{1 + k_{\text{err}}}. \quad (27)$$

By substituting (20) into (7), and substituting (21) into (8), the losses in the current rising stage and voltage falling stage can be respectively calculated as

$$E_{\text{on_}di_l/dt(\text{AGD})} = \frac{1}{2} \cdot I_L \cdot V_{dc} \cdot \times \frac{I_L R_g C_t/g_m}{V_{cc_AGD} - (0.5I_L/g_m + V_{th}) + L_g} \quad (28)$$

$$E_{\text{on_}dv/dt(\text{AGD})} = \frac{1}{2} \cdot I_L \cdot V_{\text{dc}} \cdot \frac{V_{\text{dc}} C_{gd} R_g}{V_{cc_AGD} - V_{\text{miller}}}. \quad (29)$$

It can be seen from (28) and (29) that the higher power supply reduces the losses in the current rising stage and voltage falling stage. In subsequent experiments of this article, the V_{cc_AGD} is set as 24 V, and V_{ee_AGD} is set as −8 V. After the moment t_4, the proposed AGD controls the gate-source voltage in a close loop state. As shown in (27), the gate-source voltage converges to $k_{\text{err}} v^*_{gs}/(k_{\text{err}} + 1)$. In subsequent experiments of this article, $v^*_{gs(\text{turn-on})}$ is set as 19 V during the turn ON process, and $v^*_{gs(\text{turn-off})}$ is set as −1.5 V during the turn OFF process. Thus, the proposed AGD can ensure that the gate-source voltage will not exceed the maximum gate-source voltage of SiC MOSFET.

The turn-OFF process of the proposed AGD is the inverse process of the turn-ON process. Similarly, there are also five stages in the turn-OFF process. Likewise, the proposed AGD can ensure that the gate-source voltage will not drop below the minimum allowable gate-source voltage of SiC MOSFET and reduce the switching loss.

B. Crosstalk Suppression Mechanism of Proposed AGD

Due to the complexity of solving multiorder systems in time domain, this section focuses on analyzing aspect 2, which pertains to the crosstalk suppression mechanism of the proposed AGD, from frequency domain. In SiC MOSFET bridge configuration, the drain-source voltage exhibits a trapezoidal waveform with a voltage amplitude V_{dc} and a frequency of the trapezoidal waveform is equal to the switching frequency f_{sw}. The amplitude of its nth harmonic can be obtained by Fourier decomposition as [26]

$$A_n = 2V_{\text{dc}} \left[\frac{\sin(n\pi d)}{n\pi d}\right] \left[\frac{\sin(n\pi f_{\text{sw}} T_r)}{n\pi f_{\text{sw}} T_r}\right] \quad (30)$$

where T_r is the rise time of the SiC MOSFET drain-source voltage, d is the duty cycle of v_{ds}.

The amplitude of its nth harmonic decreases with a slope of 20 dB before the cut off frequency, f_c, and it decreases with the slope of −40 dB after the cut off frequency. The cut off

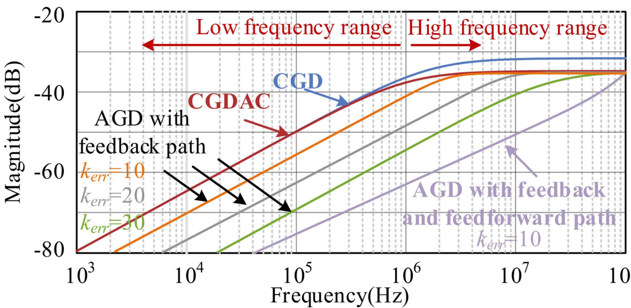

Fig. 7. Crosstalk magnitude responses of proposed AGD with feedback path and feedforward path.

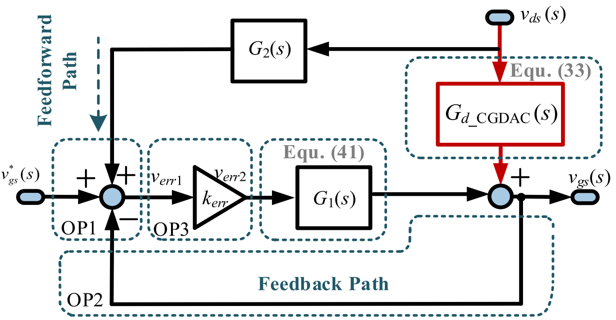

Fig. 8. Equivalent diagram of proposed AGD.

frequency can be calculated as [26]

$$f_c = \frac{1}{\pi T_r}. \tag{31}$$

Since the rise time of SiC MOSFET is only tens of nanoseconds, harmonics with the frequencies in the tens of MHz range cannot be ignored. Thus, to effectively suppress crosstalk, it is imperative to suppress not only the harmonics close to the switching frequency but also those occurring at tens of MHz.

According to (6), the transfer functions of $\Delta v_{gs}(s)$ and $v_{ds}(s)$ in CGD and CGDAC, can be respectively obtained through Laplace transformation as

$$G_{d_\mathrm{CGD}}(s) = \frac{\Delta v_{gs}(s)}{v_{ds}(s)} = \frac{L_g C_{gd} s^2 + C_{gd} R_g s}{L_g C_{gs} s^2 + R_g C_{gs} s + 1} \tag{32}$$

$$G_{d_\mathrm{CGDAC}}(s) = \frac{\Delta v_{gs}(s)}{v_{ds}(s)} = \frac{L_g C_{gd} s^2 + C_{gd} R_g s}{L_g C_t s^2 + R_g C_t s + 1}. \tag{33}$$

Fig. 7 shows the crosstalk magnitude responses of CGD, CGDAC, where $C_{gs} = 2700$ pF, $C_{gd} = 100$ pF, $C_{aux} = 2$ nF, $R_g = 10\ \Omega$, and $L_g = 1$ nH. As can be seen, CGD shows its high-pass characteristics. Compared with CGD, the CGDAC shows an approximate -3 dB reduction in crosstalk magnitude response within the high frequency range. However, the response amplitude of CGDAC to crosstalk in low frequency band is almost the same with CGD and its crosstalk suppression ability in high frequency region is still weak.

According to the structure of proposed AGD, the equivalent diagram of crosstalk suppression is shown in Fig. 8. In the feedback path of proposed AGD, after introducing the error amplifier coefficient k_{err}, the transfer functions of Δv_{gs} and v_{ds}

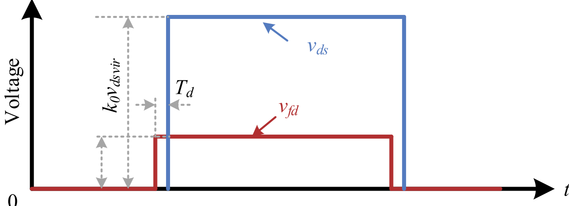

Fig. 9. Relationship between $v_{ds}(s)$ and $v_{fd}(s)$.

can be calculated as

$$G_{d_AGD}(s) = \frac{G_{d_\mathrm{CGDAC}}(s)}{1 + k_{\mathrm{err}} G_1(s)} = \frac{L_g C_{gd} s^2 + C_{gd} R_g s}{L_g C_t s^2 + R_g C_t s + k_{\mathrm{err}} + 1}. \tag{34}$$

According to (34), Fig. 7 shows the crosstalk magnitude response of the proposed AGD with feedback path. Building upon CGDAC, the proposed AGD with feedback path further mitigates the crosstalk magnitude response in the low-frequency region. However, achieving effective suppression of crosstalk in this region requires a high k_{err} value, which can potentially induce closed-loop instability, while its ability to suppress crosstalk in the high-frequency region remains limited. To address this issue, it is imperative to design $G_2(s)$ in the feedforward path.

In feedforward path, $G_2(s)$ is a linear controller and the drain-source voltage $v_{ds}(s)$ is the feedforward signal. The feedforward path is only utilized when crosstalk occurs and it not affect the switching process of SiC MOSFET. However, in bridge configuration, the amplitude of drain-source voltage is equal to the dc-link voltage. If the drain-source voltage is directly input to the amplifier, the amplifier will be damaged. For this problem, the PWM signal of complementary SiC MOSFET is selected as the feedforward signal, v_{fd}, which is proportional to $v_{ds}(s)$ approximately, as shown in Fig. 9. The relationship between $v_{ds}(s)$ and $v_{fd}\ (s)$ is shown as

$$v_{ds}(s) = k_0 v_{fd}(s) e^{-sT_d} \tag{35}$$

where k_0 is the magnitude ratio of V_{dc} and PWM signal v_{fd}, T_d is the time difference value between $v_{ds}(s)$ and $v_{fd}(s)$.

With the introduction of feedforward signal $v_{fd}\ (s)$, the drain-source voltage of SiC MOSFET can be observed indirectly. According to the superposition theorem and small signal model of SiC MOSFET at turn-OFF state, with the introduction of feedback path and feedforward path, the $\Delta v_{gs}(s)$ caused by $v_{fd}\ (s)$ and $v_{ds}(s)$ can be calculated as

$$\begin{aligned}\Delta v_{gs}(s) &= \frac{G_{d_\mathrm{CGDAC}}(s)}{1 + k_{\mathrm{err}} G_1(s)} v_{ds}(s) + \frac{k_{\mathrm{err}} G_1(s) G_2(s)}{1 + k_{\mathrm{err}} G_1(s)} v_{fd}(s) \\ &= \frac{G_{d_\mathrm{CGDAC}}(s) + \frac{k_{\mathrm{err}}}{k_0} e^{sT_d} G_1(s) G_2(s)}{1 + k_{\mathrm{err}} G_1(s)} v_{ds}(s). \end{aligned} \tag{36}$$

It can be seen from (36), the crosstalk is determined by k_{err}, k_0 and controller $G_2(s)$, if

$$G_{d_\mathrm{CGDAC}}(s) + \frac{k_{\mathrm{err}}}{k_0} e^{sT_d} G_1(s) G_2(s) = 0 \tag{37}$$

crosstalk will be theoretically suppressed. Thus, $G_2(s)$ can be calculated as

$$G_2(s) = -\frac{k_0 C_{gd}}{k_{\text{err}}}\left(L_g s^2 + R_g s\right) e^{-sT_d}. \quad (38)$$

It can be seen from (38) that crosstalk is composed of two parts one is caused by parasitic inductance L_g, and the other is caused by drive resistance R_g. In order to eliminate the crosstalk, the time domain form of $G_2(s)$ should be designed as a combination of a second-order differentiator and a first-order differentiator. However, it is difficult to implement a second-order differentiator with analog device and the introduction of differentiator will cause the system to be sensitive to noise. According to [22], the parasitic inductance in the gate driver of Kelvin package SiC MOSFET is small by proper design in practical applications. In [10], [27], [28], and [29], the parasitic inductance is ignored in the process of SiC MOSFET modeling and crosstalk suppression strategy. Therefore, the crosstalk caused by the drive resistance is the main part, and the proposed feedforward regulator $G_2(s)$ is designed as

$$G_2(s) = -\frac{k_0}{k_{\text{err}}} C_{gd} R_g s \cdot \frac{1}{T_d s + 1}. \quad (39)$$

It can be seen from (39) that the proposed $G_2(s)$ is a first order differentiator with a low-pass filter. It approximately achieves the effect of time delay T_d and the low-pass filter can effectively avoid the impact of noise on the differentiator.

According to (36) and (39), crosstalk magnitude responses of the proposed AGD with feedback path and feedforward path can be calculated as

$$\Delta v_{gs}(s) = \frac{G'_d(s) + \frac{k_{\text{err}}}{k_0} e^{sT_d} G'_1(s) G_2(s)}{1 + k_{\text{err}} G'_1(s)} v_{ds}(s) = \frac{L_g C_{gd} s^2 + C_{gd} R_g s - \frac{e^{sT_d}}{T_d s+1} C_{gd} R_g s}{L_g C_t s^2 + R_g C_t s + k_{\text{err}} + 1} v_{ds}(s). \quad (40)$$

According to (40), the crosstalk magnitude response of proposed AGD is shown in Fig. 7. It can be seen that the proposed AGD achieves comprehensive crosstalk suppression through feedforward and feedback paths in the full frequency range.

C. Design Guideline of Proposed AGD

Aiming at driving SiC MOSFET, a design example of the proposed AGD is given below. First, adjusting the AGD to the open-loop state. The gate-source loop is a second-order system in this state. The relationship between gate-source voltage and the gate driver output voltage is

$$G_1(s) = \frac{v_{gs}(s)}{v_{\text{out}}(s)} = \frac{1}{L_g C_t s^2 + R_g C_t s + 1}. \quad (41)$$

Second, carefully select the drive resistance R_g and auxiliary capacitor C_{aux} to make ensure that the gate-source loop remains in an underdamped state. The output voltage of gate driver is a step signal, on this condition, the response of the gate-source voltage in the time domain can be expressed as

$$v_{gs}(t) = v^*_{gs}\left(1 - \frac{1}{\sqrt{1-\zeta^2}}\right) e^{-\zeta\omega_n t} \sin(\omega_d t + \beta) \quad (42)$$

where ζ is damping ratio, $\omega_d$is damped oscillation frequency, $\omega_n$is natural oscillation frequency, which can be expressed respectively as

$$\zeta = \frac{R_g}{2}\sqrt{\frac{C_t}{L_g}}$$

$$\omega_n = \sqrt{\frac{1}{L_g C_t}}$$

$$\omega_d = \omega_n\sqrt{1-\zeta^2}.$$

The ω_d can be obtained by measuring the frequency of gate-source voltage oscillation with oscilloscope. It can be seen from (42), since R_g and C_{iss} are known, the parasitic inductance, L_g can be extracted by calculation.

Third, adjusting the AGD to the closed-loop state. The relationship between gate-source voltage and the gate driver output voltage when AGD in the closed-loop state is

$$G_{1_c}(s) = \frac{k_{\text{err}} G_1(s)}{1 + k_{\text{err}} G_1(s)} = \frac{k_{\text{err}}}{L_g C_t s^2 + R_g C_t s + k_{\text{err}} + 1}. \quad (43)$$

The peak gate-source voltage in the closed-loop state can be expressed as

$$v_{g\text{speak}} = v^*_{gs}(1 + e^{-\pi/\sqrt{1-\zeta_c^2}}) \quad (44)$$

where ζ is damping ratio of AGD in the closed-loop state, which can be expressed as

$$\zeta_c = \frac{R_g}{2}\sqrt{\frac{C_{iss}}{L_g(k_{\text{err}}+1)}}.$$

To avoid damaging SiC MOSFET, the peak gate-source voltage should satisfy

$$v_{g\text{speak}} < v_{gs\,\text{max}} \quad (45)$$

where $v_{gs\text{max}}$ is the maximum allowable gate-source voltage of SiC MOSFET.

It can be seen from (44), the overshoot rate of gate-source voltage is determined by the damping ratio of the system. If the overshoot is relatively large, it is necessary to increase the damping ratio, which can be achieved by increasing the drive resistance or the parallel auxiliary capacitance.

According to the Fig. 6, the SiC MOSFET based on the proposed AGD is in the open-loop state during the switching process at stages t_0-t_4. Thus, the peak time of gate-source voltage is approximately the same as the peak time of open-loop state. The peak time can be expressed as

$$t_p = \frac{\pi}{\omega_d} = \frac{\pi}{\omega_n\sqrt{1-\zeta^2}}. \quad (46)$$

Due to the limitation of the operational amplifier slew rate, the output voltage of operational amplifier is not an ideal step

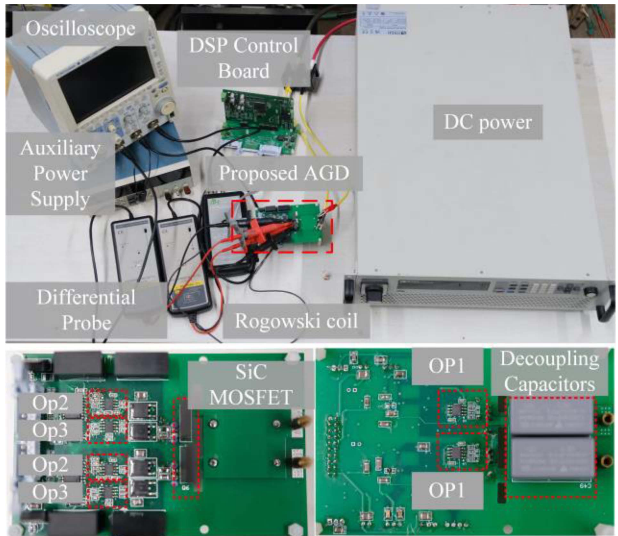

Fig. 10. Experimental hardware platform and measurement schematic diagram.

voltage. The slew rate of operational amplifier need to satisfy

$$\frac{v_{gs}^*}{\mathrm{SW}} \ll t_p. \tag{47}$$

Therefore, the main limitation of the AGD proposed in this article is that the slew rate of operational amplifier need to be very high. In order to meet the requirement, the LM6172 is selected as the operational amplifier of proposed AGD in this article, with a slew rate of 3000 V/μs. In a few nanoseconds, the output voltage of the lm6172 can rise to the gate-source given voltage, ${v_{gs}}^*$. Thus, choosing the lm6172 as a closed-loop controller does not affect the fast switching of the SiC MOSFET.

IV. Experimental Verification

In order to verify the effectiveness of the proposed AGD, the double pulse test platform with IV1Q12050T4 SiC MOSFET is built as shown in Fig. 10. The maximum positive and negative gate-source voltage of IV1Q12050T4 is 22 V and -5 V. The experimental waveforms are captured by the YOKOGAWA DLM2024 digital oscilloscope (200 MHz, 2.5 G/S). Voltage waveforms are measured by the 100 MHz differential probe Yokogawa 700924 and the current waveforms are measured by the PEM CWT3 Rogowski current waveform transducer, with a peak current slew rate of 40 A/ns.

A. Switching Loss Reduction Verification

Figs. 11 and 12 show the turn-ON process and turn-OFF process waveforms of the CGD, CDGAC, and proposed AGD (The drain-source current is at 25 A, and the dc-link voltage is at 400 V, 300 V, and 200 V, respectively). The driver resistance in CGD, CGDAC, and proposed AGD is 10 Ω, and auxiliary capacitor of CGDAC and proposed AGD is 2.2 nF. It can be seen that the loss in the turn-ON process of CGD is 307, 243, and 229 μJ when the drain-source current is 25A and the dc-link voltage is 400, 300, and 200 V, respectively. The loss in the turn-OFF process is 569, 351 and 268 μJ, respectively. The total time of the turn-ON process, including current rising stage and voltage falling stage is 119, 131, and 134 ns, respectively. The total time of the turn-OFF process, including voltage rising stage and current falling stage, is 152, 166, and 159 ns, respectively.

Due to the introduction of auxiliary capacitors, the change rate of drain-source current in CGDAC is reduced which results in increased switching time and loss. The total time of the turn-ON process is 162, 170, and 175 ns, respectively. The total time of the turn-off process is 183, 199, and 236 ns, respectively. The loss in the turn-on process of CGDAC is 438, 359, and 229 μJ respectively. The loss in the turn-OFF process of CGDAC is 630, 425, and 313 μJ, respectively. Compared with the above two methods, the proposed AGD can effectively reduce the switching time and loss. Specifically, the total time of the turn-ON process is 98, 97, and 95 ns, respectively. The total time of the turn-OFF process is 112, 114, and 107 ns, respectively. The loss in the turn-ON process is 246, 208, and 102 μJ, respectively. The loss in the turn-OFF process is 354, 336, and 175 μJ, respectively. It can be seen from the experimental results that the proposed AGD can reduce the switching loss by up to 20% and 40% compared with CGD and CGDAC which proves the effectiveness of AGD in reducing the switching loss.

B. Crosstalk Suppression Verification

Fig. 13 shows the crosstalk experimental results of the CGD, CDGAC, and proposed AGD (the drain-source current is at 25 A, and the dc-link voltage is at 400, 300, and 200 V, respectively). It can be seen from the results of CGD that during the turn-ON process of SiC MOSFET, the maximum positive gate-source voltage of its complementary SiC MOSFET is 2.8, 1.7, and 0.9 V at 400, 300, and 200 V, respectively. The corresponding change amplitude of gate-source voltage is 6.1, 5.0, and 4.2 V. During turn OFF process of SiC MOSFET, the minimum negative gate-source voltage of complementary SiC MOSFET is -7.1, -5.8, and -5.1 V, respectively. The corresponding change amplitude of gate-source voltage is -3.8, -2.5, and -1.8 V.

For CGDAC, during the turn-ON process of SiC MOSFET, the maximum positive gate-source voltage of its complementary SiC MOSFET is 1.1, 0.6, and -0.6 V at 400, 300, and 200 V, respectively. The corresponding change amplitude of gate-source voltage is 4.4, 3.9, and 2.7 V. During turn OFF process of SiC MOSFET, the minimum negative gate-source voltage of complementary SiC MOSFET is -6.2, -5.1, and -4.3 V, respectively. The corresponding change amplitude of gate-source voltage is -2.9, -1.8, and -1.0 V. Although CGDAC can partially suppress the crosstalk, the above experimental results show that compared with CGD, the switching loss of CGDAC is increased by 20% and the negative crosstalk is still lower than the minimum allowable gate-source voltage of SiC MOSFET which results in reduced lifetime.

For the proposed AGD, during the turn-ON process of SiC MOSFET, the maximum positive gate-source voltage of its complementary SiC MOSFET is 0.9, -0.1, and -0.7 V at 400, 300, and 200 V, respectively. The corresponding change amplitude of gate-source voltage is 2.15, 1.15, and 0.55 V. During turn OFF process of SiC MOSFET, the minimum negative gate-source voltage of complementary SiC MOSFET is -3.1, -2.6, and

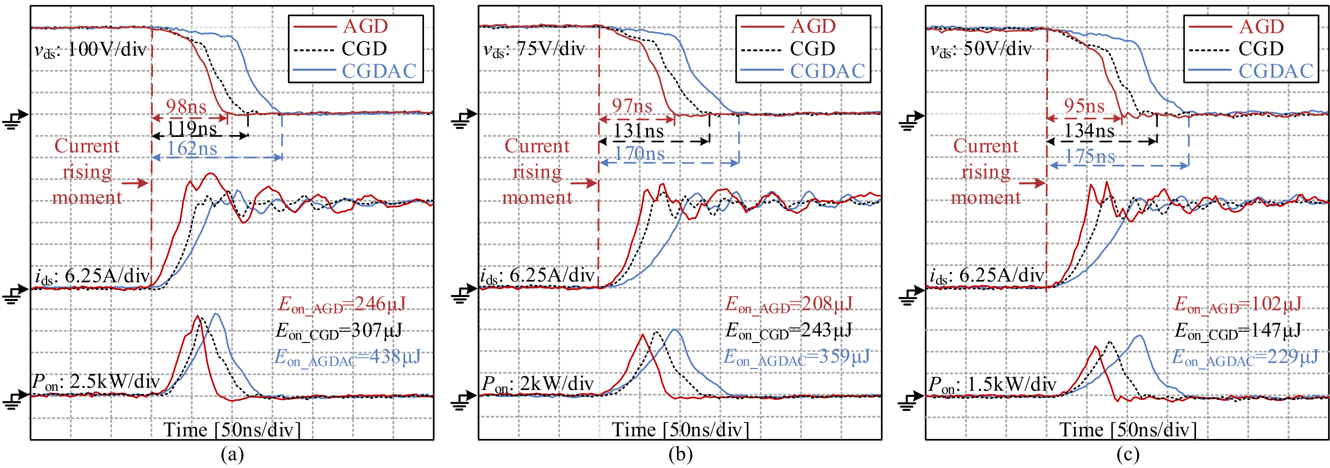

Fig. 11. Experimental results of CGD, CGDAC and proposed AGD during turn-ON process under 25 A, DC-link voltage at (a) 400 V, (b) 300 V, and (c) 200 V.

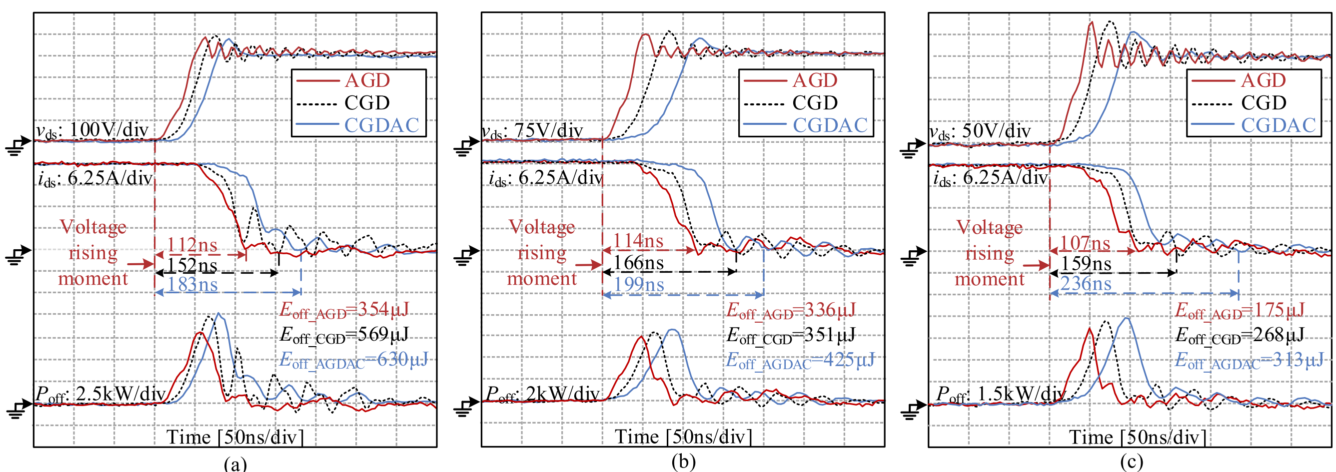

Fig. 12. Experimental results of CGD, CGDAC and proposed AGD during turn-OFF process under 2 5A, DC-link voltage at (a) 400 V, (b) 300 V, and (c) 200 V.

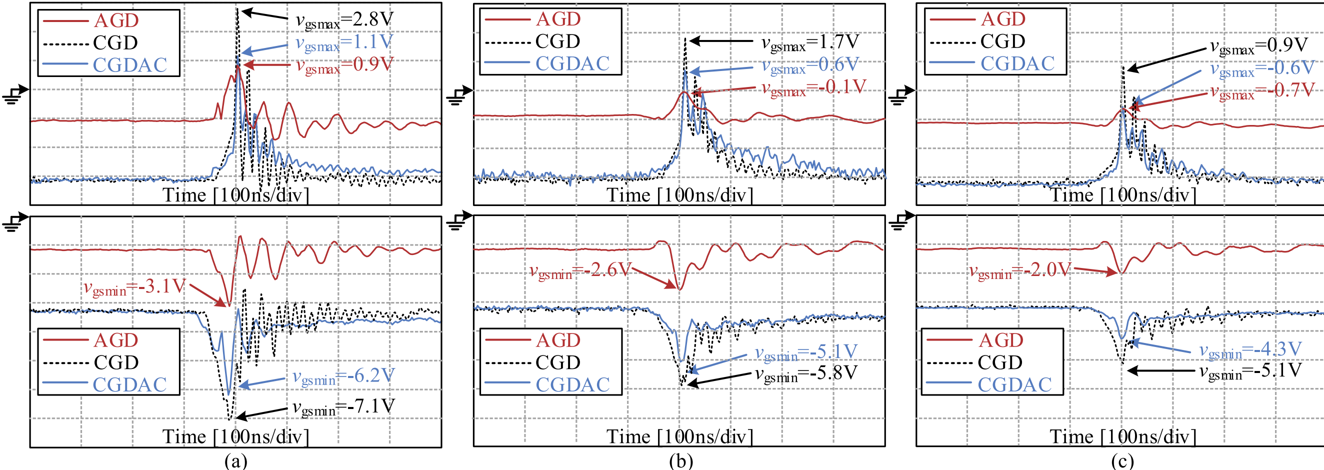

Fig. 13. Crosstalk experimental results of CGD, CGDAC and proposed AGD under 25 A, DC-link voltage at (a) 400 V, (b) 300 V, and (c) 200 V (figures above are results of positive crosstalk and figures below are results of negative crosstalk).

−2.0 V, respectively. The corresponding change amplitude of gate-source voltage is −1.85, −1.35, and −0.75 V. It can be seen from the experimental results that the proposed AGD exhibits superior crosstalk suppression capability and a smaller negative gate-source spike voltage compared with CGD and CGDAC. Thus, the proposed AGD can ensure the safe operation under various working condition, solves the contradiction between switching loss and crosstalk suppression capability, and improve the lifetime of SiC MOSFET.

V. Conclusion

In this article, an AGD based on the hardware closed-loop control mechanism is proposed. The AGD effectively reduce the amplitude of crosstalk and prevent the spurious turn-ON of SiC MOSFET by designing feedback path and feedforward path in the frequency domain. Thus, the AGD allows for higher negative turn-OFF voltage to be applied, preventing overstress of the negative gate-source voltage of SiC MOSFET and improving its lifetime. Moreover, the introduction of closed-loop control enables the power supply voltage to surpass the maximum gate-source voltage limit, thereby enhancing the switching speed of SiC MOSFET and reducing switching loss while ensuring that the gate-source voltage remains within a safe range. The experimental results show that compared with CGD and CGDAC, the proposed AGD can suppress the crosstalk and reduce switching loss under different working conditions.

References

[1] X. Yuan, I. Laird, and S. Walder, “Opportunities, challenges, and potential solutions in the application of fast-switching SiC power devices and converters,” *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3925–3945, Apr. 2021.

[2] D. Tan, “Emerging system applications and technological trends in power electronics: Power electronics is increasingly cutting across traditional boundaries,” *IEEE Power Electron. Mag.*, vol. 2, no. 2, pp. 38–47, Jun. 2015.

[3] Y. Shi, L. Wang, R. Xie, Y. Shi, and H. Li, “A 60-kW 3-kW/kg five-level T-type SiC PV inverter with 99.2% peak efficiency,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9144–9154, Nov. 2017.

[4] R. Bosshard and J. W. Kolar, “All-SiC 9.5 kW/dm^3 on-board power electronics for 50 kW/85 kHz automotive IPT system,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 419–431, Mar. 2017.

[5] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, “Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.

[6] B. Li, G. Zhang, C. Li, G. Wang, S. Liu, and D. Xu, “Crosstalk suppression method for GaN-based bridge configuration using negative voltage self-recovery gate drive,” *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4406–4418, Apr. 2022.

[7] M. R. Ahmed, R. Todd, and A. J. Forsyth, “Predicting SiC MOSFET behavior under hard-switching, soft-switching, and false turn-on conditions,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9001–9011, Nov. 2017.

[8] Z. Wu et al., “Dynamic dv/dt control strategy of SiC MOSFET for switching loss reduction in the operational power range,” *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6237–6241, Jun. 2022.

[9] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, “A novel active gate driver for improving SiC MOSFET switching trajectory,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9032–9042, Nov. 2017.

[10] T. Shao et al., “The active gate drive based on negative feedback mechanism for fast switching and crosstalk suppression of SiC devices,” *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6739–6754, Jun. 2022.

[11] S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao, and H. A. Mantooth, “An intelligent versatile model-based trajectory-optimized active gate driver for silicon carbide devices,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 429–441, Mar. 2020.

[12] N. He, M. Chen, J. Wu, N. Zhu, and D. Xu, “20-kW zero-voltage-switching SiC-MOSFET grid inverter with 300 kHz switching frequency,” *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5175–5190, Jun. 2019.

[13] T. Yao and R. Ayyanar, “A multifunctional double pulse tester for cascode GaN devices,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9023–9031, Nov. 2017.

[14] H.-T. Tang, H. S.-H. Chung, and K. J. Chen, “Adaptive level-shift gate driver with indirect gate oxide health monitoring for suppressing crosstalk of SiC MOSFETs,” *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 10196–10212, Aug. 2023.

[15] C. Li, J. Sheng, and D. Dujic, “Reliable gate driving of SiC MOSFETs with crosstalk voltage elimination and two-step short-circuit protection,” *IEEE Trans. Ind. Electron.*, vol. 70, no. 10, pp. 10066–10075, Oct. 2023.

[16] F. Gao, Q. Zhou, P. Wang, and C. Zhang, “A gate driver of SiC MOSFET for suppressing the negative voltage spikes in a bridge circuit,” *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2339–2353, Mar. 2018.

[17] J. Wang and H. S.-H. Chung, “A novel RCD level shifter for elimination of spurious turn-on in the bridge-leg configuration,” *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 976–984, Feb. 2015.

[18] J. Wang and H. S.-H. Chung, “Impact of parasitic elements on the spurious triggering pulse in synchronous buck converter,” *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6672–6685, Dec. 2014.

[19] C. Li et al., “High off-state impedance gate driver of SiC MOSFETs for crosstalk voltage elimination considering common-source inductance,” *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2999–3011, Mar. 2020.

[20] A. Liberti, G. Catalisano, and L. Abbatelli, “Mitigation technique of the SiC MOSFET gate voltage glitches with miller clamp,” STMicroelectronics, Geneva, Switzerland, Application Note AN-5355, 2019. Accessed: Mar. 18, 2020. [Online]. Available: https://www.st.com

[21] B. Zhang, S. Xie, J. Xu, Q. Qian, Z. Zhang, and K. Xu, “A magnetic coupling based gate driver for crosstalk suppression of SiC MOSFETs,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9052–9063, Nov. 2017.

[22] Y. Li, Y. Zhang, Y. Gao, S. Du, and J. Liu, “Switching characteristic analysis and application assessment of SiC MOSFET with common source inductance and kelvin source connection,” *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7941–7951, Jul. 2022.

[23] Z. Zeng and X. Li, “Comparative study on multiple degrees of freedom of gate drivers for transient behavior regulation of SiC MOSFET,” *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8754–8763, Oct. 2018.

[24] Y. Yang, Y. Wen, and Y. Gao, “A novel active gate driver for improving switching performance of high-power SiC MOSFET modules,” *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7775–7787, Aug. 2019.

[25] P. Xiang, R. Hao, J. Cai, and X. You, “An active gate driver of SiC MOSFET module based on PCB rogowski coil for optimizing tradeoff between overshoot and switching loss,” *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 245–260, Jan. 2023.

[26] O. Henry W, *Electromagnetic Compatibility Engineering*. Hoboken, NJ, USA: Wiley, 2011.

[27] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, “Intelligent gate drive for fast switching and crosstalk suppression of SiC devices,” *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.

[28] H. Li, Y. Jiang, Z. Qiu, Y. Wang, and Y. Ding, “A predictive algorithm for crosstalk peaks of SiC MOSFET by considering the nonlinearity of gate-drain capacitance,” *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2823–2834, Mar. 2021.

[29] H.-T. Tang, H. S.-H. Chung, J. W.-T. Fan, R. S.-C. Yeung, and R. W.-H. Lau, “Passive resonant level shifter for suppression of crosstalk effect and reduction of body diode loss of SiC MOSFETs in bridge legs,” *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7204–7225, Jul. 2020.