Systematic Topology Synthesis and Power Density Visualization of Partial Power Processing Architecture

Ye Tian, *Member, IEEE*, Yan Li, *Member, IEEE*, Bowu Cao, Fangyi Wei, *Graduate Student Member, IEEE*, and Yanxuan Zheng, *Graduate Student Member, IEEE*

***Abstract*—DC–DC converters based on partial power processing (PPP) offer the advantage of high power density and high efficiency and are considered an attractive solution in various systems like photovoltaic systems, energy storage systems. This article investigates the systematic topology synthesis and power density visualization of PPP architecture. PPP topologies overlap significantly with existing nonisolated topologies. To enhance the current topology synthesis approach, a synthesis method for PPP topologies is proposed. A general expression set for voltage gain is proposed for the convenience of studying the synthesized topologies. A visualization scheme for the power density of the topology is proposed for the first time. The topology synthesis method offers a fresh perspective for systematically explaining existing topologies. Through the visualization of topology power density, the power density of nonisolated topologies can be quantitatively evaluated. Nonisolated topologies can be systematically synthesized and classified from the perspective of PPP. Using the proposed power density visualization scheme, topologies with higher power density, known as PPP topologies, can be selected. The feasibility of the synthesized topologies and the power density visualization scheme are respectively validated through design and experiment.**

***Index Terms*—Circuit topology, dc–dc power conversion, nonisolated converters, switched mode power supplies.**

I. Introduction

DC–DC converters based on partial power processing (PPP) offer the advantage of high power density and high efficiency and are considered an attractive solution in various systems such as photovoltaic systems, energy storage systems, and more.

Different from full power processing, the core concept of PPP is to allow a portion of power to pass directly from the input port to the output port without processing [1], as shown in Fig. 1. It was first proposed in the aerospace field [2], and its structure was explored [3], [4], [5], [6]. Throughout, it has been considered that the core unit of a PPP topology must be an isolated topology because nonisolated units would be shorted [3]. Many PPP topologies with an isolated core unit have been proposed and studied [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. However, in fact, the core unit of a PPP topology can be nonisolated, only requiring it to be negative polarity. Li et al. conducted thorough research on this issue by introducing the concept of the VA area and demonstrated it [14], [15].

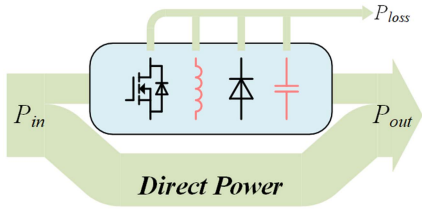

Fig. 1. Partial power processing (PPP).

Various PPP topologies continue to be developed to meet diverse application requirements. This raises a question: How many such topologies exist in total? Currently, it appears that only by inventing a systematic method for synthesizing PPP topologies can we explore all possible topologies. This would allow us to demonstrate that the selected topology is optimal for a specific requirement. Zientarski et al. demonstrated the synthesis method and the synthesized topologies of PPP with isolated core units [10]. Li et al. stated that using buck–boost converter as the core unit can synthesize both boost converter and buck converter, which are PPP topologies [14], [15].

In the syntheses of general nonisolated dc–dc converter topologies, there are also PPP topologies. Many researchers have made considerable efforts in this regard [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38]. The synthesis methods of nonisolated dc–dc converter topologies reported in the literature can be categorized into five main classes [35], arranged in order from specific to abstract as follows: methods based on circuit theorems [16], [17], [18], methods based on combinations [19], [20], [21], [22], [23], [24], methods based on converter cells [25], [26], [27], [28], [29], methods based on volt-second balance [30], [31], [32], [33], [34], [35], and methods based on topology matrices [36], [37], [38].

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Ye Tian, Yan Li, Fangyi Wei, and Yanxuan Zheng are with the Beijing Jiaotong University, School of Electrical Engineering, Beijing 100044, China (e-mail: 19117025@bjtu.edu.cn; liyan@bjtu.edu.cn; 23111451@bjtu.edu.cn; 22110472@bjtu.edu.cn).

Bowu Cao is with the Qingdao Ainuo Intelligent Instrument Company, Ltd., Qingdao 266101, China (e-mail: 20121413@bjtu.edu.cn).

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1) Methods Based on Circuit Theorems: Because the topology of converters is a special type of circuit, methods based on circuit theorems are the most direct but also relatively limited approach to topology synthesis. Swapping the input and output ports of an existing topology results in a symmetric topology with a voltage gain equal to the reciprocal of its original voltage gain. Similarly, based on an existing topology, applying the duality principle between voltage sources and current sources results in a dual topology. Furthermore, Wang and Yoon [18] reported isomorphism relationship between two classes of topologies.

2) Methods Based on Combinations: The earliest combinatorial topology synthesis method is cascading, which is a way of connecting two two-port networks [19]. The voltage gain of two topologies cascaded together is the product of their voltage gains, but typically, the resulting cascade topology is not considered as a single topology but as two separate ones. To achieve single-stage topologies, authors in [20], [21] and [22], [23], [24] proposed the layer and graft scheme and the reduced redundant power processing scheme, respectively. Meanwhile, Zhao et al. [3] formally merged switches.

3) Methods Based on Converter Cells: If, starting from a basic unit, whether it is a topology of a converter or a part of it, and after a series of simple and rigorous steps, it can synthesize all existing topologies of this type of converter, then this method can be considered a systematic approach. Since the input and output ports of most nonisolated dc–dc converters are connected by a single wire, the three-terminal canonical cell is commonly regarded as a key element for synthesizing their topologies and is widely utilized [25], [26], [27], [28], [29].

4) Methods Based on Volt-Second Balance: The volt-second balance characteristic of inductors is typically core to voltage-voltage-type converters. Therefore, in the past five years, this concept has been extensively utilized for synthesizing topologies of such converters. Based on the core concept of volt-second balancing, more comprehensive topology synthesis methods have been established. However, due to incomplete synthesis steps and a lack of necessary constraints, there are topologies that cannot be synthesized, such as superboost converter, as well as redundant topologies [30], [31], [32]. Based on the proposed topology synthesis methods, a relationship between voltage gain and the volt-second balance equations has been established. However, due to one gain corresponding to an infinite number of equations, there are certain difficulties in selecting the optimal topology [33], [34], [35].

5) Methods Based on Topology Matrices: Furthermore, if topology synthesis is abstracted to a mathematical level, it can help explain more existing topologies and synthesize new ones. Authors in [36] and [37] reported an analytical synthesis method based on the fundamental loop matrices. Unfortunately, this would make the synthesis process more complex and lead to more redundant topologies, especially for higher order converters.

A conclusion can be drawn: overly specific methods make the process of topology synthesis unmanageable, while overly abstract methods can lead to topology synthesis results that are disconnected from practical applications. Although synthesizing topologies from voltage gain is advantageous for applications, the rationale behind this approach is debatable because it essentially involves finding and solving a multivalued function, which can be quite uncertain. In essence, this problem arises due to the lack of a topology synthesis method that is both free from redundant and infeasible topologies and simple to apply.

Throughout, high-frequency operation has been considered the most effective means to enhance the power density of converters, as it can substantially reduce the volume of inductors and capacitors, which constitute a significant portion of the converter's volume [39]. However, as one of the important criteria for topology evaluation, power density has not been systematically studied. Power density optimization has only been conducted for specific topologies [40]. The theory of VA area describes the minimum power that a topology must process at specific input and output, which represents the maximum achievable power density [14], [15]. Zientarski et al. introduced the concept of nonactive power, which refers to the power of inductors and capacitors, to evaluate topologies [10], [11], [13].

This article investigates the systematic topology synthesis and power density visualization of PPP architecture. The rest of this article is as follows. Section II proposes a topology synthesis method, and a general expression set for voltage gain of topologies. Section III demonstrates the synthesis of four categories of topologies with PPP architecture and their respective voltage gains. Section IV achieves power density visualization by establishing the relationship between the volume of energy storage components and the power converted by the topology. In Section V, the voltage gain, switch voltage stress, and power density of the synthesized 11 categories of topologies are compared. Finally, in Section VI, the feasibility of the synthesized topologies and the power density visualization scheme are respectively validated through design and experiment.

II. Topology Synthesis Method, Notation System, and General Expression of Voltage Gain of PPP Topologies

In this section, a topology synthesis method based on buck–boost converter, a converter rather than individual components, is proposed. In addition, a notation system and a general expression set for voltage gain based on topology synthesis are introduced.

A. Topology Synthesis Method Based on Buck–Boost Converter

According to practical requirements, dc–dc converters with voltage source inputs and outputs are most commonly used, and the volt-second balance characteristic of inductors can precisely meet this demand, as shown in Fig. 2. By alternately turning ON and OFF switches S_1 and S_2, this topology achieves voltage conversion, where the relationship between output voltage and input voltage can be expressed as

$$U_{\text{in}} \cdot D_1 T_s = U_{\text{out}} \cdot (1 - D_1) T_s \tag{1}$$

where U_{in} and U_{out} represent the input and the output voltages, respectively, and D_1 is the duty cycle of S_1, and T_s is the switching period. However, the actions of the switches result in discontinuous input and output currents for this topology, which

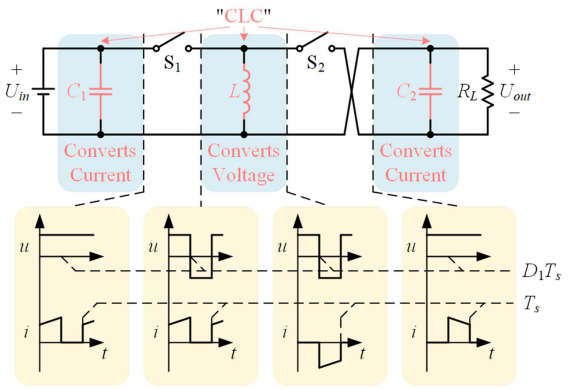


Fig. 2. Power processing of buck–boost converter.

is not desirable in most applications and capacitors can precisely absorb the ac component of the port current, thereby making the port current dc. This is buck–boost converter, which also serves as the starting point for the topology synthesis in this article.

Except for multi-input or multioutput converters, the topology of dc–dc converters can be equivalently represented as a two-port network. There are a total of five connections between two two-port networks: input parallel output series, input series output parallel, input parallel output parallel, input series output series, and cascading. However, the first four connections are not suitable for nonisolated topologies. They impose excessive external constraints on the two two-port networks, resulting in synthesized topologies that are neither positive nor negative, topologically degenerate, or even causing the original two-port networks to malfunction. When the lower two-port network is replaced by a pair of wires, two of the four form PPP topologies, as shown in steps A and B of Fig. 3. The two-port network X is referred to as the core unit. Fortunately, steps A and B only require negative polarity for the core unit, and buck–boost converter happens to be suitable. The equivalent capacitor indicated by the dashed lines is provided by the input and output capacitors, so the change in the capacitor position does not affect the static characteristics of the topology. Besides steps A and B, which directly synthesize PPP topologies, steps C to F are also indispensable in the synthesis process of PPP topologies, as shown in steps C to F of Fig. 3, where step F is the important method for single-stage topology realization. The notation for each topology shown below steps A to E will be presented in Section II-B, and the specific topology synthesis process will be presented in Section III.

B. Notation System of Topologies Based on Synthesis

To clearly distinguish the synthesized topologies, a topology notation system is used. The inductor of buck–boost converter converts the voltage while the capacitors convert the current; hence, its notation is CLC. For simplicity, the notations of X after step A, X after step B, X and Y after steps C, D, or E, and X after step F are P(X)S, S(X)P, X-Y, and X_MS, respectively, as shown in Table I. The topology notation consists of L (inductor), C (capacitor), P (parallel), and S (series). These letters correspond to the inductors, capacitors, parallel points, and series points in the topology, fully describing the structure of the topology. To provide a more intuitive description of the topology, P(CLC)S is replaced with C-P(LC)S, S(CLC)P with S(CL)P-C, and so forth.

TABLE I
NOTATION SYSTEM OF TOPOLOGIES

Topologies	Notation	Simplified Notation
Buck–Boost	CLC	L
X after Step A	P(X)S	P(X')S
X after Step B	S(X)P	S(X')P
X and Y after Steps C, D, or E	X-Y	X'-Y'
X after Step F	X_MS	X'_MS

Meanwhile, to more concisely reflect the characteristics of the topology's voltage gain, a simplified notation convention is proposed. Since the expression for the voltage gain of a topology is only related to inductors, the "C" of its notation is removed to obtain the simplified one. Topologies with the same simplified notation have the same expression for voltage gain.

C. General Expression of Voltage Gain Based on Topology Synthesis

When the topology synthesis method is based on converters rather than individual components, the voltage gains of the synthesized topologies can be easily obtained through that of CLC (buck–boost) and the six synthesis steps without listing and solving the volt-second balance equations:

$$\begin{aligned} G_u^{\mathrm{L}} &= \frac{D_1}{1-D_1} \\ G_u^{\mathrm{P(X')S}} &= 1 + G_u^{\mathrm{X'}} \\ G_u^{\mathrm{S(X')P}} &= \frac{1}{1+\frac{1}{G_u^{\mathrm{X'}}}} \\ G_u^{\mathrm{X'\text{-}Y'}} &= G_u^{\mathrm{X'}} \times G_u^{\mathrm{Y'}}. \end{aligned} \tag{2}$$

The second and third equations correspond to steps A and B, respectively. The fourth equation corresponds to steps C, D, or E. Since merging switches does not affect the voltage gain of the topology, there is no equation corresponding to step F. Interestingly, the voltage gain of cascading X after step A and X after step B is the same as that of X:

$$G_u^{\mathrm{P(X')S\text{-}S(X')P}} = \left(1 + G_u^{\mathrm{X'}}\right) \times \frac{1}{1+\frac{1}{G_u^{\mathrm{X'}}}} = G_u^{\mathrm{X'}}. \tag{3}$$

III. TOPOLOGY SYNTHESIS

In this section, according to Section II-A, three types of topologies, including existing and new ones, are synthesized: based on CLC (buck–boost), based on cascading C-P(L)S-C (boost) and C-S(L)P-C (buck), and based on cascading CLC (buck–boost) and C-S(L)P-C (buck). According to Section II-C, their voltage gains are easily obtained.

A. Topology Synthesis Based on CLC (Buck–Boost)

CLC (buck–boost) after step A is shown in Fig. 4. The topology is denoted as C-P(L)S-C, also known as boost

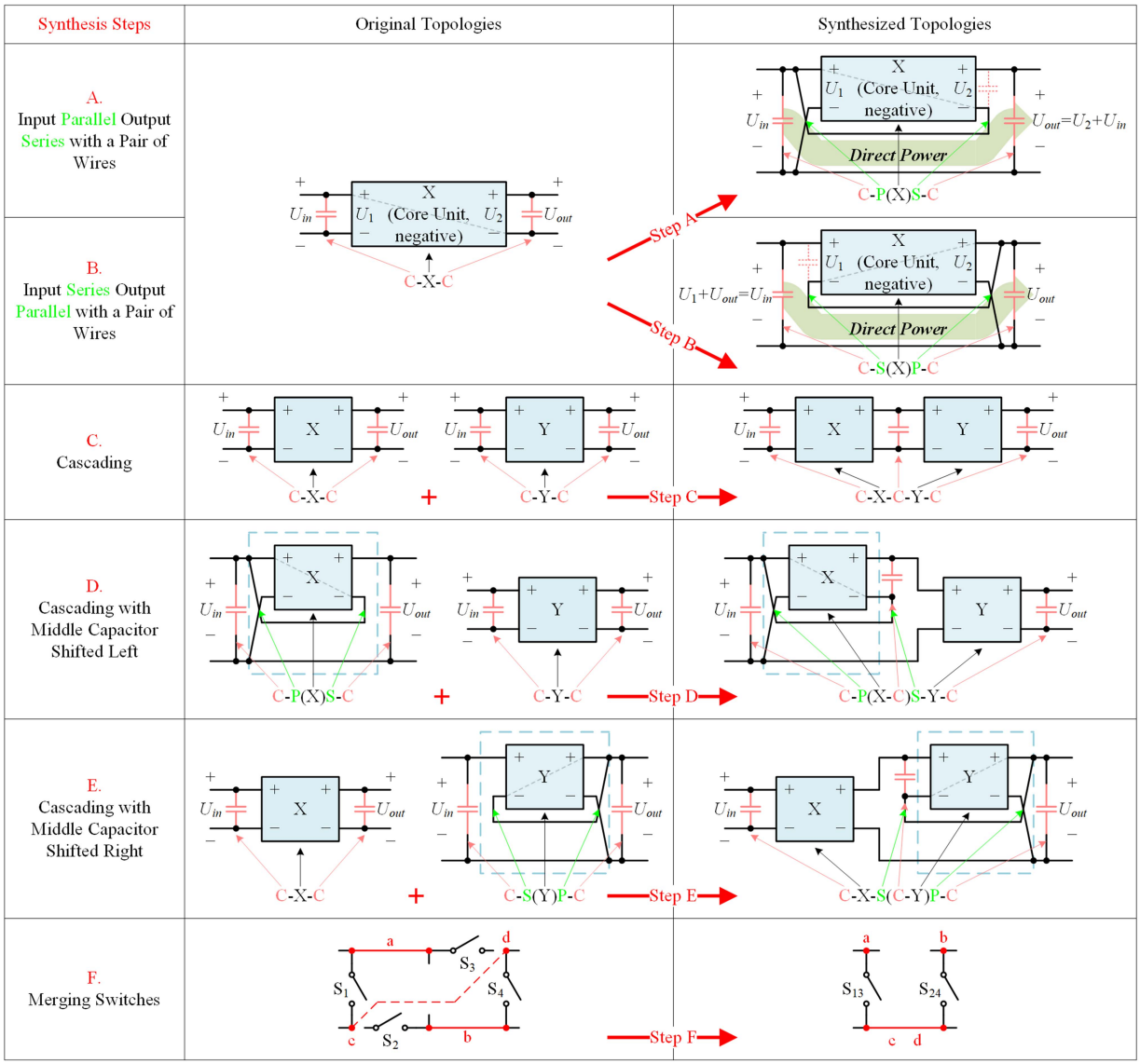


Fig. 3. Six topology synthesis steps.

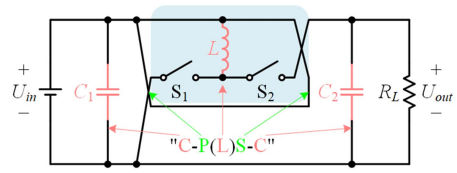


Fig. 4. Topology synthesis of C-P(L)S-C (boost): CLC (buck–boost) after step A.

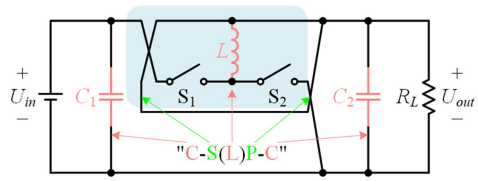


Fig. 5. Topology synthesis of C-S(L)P-C (buck): CLC (buck–boost) after step B.

converter [41]. Its voltage gain is

$$G_u^{\mathrm{P(L)S}} = 1 + \frac{D_1}{1-D_1} = \frac{1}{1-D_1}. \tag{4}$$

Similarly, CLC (buck–boost) after step B is shown in Fig. 5, denoted as C-S(L)P-C, being buck converter. Its voltage gain is

$$G_u^{\mathrm{S(L)P}} = \frac{1}{1+\frac{1}{\left(\frac{D_1}{1-D_1}\right)}} = D_1. \tag{5}$$

Therefore, the conclusion can be drawn: boost converter and buck converter are PPP topologies.

B. Topology Synthesis Based on Cascading C-P(L)S-C (Boost) and C-S(L)P-C (Buck)

C-P(L)S-C (boost) and C-S(L)P-C (buck) after steps C, D, and E are shown in Fig. 6. The differences among steps C, D, and E lie in the positions of the intermediate capacitor. The

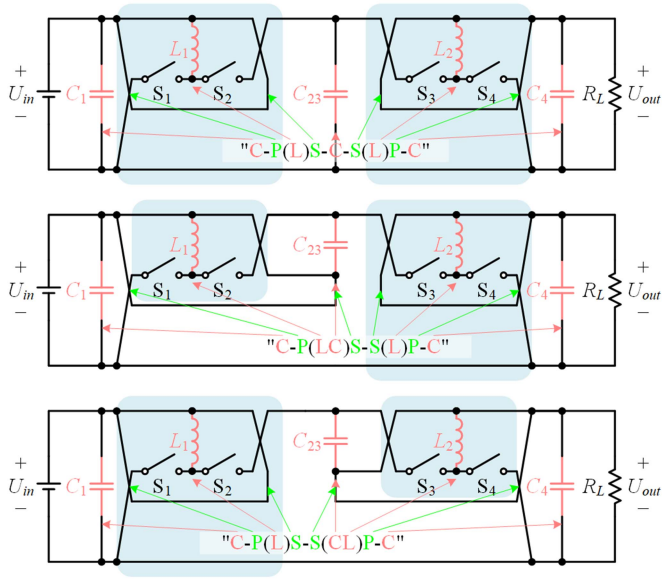


Fig. 6. Topology synthesis of C-P(L)S-C-S(L)P-C (original topology of Ćuk), C-P(LC)S-S(L)P-C (original topology of Zeta), and C-P(L)S-S(CL)P-C (original topology of SEPIC): C-P(L)S-C (boost) and C-S(L)P-C (buck) after steps C, D, and E.

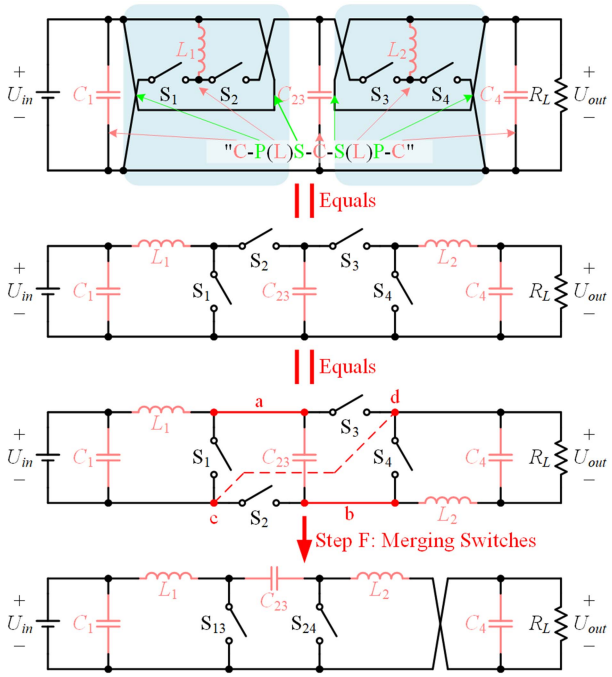


Fig. 7. Topology synthesis of C-P(L)S-C-S(L)P-C_MS (Ćuk): C-P(L)S-C-S(L)P-C (original topology of Ćuk) after step F.

synthesized topologies are denoted as C-P(L)S-C-S(L)P-C, C-P(LC)S-S(L)P-C, and C-P(L)S-S(CL)P-C, respectively. These correspond to the original topologies of Ćuk, Zeta, and SEPIC converters. Therefore, their voltage gains are the same, which is

$$G_u^{\text{P(L)S-S(L)P}} = \frac{1}{1-D_1} \times D_1 = \frac{D_1}{1-D_1}. \tag{6}$$

C-P(L)S-C-S(L)P-C (original topology of Ćuk) after step F is shown in Fig. 7. By moving S_2 and L_2 to the bottom, S_1 and S_3 have common terminals "a" and "b" with S_2 and S_4, respectively. When S_1 and S_3, as well as S_2 and S_4, are synchronized, the potentials of "c" and "d" are the same in both modes. Therefore, "c" and "d" can be connected together and S_1 and S_3, as well as S_2 and S_4, can be paralleled and merged as a single switch to form Ćuk converter. As a result of the topology after merging switches, it can also be denoted as C-P(L)S-C-S(L)P-C_MS. Zeta and SEPIC converters can also be synthesized through step F, and are denoted as C-P(LC)S-S(L)P-C_MS and C-P(L)S-S(CL)P-C_MS, respectively. The parallel merging of switches reduces the number of them at the cost of their current stress. Although its applicability is limited due to the negative polarity of C-P(L)S-C-S(L)P-C_MS (Ćuk), it enables itself to serve as a core unit for synthesizing new topologies.

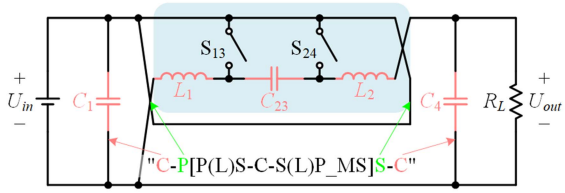


Fig. 8. Topology synthesis of C-P[P(L)S-C-S(L)P_MS]S-C (superboost): c-P(L)S-C-S(L)P-C_MS (Ćuk) after step A.

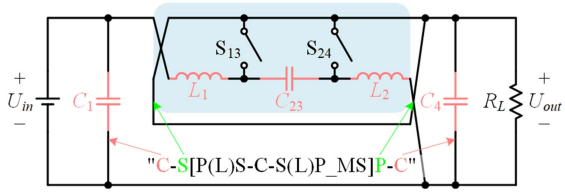


Fig. 9. Topology synthesis of C-S[P(L)S-C-S(L)P_MS]P-C (superbuck): c-P(L)S-C-S(L)P-C_MS (Ćuk) after step B.

C-P(L)S-C-S(L)P-C_MS (Ćuk) after step A is shown in Fig. 8, denoted as C-P[P(L)S-C-S(L)P-C_MS]S, being superboost converter. Its voltage gain is

$$G_u^{\text{P[P(L)S-S(L)P]S}} = 1 + \frac{D_1}{1-D_1} = \frac{1}{1-D_1}. \tag{7}$$

Likewise, C-P(L)S-C-S(L)P-C_MS (Ćuk) after step B is shown in Fig. 9, denoted as C-S[P(L)S-C-S(L)P_MS]P-C, being superbuck converter. Its voltage gain is

$$G_u^{\text{S[P(L)S-S(L)P]P}} = \frac{1}{1+\frac{1}{\left(\frac{D_1}{1-D_1}\right)}} = D_1. \tag{8}$$

Similarly, the conclusion can be drawn: superboost converter and superbuck converter are PPP topologies.

C. Topology Synthesis Based on Cascading CLC (Buck–Boost) and C-S(L)P-C (Buck)

CLC (buck–boost) and C-S(L)P-C (buck) after step C and step F are shown in Fig. 10. First, S_1 and S_2 are split into series-connected switches, denoted as S_{11} and S_{12}, and S_{21} and S_{22}, respectively. Then, S_{11} and L_2 are moved to the bottom. Similarly, S_{11} and S_3 have common terminals "a" and "b" with S_{21} and S_4, respectively. When the switches are synchronized, the potentials of "c," "d," and "e" are the same in both modes.

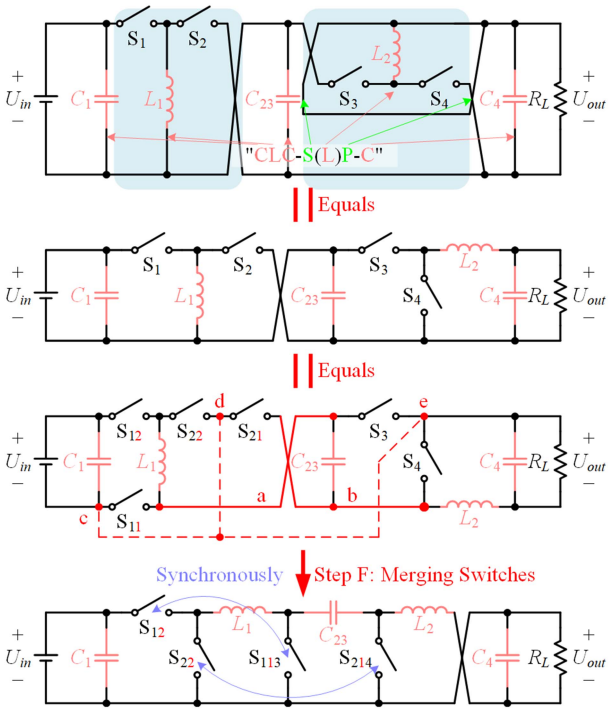


Fig. 10. Topology synthesis of CLC-S(L)P-C_MS (new topology): CLC-S(L)P-C (new topology) after step F.

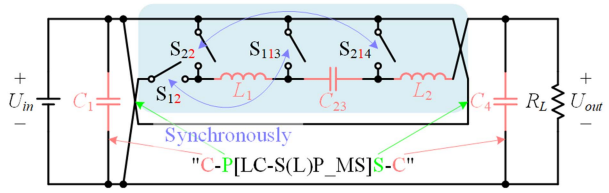


Fig. 11. Topology synthesis of C-P[LC-S(L)P_MS]S-C (new topology, experimental prototype): CLC-S(L)P-C_MS (new topology) after step A.

Therefore, "c," "d," and "e" can be connected together and S_{11} and S_3, as well as S_{21} and S_4, can be paralleled and merged as a single switch to form a new topology CLC-S(L)P-C_MS. The series splitting and parallel merging switches reducing their voltage stress at the cost of their current stress. Similarly, it is also of negative polarity, making it suitable as a core unit. Its voltage gain is

$$G_u^{\text{L-S(L)P}} = \frac{D_1}{1-D_1} \times D_1 = \frac{D_1^2}{1-D_1}. \tag{9}$$

The new topology CLC-S(L)P-C_MS after step A is shown in Fig. 11, denoted as C-P[LC-S(L)P_MS]S-C. This is another new topology and is also the experimental prototype topology in this article. Its voltage gain is

$$G_u^{\text{P[L-S(L)P]S}} = 1 + \frac{D_1^2}{1-D_1} = \frac{1-D_1+D_1^2}{1-D_1}. \tag{10}$$

The new topology CLC-S(L)P-C_MS after step B is shown in Fig. 12, denoted as C-S[LC-S(L)P_MS]P-C, which is another new topology. Its voltage gain is

$$G_u^{\text{S[L-S(L)P]P}} = \frac{1}{1+\frac{1}{\left(\frac{D_1^2}{1-D_1}\right)}} = \frac{D_1^2}{D_1^2+1-D_1}. \tag{11}$$

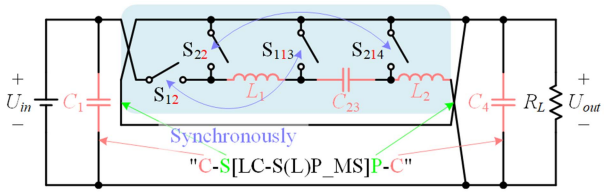


Fig. 12. Topology synthesis of C-S[LC-S(L)P_MS]P-C (new topology): CLC-S(L)P-C_MS (new topology) after step B.

Similarly, the conclusion can be drawn: topologies shown in Figs. 11 and 12 are PPP topologies.

D. Summary

Starting from CLC (buck–boost), the topologies that can be synthesized through steps A to F, within the range of single inductor and dual inductors configurations, and their synthesis paths are shown in Fig. 13. Based on their voltage gain characteristics, these topologies are divided into 11 categories, denoted by simplified notation. Categories with the same background color indicate that the two categories have voltage gain characteristics that are symmetrical with respect to the input and output. Section III-A to III-C present the synthesis processes for the topologies in categories 1, 2, 3, 7, 8, and 9. During the synthesis process, the synchronous relationships of multiple switches are provided. Except for the topologies with existing names noted in parentheses, all are new topologies. These 11 categories of topologies differ not only in voltage gain characteristics but also in PPP characteristics, power density characteristics, and switch voltage stress characteristics, all labeled next to each category's simplified notation. Among them, voltage gain characteristics are subdivided into step-up/down characteristics and voltage gain width characteristics. Besides step-up/down characteristics, these categories' other characteristics will be compared in Section V.

The implementation of ideal switches in a topology depends on whether the topology operates unidirectionally or bidirectionally. For topologies that operate only unidirectionally, ideal switches with the same ON-state current direction and OFF-state voltage direction are replaced by MOSFETs, while those with opposite directions are replaced by diodes. For topologies that operate bidirectionally, all ideal switches are replaced by MOSFETs.

IV. Power Density Visualization

In this section, the relationships between the volume of energy storage components and the power of them, as well as between the latter and the power converted by the topology, are established. These correlations unveil the connections between the volume of energy storage components and the power converted by the topology, as shown in Fig. 14. Therefore, the power density of nonisolated topologies can be visualized, and whether a topology is PPP is proven from the perspective of power density.

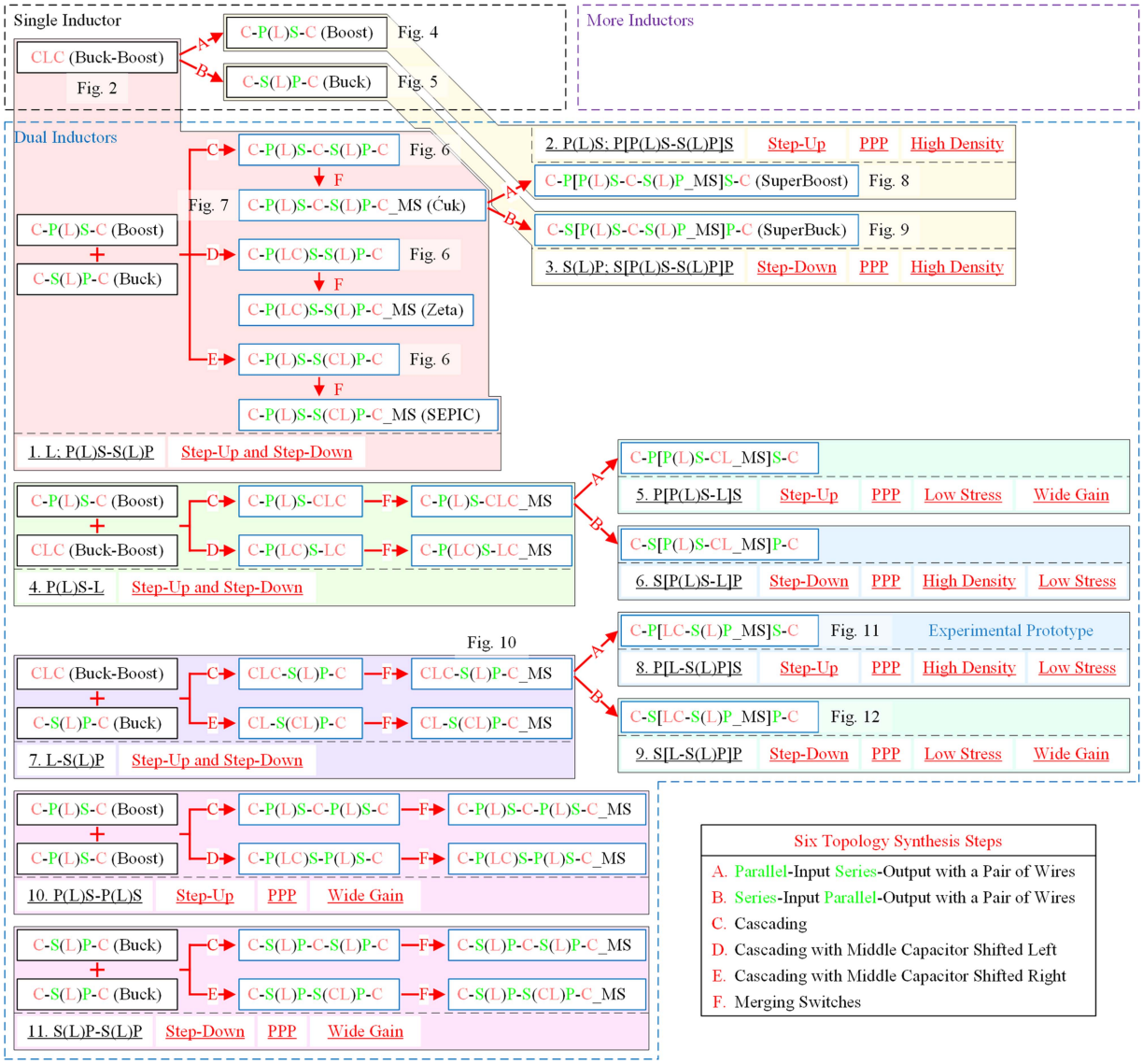


Fig. 13. Synthesized 11 categories of topologies and their synthesis paths.

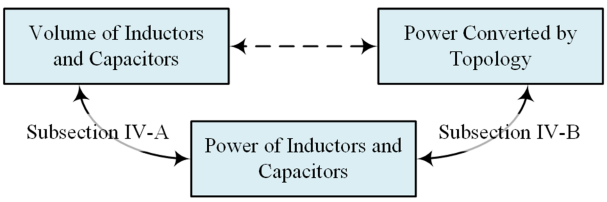


Fig. 14. Establishment of relationship between the volume of inductors and capacitors and the power converted by topology.

A. Relationships Between Volume of Inductors and Capacitors and Power of Them

According to the analysis of CLC (buck–boost) in Section II-A, it can be observed that the inductor converts the voltage while the capacitors convert the current. Energy storage mode and energy release mode of inductors alternate, and capacitors operate in a similar manner. Hence, the power of them is

$$P_L = \frac{1}{2}\frac{1}{T_s}\int_0^{T_s} |u_L(t)\cdot i_L(t)|\mathrm{d}t$$
$$P_C = \frac{1}{2}\frac{1}{T_s}\int_0^{T_s} |u_C(t)\cdot i_C(t)|\mathrm{d}t. \quad (12)$$

Assuming that under rated conditions, the current of the inductors is continuous. Because CLC (buck–boost) and topologies synthesized based on it only have two modes, the inductors and capacitors in them are also in two modes. Therefore, (12) can be simplified to

$$P_L = \frac{1}{T_s}\int_{I_{L\_\min}}^{I_{L\_\max}} L\cdot i_L(t)\cdot \mathrm{d}i_L(t)$$
$$= \frac{1}{2}\frac{1}{T_s}L\left(I_{L\_\max}^2 - I_{L\_\min}^2\right)$$

$$P_C = \frac{1}{T_s}\int_{U_{C\_\min}}^{U_{C\_\max}} C \cdot u_C(t) \cdot \mathrm{d}u_C(t)$$
$$= \frac{1}{2}\frac{1}{T_s} C \left(U_{C\_\max}^2 - U_{C\_\min}^2\right). \quad (13)$$

Due to material limitations, there is an upper limit on the energy density of the energy storage medium (ESM) of energy storage components. Therefore, it holds that

$$\frac{1}{2} L I_{L\_\max}^2 \le \frac{1}{2}\frac{B_{\max}^2}{\mu} V_{L\_ESM}$$
$$\frac{1}{2} C U_{C\_\max}^2 \le \frac{1}{2}\varepsilon E_{\max}^2 V_{C\_ESM} \quad (14)$$

where V_{L_ESM} and V_{C_ESM} are the volumes of the ESM for inductors and capacitors, respectively.

Combining (13) with (14), it can be obtained that

$$V_{L\_ESM\_\min} = \frac{2\mu}{f_s B_{\max}^2} \frac{\left(\frac{I_{L\_\max}}{I_{L\_\min}}\right)^2}{\left(\frac{I_{L\_\max}}{I_{L\_\min}}\right)^2 - 1} P_L$$
$$V_{C\_ESM\_\min} = \frac{2}{f_s \varepsilon E_{\max}^2} \frac{\left(\frac{U_{C\_\max}}{U_{C\_\min}}\right)^2}{\left(\frac{U_{C\_\max}}{U_{C\_\min}}\right)^2 - 1} P_C. \quad (15)$$

Therefore, the power of energy storage components is directly proportional to the minimum volume of their ESM. Moreover, due to the significant contribution of the ESM's volumes to the components, the volumes of energy storage components are positively correlated with the power of them.

B. Relationship Between Power of Inductors and Capacitors and Power Converted by the Topology

For simplicity, the power of inductors and capacitors in a topology X is represented as

$$P_L^{\mathrm{X}} = \sum P_{L\_i}^{\mathrm{X}}, \quad P_C^{\mathrm{X}} = \sum P_{C\_i}^{\mathrm{X}}. \quad (16)$$

The power of the input capacitor also needs to be considered [42]. Applying (13) to CLC (buck–boost), it can be obtained that

$$P_{conv}^{\mathrm{CLC}} = U_{in} I_{in} = \frac{1}{2}\frac{1}{T_s} L \left(I_{L\_\max}^2 - I_{L\_\min}^2\right)$$
$$P_L^{\mathrm{CLC}} = P_L = \frac{1}{2}\frac{1}{T_s} L \left(I_{L\_\max}^2 - I_{L\_\min}^2\right)$$
$$\lim_{\Delta i_L/I_L \to 0} P_C^{\mathrm{CLC}} = \lim_{\Delta i_L/I_L \to 0} (P_{C\_1} + P_{C\_2})$$
$$= \frac{1}{2}\frac{1}{T_s} L \left(I_{L\_\max}^2 - I_{L\_\min}^2\right), \quad (17)$$

where P_{conv}^{CLC} represents the power converted by CLC (buck–boost), assuming its efficiency is 100%. Therefore, the power converted by CLC (buck–boost) equals the power of its inductor and also equals that of capacitors, under the condition of the inductor current ripple approaching zero:

$$P_{conv}^{\mathrm{CLC}} = P_L^{\mathrm{CLC}} = \lim_{\Delta i_L/I_L \to 0} P_C^{\mathrm{CLC}}. \quad (18)$$

However, under the rated operating conditions of practical converters, $\Delta i_L/I_L$ is typically around 20%, which results in an increase in P_C^{CLC}, as shown in Fig. 15. It can be observed that an increase in inductor current ripple leads to varying degrees of increase in P_C^{CLC} outside the region where $\Delta i_L/I_L \le 2D_1, \Delta i_L/I_L \le 2(1-D_1)$, and $\Delta i_L/I_L \ge 0$, especially when $\Delta i_L/I_L$ approaches 200%. Nevertheless, fortunately, when $\Delta i_L/I_L$ equals 20%, the proportion of P_C^{CLC} to P_{conv}^{CLC} increases by up to 2.5%. Therefore, (18) can be rewritten as

$$P_{conv}^{\mathrm{CLC}} = P_L^{\mathrm{CLC}} \approx P_C^{\mathrm{CLC}}|_{\Delta i_L/I_L \le 20\%}. \quad (19)$$

For other topologies, more complex scenarios need to be considered: internal topologies must meet external requirements. Fig. 16 shows five types of external requirements and four types of internal topologies, with input and output ports linking the internal and external aspects, and feasible combinations are also listed. The VA area theory proposed by Li et al. can effectively explain the positive polarity, negative polarity, and isolation in external requirements [14], [15], as shown in Fig. 17. The areas of the green and red rectangles represent the input and output power, respectively, where the arrow indicates current direction

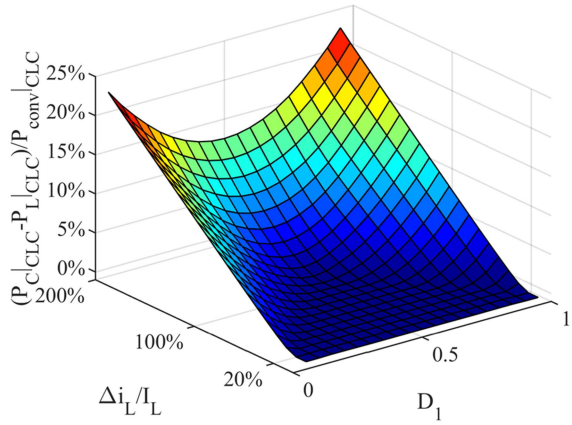


Fig. 15. Increase in the power of capacitors in CLC (buck–boost).

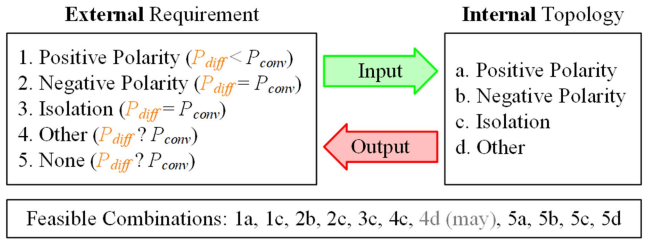


Fig. 16. Five types of external requirements and four types of internal topologies.

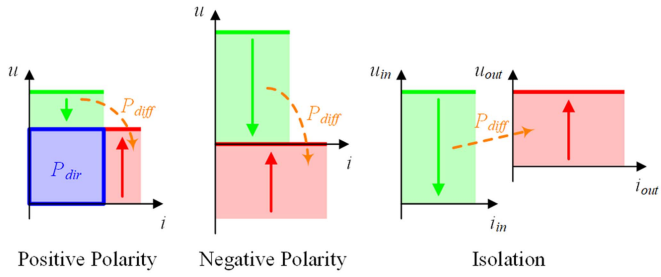


Fig. 17. Interpretation of VA area using step-down requirement as an example.

TABLE II
VOLTAGE GAIN, MAXIMUM SWITCH VOLTAGE STRESS, AND POWER PROCESSING PROPORTION OF THE 11 CATEGORIES OF TOPOLOGIES

Category	Simplified Notation	Voltage Gain, G_u	Maximum Switch Voltage Stress, $V_{s\_\max}$	Power Processing Proportion, K_{power}
1	L; P(L)S-S(L)P	$\frac{D_1}{1-D_1}$	$\frac{1}{1-D_1}V_{in}$	1
2	P(L)S; P[P(L)S-S(L)P]S	$\frac{1}{1-D_1}$	$\frac{1}{1-D_1}V_{in}$	D_1
3	S(L)P; S[P(L)S-S(L)P]P	D_1	V_{in}	$1-D_1$
4	P(L)S-L	$\frac{D_1}{(1-D_1)^2}$	$\frac{1}{(1-D_1)^2}V_{in}$ or $\max\left\{1,\frac{D_1}{1-D_1}\right\}\frac{1}{1-D_1}V_{in}$ (MS)	$1+D_1$
5	P[P(L)S-L]S	$\frac{D_1^2-D_1+1}{(1-D_1)^2}$	$\max\left\{1,\frac{D_1}{1-D_1}\right\}\frac{1}{1-D_1}V_{in}$	$\frac{D_1(D_1+1)}{D_1^2-D_1+1}$
6	S[P(L)S-L]P	$\frac{D_1}{D_1^2-D_1+1}$	$\max\left\{1,\frac{D_1}{1-D_1}\right\}\frac{1-D_1}{D_1^2-D_1+1}V_{in}$	$\frac{(D_1+1)(1-D_1)^2}{D_1^2-D_1+1}$
7	L-S(L)P	$\frac{D_1^2}{1-D_1}$	$\frac{1}{1-D_1}V_{in}$ or $\max\left\{1,\frac{D_1}{1-D_1}\right\}V_{in}$ (MS)	$2-D_1$
8	P[L-S(L)P]S	$\frac{D_1^2-D_1+1}{1-D_1}$	$\max\left\{1,\frac{D_1}{1-D_1}\right\}V_{in}$	$\frac{D_1^2(2-D_1)}{D_1^2-D_1+1}$
9	S[L-S(L)P]P	$\frac{D_1^2}{D_1^2-D_1+1}$	$\max\left\{1,\frac{D_1}{1-D_1}\right\}\frac{1-D_1}{D_1^2-D_1+1}V_{in}$	$\frac{(1-D_1)(2-D_1)}{D_1^2-D_1+1}$
10	P(L)S-P(L)S	$\frac{1}{(1-D_1)^2}$	$\frac{1}{(1-D_1)^2}V_{in}$	$2D_1$
11	S(L)P-S(L)P	D_1^2	V_{in}	$2(1-D_1)$

and the thicker bar indicates higher voltage. VA area divides the power converted by a topology X into two parts: the overlapping area represents the direct power, and the nonoverlapping area represents the differential power:

$$P_{\text{conv}}^{\text{X}} = P_{\text{dir}}^{\text{X}} + P_{\text{diff}}^{\text{X}}. \tag{20}$$

The former is the power that the topology can choose not to process, while the latter is the power that the topology must process at least. Clearly, only positive polarity external requirement can generate P_{dir}, as shown in steps A and B of Fig. 3, and correspondingly, the power converted by the core unit is P_{diff}. Therefore, the power processed by a topology is not always equal to the power converted by it.

For the topologies composed of CLCs (buck–boost) in Section III, the sum of the power converted or processed by CLCs (buck–boost) is defined as the indirect power, and combined with (19) yields

$$P_{\text{indir}}^{\text{X}} = P_L^{\text{X}} \approx P_C^{\text{X}}|_{\Delta i_L/I_L \le 20\%} \tag{21}$$

and the minimum value of the indirect power of the internal topology is the differential power of the external requirement:

$$P_{\text{diff}}^{\text{X}} = \min\left\{P_{\text{indir}}^{\text{X}}\right\}. \tag{22}$$

The power processing proportion can be defined as

$$K_{\text{power}}^{\text{X}} = \frac{P_{\text{indir}}^{\text{X}}}{P_{\text{conv}}^{\text{X}}} \in (0, +\infty). \tag{23}$$

It describes the proportion of the power processed by a topology X to the power converted by it. So if there exists a G_u such that K_{power} is less than 100%, then the topology is PPP; otherwise, it is not.

Similarly, like voltage gain, the power processing proportions of the synthesized topologies can be easily obtained through that of CLC (buck–boost) and the six synthesis steps without listing and solving the equations:

$$K_{\text{power}}^{\text{L}} = 1$$

$$K_{\text{power}}^{\text{P(X')S}} = K_{\text{power}}^{\text{X'}} \cdot \frac{G_u^{\text{X'}}}{1+G_u^{\text{X'}}}$$

$$K_{\text{power}}^{\text{S(X')P}} = K_{\text{power}}^{\text{X'}} \cdot \frac{\frac{1}{G_u^{\text{X'}}}}{1+\frac{1}{G_u^{\text{X'}}}}$$

$$K_{\text{power}}^{\text{X'-Y'}} = K_{\text{power}}^{\text{X'}} + K_{\text{power}}^{\text{Y'}}. \tag{24}$$

The second and third equations correspond to steps A and B, respectively. The fourth equation corresponds to steps C, D, or E. Since merging switches does not affect the power processing proportion of the topology, there is no equation corresponding to step F.

It is worth noting that the increase in the power of capacitors in the topologies shown in Fig. 13 is within 5%, provided that $\Delta i_L/I_L$ is within 20%, except for C-P[P(L)S-CL_MS]S-C and C-S[LC-S(L)P_MS]P-C, which can reach up to 38%. The unusually high proportion of P_C in these specific topologies is due to energy exchange between the capacitors within this particular architecture. But due to the much higher power density of capacitors compared to inductors, the increase in P_C has a negligible effect on the power density of the topology.

When comparing the power density of different topologies, the following variables should be consistent for both topologies: switching frequency, ESM of the inductor (magnetic permeability and maximum magnetic flux density), ESM of the capacitor (dielectric constant and maximum electric field strength), inductor current ripple ratio, capacitor voltage ripple ratio, as well as topology power and input–output voltage. Under these conditions, the inductance and capacitance values for each topology are determined. This process is embedded in the power density visualization scheme using K_{power}.

V. VOLTAGE GAIN, SWITCH VOLTAGE STRESS, AND POWER DENSITY OF SYNTHESIZED TOPOLOGIES

Based on (2) and (24), the voltage gains and power processing proportions of the eleven categories of topologies can be obtained, as shown in Table II. Their maximum switch voltage stress is also listed. According to Section IV, it can be concluded

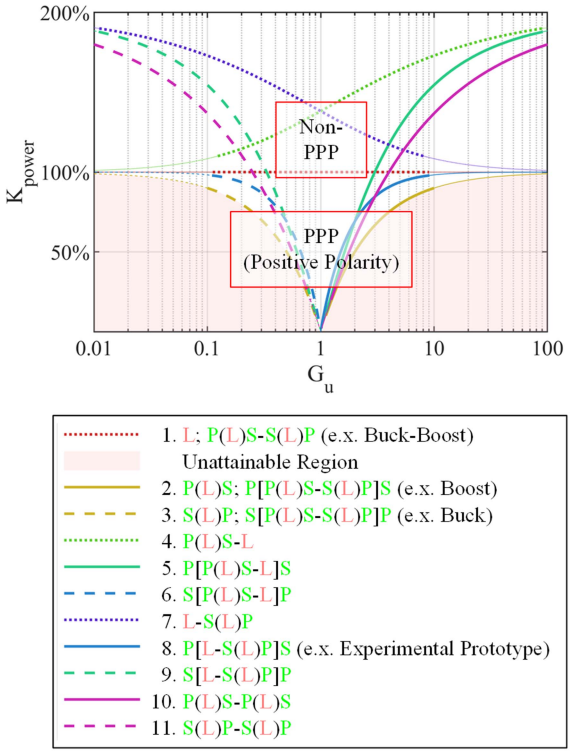


Fig. 18. Power processing proportion K_{power} of the 11 categories of topologies at different voltage gains.

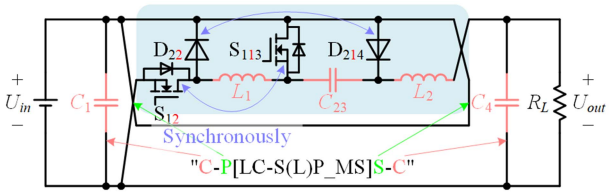


Fig. 19. Circuit of experimental prototype.

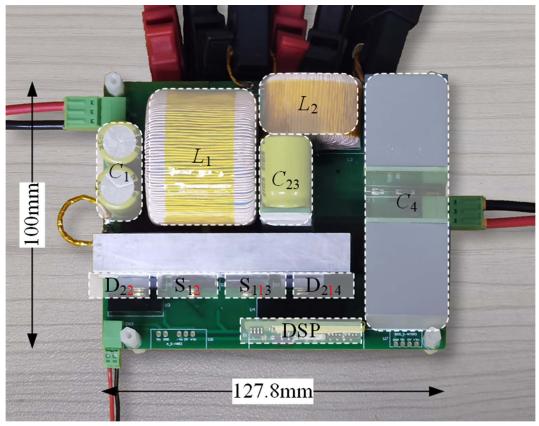


Fig. 20. Experimental prototype.

that the power density of a topology is primarily determined by its K_{power}. Fig. 18 shows the power processing proportions of the 11 categories of topologies at different voltage gains. At the same time, the power density of the topologies is also visualized. The solid curves, dashed curves, and dotted curves represent step-up topologies, step-down topologies, and step-up and step-down topologies, respectively. The former two are PPP while the latter is not and both former two are positive polarity, according to Fig. 17. Curves 2 and 3 describe P_{diff} for the positive polarity external requirement, and the shaded region represents the unattainable region for any nonisolated converter

$$K_{\text{power}}^{\text{X}} \geq \begin{cases} 1 - G_u^{\text{X}}, & G_u^{\text{X}} \leq 1 \\ 1 - \frac{1}{G_u^{\text{X}}}, & G_u^{\text{X}} > 1. \end{cases} \tag{25}$$

Therefore, the K_{power} of these two types of topologies is lowest, and the power density is highest.

However, the topologies with higher K_{power} are not without merit. This will be explained below, taking step-up topologies as an example. The curves are thicker for $D_1 \in (0.1, 0.9)$ while thinner for $D_1 \in (0, 0.1) \cup (0.9, 1)$. Categories 5 and 10 have a wider range of G_u compared to categories 2 and 8, within the same range of D_1; however, the switch voltage stress of category 8 is lower than that of category 2.

VI. Verification

In this section, the feasibility of the power density visualization scheme and the synthesized topologies is verified through design and experiment.

A. Design Verification

Taking the step-up scenario as an example, representative topologies are selected from categories 2, 5, 8 and 10, and converters are designed under given conditions. The volume of ESM is calculated according to (15), and the results are shown in Table III. The given conditions are as follows: $U_{in} = 100$ V, $G_u = 4$, $P = 1$ kW, $f_s = 100$ kHz, $\Delta i_L / I_L = 20\%$, $\mu_r = 40$, $B_{\max} = 0.15$ T, $\Delta u_C / U_C = 0.1\%$, $\varepsilon_r = 12.9$, $E_{\max} = 900$ V/μm. The last column indicates that for different topologies, K_{power} is directly proportional to the volume of ESM, with the 136 cm^3 being due to calculation errors. Thus, K_{power} can effectively represent power density, validating the analysis in Section IV.

B. Experimental Verification

According to Section V, the topology C-P[LC-S(L)P_MS]S-C of category 8 has both lower switch voltage stress and higher power density. Therefore, it is chosen for experimental verification to validate the feasibility of the synthesized topologies, as shown in Fig. 11.

According to Section III-D, ideal switches are implemented using MOSFETs and diodes. The circuit is shown in Fig. 19, and the experimental prototype is shown in Fig. 20. The parameters are listed in Table IV.

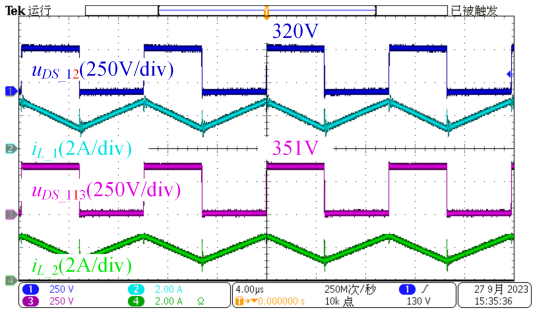
The key waveforms for 320 and 480 V input voltages are shown in Fig. 21, where u_{DS12} and u_{DS113} are the drain-source voltages of the MOSFETs and i_{L1} and i_{L2} are the currents of the inductors. The OFF-state voltage of both the MOSFETs and

TABLE III
DESIGN AND VOLUME OF ESM FOR FOUR REPRESENTATIVE STEPUP CONVERTERS

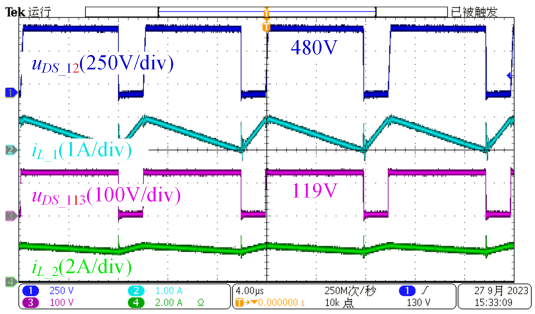
Representative Topology	Category	D_1	K_{power}	L	C	$V_{L\_ESM} + V_{C\_ESM}$	$\frac{V_{L\_ESM}+V_{C\_ESM}}{K_{\text{power}}}$
C-P(L)S-C (Boost)	2	0.750	0.750	375 μH	25.0 μF 46.9 μF	102 cm^3	135 cm^3
C-P[P(L)S-CL_MS]S-C	5	0.566	1.17	377 μH 1130 μH	142 μF 142 μF 35.4 μF	158 cm^3	135 cm^3
C-P[LC-S(L)P_MS]S-C (Experimental Prototype)	8	0.791	0.907	417 μH 1250 μH	157 μF 52.3 μF 1.60 μF	123 cm^3	136 cm^3
C-P(L)S-C-P(L)S-C_MS	10	0.500	1.00	250 μH 1000 μH	25.0 μF 131 μF 31.3 μF	135 cm^3	135 cm^3

TABLE IV
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Item	Detail	Item	Detail
U_{in}	320–480 V	f_s	100 kHz
U_{out}	500 V	S_{12}, S_{113}	SCT3060AL
P_{out}	1 kW	D_{22}, D_{214}	CI30S65D3L2
L_1 L_2	997 μH 528 μH	C_1 C_{23} C_4	56 μF×2 56 μF×3 15 μF×2



(a)



(b)

Fig. 21. Experimental waveforms of u_{DS_12}, i_{L_1}, u_{DS_113}, and i_{L_2} at 500 V output voltage. (a) 320 V input voltage. (b) 480 V input voltage.

the diodes is lower than the output voltage of 500 V, validating the analysis in Section V.

The efficiency curves, thermal images, and loss breakdown comparisons under two input voltages are shown in Figs. 22, 23, and 24, respectively. Based on the conclusion of Section IV, K_{power} of this topology at input voltages of 320 and 480 V is 53%

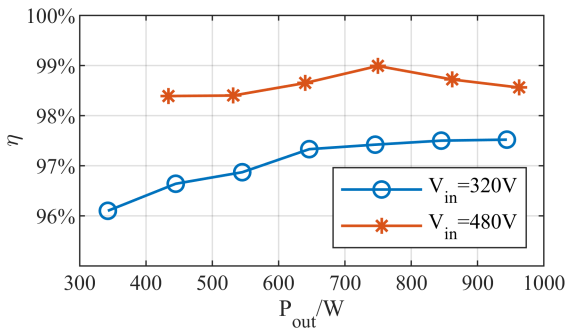
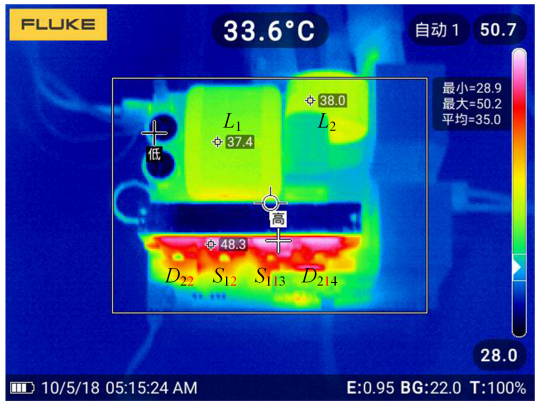
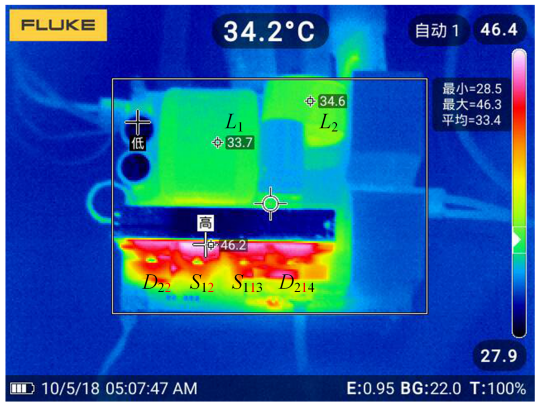


Fig. 22. Output power versus efficiency of the prototype.



(a)



(b)

Fig. 23. Thermal images with fan at 1 kW. (a) 320 V input voltage. (b) 480 V input voltage.

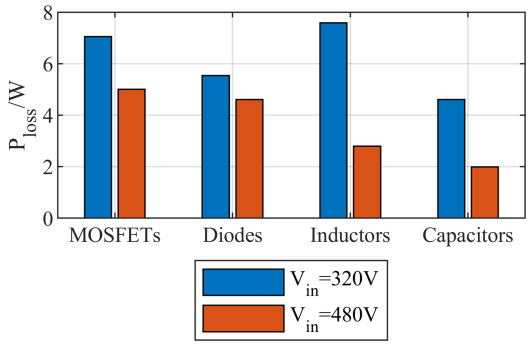


Fig. 24. Loss breakdown comparisons.

and 7.2%, respectively. Therefore, compared to the former case, the prototype achieves higher efficiency and lower temperature in the latter case, with a maximum efficiency of 98.99%.

VII. Conclusion

This article investigates the systematic topology synthesis and power density visualization of PPP architecture. PPP topologies overlap significantly with existing nonisolated topologies. To enhance the current topology synthesis approach, an in-depth investigation is conducted into the relationships among existing nonisolated topologies. A synthesis method for PPP topologies is proposed, which starts with CLC (buck–boost) and proceeds with six steps. Four categories of topologies with PPP architecture, including existing and new ones, are synthesized, such as C-P(L)S-C (boost), C-S(L)P-C (buck), C-P[P(L)S-C-S(L)P_MS]S-C (superboost), C-S[P(L)S-C-S(L)P_MS]P-C (superbuck), and new topologies based on CLC-S(CL)P-C, etc. A general expression set for voltage gain is proposed for the convenience of studying the synthesized topologies. By establishing the relationship between the volume of energy storage components and the power converted by the topology, a visualization scheme for the power density of the topology is proposed for the first time. The topology synthesis method centers on a converter rather than individual components. This ensures the avoidance of redundancy or degradation in the topology, offering a fresh perspective for systematically explaining existing topologies. The synthesized new topologies possess advantages such as high power density, low switch voltage stress, and wide range of voltage gain. Through the visualization of topology power density, not only can PPP be clearly defined, but the power density of nonisolated topologies can also be quantitatively evaluated.

Based on the academic contributions of this article, nonisolated topologies can be systematically synthesized and classified from the perspective of PPP. Using the proposed power density visualization scheme, topologies with higher power density, known as PPP topologies, can be selected. Finally, the proposed power density visualization scheme is validated by designing four PPP topologies. The feasibility of the synthesized PPP topologies is confirmed through the experimental prototype of C-P[LC-S(L)P_MS]S-C.

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Ye Tian (Member, IEEE) was born in Tianjin, China, in 1996. He received the B.S. degree in electrical engineering in 2019 from Beijing Jiaotong University, Beijing, China, where he is currently working toward the Ph.D. degree in partial power processing of dc–dc converters.

Yan Li (Member, IEEE) was born in Heilongjiang Province, China, in 1977. She received the B.S. and M.S. degrees in electrical engineering from Yanshan University, Qinhuangdao, China, in 1999 and 2003, respectively, and the Ph.D. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2009.

From 1999 to 2009, she was with Yanshan University. In 2009, she joined the Faculty of Electrical Engineering, Beijing Jiaotong University, where she is currently a Professor with the College of Electrical Engineering. She was a Visiting Scholar with Virginia Tech, USA and Technical University of Munich, Germany. Her current research interests include aerospace power supply, distributed photovoltaic power generation system, safety enhancement technologies for energy storage system, integration technology of rail transit and renewable energy, application technology of new devices.

Bowu Cao was born in Shandong, China, in 1997. He received the B.S. degree in electrical engineering from Shandong Agricultural University, Taian, China, in 2020, and the M.S. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2023.

He is currently working with Qingdao Ainuo Intelligent Instrument Co., Ltd.

Fangyi Wei (Graduate Student Member, IEEE) was born in Shenyang, Liaoning, China, in 1997. She received the B.S. and M.S. degrees in electrical engineering in 2019 and 2023, respectively, from Beijing Jiaotong University, Beijing, China, where she is currently working toward the Ph.D. degree in new energy application technology for rail transit.

Yanxuan Zheng (Graduate Student Member, IEEE) was born in Zhejiang Province, China, in 1999. She received the B.S. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2022, where she is currently working the Ph.D. degree in distributed photovoltaic generation.