Single Switch Asymmetrical High Step-Up DC–DC Converter Based on Differential Connection

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***Abstract*—High-voltage gain converters with differential connection have gained popularity. However, some hypotheses are imposed to achieve these topologies, such as the converters must be mirrored, among others. This fact makes the converters symmetrical and they have two or more switches. To demonstrate that this connection structure allows new combinations, in this article a new single switch and asymmetric topology is proposed based on the differential connection. This topology is based on a boost converter with a coupled inductor and a voltage multiplier cell. Even with a low number of components, the proposed converter has high-voltage gain, the components present low voltage and current stress. To demonstrate that the converter has good performance, two prototypes were built considering different values of the duty cycle and turns ratio of coupled inductor. From there, the maximum efficiency achieved is 97.5% at 200 W.**

***Index Terms*—Asymmetric converter, differential connection, high step-up, high-voltage gain.**

I. Introduction

THE study of high-voltage gain dc–dc converters has gained popularity in recent decades. Given the fact that these converters are applied to renewable energy sources, such as solar panels and fuel cells. Since these provide voltage levels lower than 50 V, thus implying the need to use step-up dc–dc converters to meet the requirements of the voltage dc bus (400 V) [1], [2], [3], [4], [5]. As already known, a classic boost converter theoretically has unlimited static gain when duty cycle approaches the unit; in practice, with high values of duty cycle, the voltage gain and efficiency of these converters are drastically reduced [6], [7], [8], [9]. From this, many approaches have been proposed to improve high-voltage gain converters [10], [11], [12], [13].

A recently presented technique that has gained popularity is the combination of converters with differential connection [14]. This approach, as can be seen in Fig. 1(a), is basically the combination of two converters where the output voltage of each converter is added and subtracted by the input voltage.

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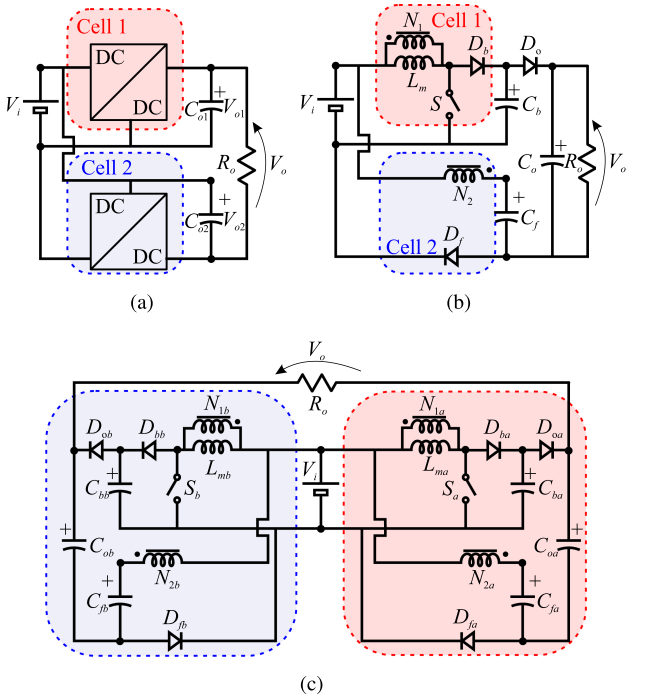

Fig. 1. Topological stages. (a) Differential connections. (b) Proposed converter with a single switch. (c) Proposed converter + mirrored proposed converter + differential load connection.

Furthermore, this type of topology requires different input and output grounding. According to [14], to carry out the differential connection, some assumptions must be made: the converters must be the same; the reference of the chosen converters must be the same; one of the converters must be drawn on its conventional form while the other must be mirrored; among other features. These assumptions lead to good performance. However, it does not allow creating other derivations and possibly finding better and more attractive solutions than conventional ones.

From this, many approaches have been studied and presented in the literature. In [15], basic converters with differential connections are shown, such as boost and SEPIC, among others. To increase the voltage gain of these converters, the article uses switched capacitor cells at the output of the differential connection. Another structure combining classic boost with differential connection is presented in [16]. This approach also places interleaved cells to reduce current stress on the semiconductors. Using the *Qzsource* cell and switched capacitor at [17], this circuit allows achieving high-voltage gains, however, it requires

a high number of components. In [18], an asymmetric combination of differential connection is proposed. This circuit is based on Cuk and buck–boost converters with coupled inductor and voltage multiplier cells. Following the same approach, Guepfrih et al. [19] proposed a symmetric boost converter with voltage multiplier and built-in transformer with differential connection. This approach allows to increase the voltage gain of the converter and achieves soft switching on the semiconductors. Using also coupled inductor, voltage multiplier, and switched capacitor, the topology proposed in [20] is obtained. To achieve soft switching, in this topology two more active switches were added, which increased the complexity and cost.

In this sense, to demonstrate that the differential connection allows reaching new topologies that use circuits of different converters (asymmetric structures) and with a single switch, in this article a new topology of high-voltage gain is proposed. The proposed converter is shown in Fig. 1(b), where it comprises a boost cell, a voltage multiplier cell, and uses the concept of differential connection. This proposed asymmetric differential converter approach has some advantages in relation to symmetric differential converters, such as: a single switch can be used, which allows for simple control and lower gate rive circuits; a low number of components to achieve high-voltage gains. Furthermore, it can be highlighted that the proposed converter presents a new approach to the voltage multiplier technique using a coupled inductor to achieve high-voltage gain. As mentioned in [14], new topologies with differential connections are not new in the literature. There are different variations, such as inverters with differential connection and symmetrical high step-up dc–dc converters with single-ended and double-ended. In this way, the proposed topology can be classified into single-ended high-voltage gain dc–dc converters. This converter can operate in all high-voltage gain dc–dc converter applications mentioned at the beginning of this section. However, following the classical structure of differential converters, as [14], the proposed converter can perform as inverters to generate a pure sinusoidal ac voltage, which requires that the outputs of the converters be symmetrical, as illustrated in Fig. 1(c).

To demonstrate that the converter has good performance, it can be competitive, and it can generate new differential connection topologies, this article is organized as follows: principle of operation in continuous-conduction mode (CCM) and in discontinuous-conduction mode (DCM), voltage gain derivation, external characteristics, voltage stress, current stress, component stress factor (CSF) in Section II. A comparative analysis of the proposed converter with other converters with differential connections is evaluated in Section III. The experimental results and the main conclusion are reported in Sections IV and V, respectively.

II. Theoretical Analysis of the Proposed Topology

In this section, the main theoretical characteristics of the proposed converter are evaluated. As mentioned above, the proposed converter uses the concept of differential connection and comprises: input voltage (V_i), cell 1, and cell 2. Cell 1 basically consists of the boost converter (switch S, diode D_b, and capacitor C_b) with the coupled inductor (primary winding N_1, inductor L_m, leakage inductance L_k). Cell 2 is basically a voltage multiplier, the components being the secondary winding N_2 of the coupled inductor diode D_f, and capacitor C_f. To increase the voltage gain of the converter, the output diode D_o and the output capacitor C_o were added in the converter. This fact will be evident in the converter's evaluations.

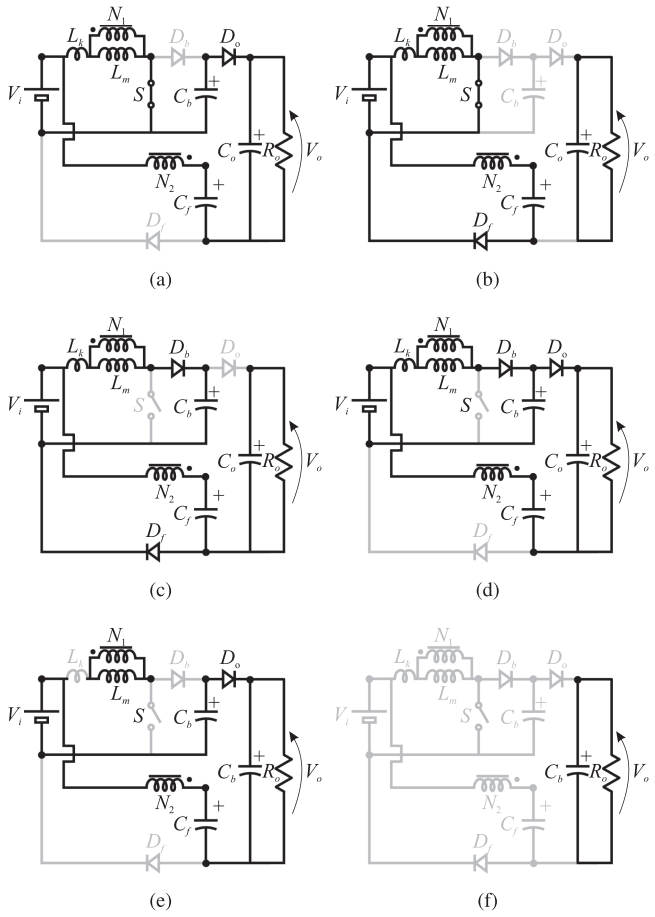

Fig. 2. Topological stages. (a) Stage I. (b) Stage II. (c) Stage III. (d) Stage IV. (e) Stage V. (f) Stage VI.

A. Principle of Operation

In CCM and DCM, the proposed converter presents five stages and four stages for each respectively mode for one switching period in steady state. In CCM, the equivalent circuit and key waveforms of operation are shown in Figs. 2(a)–(e) and 3(a), respectively. For DCM, the circuit for each stage is shown in Fig. 2(b), (d), (e), and (f), and its key waveforms are given in Fig. 3(b).

To describe the principle of operation, the following assumptions were made: the semiconductors devices are ideal; the coupled inductor is modeled by an ideal transformer where the turns ratio is represented by $N = N_2/N_1$, mangetizing inductance (L_m), and a leakage inductance (L_k). The energy from the leakage inductance (L_k) is naturally regenerated and clamped by the capacitor C_b; the capacitors are large enough for their voltage to be considered as constant during one switching

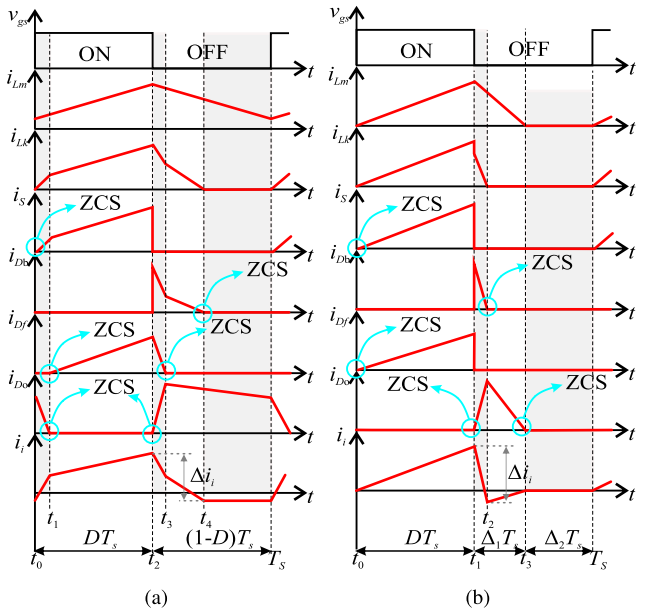

Fig. 3. Typical waveforms. (a) CCM. (b) DCM.

period; components in gray are OFF. Initially, the stages are described in CCM and after that in DCM.

Stage I [$t_0 - t_1$, CCM, Fig. 2(a)]: In this stage, switch S is turned ON with zero current switching (ZCS). It should be noted that, there is no need to add any components to achieve ZCS. To understand this, the current of L_k (i_{Lk}) must be evaluated. As can be seen in Fig. 3, i_{Lk} always starts at zero current, and this current is equal to the switch current S, so the switch will always reach ZCS. Inductor L_m is magnetized by kV_i, where $k = L_m/(L_m + L_k)$, and its current is given by (1) and i_{Lk} is given by (2). Diodes D_b and D_f are reverse-biased, while diode D_o is forward-biased. Capacitor C_o is charged by $V_o = V_{Cb} + V_{Cf} - V_i + V_{N2}$, where V_{N2} has the voltage gain characteristic of the flyback converter ($V_{N2} = NDV_i/(1 - D)$). This stage ends when the diode D_o current reaches zero with ZCS

$$i_{Lm} = \frac{kV_i}{L_m}t + I_{Lm(to)} \tag{1}$$

$$i_{Lk} = \frac{(1-k)V_i}{L_k}t + I_{Lk(to)}. \tag{2}$$

Stage II [$t_1 - t_2$, CCM, Fig. 2(b)]: In this stage, the diode starts its conduction with ZCS. The inductor L_m remains magnetized with the same voltage as the previous stage. Capacitor C_f of the voltage multiplier cell is charged by NkV_i, while capacitor C_o discharges into the load. This stage ends when the switch S is turned OFF.

Stage III [$t_2 - t_3$, CCM, Fig. 2(c)]: In this stage, switch S is blocked and diodes D_b and D_f are forward-biased, while diode D_o is blocked. The inductor L_m is demagnetizing by $k(Vi - V_{Cb})$, and its current is given by (3) and i_{Lk} is given by (4). This stage ends when the diode current i_{Df} reaches ZCS

$$i_{Lm} = \frac{k(V_i - V_{Cb})}{L_m}t + I_{Lm(t2)} \tag{3}$$

$$i_{Lk} = \frac{(1-k)(V_i - V_{Cb})}{L_k}t + I_{Lk(t2)}. \tag{4}$$

Stage IV [$t_3 - t_4$, CCM, Fig. 2(d)]: This stage starts when the diode D_o starts conducting with ZCS. The inductor L_m remains demagnetizing and all capacitors are charging. This stage ends when the leakage inductance current (L_k) reaches zero and the diode D_b is blocked with ZCS.

Stage V [$t_4 - T_s$, CCM, Fig. 2(e)]: This is the last stage of the CCM and it ends when switch S is turned ON. Inductor L_m and capacitors remain with the same characteristics as in the previous stage.

Now, the stages in DCM are described.

Stage I [$t_0 - t_1$, DCM, Fig. 2(b)]: This stage is identical to Stage II in CCM, so it is not necessary to describe this stage. *Stage* II [$t_1 - t_2$, DCM, Fig. 2(d)]: This stage is identical to the stage IV in CCM, so it is not necessary to describe this stage. *Stage* III [$t_2 - t_3$, DCM, Fig. 2(e)]. This stage is identical to the stage V in CCM, so it is not necessary to describe this stage. It should only be noted that this stage ends when the inductor current L_m reaches zero current.

Stage IV [$t_3 - T_s$, DCM, Fig. 2(f)]: In this stage, only the output capacitor (C_o) is operating and supplying energy to the load (R_o). This stage ends when switch S is turned ON.

B. Voltage Gain of Proposed Converter

Initially, the voltage gain in the CCM is shown. To find the static voltage gain of the proposed converter, the volts-second balance principle on the inductor is applied, given by

$$\int_{t_o}^{T_s} v_{L_m} dt = 0. \tag{5}$$

Knowing the operation stages, the ideal voltage gain of the proposed converter is given by

$$M = \frac{V_o}{V_i} = \frac{N+1}{1-D}. \tag{6}$$

The ideal voltage gain of capacitors is given by

$$\frac{V_{Cb}}{V_i} = \frac{1}{1-D} \tag{7}$$

$$\frac{V_{Cf}}{V_i} = N + 1. \tag{8}$$

Considering the leakage inductance (L_k) and following the same approach, the nonideal voltage gain of the proposed converter is given by:

$$M' = \frac{V_o}{V_i} = \frac{kN+1}{1-D}. \tag{9}$$

From this, the voltage gains were plotted and can be seen in Fig. 4. Two turn ratios were chosen ($N = 3$ and $N = 6$). Furthermore, in the laboratory, these inductances L_m and L_k were measured for both cases, thus generating the factor k. Finally, the experimental result was also obtained. As can be seen, the ideal, nonideal, and experimental voltage gain are coherent, that is, varying the duty cycle, the gains are close. Only for $N = 6$, the experimental gain is relatively smaller than the theoretical gains for $D > 0.65$.

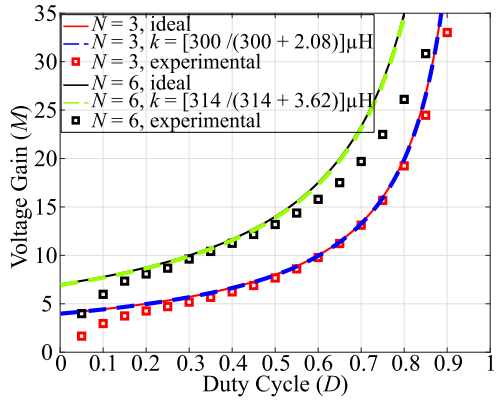

Fig. 4. Static voltage gain curves.

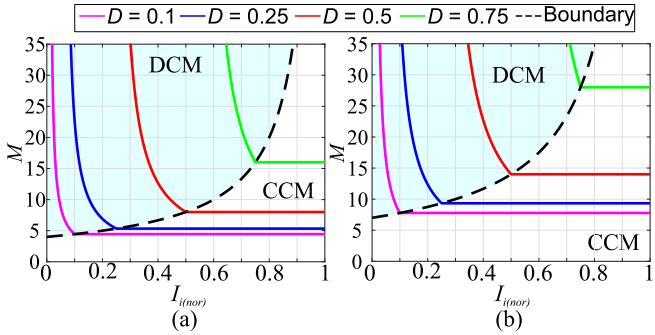

Fig. 5. External characteristics of converter keeping V_i constant. (a) M versus $I_{i(nor)}$ and $N = 3$. (b) M versus $I_{i(nor)}$ and $N = 6$.

C. External Characteristics

Following the methodology presented in [21], the voltage gain in DCM is given by

$$M_{\text{DCM}} = \frac{V_o}{V_i} = \frac{ND + I_{i(\text{nor})}}{I_{i(\text{nor})} - D^2} \tag{10}$$

where $I_{i(\text{nor})} = V_i T_s D(D + \Delta_1)/(2L_m)$.

In boundary conduction mode (BCM) operation, the voltage gain in CCM is equal to DCM, so by [21], the voltage gain in BCM (M_{BCM}) is given by

$$M_{\text{BCM}} = \frac{V_o}{V_i} = \frac{N+1}{1 - I_{i(\text{nor})}}. \tag{11}$$

Fig. 5 shows the external characteristic of the proposed converter. The dashed black line shows the boundary of the CCM and DCM. Knowing the operating stages, the voltage gains, and that the converter is operating in open loop, from this moment on, the proposed converter is evaluated only in the CCM.

D. Semiconductors Voltage Stress

From the operating stage, the voltage stresses on the semiconductors can be found. In relation to switch S, its maximum voltage stress is given by the following:

$$V_S = \frac{V_i}{1-D} = \frac{V_o}{N+1}. \tag{12}$$

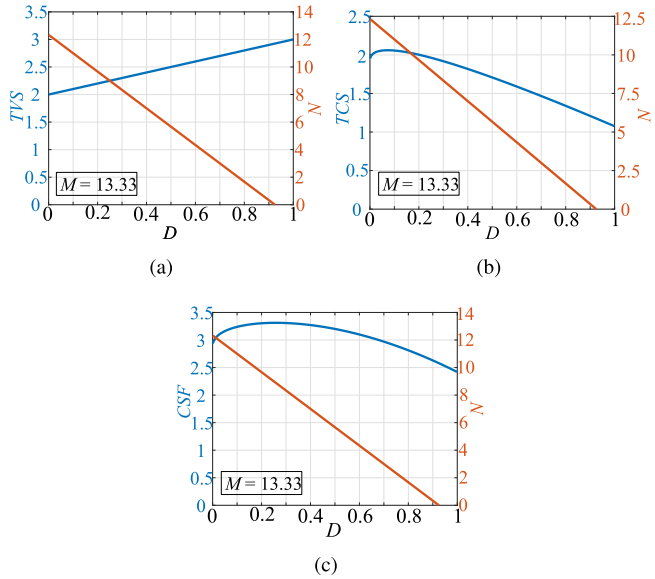

Fig. 6. Factors of (a) TVS, (b) TCS, and (c) CSF.

Regarding the diodes, their voltage stresses are given by

$$V_{Db} = \frac{V_i}{1-D} = \frac{V_o}{N+1} \tag{13}$$

$$V_{Do} = V_{Df} = \frac{NV_i}{1-D} = \frac{NV_o}{N+1}. \tag{14}$$

To evaluate the voltage stress, the total voltage stress (TVS) factor was used. The TVS factor is the sum of the stresses across the semiconductors of the converter, given by

$$\text{TVS} = \sum V_s + \sum V_D. \tag{15}$$

From that, Fig. 6(a) was plotted considering the fixed $M = 13.33$, for different D and N, thus generating the TVS curve. For this evaluation, the voltage gain was considered fixed, consequently, the values of D and N must update to guarantee the desired voltage gain ($M = 13.33$). This way the TVS value is obtained for these values of D and N. For this case, it is evident that by increasing D and decreasing N, the TVS tends to be worse, which means high stress on the components.

E. Current Stress

The semiconductors current stresses are given by

$$I_{s(\text{rms})} = I_i\sqrt{D} \tag{16}$$

$$I_{Db(\text{avg})} = (1-D)(I_i - I_o) \tag{17}$$

$$I_{Df(\text{avg})} = DI_o \tag{18}$$

$$I_{Do(\text{avg})} = (1-D)I_i. \tag{19}$$

The capacitors current stresses are given by

$$I_{Cb(\text{rms})} = I_i\sqrt{1-D} \tag{20}$$

$$I_{Cf(\text{rms})} = I_i\sqrt{1-D} + I_o\sqrt{D} \tag{21}$$

$$I_{Co(\text{rms})} = I_i\sqrt{1-D} + I_o\sqrt{D}. \tag{22}$$

The coupled inductor stresses are given by

$$I_{Lm(\text{rms})} = I_o\,(N+1) \tag{23}$$

$$I_{N2(\text{rms})} = I_i\sqrt{1-D} + I_o\sqrt{D}. \tag{24}$$

To evaluate the current stress, the TCS factor was used. The TCS factor is the sum of the stresses across the semiconductors of the converter, given by

$$\text{TCS} = \sum I_s + \sum I_D. \tag{25}$$

From that, Fig. 6(b) was plotted considering $M = 13.33$, for different D and N, thus generating the TCS curve. For this case, it is evident that by increasing D and decreasing N, the TCS tends to be better, which means lower stress on the components. In this evaluation, the voltage gain is fixed and the normalized input current is considered at $I_i = 1\text{A}$, consequently, the values of D and N must update to guarantee the desired voltage gain. This way the TCS value is obtained for these values of D and N.

F. Component Stress Factor

The CSF analysis is calculated by the multiplication of the maximum voltage of the component and the current stress of the component, and dividing the product by the output power. From this, operating points can be found where the converter presents lower global stress. This implies that you can choose an operating point where the converter can have fewer losses and consequently better efficiency. From this, the CSF factor was calculated and plotted as can be seen in Fig. 6(c). Initially, the CSF starts increasing, which means that for the region of $D < 0.5$ and $N > 6$, the proposed converter presents high stress. On the other hand, for $D > 0.5$ and $N < 6$, the CSF is lower, so this region tends to be better to operate. The same conditions as M, N and D highlighted in the TVS and TCS sections are valid.

G. Input Current Ripple of the Proposed Converter

The input current and the input current ripple of the proposed converter can be seen in Fig. 3. For CCM, this input current can be given as

$$i_{i(t)} = i_{Lk(t)} + i_{N2(t)} \tag{26}$$

Knowing the operation steps and (27), the input current ripple can be rewritten as

$$\Delta i_{i(t)} = \frac{DT_sV_i}{L_m + L_k} + \frac{(1-k)(V_i - V_{Cb})}{L_k}(t_4 - t_2) + I_o\left[2\,(T_s - t_4) - (t_4 - t_2)\right]. \tag{27}$$

As can be seen in Fig. 3, the input current ripple of the differential converters is high. It should be noted that, without using some auxiliary circuit technique, the proposed topology cannot achieve a low input current ripple.

III. Performance Comparison

This section demonstrates a comparative evaluation of the proposed converter with others presented in the literature. In addition, a new type of voltage multiplier technique is demonstrated.

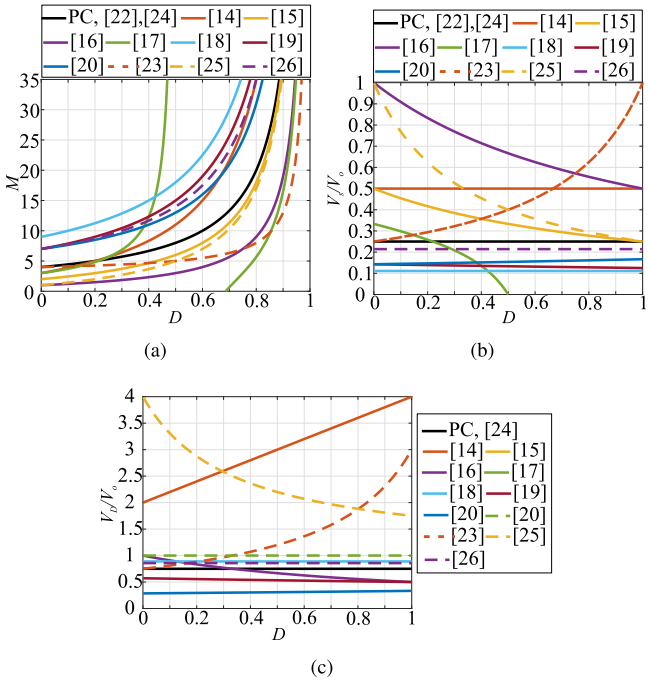

Fig. 7. Comparative evaluation of (a) M versus D, $N = 3$. (b) V_s/V_o versus D, $N = 3$. (c) V_D/V_o versus D, $N = 3$.

A. Performance Comparison

To demonstrate that the proposed topology is competitive and attractive for high-voltage gain applications, Table I presents a comparative analysis of the proposed converter with other high-voltage gain topologies with differential connection [14], [15], [16], [17], [18], [19], [20] and the same number of components with coupled inductor [22], [23], [24], [25], [26]. The first point to highlight is the number of switches. The proposed converter has a single switch among the converters with differential connection, which means lower complexity and a lower auxiliary gate driver circuit. In addition, it has fewer components. Regarding voltage gain and voltage stress on semiconductors, Fig. 7 shows the plotted curves. Fig. 7(a) shows the voltage gain curve of the converters. As can be seen, the proposed converter is among the best voltage gain. Regarding the stress on semiconductors, Fig. 7(b) for the switch and Fig. 7(c) for the diode, the proposed converter presents satisfactory features. In relation to input current ripple, basically, the converters present high ripple current, except for the converter [16]. Furthermore, it should be noted that without any additional switches, the proposed converter can achieve ZCS in semiconductors. From this, it is evident that the proposed topology is attractive for high-voltage gain applications.

B. Proposed Voltage Multiplier Discussion

The voltage multiplier technique with coupled inductor consists of, usually, on the primary side (N_1), the coupled inductor is connected to the branch of a current source converter at the input

TABLE I
COMPARISON EVALUATION

Converter	Gain (M)	Maximum Voltage Stress on Switch	Maximum Voltage Stress on Diode	S	D	L	C	Input Current Ripple
Proposed	$\frac{N+1}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{N+1}$	$\frac{NV_i}{1-D}=\frac{NV_o}{N+1}$	1	3	1	3	High
Fig. 16(a) [14]	$\frac{3+5D}{1-D}$	$\frac{(5D+3)\,V_i}{2\,(1-D)}=\frac{V_o}{2}$	$\frac{(4+4D)\,V_i}{1-D}=\frac{(4+4D)\,V_o}{5D+3}$	4	7	4	3	High
[15]	$\frac{2+2D}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{2+2D}$	$\frac{2V_i}{1-D}=\frac{2V_o}{2+2D}$	2	3	3	4	High
[16]	$\frac{1+D}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{1+D}$	$\frac{V_i}{1-D}=\frac{V_o}{1+D}$	4	0	2	2	Low
[17]	$\frac{3-3D-2D^2}{(1-D)\,(1-2D)}$	$\frac{V_i}{1-D}=\frac{(1-2D)\,V_o}{3-3D-2D^2}$	$\frac{(3D-2)\,V_i}{(1-D)\,(1-2D)}=\frac{(3D-2)\,V_o}{3-3D-2D^2}$	2	3	3	5	High
[18]	$\frac{2N+3}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{3+2N}$	$\frac{(2+2N)\,V_i}{1-D}=\frac{(2+2N)\,V_o}{3+2N}$	2	4	2	5	High
[19]	$\frac{2N+1+D}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{2N+1+D}$	$\frac{(N+1)\,V_i}{1-D}=\frac{(N+1)\,V_o}{2N+1+D}$	2	4	4	6	High
[20]	$\frac{7-D}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{7-D}$	$\frac{2V_i}{1-D}=\frac{2V_o}{7-D}$	4	6	2	8	High
Fig. 14(a) [22]	$\frac{N+1}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{N+1}$	$\frac{(N+1)V_i}{1-D}=V_o$	1	2	2	2	High
T1-CL [23]	$\frac{N+1-ND}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{N+1-ND}$	$\frac{NV_i}{1-D}=\frac{NV_o}{N+1-ND}$	1	2	1	3	High
[24]	$\frac{N+1}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{N+1}$	$\frac{NV_i}{1-D}=\frac{NV_o}{N+1}$	1	3	1	3	High
[25]	$\frac{ND+1}{1-D}$	$\frac{V_i}{1-D}=\frac{V_o}{ND+1}$	$\frac{(ND+1+N)V_i}{1-D}=\frac{(ND+1+N)V_o}{ND+1}$	2	2	1	1	High
[26]	$\frac{2+N_1-N_2}{(1-N_2)(1-D)}$	$\frac{V_i}{1-D}=\frac{V_o}{2+N_1-N_2}$	$\frac{(ND+1+N)V_i}{1-D}=\frac{(3+N_1)(1-N_2)V_o}{2+N_1-N_2}$	1	3	1	4	High

(such as boost converter), as shown in Fig. 8(a). While on the secondary side (N_2) of the coupled inductor, commonly, a diode (D_f) and a capacitor (C_f) are combined to achieve the voltage gain. Of course, more diodes and capacitors can be associated in this configuration.

Considering the coupled inductor converters presented in Table I, different voltage multiplier circuits can be redesigned. Initially, it should be noted that the evaluations described below, considering the primary side of the coupled inductor according to Fig. 8(a). The first approach given in Fig. 8(b) are illustrated in [18] and [23]. As can be seen, considering that the capacitor (C_f) charges with the voltage NV_i. This also occurs for the other voltage multiplier circuit, Fig. 8(c), these being presented in [19] and [22]. For this circuit, the capacitor (C_F) is charged by NV_i. The same happens for the circuit in Fig. 8(d) [24].

In the case of the proposed converter, a new voltage multiplier circuit can be obtained. As can be seen in Fig. 8(e), the circuit mesh that charges the capacitor (C_f) is composed of V_i and $V_{N2} = NV_i$. Thus, it is evident that the capacitor is charged by $(N+1)V_i$. This clearly demonstrates that the proposed multiplier circuit has a higher voltage gain compared to the other circuits discussed. Thus, demonstrating more advantages of the proposed topology. Finally, this approach allows new topologies to be generated and derived using the proposed voltage multiplier circuit.

IV. EXPERIMENTAL RESULTS

Two 250-W laboratory prototypes were assembled and tested with the specifications given in Table II in open-loop and the photo of the prototype is shown in Fig. 9. For this, two coupled inductors were built with different values of turn ratio, $N = 3$ and $N = 6$. Thus, to reach the desired voltage gain ($M = 13.33$), two duty cycle were used, $D = 0.7$, and $D = 0.475$. Hence, the converter passive and active components are designed according to ordinary switching power supply design methodologies presented in [21] and [27]. These choices were made from the TCS, TVS, and CSF factors shown in Fig. 6, where it can be

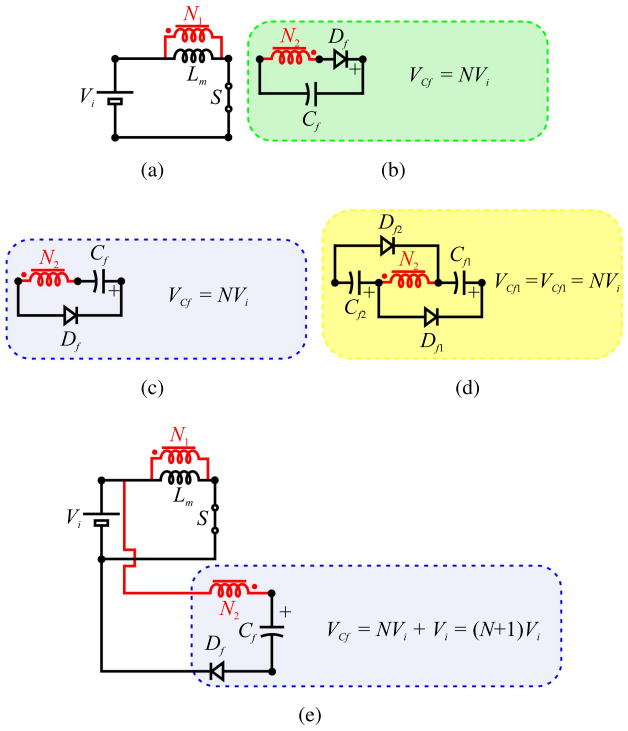

Fig. 8. Circuits. (a) Boost converter with primary side of coupled inductor. (b) Voltage multiplier 1. (c) Voltage multiplier 2. (d) Voltage multiplier 3. (e) Proposed voltage multiplier.

TABLE II
SPECIFICATIONS AND COMPONENTS OF THE CONVERTER

Symbol	Name	Value
P_i	Input Power	250 W
M	Voltage Gain	13.33
V_o	Output Voltage	400 V
V_i	Input Voltage	30 V
f_s	Switching Frequency	50 kHz
S	Switch	IPB044N15N5 (150 V, 123 A, 5 mΩ)
$D_o ll$	All Diodes	STTH20R04FP (400 V, 20 A, v_f = 0.8 V)
L_m, L_k and N	Coupled inductor 1	330 μH, 2.08 μH, 3 (17 mΩ, 35 mΩ) Core E-55
L_m, L_k and N	Coupled inductor 2	314.3μH, 3.62 μH, 6 (15 mΩ, 65 mΩ) Core E-55
C_{all}	All Capacitors	9 μF (15 mΩ)

seen that $D > 0.5$, the stresses are lower. These two options of $N = 3$ and 6 allow us to use two different duty cycle. Thus, a reduction in magnetic losses can be seen, as presented in this section. Thus, to demonstrate that these evaluations are coherent, two operating points were chosen to evaluate experimentally. A TMS320F28335 Digital Signal Processor was implemented to provide the PWM signal. An Agilent E4360A dc voltage source was used to provide the input voltage source. To perform the measurements, Tektronix Encore MD03000 oscilloscope was used to measure the experimental waveforms and Yokogawa WT1800 power meter to measure the efficiency.

Initially, the experimental results shown in Fig. 10 are to validate the voltage gain of the converter. The experimental results are for the two prototypes, on the left side for $N = 3$ and $D = 0.7$, and on the right side $N = 6$ and $D = 0.475$. Fig. 10(a) and (b) shows the experimental waveforms of v_gs signal (D), input voltage $v_i = 30$ V, and output voltage $v_o = 400$ V. For $N = 3$, Fig. 10(c) shows capacitor C_b voltage $v_{Cb} = 100$ V, capacitor C_f voltage $v_{Cb} = 120$ V. For $N = 6$, Fig. 10(c) shows capacitor C_b voltage $v_{Cb} = 57.14$ V, capacitor C_f voltage $v_{Cb} = 210$ V. For these results, it is clear that the option of $N = 3$ has more attractive results, since the voltage in the capacitors has low voltage values.

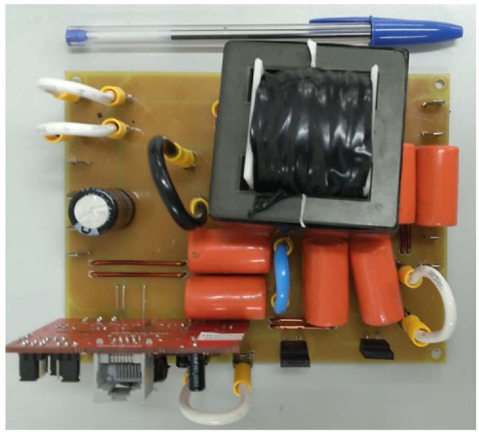

Fig. 9. Proposed converter photograph.

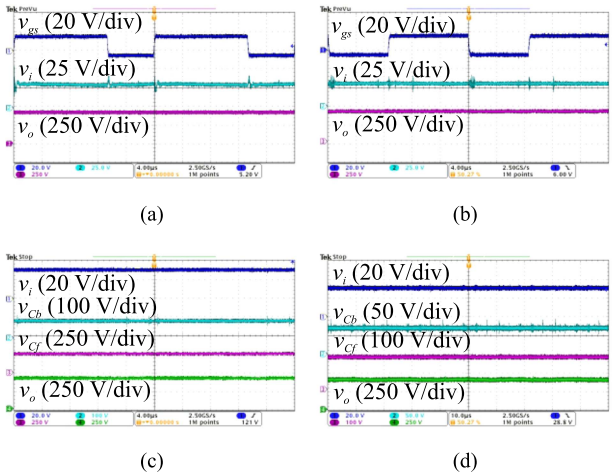

Fig. 10. Experimental waveforms of (a) v_{gs}, v_i, and v_o for $N = 3$ (4 μs/div). (b) v_{gs}, v_i, and v_o for $N = 6$ (4 μs/div). (c) v_i, v_{Cb}, v_{Cf}, and v_o for $N = 3$ (10 μs/div). (d) v_i, v_{Cb}, v_{Cf}, and v_o for $N = 6$ (10 μs/div).

To demonstrate the voltage stress on semiconductors and the ZCS results, Figs. 11 and 12 illustrate these experimental results. For $N = 3$, Fig. 11(a) presents the results of voltage and current on semiconductors S and D_b. As expected, the maximum voltage of these semiconductors are 100 V. It should be noted that there is a voltage spike at switch S caused by the leakage inductance L_k. There is no need to include any type of auxiliary clamp circuit, since the capacitor C_b is a natural clamp of the proposed converter. Fig. 11(c) depicted the ZCS results, switch S shows ZCS at turn ON while diode D_b shows ZCS at turn OFF. Fig. 12(a) shows of voltage and current on semiconductors D_o and D_f. The maximum voltage in these semiconductors are $v_{Do} = v_{Df} = 300$ V. Furthermore, Fig. 12(c) demonstrates that these semiconductors achieve ZCS at turn ON and OFF. For $N = 6$, Fig. 11(b) presents the results of voltage and current on semiconductors S and D_b. The maximum voltage of these semiconductors is 57 V. Also, there is a voltage spike at switch

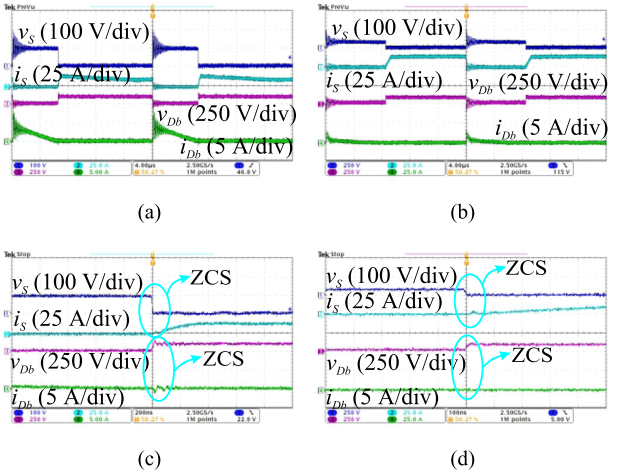

Fig. 11. Experimental waveforms of (a) v_s, i_s, v_{Db}, and i_{Db} for $N = 3$ (4 μs/div). (b) v_s, i_s, v_{Db}, and i_{Db} for $N = 6$ (4 μs/div). (c) ZCS of S at turn ON and ZCS of D_b at turn OFF for $N = 3$ (0.2 μs/div). (d) ZCS of S at turn ON and ZCS of D_b at turn OFF for $N = 6$ (0.2 μs/div).

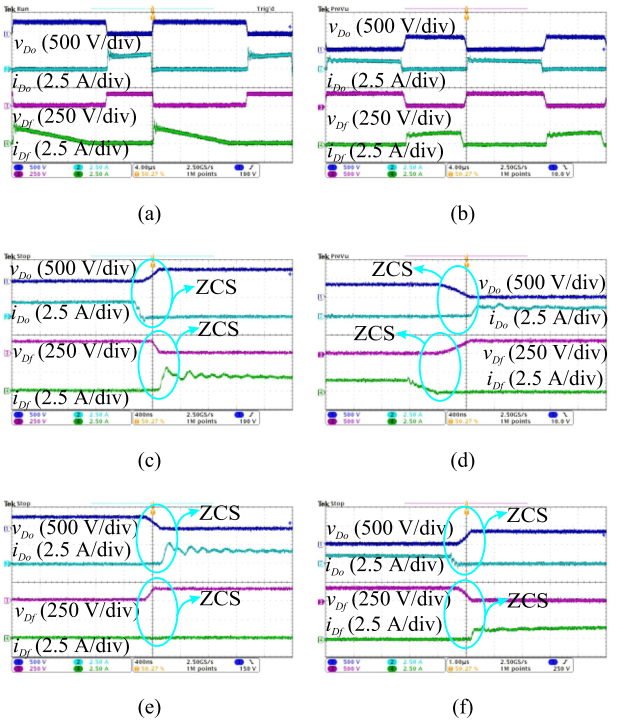

Fig. 12. Experimental waveforms of (a) v_{Do}, i_{Do}, v_{Df}, and i_{Df} for $N = 3$ (4 μs/div). (b) v_{Do}, i_{Do}, v_{Df}, and i_{Df} for $N = 6$ (4 μs/div). (c) ZCS of Db at turn OFF and ZCS of D_f at turn ON for $N = 3$ (0.4 μs/div). (d) ZCS of Db at turn OFF and ZCS of D_f at turn ON for $N = 6$ (0.4 μs/div). (e) ZCS of Db at turn ON and ZCS of D_f at turn OFF for $N = 3$ (0.4 μs/div). (f) ZCS of Db at turn ON and ZCS of D_f at turn OFF for $N = 6$ (1 μs/div).

S caused by the leakage inductance L_k. Fig. 11(d) depicted the ZCS results, switch S shows ZCS at turn ON, while diode D_b shows ZCS at turn OFF. Fig. 12(b) shows the voltage and current on semiconductors D_o and D_f. The maximum voltage in these semiconductors is $v_{Do} = v_{Df} = 342$ V. Furthermore, Fig. 12(d) demonstrates that these semiconductors achieve ZCS at turn ON and OFF. Again, the option of $N = 3$ has better results, since it presents lower stress.

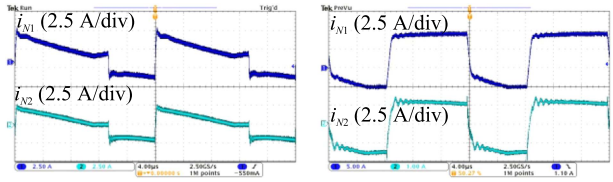

Fig. 13. Experimental waveforms of (a) i_{N1} and i_{N2} for $N = 3$ (4 μs/div). (b) i_{N1} and i_{N2} for $N = 6$ (4 μs/div).

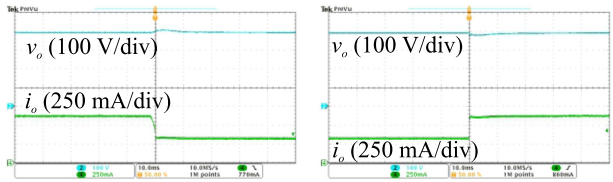

Fig. 14. Dynamic response of the proposed converter. (a) Load step 250–125 W (10 ms/div). (b) Load step 125–250 W (10 ms/div).

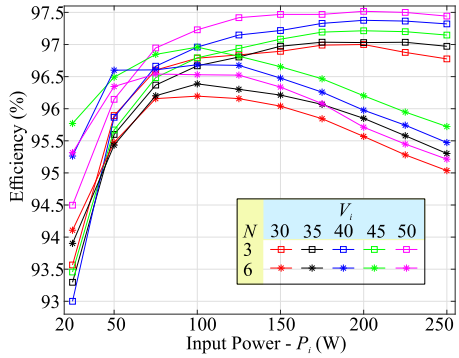

Fig. 15. Efficiency versus input power under different V_i.

In Fig. 13, the current results of the coupled inductor windings are presented. Fig. 14 demonstrates experimental results on the closed-loop dynamic response of the proposed converter considering load step. During the experiment, the output voltage is controlled to be stabilized at 400 V by the PI controller. In Fig. 14(a), the converter is operating at nominal power (250 W), and subsequently, a load step is applied to 125 W, and in Fig. 13(b), the opposite was done. In both cases, the proposed converter achieved a satisfactory response.

Fig. 15 shows the efficiency of the proposed converter under different input power values and input voltage voltage. As expected, the results for $N = 3$ perform better for $N = 6$. As can be seen in Fig. 15, different evaluations were made, different values of N and D and input voltage V_i. This allows checking the variation in voltage gain of the proposed converter considering different cases, in order to demonstrate which is the best operating option. The proposed converter achieves attractive efficiency results, having a maximum peak of 97.51 % for $V_i = 50$ V, $P_i = 200$ W, and $N = 3$. Regarding the nominal input voltage ($V_i = 30$ V), the maximum efficiency achieved is 97.00 % at $P_i = 200$ W, and $N = 3$.

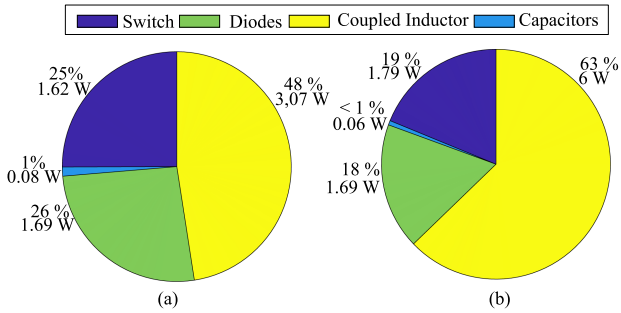

Fig. 16. Losses distribution. (a) For $D = 0.7$ and $N = 3$. (b) For $D = 0.475$ and $N = 6$.

Knowing the parameters and specifications of the proposed converter, it is possible to estimate the losses. Switch S presents conduction and switching losses, given by

$$P_S = R_{DS(\text{on})} {I_{S(\text{rms})}}^2 + 0.5 f_s V_s \left[I_s \left(t_{\text{off}} \right) + C_{\text{OSS}} \right] \tag{28}$$

where $R_{DS(\text{on})}$ is the MOSFET ON-state resistance, t_{off}, t_{on}, and C_{OSS} were estimated by the fall time provided in the device manufacture's datasheet, f_s is the switching frequency.

In relation to the diodes (D_b, D_f, and D_o), their losses are given by

$$P_D = v_f I_{D(\text{avg})} + r_D {I_{D(\text{rms})}}^2 \tag{29}$$

where in the manufacturer datasheet can be estimated the diode conduction resistance r_D, and the forward drop voltage v_f of diodes.

Since the semiconductors operate with ZCS, switch is turned ON with ZCS and diodes are turned ON and OFF with ZCS, the switching losses are relatively low.

The coupled inductor losses are given by

$$P_{\text{CI}} = r_{N1} {I_{Lk(\text{rms})}}^2 + r_{N2} {I_{N2(\text{rms})}}^2 + V_e f_s^a K_c \Delta B^b \tag{30}$$

where r_{N1} and r_{N2} are the copper wire resistance of CI, V_e is the core volume, K, c, a, and b are constants provided by the manufacturer's datasheet.

Capacitors losses, C_b, C_f, and C_o, are given by

$$P_C = ESR {I_{C(\text{rms})}}^2 \tag{31}$$

Considering the voltage and current stresses and the parameters given in Table II and the nominal power condition, the estimated losses and efficiency can be calculated by

$$P_{\text{all}} = P_S + \sum_{i=b}^{f,o} P_{Di} + P_{\text{CI}} + \sum_{i=b}^{f,o} P_{Ci} \tag{32}$$

$$\eta = 100\% \left(P_i - P_{\text{all}} \right) / P_i. \tag{33}$$

Fig. 16 shows the distribution of component losses considering the nominal operating point, $V_i = 30$ V, $V_o = 400$ V, and $P_i = 250$ W. For $N = 3$, the converter has a considerably lower loss in relation to the coupled inductor. Finally, it should be remembered that the results of the voltage gain curve are shown in Fig. 4.

According to [28], the converter power density (CPD) can be calculated as

$$\text{CPD} = \frac{P_o}{2 \sum \text{Vol}} \tag{34}$$

where the factor 2 is used to compensate for the volumes of the components not considered. From this, considering the volume of all the components of the converter and knowing the output power, for: $N = 3$, the CPD is 0.868 W/cm^3; and for $N =$, the CPD is 0.566 W/cm^3.

V. Conclusion

Initially, it can be said that the first conclusion of the article is that it is possible to achieve a topology with differential connection with asymmetric cells and with a single switch. In addition, the proposed topology demonstrated high-voltage gain, low voltage stress, and current on the components. From the evaluation of the stress, it is evident that the proposed converter has better performance for high duty and low turns ratio of coupled inductor with $M = 13.33$. Regarding the comparative evaluations, the proposed topology stands out in the aspect of the low number of components, mainly in relation to the number of switches. In addition, it has competitive voltage gain, and voltage stress on semiconductors. However, this type of converter with differential connection has the disadvantage of high input current ripple and requires different grounding between the converter input and output. Finally, the experimental results demonstrated that the best operation option is for $D = 0.7$ and $N = 3$, having reached a peak efficiency of 97.5% at 200 W. Besides that, experimental results show the ZCS condition for the main switch and the diodes, reducing switching losses of the converter. This set of factors demonstrates that the proposed converter is attractive for high-voltage gain applications and also allows new asymmetric topologies with differential connection to be generated.

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