

# Single-Input Dual-Output Digital Gate Driver IC Automatically Equalizing Drain Current Variations of Two Parallel-Connected SiC MOSFETs

Kohei Horii<sup>1</sup>, Katsuhiko Hata, *Member, IEEE*, Shin-Ichiro Hayashi<sup>2</sup>, *Member, IEEE*, Keiji Wada<sup>3</sup>, *Senior Member, IEEE*, Ichiro Omura, *Member, IEEE*, and Makoto Takamiya<sup>4</sup>, *Senior Member, IEEE*

**Abstract**—A single-input, dual-output digital gate driver (DGD) IC is proposed, to solve the device characteristic variation problem and the parasitic inductance variation problem on PCBs in two parallel-connected SiC MOSFETs. This article is the first in the world to achieve all of 1) fully integrated two sensor output processing circuits, two DGDs and a controller required to detect and equalize the drain current variation of two parallel-connected SiC MOSFETs on a gate driver IC, 2) equalization of dc and surge components of drain current of each MOSFET in a closed loop, and 3) demonstration measurements of drain current equalization under a total of four conditions, with and without SiC MOSFET characteristic variations and with and without parasitic inductance variations.

**Index Terms**—Drain current, gate driver, parallel, SiC MOSFETs.

## I. INTRODUCTION

THE target of this article is to provide an active gate driver IC integrated on a single chip that detects variations in the drain current flowing through each of two parallel-connected silicon carbide (SiC) MOSFETs and automatically equalizes the drain current. In order to expand the application of power electronics to high-power areas such as renewable energy and electric vehicles, it is essential to increase the current of power converters. In power electronics applications where the current greater than the rated current of the power device is required, power devices are connected in parallel. A technical challenge in parallel-connected power devices is the generation of hot spots,

Received 7 April 2024; revised 22 July 2024; accepted 9 September 2024. Date of publication 17 September 2024; date of current version 12 December 2024. This work was supported by NEDO under Grant JPNP14004. Recommended for publication by Associate Editor D. Dong. (*Corresponding author: Makoto Takamiya.*)

Kohei Horii was with The University of Tokyo, Tokyo 153-8505, Japan. He is now with the Toshiba Corporation, Kanagawa 212-8582, Japan.

Katsuhiko Hata was with The University of Tokyo, Tokyo 153-8505, Japan. He is now with the Shibaura Institute of Technology, Tokyo 135-8548, Japan.

Shin-Ichiro Hayashi was with the Tokyo Metropolitan University, Tokyo 191-0065, Japan. He is now with the Chiba Institute of Technology, Chiba 275-0016, Japan.

Keiji Wada is with the Tokyo Metropolitan University, Tokyo 191-0065, Japan.

Ichiro Omura is with the Kyushu Institute of Technology, Fukuoka 808-0196, Japan.

Makoto Takamiya is with The University of Tokyo, Tokyo 153-8505, Japan (e-mail: mtaka@iis.u-tokyo.ac.jp).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2024.3462535>.

Digital Object Identifier 10.1109/TPEL.2024.3462535

where current concentrates in some power devices and generates heat locally. Since hot spots determine the system lifetime of the entire power converters, it is very important to avoid hot spots by equalizing the currents of parallel-connected power devices. Current nonuniformity problems between parallel-connected power devices are more severe in SiC MOSFETs than in silicon power devices [1]. There are three reasons for this as follows.

- 1) Due to the poor crystal quality of SiC compared to silicon, the chip area of SiC MOSFETs is smaller than that of silicon power devices, so the number of parallel connections must be increased for SiC compared to silicon to achieve the required current.
- 2) Compared to silicon power devices, SiC MOSFETs have larger variations in device characteristics (e.g., threshold voltage, transconductance, and  $C_{ISS}$ ) than silicon power devices due to the lack of mature device manufacturing technologies. Therefore, compared to silicon, SiC has a larger dc and dynamic (surge) [5], [6] variation of current between parallel-connected power devices.
- 3) Due to the high switching speed of SiC MOSFETs compared to silicon power devices, SiC has a larger surge component variation of current between parallel-connected power devices due to parasitic inductance variation compared to silicon. Therefore, compared to silicon, SiC is prone to power device breakdown due to large surge voltage and/or surge current.

Many research works [1] have been conducted to equalize the current in parallel-connected SiC MOSFETs or silicon IGBTs, such as

- 1) a method to measure the electrical characteristics of power device chips and preselect chips with matching characteristics before mounting the chips in power modules;
- 2) layout design method to reduce parasitic inductance variations inside power modules and on PCBs;
- 3) methods using current transformer;
- 4) methods of gate waveform control using active gate drivers [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27].

None of the above methods, however, is practical, because they increase either test cost, design cost, component cost, or component size. 1) increases the test cost, 2) increases the design cost, and 3) increases the component cost and size.

This article focuses on “4) methods of gate waveform control using active gate drivers,” because the active gate drivers have the potential to solve the above issues by integrating the circuits required to equalize the current into a gate driver IC. Most prior works [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [22], [23], [24], [25], [26], [27] have used three or more general-purpose ICs to realize the current sensors, controller, and active gate drivers required for current equalization of parallel-connected power devices, which is not practical due to the increased component cost and component size. In [21], a current sensor, a controller, and an active gate driver are integrated on a single chip to equalize the collector current of two parallel-connected IGBTs. The work [21], however, is not practical, because it does not have a function to equalize the dc component variation of the collector current and measurements addressing IGBT variations and parasitic inductance variations are not shown.

To solve the problems, in this article, a single-input, dual-output (SIDO) digital gate driver (DGD) IC, which integrates the sensor output processing circuits, controller, and active gate drivers necessary to equalize the drain current ( $I_{D1}$  and  $I_{D2}$ ) of two parallel-connected SiC MOSFETs on a single chip, is proposed. SIDO DGD IC is practical, because it automatically performs both the equalization of the dc component ( $I_{D1,DC}$  and  $I_{D2,DC}$ ) and the surge component ( $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ ) of  $I_{D1}$  and  $I_{D2}$ , respectively, which does not increase test cost, design cost, component cost, or component size. SIDO DGD IC is innovative in that it automatically solves both the device characteristic variation problem and the parasitic inductance variation problem in parallel-connected power devices using a gate driver IC.

We previously reported at [20] on the first-generation SIDO DGD IC, which integrates the sensor output processing circuits, controller, and active gate drivers necessary for SiC MOSFET drain current equalization, all on a single chip for the first time in the world. In this article, the second-generation SIDO DGD IC is reported, which solves the problems of the first generation IC (details are described later in Fig. 7). The three main differences between paper [20] and this article are as follows. See also Table II for details.

- 1) Active gate driving methods are different. While work [20] used the simple  $V_{GS1}$  control shown in Fig. 7(b) and the  $V_{GS1}$  and  $I_{G2}$  control shown in Fig. 7(c), this article uses the gate amplitude twice control (GATC) shown in Fig. 7(d). As a result, as shown in Fig. 25(c) and (d), this article reduced the switching losses by 59% compared to [20].
- 2) The function of current sensor and closed loop are different. In [20],  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization was achieved in a closed loop using current sensors measuring  $I_{D1,DC}$  and  $I_{D2,DC}$ , but there was no function to achieve  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization. On the other hand, in this article, using two types of current sensors that measure  $I_{D1,DC}$  and  $I_{D2,DC}$  and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ ,  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization are both achieved in a closed loop, as shown in Figs. 17–20.

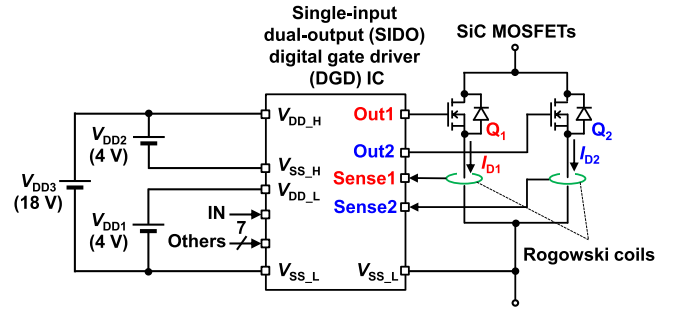


Fig. 1. Circuit schematic of proposed single-input dual-output (SIDO) digital gate driver (DGD) IC and two SiC MOSFETs  $Q_1$  and  $Q_2$  connected in parallel.

- 3) Two parallel-connected SiC MOSFETs have different variation conditions. The paper [20] performed demonstration measurements of drain current equalization in only one condition of two SiC MOSFETs of the same model number with different threshold voltages under the condition of no parasitic inductance variation. On the other hand, in this paper, demonstration measurements of drain current equalization (see Figs. 17–20) are conducted under a total of four conditions (see Fig. 14), with and without SiC MOSFET characteristic variations and with and without parasitic inductance variations. In addition, in order to emulate SiC MOSFETs with large variations in device characteristics, SiC MOSFETs from different manufacturers shown in Table I are used.

The greatest contribution of this article is the integration of all the circuits required for  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization into a single chip, as will be shown later in Table II, the row “Functions integrated into gate driver IC.” The main challenge of integrating these functions into a single chip is how to generate the voltage for variable  $V_{GS}$  amplitude using only the internal circuits of the IC without increasing the number of external components outside the IC in order to realize  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization using GATC shown in Fig. 7(d). For example, in [26] in Table II, three buck converters are used to achieve variable  $V_{GS}$  amplitude to achieve  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization, but this does not satisfy our design goal because the buck converters add many external components (inductors and capacitors) outside the IC. The innovation to solve the problem is the proposed DGD-based  $V_{GS}$  amplitude control, where details are described later in Fig. 4.

## II. PROPOSED DRAIN CURRENT EQUALIZATION USING SIDO DGD IC

### A. Overall Circuits of SIDO DGD IC

Fig. 1 shows a circuit schematic of the proposed SIDO DGD IC and two SiC MOSFETs  $Q_1$  and  $Q_2$  connected in parallel. In order to equalize the variation of dc ( $I_{D1,DC}$  and  $I_{D2,DC}$ ) and surge ( $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ ) components of  $I_D$  of  $Q_1$  and  $Q_2$  ( $I_{D1}$  and  $I_{D2}$ ) due to the variation of device characteristics and the parasitic inductance of MOSFETs, SIDO DGD IC is newly

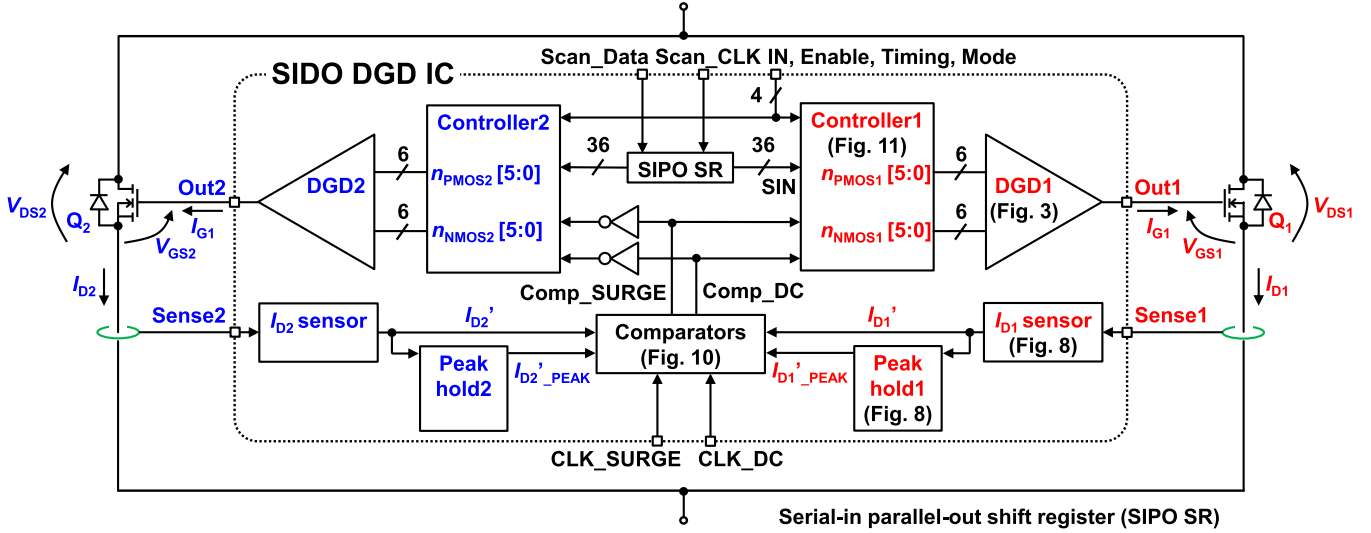


Fig. 2. Circuit schematic of the proposed SIDO DGD IC.

developed. Except for the PCB Rogowski coil [28] inserted in the source pins of  $Q_1$  and  $Q_2$ , all functions required for current equalization of  $I_{D1}$  and  $I_{D2}$  are integrated in SIDO DGD IC. As shown in Fig. 1, no external gate resistors are used in this article. This is because, in DGDs, the gate current is programmable, eliminating the need for an external gate resistor.

SIDO DGD IC has the function of feedback control of Out1 and Out2 for each switching to equalize  $I_{D1}$  and  $I_{D2}$  by measuring  $I_{D1}$  and  $I_{D2}$  at the outputs Sense1 and Sense2 of two PCB Rogowski coils. SIDO DGD IC has an “IN” input, which is the on/off input of the gate driver, and seven “Others” input pins (see Fig. 2 for details). The 18 V supply ( $V_{DD3}$ ) between  $V_{DD\_H}$  and  $V_{SS\_L}$  determines the output voltage of the gate driver. The 4 V power supplies between  $V_{DD\_L}$  and  $V_{SS\_L}$  ( $V_{DD1}$ ) and between  $V_{DD\_H}$  and  $V_{SS\_H}$  ( $V_{DD2}$ ) are for low-side and high-side of SIDO DGD IC, respectively.

Fig. 2 shows a circuit schematic of the proposed SIDO DGD IC. The sensor output processing circuits that measures  $I_{D1}$  of  $Q_1$  ( $I_{D1}$  sensor), the digital gate driver (DGD1) that controls the gate–source voltage  $V_{GS1}$  of  $Q_1$  and its controller (Controller1) are shown in red letters. Similarly, the sensor output processing circuits that measures  $I_{D2}$  of  $Q_2$  ( $I_{D2}$  sensor) and the digital gate driver (DGD2) that controls the gate–source voltage  $V_{GS2}$  of  $Q_2$  and its controller (Controller2) are shown in blue letters. The IC operates in two modes: closed loop mode and open loop mode, with mode switching performed by the “Mode” input. The operation of the closed loop mode is described as follows.

This IC has a feedback control function to achieve both  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization. To equalize  $I_{D1,DC}$  and  $I_{D2,DC}$ , the output  $I_{D1}'$  of  $I_{D1}$  sensor and the output  $I_{D2}'$  of  $I_{D2}$  sensor are compared by a comparator and the comparison result is given as Comp\_DC to Controller1 and Controller2. Similarly, to equalize  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ ,  $I_{D1}'_{PEAK}$  with peak hold of  $I_{D1}'$  and  $I_{D2}'_{PEAK}$  with peak hold of  $I_{D2}'$  are compared by a comparator and the comparison result is given as Comp\_SURGE to Controller1 and

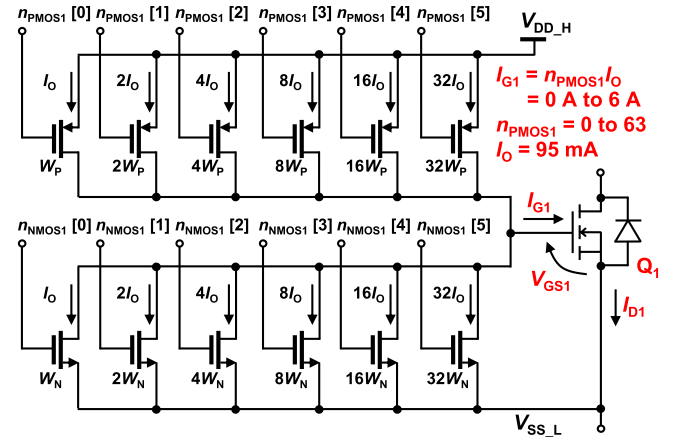


Fig. 3. Circuit schematic of DGD1 for  $Q_1$  in Fig. 2.

Controller2. Based on the comparison results Comp\_DC and Comp\_SURGE, Controller1 and Controller2 output appropriate control signals ( $n_{PMOS1}[5:0]$  and  $n_{NMOS1}[5:0]$  for DGD1, and  $n_{PMOS2}[5:0]$  and  $n_{NMOS2}[5:0]$  for DGD2) to the 12-bit input DGD1 and DGD2 to feedback control  $V_{GS1}$  and  $V_{GS2}$ , respectively, thereby achieving both  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization. The initial values of  $n_{PMOS1}[5:0]$ ,  $n_{NMOS1}[5:0]$ ,  $n_{PMOS2}[5:0]$ , and  $n_{NMOS2}[5:0]$  are set by input from Scan\_Data of a serial-in parallel-out shift register (SIPO SR).

Fig. 3 shows a circuit schematic of DGD1 for  $Q_1$  in Fig. 2. The gate current ( $I_{G1}$ ) can be varied in 64 levels at turn-ON depending on 6-bit digital signals  $n_{PMOS1}[5:0]$ , where  $n_{PMOS1}$  represents  $n_{PMOS1}[5:0]$  in decimal and  $n_{PMOS1}$  is an integer between 0 and 63. The 64-level  $I_{G1}$  control from 0 A to 6 A in 95 mA increments at turn-ON of  $Q_1$  is achieved by selectively turning ON or OFF six pMOSFETs with binary weighted gate widths ( $W_P$ ,  $2W_P$ ,  $4W_P$ ,  $8W_P$ ,  $16W_P$ , and  $32W_P$ ) in the output stage depending

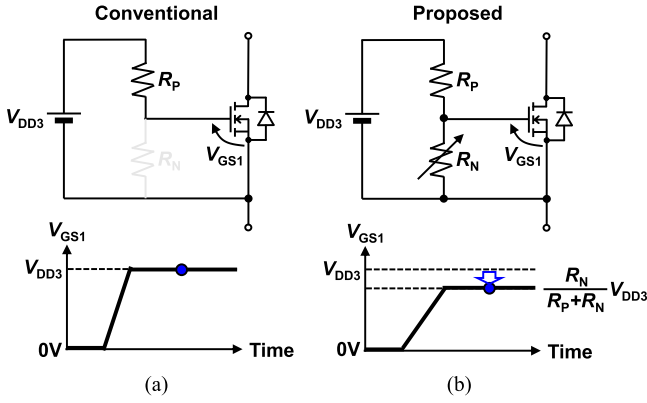


Fig. 4. Principle of operation. (a) Conventional gate driving with constant  $V_{GS1}$ . (b) Proposed DGD-based  $V_{GS1}$  amplitude control.

on  $n_{PMOS1}$  [5:0]. The same design is applied to the turn-off of  $Q_1$  by controlling  $n_{NMOS1}$  [5:0]. In subsequent measurements in this article, however,  $n_{PMOS1}$  is varied from 0 to 31, and DGD1 and DGD2 are used as 5-bit DGDs, because the maximum gate current of 3 A is sufficient for the SiC MOSFETs used in this article.

Fig. 4 shows a principle of operation of the proposed DGD-based  $V_{GS1}$  amplitude control. In the conventional gate driving in Fig. 4(a),  $V_{GS1}$  is equal to the supply voltage ( $V_{DD3}$ ), because  $n_{NMOS1}$  in the on state is zero. In contrast, in the proposed  $V_{GS1}$  amplitude control in Fig. 4(b),  $V_{GS1}$  amplitude can be digitally controlled by  $n_{NMOS1}$  on the principle of a shunt regulator, where all six pMOSFETs and some of the six nMOSFETs in Fig. 3 are turned ON.

### B. Proposed Gate Amplitude Twice Control (GATC)

Fig. 5(a) shows a conventional timing chart without control, and Fig. 5(b) and (c) show timing charts of the proposed GATC. Fig. 5(b) and (c) show the timing charts for the cases  $I_{D1} > I_{D2}$  and  $I_{D1} < I_{D2}$ , respectively, at the initial state without control.  $n_{PMOS1}$ ,  $n_{NMOS1}$ ,  $n_{PMOS2}$ , and  $n_{NMOS2}$  represent the 6-bit control signals  $n_{PMOS1}[5:0]$ ,  $n_{NMOS1}[5:0]$ ,  $n_{PMOS2}[5:0]$ , and  $n_{NMOS2}[5:0]$  in decimal, respectively. In the proposed GATC, as shown in Fig. 5(b) and (c), during the period when IN is ON, both  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization are achieved by changing the gate amplitude of either  $Q_1$  or  $Q_2$  twice. On the other hand, nothing is controlled during the period when IN is OFF.

Specifically, when the same gate drive is first applied to  $Q_1$  and  $Q_2$  as shown in Fig. 5(a) and  $I_{D1} > I_{D2}$  is sensed, as shown in Fig. 5(b),  $n_{NMOS1}$  is controlled to  $n_{SURGE1}$  instead of fixed to 0 during  $t_1$  after turn-ON to achieve  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization. During the remaining ON period after the end of  $t_1$ ,  $I_{D1,DC}$  and  $I_{D2,DC}$  are equalized by controlling  $n_{NMOS1}$  to  $n_{DC1}$  instead of fixed to 0. Note that to achieve  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization and  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization, a feedback control of two variables ( $n_{SURGE1}$  and  $n_{DC1}$ ) is essential, not a feedback control of one variable. In exactly the same way, when  $I_{D1} < I_{D2}$  is sensed at first,  $n_{NMOS2}$  is feedback

controlled by two variables,  $n_{SURGE2}$  and  $n_{DC2}$ , as shown in Fig. 5(c).

As shown later in the measured results in Figs. 17–20, in this article,  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization at turn-ON and  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization using the GATC shown in Fig. 5(b) also automatically achieved  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization at turn-OFF, because the turn-OFF starts from the state  $I_{D1,DC} = I_{D2,DC}$  in this proposal. Therefore, this article does not discuss  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization at turn-OFF.

Fig. 6 shows a timing chart to achieve  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization by using GATC in SIDO DGD IC when  $I_{D1} > I_{D2}$  in the initial state. In the initial state when GATC is not performed,  $I_{D1,SURGE} > I_{D2,SURGE}$  and  $I_{D1,DC} > I_{D2,DC}$ . Fig. 6 shows an example of how the proposed GATC achieves  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization in steady state by feedback controlling the two variables of  $n_{SURGE1}$  from 0 to 17 and  $n_{DC1}$  from 0 to 23, over 23 cycles. The length of the first time slot  $t_1$  of GATC is set by the pulsewidth of the “Timing” input from an external pulse generator synchronized to “IN.” The detailed operation of Fig. 6 is described as follows.

(Step 1 at  $t_A$ )

First, when “Enable” is low, the IC is reset, and the initial values of the digital control bits are written to the SIPO SR in Fig. 2. The initial values of  $n_{SURGE1}$  and  $n_{DC1}$  are both zero.

(Step 2 at  $t_B$ )

Immediately after the first rise edge of “IN,” the rise edge of “CLK\_SURGE” is input from outside the IC, and the clocked comparator shown in Figs. 2 and 10 compares  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  at the moment of  $t_B$ . In Fig. 6, the comparator output “Comp\_SURGE” = High, because  $I_{D1,SURGE} > I_{D2,SURGE}$ . This causes the controllers shown in Figs. 2, 11, and 12 to increment  $n_{SURGE1}$  from 0 to 1.

(Step 3 at  $t_C$ )

At the fall edge of “Timing”,  $n_{NMOS1}$  changes from  $n_{SURGE1}$  to  $n_{DC1}$ . As a result, in GATC, the gate amplitude of  $V_{GS1}$  changes twice in the ON period, in the first  $t_1$  and in the rest of the period. In Fig. 6, initially no two changes in  $V_{GS1}$  are shown because  $n_{SURGE1} = n_{DC1} = 0$ , while two changes in  $V_{GS1}$  are shown in the steady state.

(Step 4 at  $t_D$ )

After the surge currents of  $I_{D1}$  and  $I_{D2}$  have sufficiently settled down, the rise edge of “CLK\_DC” is input from outside the IC, and the clocked comparator in Figs. 2 and 10 compares  $I_{D1,DC}$  and  $I_{D2,DC}$  at the moment of  $t_D$ . In Fig. 6, the comparator output “Comp\_DC” = High, because  $I_{D1,DC} > I_{D2,DC}$ . This causes the controller shown in Figs. 2, 11, and 12 to increment  $n_{DC1}$  from 0 to 1. In the measurements in Figs. 17–20, the time between the turn-ON edge of IN and  $t_D$  is 1  $\mu$ s. As can be seen from the measured waveforms of  $I_{D1}$  and  $I_{D2}$  in Fig. 19(b), the above time cannot be reduced to 1  $\mu$ s or less, because the comparison must be made at  $t_D$  after  $I_{D1}$  and  $I_{D2}$  reach a steady state. Therefore,  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization function does not work for the proposed gate driver IC when the IN pulse width is less than 1  $\mu$ s.

(Step 5 at  $t_E$ )

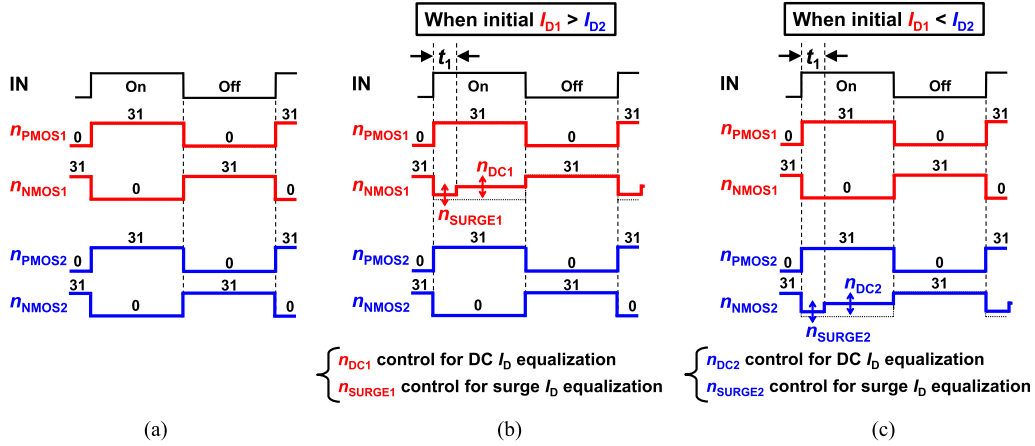


Fig. 5. Timing charts. (a) Conventional without control. (b) Proposed  $V_{GS1}$  gate amplitude twice control (GATC) at initial  $I_{D1} > I_{D2}$ . (c) Proposed  $V_{GS2}$  gate amplitude twice control (GATC) at initial  $I_{D1} < I_{D2}$ .

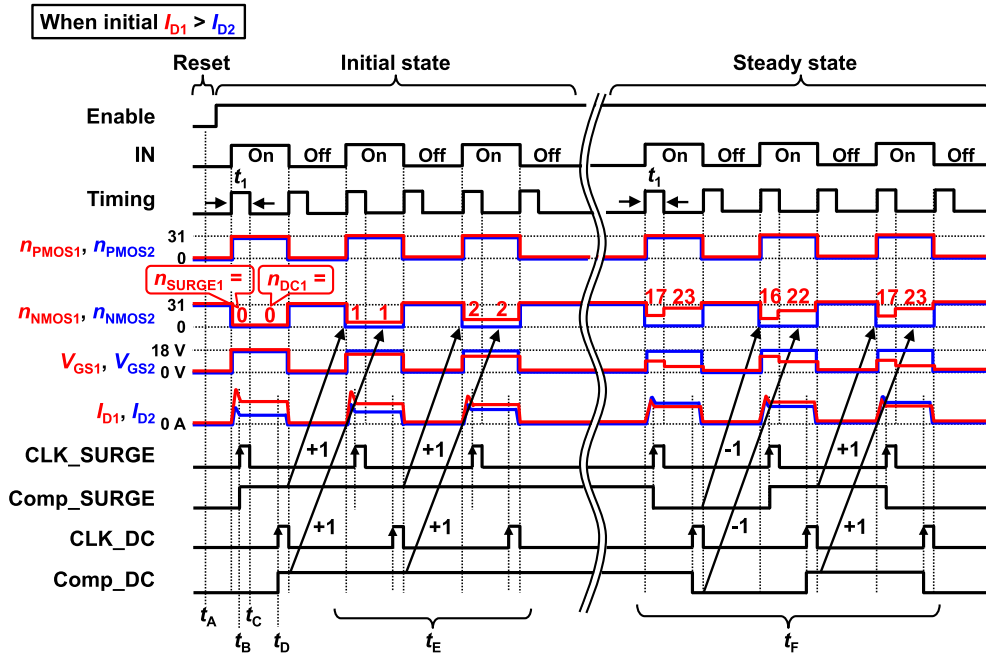


Fig. 6. Timing chart to achieve  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization by using GATC in SIDO DGD IC when  $I_{D1} > I_{D2}$  in initial state.

After the second turn-ON of “IN,”  $n_{SURGE1}$  and  $n_{DC1}$  continue to increment when  $I_{D1,SURGE} > I_{D2,SURGE}$  and  $I_{D1,DC} > I_{D2,DC}$ .

(Step 6 at  $t_F$ )

In the steady state, when the feedback control of GATC is completed,  $n_{SURGE1}$  and  $n_{DC1}$  repeat up and down every cycle of “IN.” In this state, both  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization are achieved.

### C. Comparison With Previous Work

Fig. 7(a)–(d) show schematic diagrams of waveforms at turn-on of the conventional and proposed gate drivings to achieve

$I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization using SIDO DGD IC. Fig. 7(a) shows the conventional gate driving, Fig. 7(b) and (c) show the gate drivings shown in [20], and Fig. 7(d) shows the proposed GATC. In order to achieve  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ , the technique of adjusting the gate voltage amplitude twice for GATC is similar to that of the multilevel active gate driver [14]. The difference, however, is that [14] implements the entire circuit on a PCB, whereas this article implements the entire circuit on a single chip.

In the conventional gate driving where  $V_{GS1}$  and  $V_{GS2}$  waveforms are identical for  $Q_1$  and  $Q_2$  in Fig. 7(a),  $I_{D1,DC} > I_{D2,DC}$  and  $I_{D1,SURGE} > I_{D2,SURGE}$ .

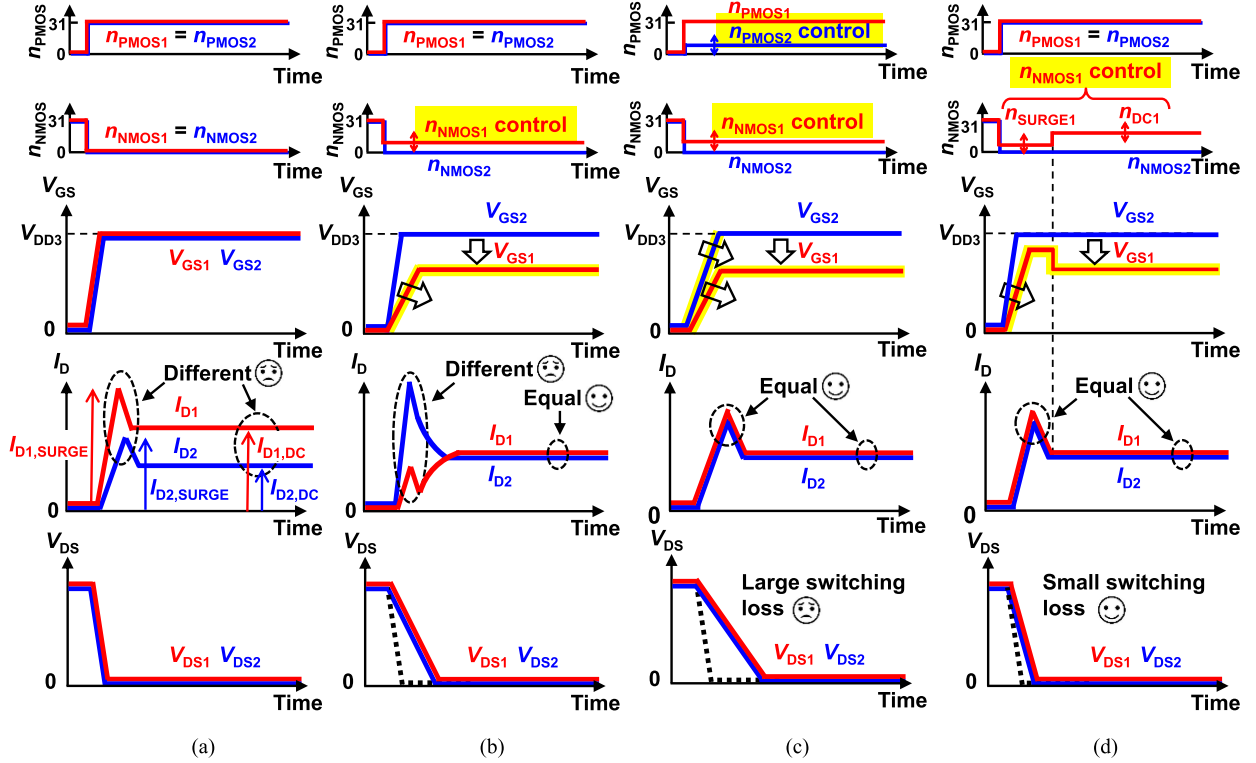


Fig. 7. Schematic diagrams of waveforms at turn-ON to achieve  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization using SIDO DGD IC. (a) Conventional gate driving without control. (b) Conventional simple  $V_{GS1}$  amplitude control by increasing  $n_{NMOS1}$  from zero [20]. (c) Conventional  $V_{GS1}$  and  $I_{G2}$  control by controlling  $n_{NMOS1}$  and  $n_{PMOS2}$  [20]. (d) Proposed  $V_{GS1}$  gate amplitude twice control (GATC).

In order to equalize  $I_{D1,DC}$  and  $I_{D2,DC}$ , Fig. 7(b) shows a conventional simple  $V_{GS1}$  amplitude control by increasing  $n_{NMOS1}$  from zero [20]. The conventional simple  $V_{GS1}$  amplitude control is an important conventional technique for realizing  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization. In [26], the conventional simple  $V_{GS1}$  amplitude control is implemented using buck converters. In Fig. 7(b),  $I_{D1,DC}$  and  $I_{D2,DC}$  are adjusted to be equal, by reducing  $V_{GS1}$  amplitude below  $V_{GS2}$  amplitude, while  $I_{D1,SURGE} < I_{D2,SURGE}$ , because  $I_{G1} < I_{G2}$  at turn-on due to the increased  $n_{NMOS1}$ , where  $I_{G1}$  and  $I_{G2}$  are the gate currents of  $Q_1$  and  $Q_2$ , respectively, as shown in Fig. 2. Please note that  $I_{D1,SURGE} > I_{D2,SURGE}$  in Fig. 7(a), while  $I_{D1,SURGE} < I_{D2,SURGE}$  in Fig. 7(b).

In order to equalize  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ , Fig. 7(c) shows a conventional  $V_{GS1}$  and  $I_{G2}$  control by controlling  $n_{NMOS1}$  and  $n_{PMOS2}$  [20].  $I_{D1,DC}$  and  $I_{D2,DC}$  are equalized by tuning  $n_{NMOS1}$ , and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  are equalized by decreasing  $I_{G2}$  at turn-ON by decreasing  $n_{PMOS2}$ .

Fig. 7(b) and (c), however, have the disadvantage that the switching loss increases compared to Fig. 7(a), because  $n_{NMOS1}$  is set to a value greater than 0 by feedback control to equalize  $I_{D1,DC}$  and  $I_{D2,DC}$ , which decreases  $dV_{GS1}/dt$ ,  $|dV_{DS1}/dt|$ , and  $|dV_{DS2}/dt|$  at turn-ON.

To solve this problem, in the proposed GATC shown in Fig. 7(d), the surge and dc components of  $I_{D1}$  and  $I_{D2}$  are independently controlled by twice change of  $n_{NMOS1}$ , i.e.,  $n_{SURGE1}$  and  $n_{DC1}$  (typically  $n_{SURGE1} < n_{DC1}$ ), thereby achieving  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$

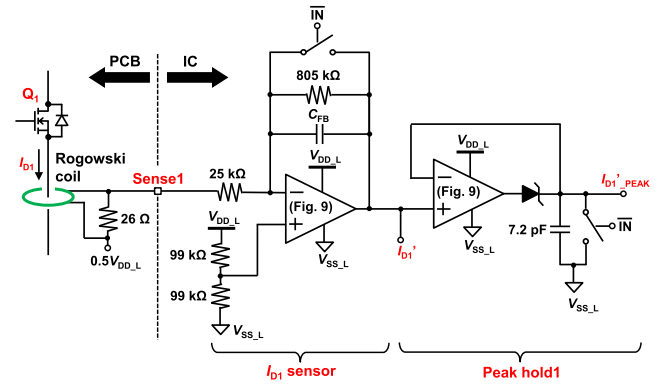


Fig. 8. Circuit schematic of  $I_{D1}$  sensor and Peak hold1 in Fig. 2.

equalization while suppressing the increase in the switching loss compared to Fig. 7(b) and (c).

### III. CIRCUIT DETAILS OF SIDO DGD IC

#### A. $I_{D1}$ Sensor and Peak Hold1

Fig. 8 shows a circuit schematic of the  $I_{D1}$  sensor and Peak hold1 in Fig. 2. The differentiated waveform of  $I_{D1}$  is output from the Rogowski coil to “Sense1.” To restore the  $I_{D1}$  waveform, “Sense1” is integrated by an operational amplifier in the  $I_{D1}$  sensor to provide a voltage waveform ( $I_{D1}'$ ) proportional to  $I_{D1}$ , which will be used in  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization.

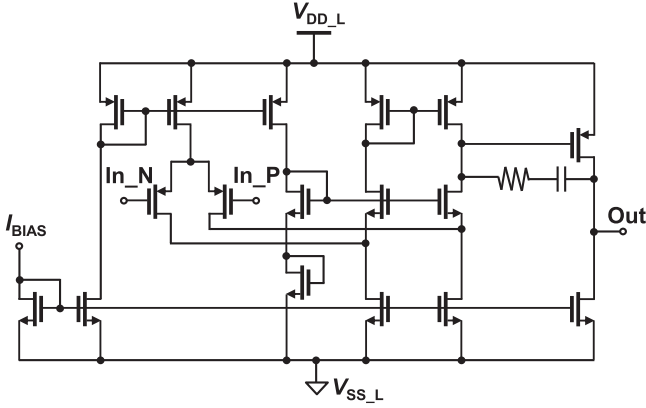


Fig. 9. Circuit schematic of operational amplifier shown in Fig. 8.

In addition, the peak value of  $I_{D1}'$  ( $I_{D1}'_{PEAK}$ ) is output by holding the peak value of  $I_{D1}'$  at Peak hold1, which will be used in  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization. Both  $I_{D1}$  sensor and Peak hold1 are reset during the period when “IN” is low and start measurement at the rise edge of “IN”, i.e., the moment of turn-ON. To avoid the gate of the op-amp transistor being destroyed by overvoltage when Sense1 goes above 5 V, the voltage amplitude of Sense1 was adjusted with a resistor at the Rogowski coil output (26  $\Omega$  in Fig. 8).

Fig. 9 shows a circuit schematic of the operational amplifier shown in Fig. 8. The operational amplifier consists of two stages of a PMOSFET differential input folded cascode amplifier and a common source amplifier, with a phase compensation resistor and capacitor inserted between the first and second stages.

The upper bandwidth required for the  $I_{D1}$  sensor in Fig. 8 is 50 MHz, because the measured maximum  $I_{D1}$  ringing frequency during the switch transient is 50 MHz. On the other hand, the  $I_{D1}$  sensor has a bandwidth of 80 kHz to 80 MHz, which meets the above requirement, because the upper bandwidth of the Rogowski coil is 100 MHz and the simulated bandwidth of the integrator circuit in Fig. 8 is 80 kHz to 80 MHz.

The effect of operational amplifier nonidealities such as input voltage offset and bias currents on the integrator circuit in  $I_{D1}$  sensor in Fig. 8 is negligibly small, because the time from the integration start timing, the first rise edge of IN in Fig. 6, to the timing of the comparison of  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ ,  $t_B$  in Fig. 6, i.e., at the rise edge timing of CLK\_SURGE, is very short, 200 ns in the measurement in this article.

### B. Comparators

Fig. 10 shows a schematic of Comparators in Fig. 2, including two clocked comparators. The comparator above in Fig. 10 compares  $I_{D1}'_{PEAK}$  and  $I_{D2}'_{PEAK}$  at the rise edge of “CLK\_SURGE” as shown in Fig. 6, and outputs the comparison result to “Comp\_SURGE.” Similarly, the comparator below in Fig. 10 compares  $I_{D1}'$  and  $I_{D2}'$  at the rise edge of “CLK\_DC” as shown in Fig. 6, and outputs the comparison result to “Comp\_DC.” The propagation delay of the  $I_{D1}$  sensor shown in Fig. 8 and the comparator shown in Fig. 9 are not a

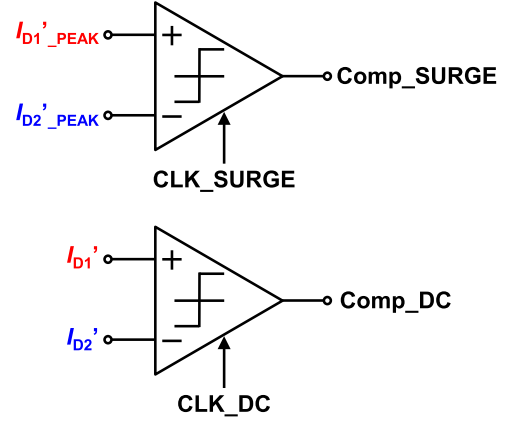


Fig. 10. Schematic of Comparators in Fig. 2, including two clocked comparators.

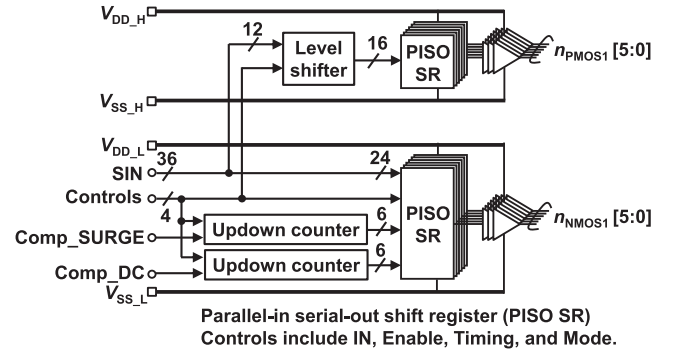


Fig. 11. Circuit schematic of Controller1 in Fig. 2.

problem at all, because, as shown in Fig. 6, the results of the comparison between  $I_{D1}$  and  $I_{D2}$  in one turn-on are applied to  $n_{NMOS1}$  and  $n_{NMOS2}$  in the next turn-ON.

### C. Controller

Fig. 11 shows a circuit schematic of Controller1 in Fig. 2. Among the 36 bits of SIN given by SIPO SR in Fig. 2, 12 bits (6 bit for turn on + 6 bit for turn off) for  $n_{PMOS1}[5:0]$  are given to the high-side parallel-in serial-out shift register (PISO SR), and 24 bits (6 bit  $\times$  2 slot for turn on + 6 bit  $\times$  2 slot for turn OFF) for  $n_{NMOS1}[5:0]$  are given to the low-side PISO SR. “Controls” represents “IN,” “Enable,” “Timing,” and “Mode” inputs in Fig. 2. In the open loop mode,  $n_{PMOS1}[5:0]$  and  $n_{NMOS1}[5:0]$  are determined by “SIN” and are fixed. In the closed loop mode, on the other hand,  $n_{SURGE1}$  is determined by the up-down counter with “Comp\_SURGE” input, and  $n_{DC1}$  by the up-down counter with “Comp\_DC” input.  $n_{SURGE1}$  and  $n_{DC1}$  are updated every “IN” cycle as shown in Fig. 6.

Fig. 12(a) and (b) show flowcharts to control  $n_{DC1}$  and  $n_{DC2}$  to equalize  $I_{D1,DC}$  and  $I_{D2,DC}$ , and to control  $n_{SURGE1}$  and  $n_{SURGE2}$  to equalize  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ , respectively. The flowcharts are implemented in Controller1 and Controller2 shown in Fig. 2. In Fig. 12(a), initially  $n_{DC1}$  and  $n_{DC2}$  are reset to zero. When  $I_{D1,DC}$  is greater than  $I_{D2,DC}$ ,  $n_{DC1}$  is incremented

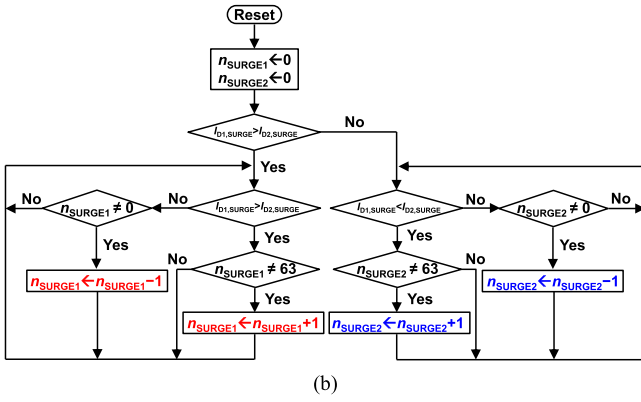
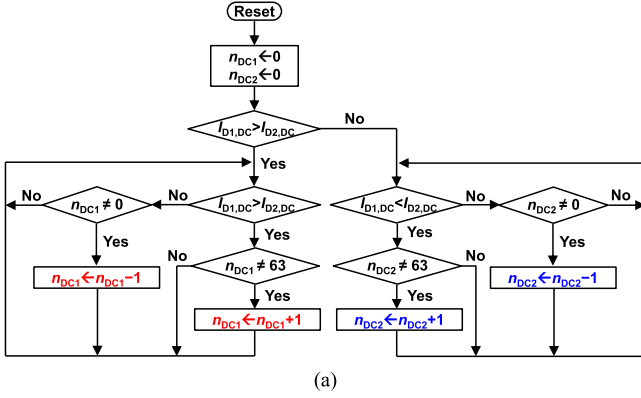


Fig. 12. (a) Flowcharts to control  $n_{DC1}$  and  $n_{DC2}$  to equalize  $I_{D1,DC}$  and  $I_{D2,DC}$ . (b) Flowcharts to  $n_{SURGE1}$  and  $n_{SURGE2}$  to equalize  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ .

by one from 0. Next, a steady state is reached at the value of  $n_{DC1}$  where  $I_{D1,DC}$  and  $I_{D2,DC}$  are equal. Similarly, when  $I_{D1,DC}$  is smaller than  $I_{D2,DC}$ ,  $n_{DC2}$  is incremented from 0. Then, a steady state is reached at the value of  $n_{DC2}$  where  $I_{D1,DC}$  and  $I_{D2,DC}$  are equal. In Fig. 12(b), the control of  $n_{SURGE1}$  and  $n_{SURGE2}$  is exactly the same as in Fig. 12(a).

#### IV. MEASURED EQUALIZATION OF DC AND SURGE COMPONENTS OF DRAIN CURRENT

##### A. Measurement Setup

Fig. 13 shows a circuit schematic of the fabricated half-bridge circuit and SIDO DGD IC for the double- and multipulse tests. The half-bridge consists of three SiC MOSFETs ( $Q_1 - Q_3$ ) including the low-side two-parallel  $Q_1$  and  $Q_2$ . Measurements were done with the main circuit power supply voltage ( $V_{DD}$ ) of 300 V.  $I_{D1}$  and  $I_{D2}$  are measured using two commercial current probes (SS-284A, IWATSU) and our developed two current sensors in DGD IC. The current probes are used in Figs. 17–20 and 22–25 to measure  $I_{D1}$  and  $I_{D2}$  waveforms, while the current sensors are used in closed loop measurements in Figs. 17–20. The bandwidth of the current probes is 30 MHz, while the rise time of the measured  $I_{D1}$  and  $I_{D2}$  waveforms is about 50 ns. Since bandwidth  $\times$  rise time  $>$  0.35, the bandwidth of the current probes for  $I_{D1}$  and  $I_{D2}$  measurements is sufficient.

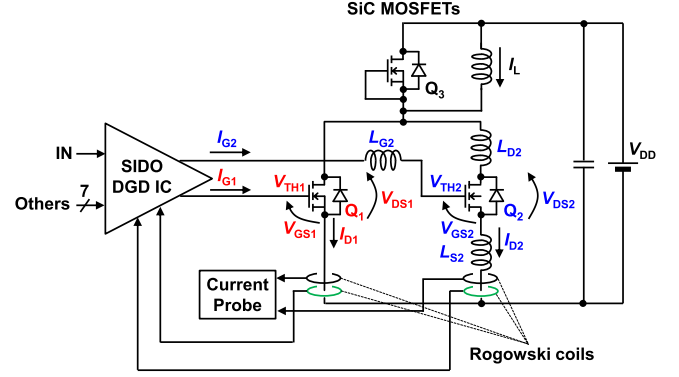


Fig. 13. Circuit schematic of fabricated half-bridge circuit and SIDO DGD IC for double- and multipulse tests.  $V_{DD} = 300$  V.

Two major factors known to cause variations in the drain current of parallel-connected SiC MOSFETs are variations in the device characteristics of the MOSFETs (e.g., threshold voltage, transconductance) and the parasitic inductance of the MOSFETs [1]. Therefore, this article demonstrates in multipulse tests that the proposed SIDO DGD IC can address one or both of the two major factors and achieve both  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization.

Fig. 14 shows schematic diagrams of the four types of two-parallel connected SiC MOSFETs used in the measurement and the  $I_{D1}$  and  $I_{D2}$  waveforms. In Fig. 14, the ON-resistances of  $Q_1$  and  $Q_2$  are denoted as  $R_{ON1}$  and  $R_{ON2}$ , respectively, as representative values of MOSFET device characteristics. Fig. 14(a) and (b) show the case where  $R_{ON1} = R_{ON2}$ , and Fig. 14(c) and (d) show the case where  $R_{ON1} < R_{ON2}$ . Fig. 14(a) and (c) show the case without parasitic inductance variation, and Fig. 14(b) and (d) show the case with parasitic inductance variation. As shown in Fig. 14(b) and (d), when the leg length of  $Q_2$  is longer than that of  $Q_1$ , drain parasitic inductance ( $L_{D2}$ ), gate parasitic inductance ( $L_{G2}$ ), and source parasitic inductance ( $L_{S2}$ ) are added to  $Q_2$  as shown in Fig. 13.

Fig. 14(a) shows the case where  $R_{ON1} = R_{ON2}$  and no parasitic inductance variation, which is named IDEAL. In this case, the  $I_{D1}$  and  $I_{D2}$  waveforms are identical. Fig. 14(b) shows the case where  $R_{ON1} = R_{ON2}$  with parasitic inductance variation, which is named L\_VARIATION. This emulates the assembly variation of SiC MOSFETs. In this case,  $I_{D1,SURGE} > I_{D2,SURGE}$  and  $I_{D1,DC} = I_{D2,DC}$ . Fig. 14(c) shows the case where  $R_{ON1} < R_{ON2}$  and no parasitic inductance variation, which is named MOS\_VARIATION. In this case,  $I_{D1,SURGE} > I_{D2,SURGE}$  and  $I_{D1,DC} > I_{D2,DC}$ . Fig. 14(d) shows the case with  $R_{ON1} < R_{ON2}$  and parasitic inductance variations, which is named L&MOS\_VARIATION. This emulates the worst case where both assembly variation and device characteristic variation of the SiC MOSFETs have occurred. In this case,  $I_{D1,SURGE} > I_{D2,SURGE}$  and  $I_{D1,DC} > I_{D2,DC}$ .

As SiC MOSFETs with variations in device characteristics, [20] used  $Q_1$  and  $Q_2$  with the same model number and 0.5 V variation in threshold voltage. In this article, it is desired to demonstrate that our proposal can manage larger device characteristic variations. It is not easy, however, to prepare SiC

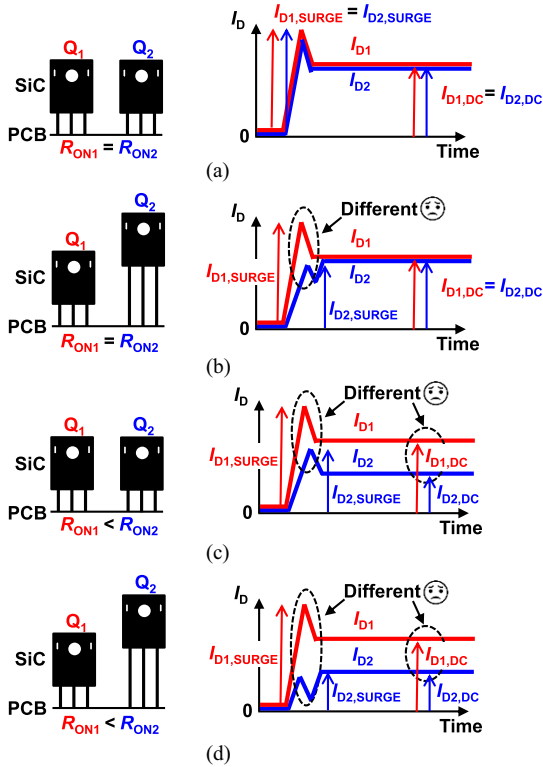


Fig. 14. Schematic diagrams of four types of two-parallel connected SiC MOSFETs used in measurement and  $I_{D1}$  and  $I_{D2}$  waveforms. (a) Case where  $R_{ON1} = R_{ON2}$  and no parasitic inductance variation, which is named IDEAL. (b) Case where  $R_{ON1} = R_{ON2}$  with parasitic inductance variation, which is named L\_VARIATION. (c) Case where  $R_{ON1} < R_{ON2}$  and no parasitic inductance variation, which is named MOS\_VARIATION. (d) Case with  $R_{ON1} < R_{ON2}$  and parasitic inductance variations, which is named L&MOS\_VARIATION.

TABLE I  
Q<sub>1</sub> AND Q<sub>2</sub> IN FIG. 14(C) AND (D)

	Q <sub>1</sub> , Q <sub>3</sub>	Q <sub>2</sub>
Device name	MSC015SMA070B	SCT3030AL
Max $V_{DS}$ [V]	700	650
Max $I_D$ (DC) [A]	140	70
$R_{ON}$ (Typ.) [mΩ]	15	30
Total gate charge [nC]	215	104
$V_{TH}$ [V]	2.7-5.6	2.4 (Typ.)

MOSFETs with large variations in device characteristics. Therefore, in order to emulate SiC MOSFETs with large variations in device characteristics, in this article, SiC MOSFETs from different manufacturers shown in Table I are used for Q<sub>1</sub> and Q<sub>2</sub> in Fig. 14(c) and (d). Specifically, MSC015SMA070B is used for Q<sub>1</sub> and SCT3030AL for Q<sub>2</sub>. Since the MSC015SMA070B and SCT3030AL are all different in terms of maximum rated current, on-resistance ( $R_{ON}$ ),  $V_{TH}$ , etc., if both  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization can be achieved, it will provide a solid demonstration that the proposal can address device characteristic variations. On the other hand,

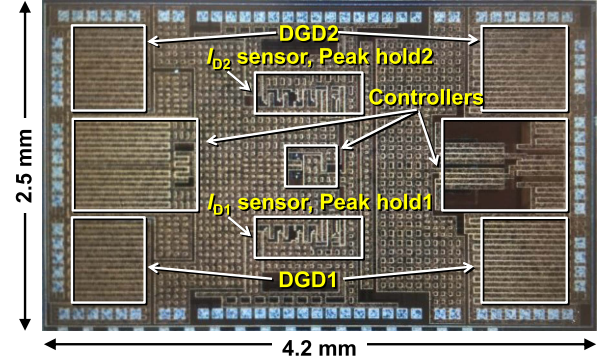


Fig. 15. Die photograph of SIDO DGD IC fabricated with 180 nm BCD process. All circuits shown in Fig. 2 are integrated on single chip.

SCT3030AL is used for both Q<sub>1</sub> and Q<sub>2</sub> in Fig. 14(a) and (b) with no device characteristic variation. In all measurements, MSC015SMA070B is used for Q<sub>3</sub>.

Fig. 15 shows a die photo of SIDO DGD IC fabricated with 180 nm BCD process. All the circuits shown in Fig. 2 are integrated on a single chip. The die size is 2.5 mm by 4.2 mm.

Fig. 16(a) and (b) show top and side views of the PCB of L&MOS\_VARIATION in Fig. 14(d), respectively. As shown in Fig. 16(a), PCB is designed symmetrically so that the PCB parasitic inductances of Q<sub>1</sub> and Q<sub>2</sub> are equal. The PCB Rogowski coil is not built into the main PCB, but is fabricated on a separate PCB and placed on top of the main PCB. PCB Rogowski coils can be made smaller if necessary, because PCB Rogowski coils with an outer diameter of 3.2 mm are also shown in [28], although PCB Rogowski coils with an outer diameter of 19 mm [28] are used in this article. As shown in Fig. 16(b), the leg length of Q<sub>2</sub> is intentionally implemented 8 mm longer than that of Q<sub>1</sub> to achieve the parasitic inductance variation in Fig. 14(b) and (d).

### B. Closed Loop Measurements

Figs. 17–20 show the measured waveforms of  $V_{GS1}$  and  $V_{GS2}$ ,  $I_{D1}$  and  $I_{D2}$ ,  $n_{PMOS1}$  and  $n_{PMOS2}$ , and  $n_{NMOS1}$  and  $n_{NMOS2}$  in the four multipulse tests of IDEAL, L\_VARIATION, MOS\_VARIATION and L&MOS\_VARIATION shown in Fig. 14, respectively. In the following measurements,  $t_1$  shown in Fig. 6 is fixed at 240 ns.  $t_1$  may be determined arbitrarily within the range  $t_1 > t_{1(MIN)}$ , where  $t_{1(MIN)}$  is the time from the rise edge of IN to the timing when the drain current surge reaches its peak, which is 80 ns in the measurements. If  $t_1$  is too long,  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization will be delayed, which is not a good idea. In each of Figs. 17–20, (a) shows the conventional uncontrolled gate driving [see Fig. 7(a)], and (b) shows the proposed GATC [see Figs. 6 and 7(d)]. In Figs. 17–20, at the end of the multipulse test (time = 400 to 410  $\mu$ s) the load current  $I_L (= I_{D1} + I_{D2})$  defined in Fig. 13 reaches 120 A. Note that,  $I_L = 120$  A is an appropriate measurement condition for two parallel connected SCT3030ALs, since the maximum current rating of SCT3030AL is 70 A as shown in Table I.

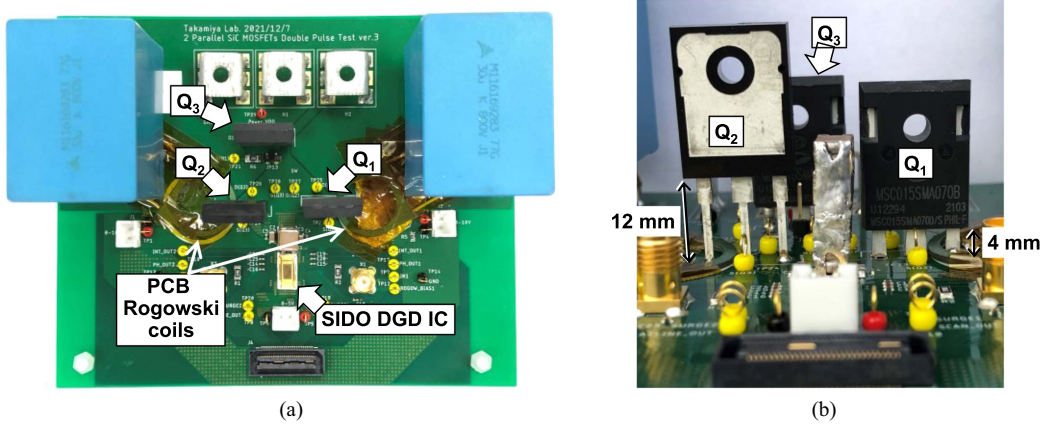


Fig. 16. PCB of L&MOS\_VARIATION in Fig. 14(d). (a) Top view. (b) Side view.

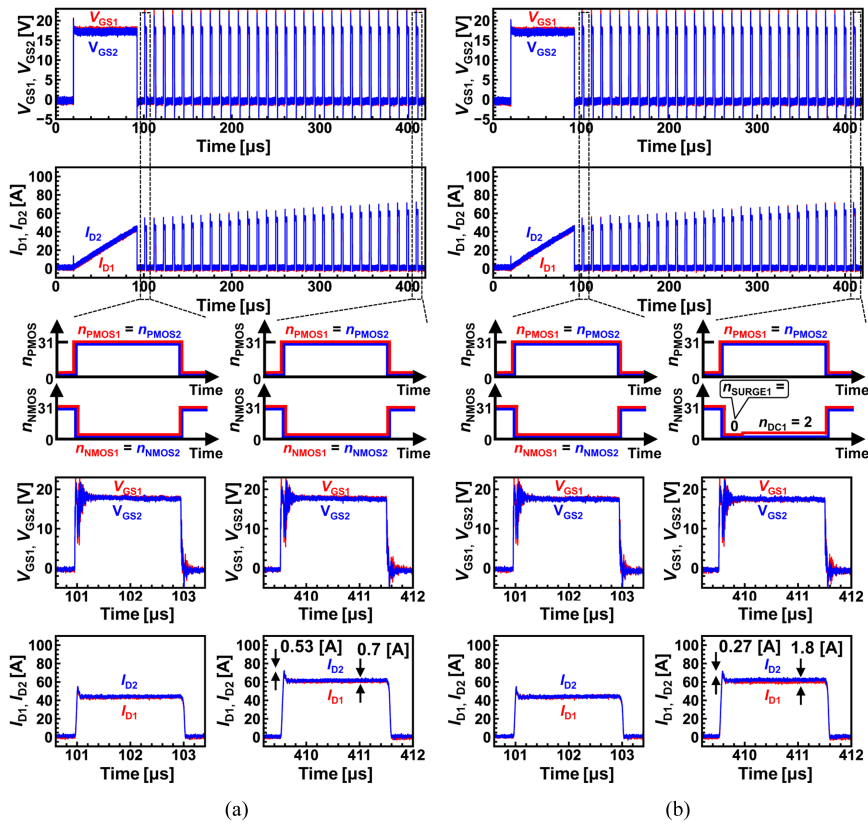


Fig. 17. Measured waveforms in multipulse test of IDEAL shown in Fig. 14(a).

In IDEAL in Fig. 17,  $I_{D1}$  and  $I_{D2}$  waveforms are nearly identical, as expected. In GATC in Fig. 17(b), ideally  $n_{NMOS1} = 0$  during ON, but  $n_{DC1} = 2$  at the end of the multipulse test, resulting in a larger difference between  $I_{D1,DC}$  and  $I_{D2,DC}$  compared to the conventional uncontrolled gate drive in Fig. 17(a). This is presumably due to the measurement errors of the  $I_{D1}$  sensor and  $I_{D2}$  sensor in Fig. 2.

In the conventional uncontrolled gate driving in L\_VARIATION shown in Fig. 18(a),  $I_{D1,SURGE} > I_{D2,SURGE}$  and  $I_{D1,DC} = I_{D2,DC}$  as shown in the schematic waveforms in

Fig. 14(b). In contrast, the proposed GATC in L\_VARIATION shown in Fig. 18(b) reduces  $I_{D1,SURGE} - I_{D2,SURGE}$  by 76% from 30 A in Fig. 18(a) to 7.3 A by feedback control to  $n_{SURGE1} = 13$ .

In the conventional uncontrolled gate driving in MOS\_VARIATION shown in Fig. 19(a), the difference between  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  is small, but  $I_{D1,DC} > I_{D2,DC}$  because  $R_{ONS}$  of  $Q_1$  and  $Q_2$  are about twice as different as shown in Table I. In contrast, the proposed GATC in MOS\_VARIATION shown in Fig. 19(b) reduces  $I_{D1,DC} -$

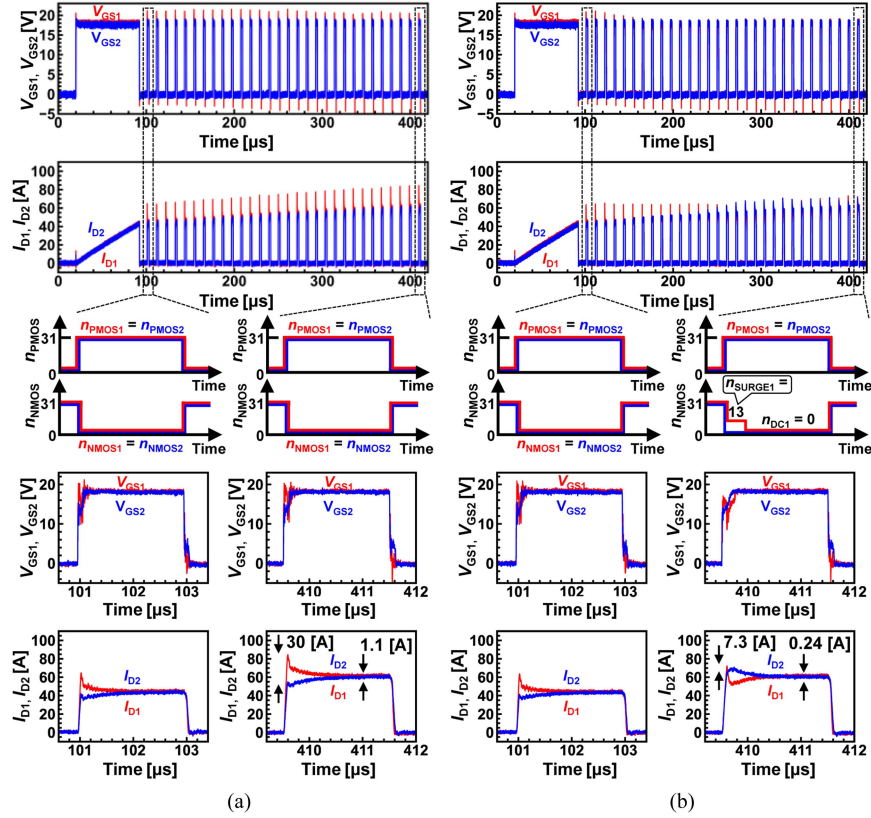


Fig. 18. Measured waveforms in multipulse test of  $L\_VARIATION$  shown in Fig. 14(b). (a) Conventional uncontrolled gate driving [Fig. 7(a)]. (b) Proposed GATC [Fig. 7(d)].

$I_{D2,DC}$  by 95% from 37 A in Fig. 19(a) to 1.8 A by feedback control to  $n_{DC1} = 22$  and  $V_{GS2} - V_{GS1} = 5.0$  V.

In the conventional uncontrolled gate driving in  $L\&MOS\_VARIATION$  shown in Fig. 20(a),  $I_{D1,SURGE} > I_{D2,SURGE}$  and  $I_{D1,DC} > I_{D2,DC}$  as shown in the schematic waveforms in Fig. 14(d). In contrast, the proposed GATC in  $L\&MOS\_VARIATION$  shown in Fig. 20(b) reduces  $I_{D1,SURGE} - I_{D2,SURGE}$  by 86% from 27 A in Fig. 20(a) to 3.9 A by feedback control to  $n_{SURGE1} = 14$ , and reduces  $I_{D1,DC} - I_{D2,DC}$  by 95% from 37 A in Fig. 20(a) to 1.7 A by feedback control to  $n_{DC1} = 22$  and  $V_{GS2} - V_{GS1} = 5.0$  V.

In summary, it has been successfully demonstrated that the proposed GATC using SIDO DGD IC achieves both  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization in all four cases of IDEAL,  $L\_VARIATION$ ,  $MOS\_VARIATION$ , and  $L\&MOS\_VARIATION$ .

### C. Open Loop Measurements ( $n_{DC1}$ and $n_{SURGE1}$ Dependence)

In the following sections, measurements are performed in open loop to investigate in detail the meaning of the feedback-controlled  $n_{SURGE1} = 14$  and  $n_{DC1} = 22$  values in GATC at  $L\&MOS\_VARIATION$  in Fig. 20(b).

Figs. 21–23 show the measured  $n_{DC1}$  dependence of  $V_{GS1}$  amplitude,  $n_{DC1}$  dependence of  $I_{D1,DC}$  and  $I_{D2,DC}$ , and  $n_{SURGE1}$  dependence of  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  when

GATC [see Fig. 7(d)] is operated in open loop under  $L\&MOS\_VARIATION$  [Fig. 14(d)],  $I_L = 60$  and 120 A conditions, respectively. In Fig. 23,  $n_{DC1}$  is fixed to 22. At  $I_L = 60$  A, by increasing  $n_{DC1}$  from 0 to 22,  $V_{GS1}$  amplitude reduces from 18 to 11.8 V (see Fig. 21) and  $I_{D1,DC} - I_{D2,DC}$  reduces from 24 to 2.5 A by 90% (see Fig. 22). Similarly, at  $I_L = 120$  A, by increasing  $n_{DC1}$  from 0 to 22,  $V_{GS1}$  amplitude reduces from 18 to 11.8 V (see Fig. 21) and  $|I_{D1,DC} - I_{D2,DC}|$  reduces from 48 to 3.9 A by 92% (see Fig. 22). As shown in Fig. 23, at  $I_L = 60$  A, by increasing  $n_{SURGE1}$  from 0 to 12,  $|I_{D1,SURGE} - I_{D2,SURGE}|$  reduces from 18 to 0.94 A by 95%. Similarly, at  $I_L = 120$  A, by increasing  $n_{SURGE1}$  from 0 to 16,  $I_{D1,SURGE} - I_{D2,SURGE}$  reduces from 42 to 1.9 A by 95%. Note that the optimal  $n_{SURGE1} = 16$  roughly corresponds to  $n_{SURGE1} = 14$  obtained with the feedback control in Fig. 20(b).

### D. Open-Loop Measurements (Comparison of Four Gate Driving Methods)

In order to quantitatively compare the four gate driving methods shown in Fig. 7 by measurements, Figs. 24 and 25 show the measured turn-ON waveforms at  $I_L = 60$  A and 120 A when the four gate driving methods shown in Fig. 7 are operated in open loop under the condition of  $L\&MOS\_VARIATION$  [see Fig. 14(d)], respectively. The measured waveforms of the conventional uncontrolled gate driving shown in Figs. 24(a) and 25(a) correspond to  $n_{DC1} = 0$  in Fig. 22, where  $I_{D1,DC}$

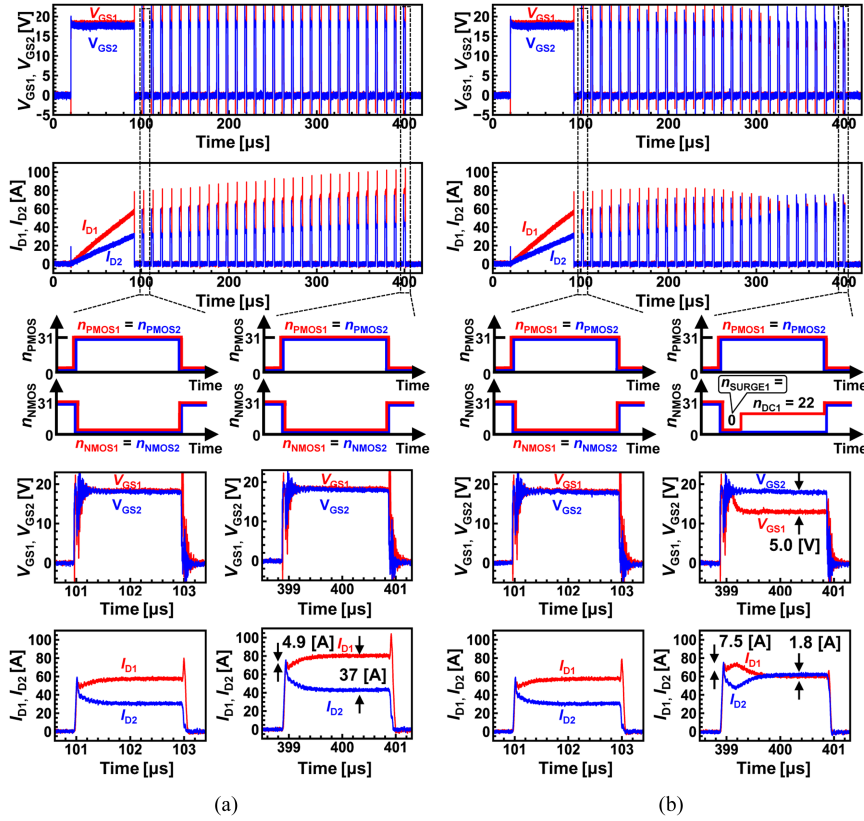


Fig. 19. Measured waveforms of in multipulse test of MOS\_VARIATION shown in Fig. 14(c). (a) Conventional uncontrolled gate driving [Fig. 7(a)]. (b) Proposed GATC [Fig. 7(d)].

$-I_{D2,DC} = 24 \text{ A}$  @  $I_L = 60 \text{ A}$  and  $I_{D1,DC} - I_{D2,DC} = 48 \text{ A}$  @  $I_L = 120 \text{ A}$ . The proposed GATC [see Figs. 24(d) and 25(d)] uses the optimal  $(n_{DC1}, n_{SURGE1}) = (22, 12)$  @  $I_L = 60 \text{ A}$  [see Fig. 24(d)] and  $(n_{DC1}, n_{SURGE1}) = (22, 16)$  @  $I_L = 120 \text{ A}$  [see Fig. 25(d)], obtained in Figs. 22 and 23. In the conventional simple  $V_{GS1}$  amplitude control [see Figs. 24(b) and 25(b)] and the conventional  $V_{GS1}$  and  $I_{G2}$  control [see Figs. 24(c) and 25(c)],  $n_{DC1} = 22$  is used. Since Figs. 24 and 25 show similar results, Fig. 25 for  $I_L = 120 \text{ A}$  will be discussed in detail.

In the conventional uncontrolled gate driving shown in Fig. 25(a), where the gate drive is identical for Q1 and Q2,  $I_{D1,SURGE} - I_{D2,SURGE} = 42 \text{ A}$  and  $I_{D1,DC} - I_{D2,DC} = 48 \text{ A}$ .

In order to equalize  $I_{D1,DC}$  and  $I_{D2,DC}$ , Fig. 25(b) shows the conventional simple  $V_{GS1}$  amplitude control by increasing  $n_{NMOS1}$  from 0 to 22 [20]. In Fig. 25(b),  $I_{D2,DC} - I_{D1,DC} = 5.9 \text{ A}$  by reducing  $V_{GS1}$  amplitude below  $V_{GS2}$  amplitude by 6.2 V, while  $I_{D2,SURGE} - I_{D1,SURGE} = 40 \text{ A}$ , because  $I_{G1} < I_{G2}$  at turn-on due to the increased  $n_{NMOS1}$ . Note that  $I_{D1,SURGE} > I_{D2,SURGE}$  in Fig. 25(a), while  $I_{D1,SURGE} < I_{D2,SURGE}$  in Fig. 25(b).

In order to equalize  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$ , Fig. 25(c) shows the conventional  $V_{GS1}$  and  $I_{G2}$  control by controlling  $n_{NMOS1}$  and  $n_{PMOS2}$  [20].  $I_{D1,DC}$  and  $I_{D2,DC}$  are equalized by increasing  $n_{NMOS1}$  from 0 to 22, and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  are equalized by decreasing  $I_{G2}$  at turn-ON by decreasing  $n_{PMOS2}$  from 31 to 3.

Fig. 25(b) and (c), however, have the disadvantage that the total switching loss ( $E_{LOSS,TOTAL}$ ) increases compared to Fig. 25(a), because increasing  $n_{NMOS1}$  and decreasing  $n_{PMOS2}$  decreases  $|dV_{DS1}/dt|$  and  $|dV_{DS2}/dt|$  at turn-ON. Specifically, compared to  $E_{LOSS,TOTAL} = 1.3 \text{ mJ}$  in Fig. 25(a),  $E_{LOSS,TOTAL} = 2.9 \text{ mJ}$  in Fig. 25(b) is increased by a factor of 2.2 and  $E_{LOSS,TOTAL} = 4.9 \text{ mJ}$  in Fig. 25(c) is increased by a factor of 3.8.

To solve this problem, in the proposed GATC shown in Fig. 25(d), both  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization ( $I_{D2,DC} - I_{D1,DC} = 3.9 \text{ A}$ ) and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization ( $I_{D1,SURGE} - I_{D2,SURGE} = 1.9 \text{ A}$ ) are achieved, while suppressing the increase in  $E_{LOSS,TOTAL}$  compared to Fig. 25(b) and (c). Specifically,  $E_{LOSS,TOTAL} = 2.0 \text{ mJ}$  in Fig. 25(d) is 31% less than in Fig. 25(b) and 59% less than in Fig. 25(c). On the other hand,  $E_{LOSS,TOTAL} = 2.0 \text{ mJ}$  in Fig. 25(d) is 1.5 times larger than in Fig. 25(a), while the difference in switching loss between Q1 and Q2 ( $E_{LOSS1} - E_{LOSS2}$ ) is reduced 43% by from 0.35 mJ in Fig. 25(a) to 0.20 mJ in Fig. 25(d), which indicates that the original goal of this paper has been successfully achieved.

## V. COMPARISON OF DIGITAL CLOSED-LOOP ACTIVE GATE DRIVERS TO EQUALIZE CURRENT IN PARALLEL-CONNECTED POWER DEVICES

Table II shows a comparison table of digital closed-loop active gate drivers to equalize current in parallel-connected power

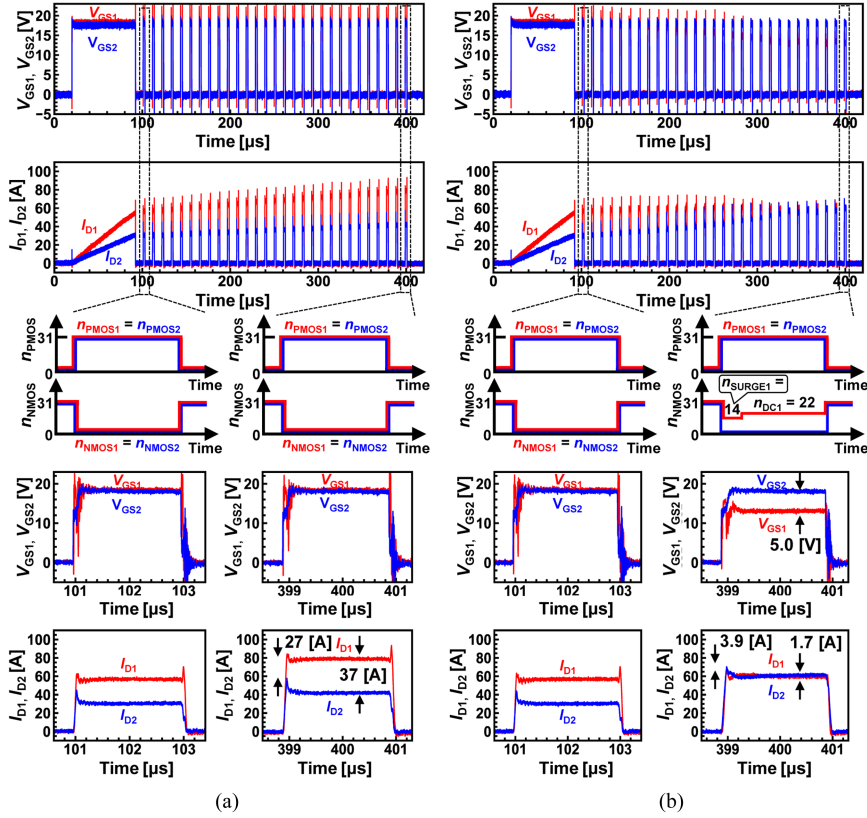


Fig. 20. Measured waveforms in multipulse test of L&MOS\_VARIATION shown in Fig. 14(d). (a) Conventional uncontrolled gate driving [Fig. 7(a)]. (b) Proposed GATC [Fig. 7(d)].

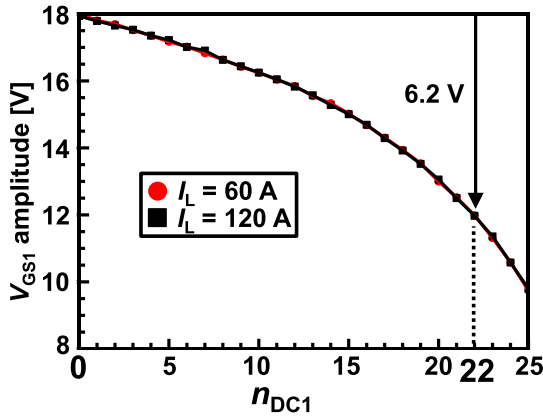


Fig. 21. Measured  $n_{DC1}$  dependence of  $V_{GS1}$  amplitude when GATC [Fig. 7(d)] is operated in open loop under L&MOS\_VARIATION [Fig. 14(d)],  $I_L = 60$  and  $120$  A conditions.

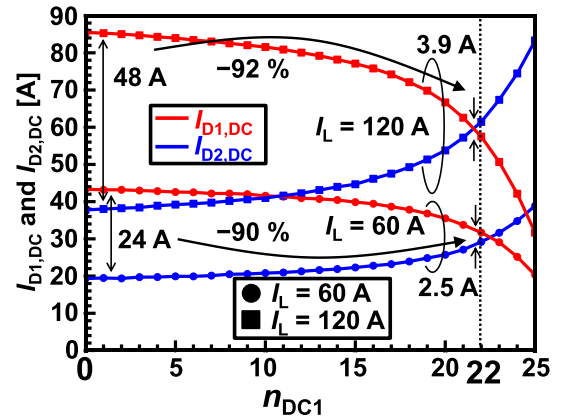


Fig. 22. Measured  $n_{DC1}$  dependence of  $I_{D1,DC}$  and  $I_{D2,DC}$  when GATC [Fig. 7(d)] is operated in open loop under L&MOS\_VARIATION [Fig. 14(d)],  $I_L = 60$  and  $120$  A conditions.

devices. This article is the first in the world to achieve all of the following:

- 1) fully integrated two sensor output processing circuits, two DGDs and a controller required to detect and equalize the drain current variation of two parallel-connected SiC MOSFETs on a gate driver IC,
- 2)  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization in a closed loop,

- 3) demonstration measurements of drain current equalization under a total of four conditions (see Fig. 14), with and without SiC MOSFET characteristic variations and with and without parasitic inductance variations.

By using the proposed SIDO DGD IC, the device characteristic variation problem and the parasitic inductance variation problem on PCBs in parallel-connected power devices can be automatically solved without increasing test cost, design cost,

TABLE II  
COMPARISON TABLE OF DIGITAL CLOSED-LOOP ACTIVE GATE DRIVERS TO EQUALIZE CURRENT IN PARALLEL-CONNECTED POWER DEVICES

Reference, Year	[18] 2021	[25] 2023	[26] 2023	[21] 2021	[20] 2022	This work
Target power device	SiC MOSFET	SiC MOSFET	SiC MOSFET	IGBT	SiC MOSFET	SiC MOSFET
Measured conditions	550 V, 300 A	400 V, 50 A	600 V, 30 A	40 V, 40 A	300 V, 40 A	300 V, 120 A
Implementation	PCB	PCB	PCB	IC	IC	IC
Functions integrated into gate driver IC				1 driver, 1 current sensor, controller	2 drivers, 2 sensor output processing circuits, controller	2 drivers, 2 sensor output processing circuits, controller
Additional circuits other than gate driver IC	CPLD, current sensors	MCU, programmable delay line	DSP (ADC), 3 buck converters	None	None	None
Drive strength change per switching	3	1	3	2	1	2
Target variations	Gate timing, device, parasitic inductance	Device	Device	Gate timing	Device	Device, parasitic inductance
Current sense method	$V_{SS}$	Thermocouples on MOSFETs	Current transformer	Sense emitter	PCB Rogowski coil	PCB Rogowski coil
Parameters to equalize current	Gate timings in 3-level $V_{GS}$	Gate timing	Gate timing, $V_{GS}$	$I_G$	$V_{GS1}, I_{G2}$	$V_{GS}$ (GATC)
Number of parameters adjusted in closed loop per switching	2	1	2	1	2	2
Closed loop $I_{D1,DC}$ and $I_{D2,DC}$ equalization (Required switching cycles)	No	No	Yes (50 cycles)	No	Yes (18 cycles)	Yes (22 cycles)
Closed loop $I_{D1,SURGE}$ and $I_{D2,SURGE}$ equalization (Required switching cycles)	Yes (4 cycles)	Yes (NA)	Yes (35 cycles)	Yes (13 cycles)	No	Yes (14 cycles)
Measurements addressing device variations	No	Yes	Yes	No	Yes	Yes
Measurements addressing parasitic inductance variations	No	No	No	No	No	Yes

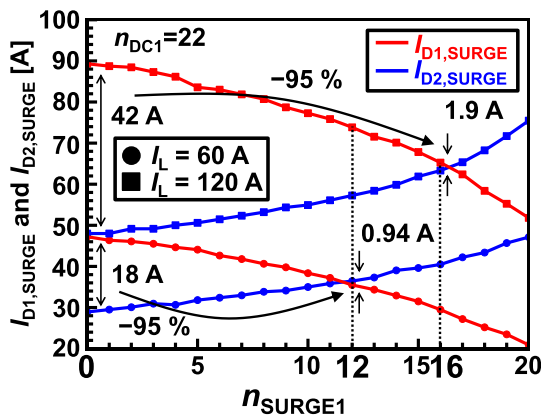


Fig. 23. Measured  $n_{SURGE1}$  dependence of  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  when GATC [Fig. 7(d)] is operated in open loop under L&MOS\_VARIATION [Fig. 14(d)],  $I_L = 60$  and 120 A conditions.  $n_{DC1}$  is fixed to 22.

component cost, or component size. In other words, the proposed SIDO DGD IC has practical value in that the gate driver IC can automatically address the issues of power devices and PCBs in parallel-connected power devices without increasing test cost, design cost, component cost, or component size.

The required switching cycles in this article (22 cycles for  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and 14 cycles for  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization) are longer than those in [18], yet comparable to papers [20], [21], and [26]. To shorten the required switching cycles, the comparator in Fig. 10 can be replaced with an analog-to-digital converter of 2 bits or more, and the controller in Fig. 12 can be modified to change the control bits by  $q$ , where  $q$  is an integer greater than or equal to 1, for each switching cycle. In the use case where large drain current flows in the first switching cycle, the imbalance of the drain current may damage the SiC MOSFETs before the closed-loop control of this IC works. In case of an inductor load, however, as shown in Fig. 20, the

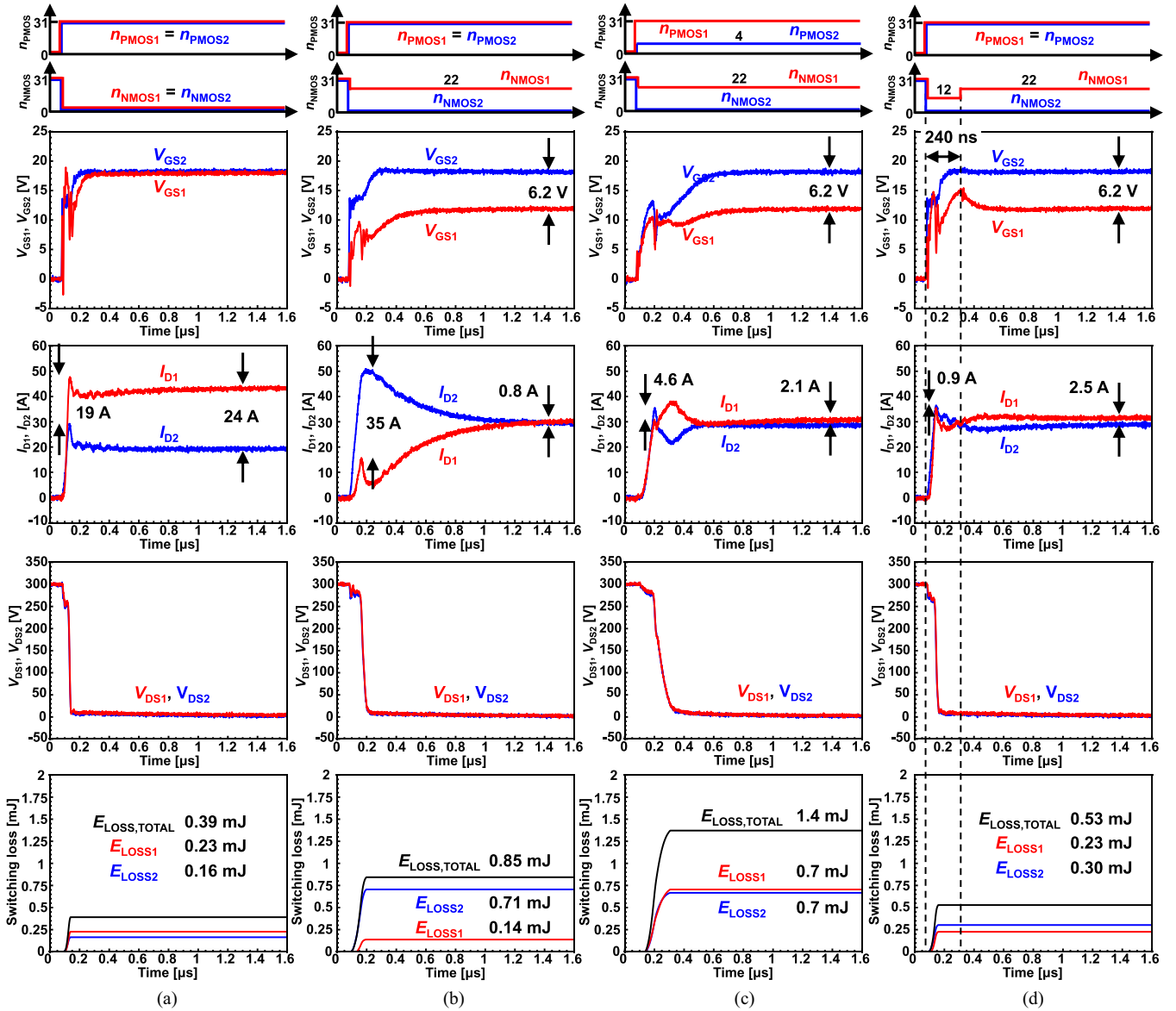


Fig. 24. Measured turn-ON waveforms at  $I_L = 60$  A when four gate driving methods shown in Fig. 7 are operated in open loop under condition of L&MOS\_VARIATION [Fig. 14(d)]. (a) Conventional w/o control. (b) Simple VGS1 control. (c) Conventional VGS1 and IG2 control. (d) Proposed VGS1 gate amplitude twice control (GATC).

drain current gradually increases from zero with each switching, and the closed-loop control of this IC is in time, thus avoiding the damage to the SiC MOSFETs due to the imbalance of the drain current.

## VI. DISCUSSION

### A. DC Power Consumption

In the proposed SIDO DGD IC, the dc power consumption of the gate driver flowing through  $R_P$  and  $R_N$  in Fig. 4(b) is a critical issue, because  $V_{GS1}$  and  $V_{GS2}$  amplitudes are controlled on the principle of a shunt regulator as shown in Fig. 4(b). Therefore, in this section, this dc power consumption problem and its solution are discussed based on the measured results in this article.

In the measured results in this article, the worst case with the maximum dc power consumption is the case of L&MOS\_VARIATION shown in Fig. 14(d) with  $V_{GS1}$  lowered by 5.0 V compared to  $V_{GS2}$  by setting  $n_{DC1} = 22$ , as shown in Fig. 20(b). Since L&MOS\_VARIATION is the most extreme example of variation, it is unlikely to occur in practice, however, the dc power consumption of this example is discussed as a worst-case scenario. During the period of  $n_{DC1} = 22$  in Fig. 20(b), dc current of 1.6 A (simulated) flows through  $R_P$  and  $R_N$  in Fig. 4(b), consuming 30 W ( $= 1.6 \text{ A} \times 18 \text{ V}$ ), which unacceptably high power for a gate driver.

One possible solution to reduce the dc power consumption is a sub DGD circuit shown in Fig. 26. Sub DGD1 is a DGD in which the drain current through each of the six parallel transistors of DGD1 in Fig. 3 is reduced by a factor of  $1/m$  ( $m > 1$ ) (e.g.,

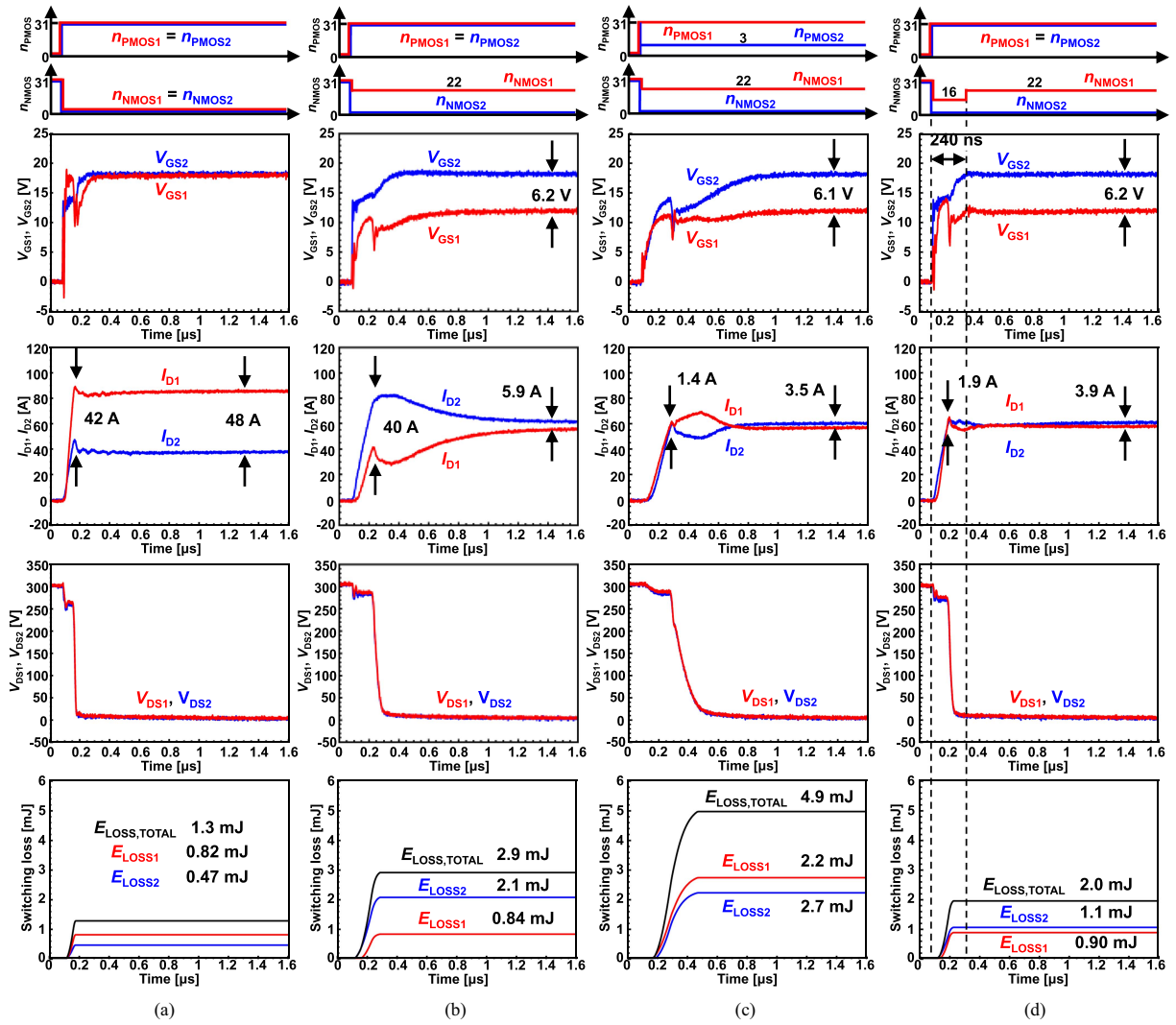


Fig. 25. Measured turn-ON waveforms at  $I_L = 120$  A when four gate driving methods shown in Fig. 7 are operated in open loop under condition of L&MOS\_VARIATION [Fig. 14(d)]. (a) Conventional w/o control. (b) Simple VGS1 control. (c) Conventional VGS1 and IG2 contro. (d) Proposed VGS1 gate amplitude twice control (GATC).

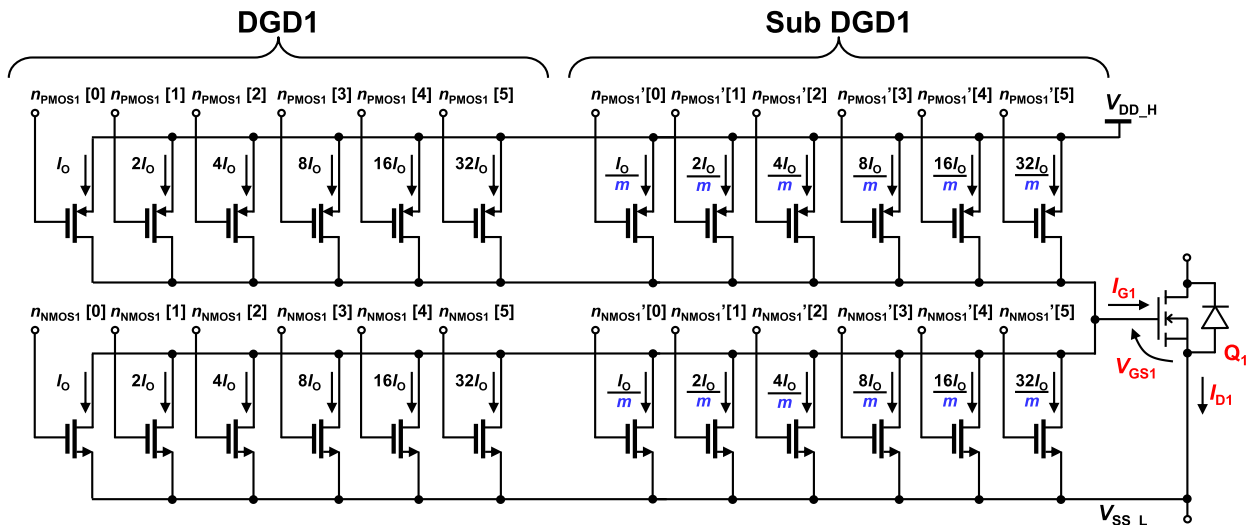


Fig. 26. Circuit schematic of DGD1 and sub DGD1 for  $Q_1$  in Fig. 2 to reduce dc power consumption.

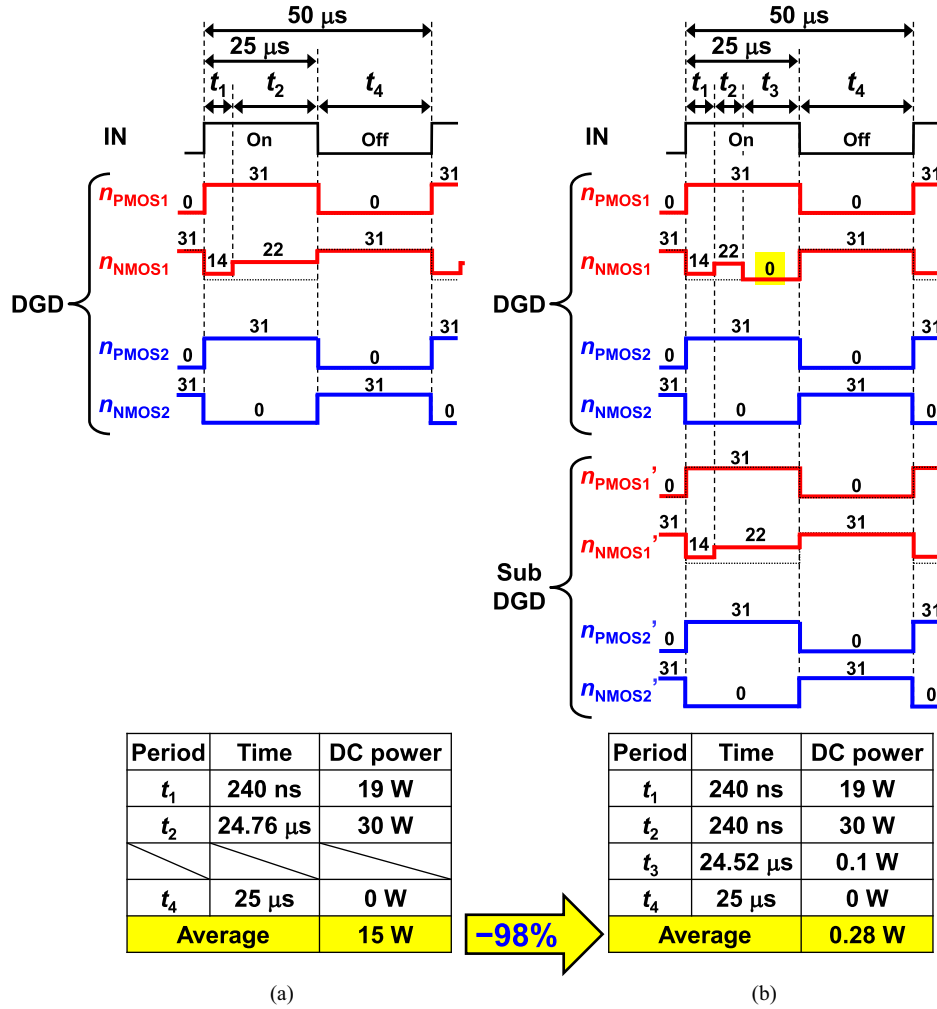


Fig. 27. Timing charts and calculated average DC power consumption of SIDO DGD IC. (a) Without sub DGD. (b) With sub DGD.

$m = 300$ ), and is used in parallel with DGD1. The purpose of sub DGD1 is to reduce the dc power consumption by a factor of  $1/m$  while maintaining steady-state  $V_{GS1}$  at the desired value. Sub DGD1 is always active, while DGD1 is only active during turn-ON or turn-off transients that require a sudden change in  $V_{GS1}$ , and is turned OFF when  $V_{GS1}$  is steady, thereby reducing dc power consumption.

Fig. 27 shows the timing charts and the calculated average dc power consumption of the SIDO DGD IC without and with sub DGD. Fig. 27(a) corresponds to Fig. 5(b), and Fig. 27(b) is Fig. 5(b) with sub DGDs added. The parameters assumed in the calculations are as follows: initial  $I_{D1} > I_{D2}$ , 20 kHz pulsewidth modulation inverter, average duty ratio = 50%,  $m = 300$ ,  $t_1 = 240$  ns,  $t_2 = 240$  ns in Fig. 27(b), and dc power consumption of DGD during  $t_1 = 19$  W (simulated). In Fig. 27(b) with sub DGDs, the 6-bit control signals of DGD1 ( $n_{PMOS1}$  and  $n_{NMOS1}$ ) and those of sub DGD1 ( $n_{PMOS1}'$  and  $n_{NMOS1}'$ ) are identical except during  $t_3$ . In Fig. 27(a), the average dc power consumption is 15 W, which is large and unacceptable since DGD1 consumes 30 W during  $t_2$ . In contrast, in Fig. 27(b), the average dc power consumption is 0.28 W, because the dc power

consumption of sub DGD1 during  $t_3$  is 0.1 W ( $= 30$  W / 300). During  $t_3$ , the dc power consumption of DGD1 is set to zero by setting  $n_{NMOS1} = 0$  in DGD1, while  $V_{GS1}$  is maintained at a steady value by keeping  $V_{GS1}$  in sub DGD1. Thus, comparing Fig. 27(a) and (b), the average dc power consumption can be reduced by 98% from 15 to 0.28 W by using sub DGDs, where 0.28 W is acceptable for gate drivers.

### B. Scaling Up to 3 or More Parallels

While this article describes the SIDO DGD IC for 2-parallel connected SiC MOSFETs, in this section, the possibility of extending the SIDO DGD IC to  $p$ -parallel connected SiC MOSFETs is discussed, where  $p$  is an integer greater than or equal to 3, e.g.,  $p = 4, 6$ , and 8. It is not easy to simply scale up the SIDO DGD IC to four or eight parallel devices with the constraints of single-chip integration, because the chip area of the IC and the dc power consumption increase in proportion to  $p$ . Yet, if the functionality of the SIDO DGD IC is divided into multiple IC chips, extensions to  $p$ -parallel connected SiC MOSFETs would be possible. Fig. 28 shows an example of the extension of the SIDO

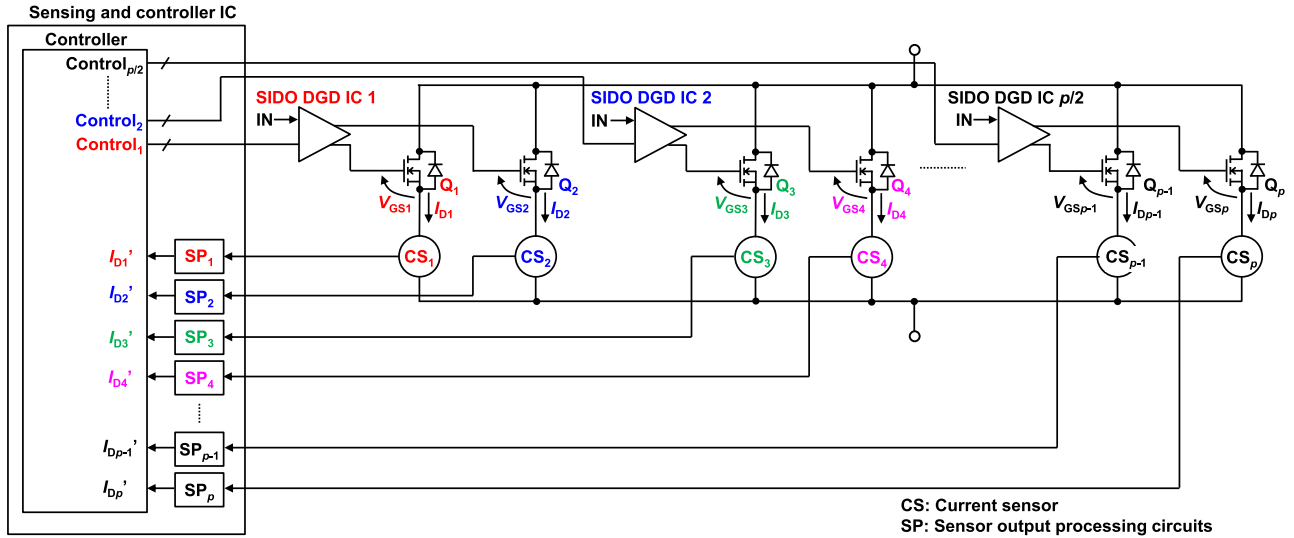


Fig. 28. Extension of SIDO DGD IC to  $p$ -parallel SiC MOSFETs, where  $p$  is integer greater than or equal to 3.

DGD IC to  $p$ -parallel SiC MOSFETs.  $p/2$  SIDO DGD ICs, where the sensor output processing circuits and controller functions are removed, and one sensing and controller IC integrating  $p$  sensor output processing circuits are used to equalize the drain currents of the  $p$ -parallel connected SiC MOSFETs. Drain current equalization algorithms in the controller are future challenges.

## VII. CONCLUSION

SIDO DGD IC, which integrates the sensor output processing circuits, controller, and active gate drivers necessary to equalize  $I_{D1}$  and  $I_{D2}$  of two parallel-connected SiC MOSFETs on a single chip, is proposed. SIDO DGD IC is innovative in that it automatically solves both the device characteristic variation problem and the parasitic inductance variation problem in parallel-connected power devices using a gate driver IC. The proposed GATC in L&MOS\_VARIATION shown in Fig. 20(b) reduces  $I_{D1,SURGE} - I_{D2,SURGE}$  by 86% from 27 A in Fig. 20(a) to 3.9 A by feedback control to  $n_{SURGE1} = 14$ , and reduces  $I_{D1,DC} - I_{D2,DC}$  by 95% from 37 A in Fig. 20(a) to 1.7 A by feedback control to  $n_{DC1} = 22$  and  $V_{GS2} - V_{GS1} = 5.0$  V. In summary, it has been successfully demonstrated that the proposed GATC using SIDO DGD IC achieves both  $I_{D1,DC}$  and  $I_{D2,DC}$  equalization and  $I_{D1,SURGE}$  and  $I_{D2,SURGE}$  equalization under a total of four conditions, with and without SiC MOSFET characteristic variations and with and without parasitic inductance variations.

Future applications of the SIDO DGD IC could include SiC modules for high-temperature, high-current applications [1], [2], [3] that contain this IC ported on a SiC CMOS process compatible with high temperatures and SiC power dies connected in parallel in a single power module.

## REFERENCES

- [1] H. Li, S. Zhao, X. Wang, L. Ding, and H. A. Mantooth, "Parallel connection of silicon carbide MOSFETs—Challenges, mechanism, and solutions," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9731–9749, Aug. 2023.
- [2] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, and H. A. Mantooth, "A review of switching slew rate control for silicon carbide devices using active gate drivers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4096–4114, Aug. 2021.
- [3] D. Bortis, J. Biela, and J. W. Kolar, "Active gate control for current balancing of parallel-connected IGBT modules in solid-state modulators," *IEEE Trans. Plasma Sci.*, vol. 36, no. 5, pp. 2632–2637, Oct. 2008.
- [4] M. Sasaki, H. Nishio, A. Shorten, and W. T. Ng, "Current balancing control for parallel connected IGBTs using programmable gate driver output resistance," in *Proc. 25th Int. Symp. Power Semicond. Devices IC's*, 2013, pp. 65–68.
- [5] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 1563–1569.
- [6] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active compensation of current unbalance in paralleled silicon carbide MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1471–1477.
- [7] V. Jadhav, Y. Zhou, and U. Jansen, "Analysis of different IGBT gate driver strategies influencing dynamic paralleling performance," in *Proc. PCIM Asia Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2016, pp. 1–9.
- [8] Y. Chen, F. Zhuo, W. Pan, F. Zhang, and L. Feng, "A novel active gate driver for static and dynamic current balancing of parallel-connected IGBTs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 795–799.
- [9] J. Hackel, M. Ebli, and M. Pfoth, "A novel gate driving approach to balance the transient current of parallel-connected GaN-HEMTs," in *Proc. 10th Int. Conf. Integr. Power Electron. Syst.*, 2018, pp. 1–4.
- [10] C. Luedecke, F. Krichel, M. Laumen, and R. W. De Doncker, "Balancing the switching losses of paralleled SiC MOSFETs using an intelligent gate driver," in *Proc. PCIM Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2020, pp. 1–7.
- [11] R. N. Tripathi, M. Tsukuda, and I. Omura, "Dynamic current balancing of parallel connected IGBT devices using PCB sensor for integration in power modules," in *Proc. 11th Int. Conf. Integr. Power Electron. Syst.*, 2020, pp. 1–5.
- [12] Y. Wei, R. Sweeting, M. M. Hossain, H. Mhiesan, and A. Mantooth, "Variable gate voltage control for paralleled SiC MOSFETs," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, 2020, pp. 1–7.
- [13] Y. Funaki and K. Wada, "Gate drive circuit implementation for parallel connection of power devices considering parasitic inductance," *IEEJ J. Ind. Appl.*, vol. 12, no. 2, pp. 176–182, 2023.
- [14] Y. Wei, L. Du, X. Du, and A. Mantooth, "Multi-level active gate driver for SiC MOSFETs with paralleling operation," in *Proc. IEEE 22nd Workshop Control Model. Power Electron.*, 2021, pp. 1–7.
- [15] C. Luedecke, M. Laumen, and R. W. De Doncker, "Balancing unequal temperature distributions of parallel-connected SiC MOSFETs using an intelligent gate driver," in *Proc. IEEE 8th Workshop Wide Bandgap Power Devices Appl.*, 2021, pp. 299–304.

[16] X. Wang, Y. He, J. Zhang, S. Shao, H. Li, and C. Luo, "An active gate driver for dynamic current sharing of paralleled SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5407–5411.

[17] C. Ludecke, A. Aghdaei, M. Laumen, and R. W. D. Doncker, "Balancing the switching losses of paralleled SiC MOSFETs using a step-wise gate driver," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5400–5406.

[18] Y. Wen, Y. Yang, and Y. Gao, "Active gate driver for improving current sharing performance of paralleled high-power SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1491–1505, Feb. 2021.

[19] J. Brandelero, J. Ewanchuk, and S. Mollov, "Selective gate driving in intelligent power modules," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 898–910, Jan. 2021.

[20] K. Horii et al., "Equalization of DC and surge components of drain current of two parallel-connected SiC MOSFETs using single-input dual-output digital gate driver IC," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 1406–1412.

[21] M. Sasaki, K. Takagiwa, and K. Yano, "Gate driver ICs with closed-loop current balancing control for parallel connected IGBTs," *IEEJ J. Ind. Appl.*, vol. 11, no. 6, pp. 822–832, 2022.

[22] M. Parker, I. Sahin, R. Mathieson, S. Finney, and P. D. Judge, "Investigation into active gate-driving timing resolution and complexity requirements for a 1200 V 400 A silicon carbide half bridge module," *IEEE Open J. Power Electron.*, vol. 4, pp. 161–175, 2023.

[23] H. Takayama, S. Fukunaga, and T. Hikiyama, "Binary-weighted modular multi-level digital active gate driver," in *Proc. 25th Eur. Conf. Power Electron. Appl.*, 2023, pp. 1–8.

[24] Y. He, X. Wang, S. Shao, and J. Zhang, "Active gate driver for dynamic current balancing of parallel-connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6116–6127, May 2023.

[25] C. Lüdecke, N. Fritz, and R. W. De Doncker, "Design of a closed-loop control to balance unequal temperature distributions of parallel-connected SiC MOSFETs," in *Proc. 11th Int. Conf. Power Electron. ECCE Asia*, 2023, pp. 105–111.

[26] L. Du et al., "Digital close-loop active gate driver for static and dynamic current sharing of paralleled SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1372–1384, Apr. 2024.

[27] N. Lin, A. J. R. A. Hmoud, and Y. Zhao, "An active gate driver control scheme for steady-state current balancing of paralleled SiC MOSFETs," *IEEE Trans. Circuits Syst. II Exp. Briefs*, vol. 71, no. 9, pp. 4341–4345, Sep. 2024.

[28] M. Koga, M. Tsukuda, K. Nakashima, and I. Omura, "Application-specific micro Rogowski coil for power modules - design tool, novel coil pattern and demonstration," in *Proc. 9th Int. Conf. Integr. Power Electron. Syst.*, 2016, pp. 1–5.



**Shin-Ichiro Hayashi** (Member, IEEE) was born in Toyama, Japan, in 1990. He received the B.S. and M.S. degrees in electrical and electronic engineering and the Ph.D. degree in electrical engineering from Tokyo Metropolitan University, Tokyo, Japan, in 2014, 2016, and 2022, respectively.

From 2016 to 2019, he worked for Mitsubishi Electric Corporation, where he was involved in the design and development of power supplies for rolling stock. Since 2022, he has been an Assistant Professor with the Department of Electrical and Electronic Engineering, Chiba Institute of Technology, Chiba, Japan. His research interests include long-term reliability of power semiconductor devices, condition monitoring of power converters, and circuit implementation technology.



**Keiji Wada** (Senior Member, IEEE) He received the Ph.D. degree in electrical engineering from Okayama University, Okayama, Japan, in 2000.

From 2000 to 2006, he was an Assistant Professor with Tokyo Metropolitan University, Tokyo, Japan, and Tokyo Institute of Technology, Tokyo. From 2006 to 2020, he was an Associate Professor with Tokyo Metropolitan University. Since 2021, he has been a Professor with Tokyo Metropolitan University. His research interests include medium-voltage inverters, electromagnetic interference filters, and gate drive circuits.

Dr. Wada is a Senior Member of IEEEJ.



**Ichiro Omura** (Member, IEEE) was born in Japan in 1961. He received the B.S. and M.S. degrees in mathematics from Osaka University, Osaka, Japan, in 1985 and 1987, respectively, and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH Zurich), Zurich, Switzerland, in 2001.

He worked with the Research and Development Center, Toshiba Corporation and Toshiba Semiconductor. He was a Guest Researcher at ETH Zurich, from 1996 to 1997. He has been a Professor with the Kyushu Institute of Technology, Fukuoka, Japan,

where he established the Next Generation Power Electronics Research Center. His research interests include power semiconductor devices and power electronics.

Dr. Omura is a member of IEEEJ.



**Kohei Horii** received the B.S. degree from The University of Electro-Communications, Tokyo, Japan, in 2020, and the M.S. degree in electronic engineering from The University of Tokyo, Tokyo, in 2022, both in electronic engineering.

In 2022, he joined Sony Semiconductor Solutions Corporation, Atsugi, Japan, where he was engaged in the design of analog circuits for image sensors. Since 2024, he has been with Toshiba Corporation, Kawasaki, Japan, where he is currently engaged in the research and development of integrated gate driver.



**Katsuhiko Hata** (Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Tokyo, Tokyo, Japan, in 2018.

From 2016 to 2019, he was a Research Fellow (DC1) with the Japan Society for the Promotion of Science (JSPS). From 2019 to 2024, he was a Research Associate with the Institute of Industrial Science, University of Tokyo. Since 2024, he has been an Associate Professor with the Shibaura Institute of Technology, Tokyo. His research interests include hybrid dc–dc converters, digital active gate driving,

wireless power transfer, and e-mobility for transportation.



**Makoto Takamiya** (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the University of Tokyo, Tokyo, Japan, in 1995, 1997, and 2000, respectively, all in electronic engineering.

In 2000, he joined NEC Corporation, Japan, where he was engaged in the circuit design of high speed digital LSI's. In 2005, he joined the University of Tokyo, where he is currently a Professor with the Institute of Industrial Science. From 2013 to 2014, he stayed at the University of California, Berkeley, as a Visiting Scholar. His research interests include the

digital gate driver and sensor ICs for power electronics and the integrated power management circuits for automotive and industrial applications.

Dr. Takamiya is an elected member of administrative committee in IEEE Solid-State Circuits Society from 2023 to 2025. He is a member of the technical program committee of IEEE Symposium on VLSI Technology and Circuits, IEEE Asian Solid-State Circuits Conference, and IEEE International Symposium on Power Semiconductor Devices and ICs. He formerly served on the technical program committees of IEEE International Solid-State Circuits Conference (ISSCC) from 2015 to 2020 and IEEE Custom Integrated Circuits Conference from 2006 to 2011. He was a Far East Regional Chair in ISSCC 2020. He was a Distinguished Lecturer of IEEE Solid-State Circuits Society from 2019 to 2020. He was the recipient of 2009 and 2010 IEEE Paul Rappaport Awards and the best paper award in 2013 IEEE Wireless Power Transfer Conference.