One-Step Method of Dynamic Capacitances Extraction From a SiC Power MOSFET in a Half-Bridge Package for EMI Analysis

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***Abstract*—The electromagnetic interference (EMI) and dynamic capacitance characteristics of metal-oxide-semiconductor field-effect transistors (MOSFETs) are essential considerations in circuit design and electromagnetic compatibility. A MOSFET is a semiconductor widely used in switching applications. The dynamic capacitance characteristics of a MOSFET are closely related to the switching behavior of the circuit and EMI generation. Therefore, for EMI analysis and to control power conversion systems, the capacitances of the MOSFETs have to be accurately known. The capacitance of a MOSFET changes depending on the dc bias voltage. In other words, this means that EMI characteristics may vary depending on operating conditions, so capacitance must be obtained based on the dc voltage. Much research has been conducted on the capacitance extraction of a single MOSFET. However, the complexity of the half-bridge structure increases as the number of terminals increases, so conventional research has limitations. This article proposes a method to extract the half-bridge MOSFET dynamic capacitances simply using a one-step measurement. By changing the terminal connection of the half-bridge MOSFET, the dynamic capacitances were obtained through two-port S-parameter measurement. The proposed method was verified through simulation and experiment, and a switching test was performed for EMI analysis.**

***Index Terms*—Electromagnetic interference (EMI), half-bridge metal-oxide-semiconductor field-effect transistors (MOSFETs), MOSFET capacitances, S-parameter, switching noise.**

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I. Introduction

MOST power conversion systems, especially inverters, and converters, use silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) in a half-bridge configuration [1], [2]. In other words, the MOSFET plays a vital role in the power conversion system. In these systems, the efficient operation of the MOSFET is an essential factor that determines the performance and reliability of the overall system. The dynamic capacitance of MOSFETs is closely related to the efficiency, reliability, and electromagnetic compatibility (EMC) of the system, and its importance in the design and optimization process of power conversion systems cannot be overemphasized [3], [4], [5].

In power electronics, electromagnetic interference (EMI) mitigation is crucial due to its significant impact on the performance and reliability of electronic systems. EMI can cause malfunctions, degrade signal integrity, and lead to noncompliance with regulatory standards, potentially resulting in the failure of power electronic devices. Effective EMI mitigation ensures that power electronics systems operate efficiently within the electromagnetic environment, reducing noise emissions and susceptibility to external disturbances. This is particularly important in applications such as electric vehicles, renewable energy systems, and industrial automation, where maintaining EMC is essential for system reliability and safety. Therefore, incorporating robust EMI mitigation strategies during the design and development phases is vital to achieving optimal performance and compliance with global EMC standards.

In particular, accurately extracting the dynamic capacitance of the MOSFET in a half-bridge configuration is very important during the design process. This allows designers to minimize switching losses and optimize power conversion efficiency. Additionally, EMC standards can be satisfied by planning the EMI filtering strategy more accurately [6]. In conclusion, the accurate extraction and management of dynamic capacitances in a half-bridge MOSFET package is essential for the efficiency, reliability, and EMC standards of power conversion systems. So, minimizing switching losses, managing heat generation, and reducing EMI are critical factors in developing power conversion solutions. Therefore, when starting the design process, it is

crucial to consider dynamic capacitances from the initial design stage [7].

Existing methods for extracting the dynamic capacitance of a MOSFET are mainly divided into two types. The first is to change the dc voltage between the drain and source with the gate voltage at 0 and measure it using an impedance analyzer, curve tracer, or vector network analyzer (VNA) [8], [9]. Impedance analyzers and curve tracers both measure impedance by evaluating voltage and current, with curve tracers being more specialized for power device measurements. Impedance analyzers extract impedance through radio frequency (RF) V-I measurements across a wide frequency range using frequency sweeps. Curve tracers, on the other hand, extract capacitance by generating high-voltage, high-current curves at a single frequency. Additionally, the network analyzer measures the reflection and transmission characteristics of a signal as S-parameters, which can be converted into impedance. The second involves characterizing dynamic capacitance using transient waveforms measured during switching operations [10], [11], [12], [13].

Manufacturers primarily provide datasheets using the first method, which typically involves the use of curve tracers. This method is advantageous for reliably extracting the dynamic capacitance of MOSFETs. Additionally, numerous studies have been conducted using impedance analyzers and network analyzers for more precise impedance measurements [8], [9], [15], [16]. These instruments are particularly useful for analyzing impedance in high-frequency environments, allowing for the precise evaluation of stray inductance and capacitance that can affect circuit performance, especially through high-frequency response and S-parameter measurements [14].

However, terminal floating issues may occur when applying this method to a half-bridge configuration. Since the impedance analyzer is based on a one-port network measurement method, three of the five terminals in the half-bridge MOSFETs are inevitably floating [8]. A two-port network measurement using a VNA generates at least two floating terminals, affecting the measurement results [9]. Curve tracers adopt an internal wiring change method to prevent floating issues that can occur during measurements with impedance analyzers or network analyzers. This internal adjustment allows the curve tracer to automate the process while conducting multiple measurements [14].

To solve these problems, research was conducted to extract capacitances while changing the terminal wiring to eliminate open terminals [15], [16]. Liu et al. [15] and Zhong et al. [16] proposed a method to measure the device capacitances of a half-bridge MOSFET while changing the terminal wiring in 5 or 3 steps, respectively. These methods can eliminate terminal floating issues, but there is a problem with multiple measurement steps, and additional test fixtures must be manufactured accordingly. In addition, there is a method to extract the dynamic capacitance of a single MOSFET depending on the dc voltage by inductively measuring the two-port S-parameter using two current probes [17]. This method can also eliminate floating issues but has the limitation that the wiring has to be changed depending on the measurement conditions. Additionally, when this method is applied to a half-bridge MOSFET, additional floating terminals are generated, further increasing the number of measurement setups required.

The second type of method is an approach that inversely characterizes the capacitances by fitting the switching waveform during operation. This has an advantage in that it allows the correlation between the phenomenon and the extraction results to be identified with high accuracy but has the limitation that the results are dominated by the measurement environment [10], [11], [12], [13]. If the measurement environment and settings are changed and unstable, transient results may occur, reducing the accuracy of device component extraction. Additionally, these methods have more complicated procedures than the first methods.

Therefore, to increase the convenience of the measurement method, this article focuses on a two-port network analysis using VNA. This article proposes a topology that allows the measurement of a two-port network without floating issues, and using this, the device capacitance of the half-bridge MOSFET, depending on each voltage level, can be extracted through a one-step measurement. Unlike conventional research, it can perform an extraction with a single test fixture and fixed measurement environment without changing the terminal wiring. This is critical to ensure measurement accuracy and reproducibility. The proposed method was verified through three-dimensional (3-D) EM simulation and experiment, and extraction was performed from 300 kHz to 30 MHz for EMI analysis [18].

In order to analyze EMI during switching based on the result of the proposed method, a switching circuit was designed, and the switching waveform was measured. The relationship between the ringing phenomenon occurring at the measured switching voltage and parasitic capacitance was analyzed, and switching noise was analyzed and compared with simulation in the frequency domain.

The rest of this article organized as follows. Section I introduces the motivation and purpose of this research. In Section II, circuit analyses of a single MOSFET and a half-bridge MOSFET are conducted. Section III shows the proposed parasitic capacitance extraction method. In Sections IV and V, the proposed method is verified through simulation and experiment, respectively. Section VI shows the relationship between this research and EMI through switching tests. In Section VII, the limitations of this study are discussed. Finally, Section VIII concludes this article.

II. Circuit Analysis of Power MOSFET

This section shows a circuit model analysis, including MOSFET components and the relationship between the MOSFET and EMI. In addition, the existing method of extracting the device capacitances of the MOSFET using delta-star conversion and the circuit of the half-bridge MOSFET package to form a module is introduced.

A. Device Capacitances and Ringing

The equivalent circuit model, including the device components of the MOSFET, is important for understanding and

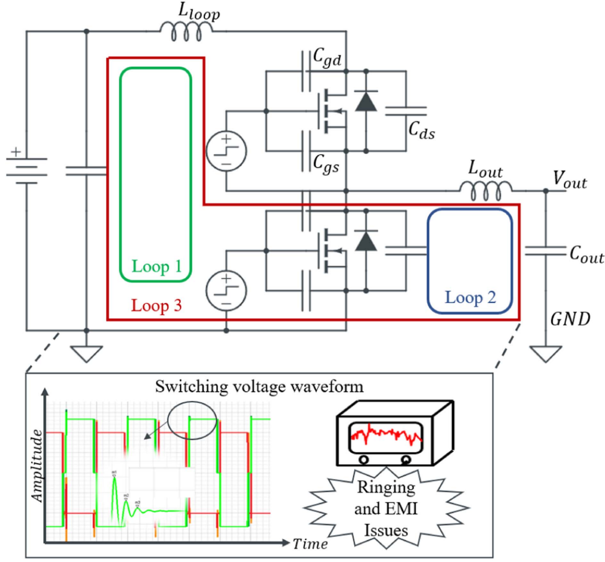


Fig. 1. Example concept of the ringing and EMI issues of MOSFETs in power conversion circuit.

designing the actual operation of the MOSFET. Fig. 1 shows the internal device components of a MOSFET and the circuit containing them. This model includes various device components inside the MOSFET, allowing for more accurate performance prediction under actual operating conditions.

MOSFET includes dynamic capacitance, device inductance, and resistance. Among these, device capacitances are one of the important dynamic characteristics found in MOSFETs. They are mainly classified into three terminals: 1) gate-source (C_{gs}), 2) gate-drain (C_{gd}), and 3) drain-source (C_{ds}) capacitance. C_{gs} transfers changes in gate voltage to the source during switching operations, and C_{gd} causes voltage fluctuations during switching, affecting switching performance. C_{ds} is observed when the MOSFET is turned OFF.

These device capacitances can resonate with the loop inductance during switching, causing the ringing. For example, as shown in Fig. 1, high-frequency noise loops such as loop 1 may be generated in addition to loops 2 and 3, and these loops cause ringing. During switching operations, the capacitance of the MOSFET causes a change in the switching voltage, which leads to a change in current. Loop inductance limits the rate of this current change and can cause voltage spikes. Therefore, voltage spikes can cause switching loss and increase EMI.

In Fig. 1, the noise paths attributed to the intrinsic capacitances of the MOSFET are illustrated. However, it is important to note that when a gate driver is employed, the parasitic capacitance generated by the isolation barrier of the driver power supply can also significantly contribute to the noise path [19]. Additionally, parasitic capacitance that arises between the ground and power lines in a power system can influence both the noise path and the magnitude of the noise [20]. Nevertheless, these factors can vary depending on the design of the power electronics systems. In other words, engineers need to know the intrinsic capacitance of the MOSFET accurately so that they can design the system taking its influence into account. So, this article focuses

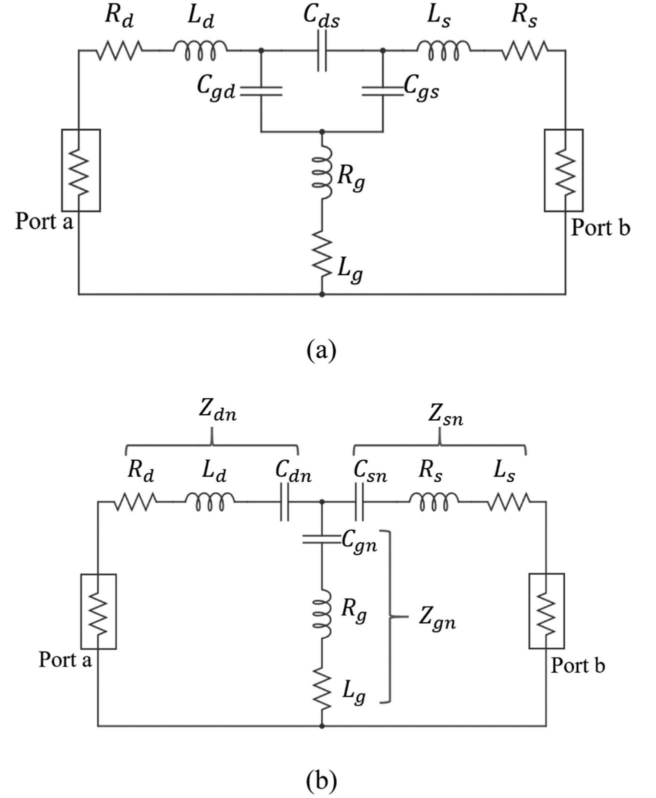


Fig. 2. General equivalent circuit of a MOSFET. (a) Delta-connected equivalent circuit model. (b) Star-connected equivalent circuit model.

on the method of extracting the intrinsic capacitances of the MOSFET, specifically in a half-bridge module, which involves the extraction of the intrinsic capacitances.

In addition to device capacitances, stray inductances, and resistances are also included. However, in general, the inductance of a trace or cable is much larger than the stray inductance of a package-type half-bridge MOSFET, so capacitance is an important factor affecting EMI [21].

B. Circuit Analysis

The components of the MOSFET are expressed as an equivalent circuit, as shown in Fig. 2(a) and (b). The first step to finding the capacitances of each terminal in a circuit, such as Fig. 2(a) composed of a delta circuit, is to measure it with a star circuit and then obtain the capacitance through delta-star inverse conversion [22]. Equations (1)–(3) refer to the impedance of each terminal

$$Z_{dn} = R_d + j\omega L_d + \frac{1}{j\omega C_{dn}} \quad (1)$$

$$Z_{gn} = R_g + j\omega L_g + \frac{1}{j\omega C_{gn}} \quad (2)$$

$$Z_{sn} = R_s + j\omega L_s + \frac{1}{j\omega C_{sn}}. \quad (3)$$

Using the impedance of each terminal, the series equivalent capacitances C_{gn}, C_{dn}, and C_{sn} can be obtained, respectively,

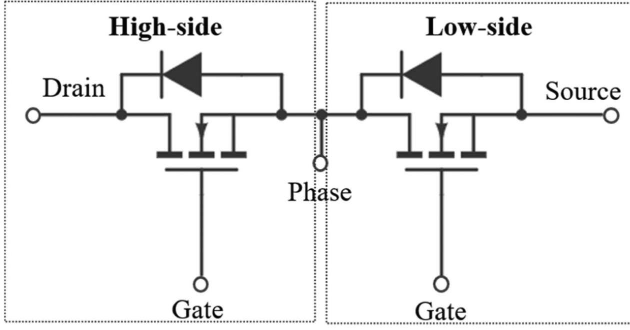


Fig. 3. Typical half-bridge MOSFET configuration.

as follows:

$$C_{gd} = \frac{C_{gn}C_{dn}}{C_{dn} + C_{gn} + C_{sn}} \tag{4}$$

$$C_{gs} = \frac{C_{gn}C_{sn}}{C_{dn} + C_{gn} + C_{sn}} \tag{5}$$

$$C_{ds} = \frac{C_{dn}C_{sn}}{C_{dn} + C_{gn} + C_{sn}}. \tag{6}$$

Equations (4)–(6) above calculate the capacitance between each terminal using the capacitance obtained from the series impedance [22]

$$C_{iss} = C_{gs} + C_{gd} \tag{7}$$

$$C_{oss} = C_{ds} + C_{gd} \tag{8}$$

$$C_{rss} = C_{gd}. \tag{9}$$

To compare the extracted capacitances between each terminal with the datasheet, C_{iss}, C_{oss}, and C_{rss} are obtained using (7)–(9). C_{iss} represents the amount of charge required when the gate of a MOSFET is charged or discharged, depending on the voltage change applied to the gate. C_{oss} means the amount of charge that can be stored between a drain and source and is especially important when the MOSFET is OFF. Finally, C_{rss} describes the change in capacitance between the gate and drain during the switching operation and is related to the switching speed [23]

$$Z_{aa} = Z_{dn} + Z_{gn} \tag{10}$$

$$Z_{ba} = Z_{ab} = Z_{gn} \tag{11}$$

$$Z_{bb} = Z_{sn} + Z_{gn}. \tag{12}$$

The impedance of each terminal that can be obtained from a two-port network, as shown in Fig. 2, is equal to (10)–(12), and the capacitance can be obtained through these equations. Based on the two-port network theory, the capacitances of a single MOSFET can be easily obtained. For measurement depending on the dc voltage, a method using a bias-tee, or dual current probes can be used based on an equivalent circuit model [17], [24].

However, the half-bridge package, which has a structure of two single MOSFETs connected in series, as shown in Fig. 3, cannot use the previous method directly. A single MOSFET has three terminals, but a half-bridge MOSFET has at least five terminals: 1) high-side drain, 2) low-side source, high-side and low-side gate, and a phase where the high-side source and low-side drain meet. Therefore, when configuring the same two-port network as a single MOSFET, issues due to floating terminals may occur, and even if floating issues are eliminated by changing the wiring between terminals as in previous studies, at least three or five test fixtures are required [15], [16].

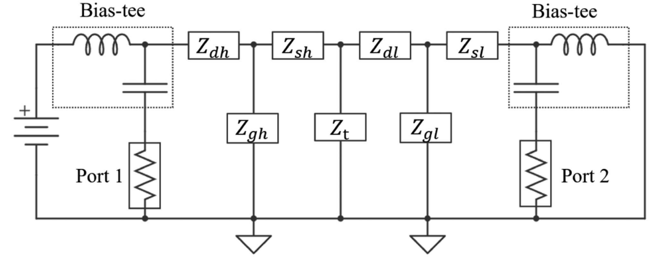


Fig. 4. Equivalent circuit model of the proposed method.

Additionally, even if you connect a dc voltage across the high-side drain and low-side source without changing the wiring, the capacitor does not allow dc to pass, so no voltage is distributed between the high-side and low-side, respectively.

In other words, the dynamic capacitances of the half-bridge package cannot be extracted using the previously proposed two-port network theory method. A method to solve this problem and extract the capacitance with a single measurement is proposed in the next chapter.

III. Proposed One-Step Extraction Method

This section proposes a topology for extracting the dynamic capacitances of a MOSFET in a half-bridge configuration with a single measurement. A measurement method using a bias-tee based on a two-port network is explained, and a method for extracting the capacitance in a static state where the dc voltage is 0 V, and the nonlinear dynamic capacitance depending on the dc voltage is proposed. Only one test fixture is required to apply this method, and measurement steps using the proposed method are presented.

A. Proposed Topology for Extraction

Previous research measured S-parameters using a VNA and protected the VNA using bias tees to simultaneously apply dc voltage [25]. The proposed topology, including bias-tee, is shown in Fig. 4.

In Figs. 3 and 4, when the phase between the source of the high-side and the drain of the low-side is open, even if a dc voltage is connected to port 1, no voltage is applied to the high-side and low-side MOSFET. This is due to the characteristics of the capacitors that do not pass dc.

Therefore, in order to apply dc voltage between the drain and the source, the phase terminal has to be connected to the ground. Now, two methods can be considered: One is to short-circuit the phase and ground, and the other is to connect the phase and ground through different impedance components. Shorting phase and ground and then connecting a dc voltage to port 1

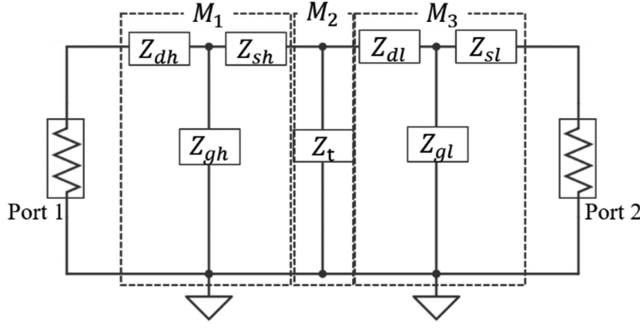


Fig. 5. Simplified two-port network of the proposed method.

causes a dc voltage to be applied between the drain and the source of the high side. On the other hand, the voltage between the low-side drain and the source becomes zero. In other words, in the short-circuit, the voltage can be input, but since all current flows through the shorted part S_{21}, this means transfer characteristics become very small. Ideally, when the phase is short-circuited, the component passing to port 2 disappears, so S_{21} becomes minus infinity, which is a value that cannot be measured. To solve this, the proposed method connects Z_t, a 50 Ω resistor between the phase and ground, as shown in Fig. 4.

However, the resistance to connect the phase and ground does not necessarily have to be 50 Ω. The reason why 50 Ω was used in the proposed topology is because a component with constant impedance depending on frequency is required. In other words, by using a 50-Ω load connector in the calibration kit, a constant impedance can be maintained within the frequency range to be verified in the proposed method, and its value can be known. Therefore, in this research, a 50-Ω load calibration kit was used to ensure stable measurement and measurement accuracy of S_{21}. Additionally, if the phase and ground are short-circuited and Z_t is 0, the two-port network of the proposed topology cannot be calculated.

Also, in general, it is not easy to know the internal structure of a MOSFET, and manufacturers do not disclose it. The datasheet of the half-bridge MOSFET provided by the vendor does not offer separate high-side and low-side capacitances. Additionally, several existing studies have demonstrated that the capacitances of the high side and low side of a MOSFET are identical [9], [15], [16]. This leads us to assume that the high-side capacitance and low-side capacitance are equal. Therefore, in this research, based on this assumption, the high-side dynamic capacitance was extracted using the device capacitance measurement results when the dc voltage was 0 V. Specific methods and theories are explained in the following sections.

B. Static Capacitances Extraction Method

First, this is a method of extracting the device capacitance of the half-bridge MOSFET in a static state when the dc bias voltage is 0 V. Before the explanation, in order to simplify the proposed topology, the Z matrix was characterized by the ABCD matrix calculation [26]. Equations (13)–(15) divide the circuit in Fig. 5 into three parts and express them as an ABCD matrix

$$M_1 = \begin{bmatrix} Z_{dh}/Z_{gh}+1 & Z_{sh}\left(Z_{dh}/Z_{gh}+1\right) \\ 1/Z_{gh} & Z_{sh}/Z_{gh}+1 \end{bmatrix} \tag{13}$$

$$M_2 = \begin{bmatrix} 1 & 0 \\ 1/Z_t & 1 \end{bmatrix}, \text{ where } Z_t = 50 \tag{14}$$

$$M_3 = \begin{bmatrix} Z_{dl}/Z_{gl}+1 & Z_{sl}\left(Z_{dl}/Z_{gl}+1\right) \\ 1/Z_{gl} & Z_{sl}/Z_{gl}+1 \end{bmatrix}. \tag{15}$$

With the three matrices above, the two-port network of the entire circuit can be obtained using

$$M = M_1\, M_2\, M_3 = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{16}$$

$$A = Z_{gh}\, Z_{gl} + (Z_{dl}+Z_{gl})\left(Z_{dh}+Z_{gh}+\frac{Z_{gh}}{Z_t}\right) \tag{17}$$

$$B = Z_{gl}\left(Z_{dh}+Z_{gh}+\frac{Z_{gh}}{Z_t}\right) + Z_{gh}\left(Z_{gl}+Z_{sl}\right) \tag{18}$$

$$C = (Z_{dl}+Z_{gl})\left(Z_{gh}+\frac{Z_{gh}+Z_{sh}}{Z_t}\right) + Z_{gl}\left(Z_{gh}+Z_{sh}\right) \tag{19}$$

$$D = (Z_{gh}+Z_{sh})\,(Z_{gl}+Z_{sl}) + Z_{gl}\left(Z_{gh}+\frac{Z_{gh}+Z_{sh}}{Z_t}\right). \tag{20}$$

Using network theory, the ABCD matrix in (16) can be converted to the Z parameter as in

$$Z = \frac{1}{C}\begin{bmatrix} A & |AD-BC| \\ 1 & D \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}. \tag{21}$$

From the obtained matrix, the impedance can be obtained in a static state, and Z_{12} and Z_{21} are the same [26]. First, at 0 V, the impedance of the high-side and low-side can be assumed to be the same as [16]

$$Z_{dh}\,|_{V=0} = Z_{dl}\,|_{V=0} = Z_{dl} \tag{22}$$

$$Z_{gh}\,|_{V=0} = Z_{gl}\,|_{V=0} = Z_{gl} \tag{23}$$

$$Z_{sh}\,|_{V=0} = Z_{sl}\,|_{V=0} = Z_{sl}. \tag{24}$$

At this time, since the only unknowns in the Z matrix obtained in (21) are Z_{dl}, Z_{sl}, and Z_{gl}, the solution can be obtained using a cubic system of equations.

Equations (25)–(27) are cubic equations for calculating the impedance of each terminal in a static state

$$Z_{11}\,|_{V=0} = \frac{Z_{gl}^2 + (Z_{dl}+Z_{gl})\left(Z_{dl}+Z_{gl}+\frac{Z_{gl}}{Z_t}\right)}{(Z_{dl}+Z_{gl})\left(Z_{gl}+\frac{Z_{gl}+Z_{sl}}{Z_t}\right)+Z_{gl}\left(Z_{gl}+Z_{sl}\right)} \tag{25}$$

$$Z_{12}\,|_{V=0} = Z_{21}\,|_{V=0} = \frac{1}{(Z_{dl}+Z_{gl})\left(Z_{gl}+\frac{Z_{gl}+Z_{sl}}{Z_t}\right)+Z_{gl}\left(Z_{gl}+Z_{sl}\right)} \tag{26}$$

$$Z_{22}\mid_{V=0}=\frac{\left(Z_{gl}+Z_{sl}\right)^2+Z_{gl}\left(Z_{gl}+\frac{Z_{gl}+Z_{sl}}{Z_t}\right)}{\left(Z_{dl}+Z_{gl}\right)\left(Z_{gl}+\frac{Z_{gl}+Z_{sl}}{Z_t}\right)+Z_{gl}\left(Z_{gl}+Z_{sl}\right)}. \tag{27}$$

The impedance of each terminal obtained using (25)–(27) is the same as (28) shown at bottom of this page, (29) and (30), and the device capacitance can be obtained using (4)–(6),

$$Z_{dl}=Z_{sl}-\frac{Z_{11}Z_t-Z_{22}Z_t}{Z_{21}-Z_t} \tag{29}$$

$$Z_{gl}=-Z_{sl}-\frac{Z_{21}Z_t+Z_{22}Z_t}{Z_{21}-Z_t}. \tag{30}$$

In other words, the Z-parameter can be obtained using the measured two-port S-parameter, and through this, the capacitances in the static state can be extracted using (28)–(30).

In this section, a method for extracting the device capacitances of a half-bridge MOSFET when the dc voltage is 0 V is proposed, and in the following section, a method for extracting the dynamic capacitance when the dc voltage is not 0 V is proposed using this method.

B. Dynamic Capacitances Extraction Method

When a dc voltage of n V rather than 0 V is applied, the MOSFET has the characteristic of nonlinearly decreasing capacitance as the voltage increases. A dc voltage was applied to the high-side MOSFET using the topology in Fig. 4. In this case, as mentioned in Section II, the dc voltage is only applied to the high side.

The proposed topology with or without dc bias voltage can be expressed as (13)–(21). However, when the dc voltage is not 0 V, the high-side and low-side impedances are different, so conditions (22)–(24) cannot be satisfied. Since no voltage is applied to the low-side, the low-side impedance can be obtained through (28)–(30), so these are the only known parameters now.

In other words, when measuring a two-port network in a dynamic state, there are a total of three unknowns: Z_{dh}, Z_{sh}, and Z_{gh}, and a simultaneous equation can be created by converting the measured S-parameters into Z-parameters. Equations (31)–(33) are the third-order simultaneous equations to find the high-side impedance under dynamic conditions

$$Z_{11\mathrm{n}}\mid_{V=n}=\frac{Z_{gh}Z_{gl}+\left(Z_{dl}+Z_{gl}\right)\left(Z_{dh}+Z_{gh}+\frac{Z_{gh}}{Z_t}\right)}{\left(Z_{dl}+Z_{gl}\right)\left(Z_{gh}+\frac{Z_{gh}+Z_{sh}}{Z_t}\right)+Z_{gl}\left(Z_{gh}+Z_{sh}\right)} \tag{31}$$

$$Z_{12\mathrm{n}}\mid_{V=n}=Z_{21}\mid_{V=0}=\frac{1}{\left(Z_{dl}+Z_{gl}\right)\left(Z_{gh}+\frac{Z_{gh}+Z_{sh}}{Z_t}\right)+Z_{gl}\left(Z_{gh}+Z_{sh}\right)} \tag{32}$$

$$Z_{22\mathrm{n}}\mid_{V=n}=\frac{\left(Z_{gh}+Z_{sh}\right)\left(Z_{gl}+Z_{sl}\right)+Z_{gl}\left(Z_{gh}+\frac{Z_{gh}+Z_{sh}}{Z_t}\right)}{\left(Z_{dl}+Z_{gl}\right)\left(Z_{gh}+\frac{Z_{gh}+Z_{sh}}{Z_t}\right)+Z_{gl}\left(Z_{gh}+Z_{sh}\right)}. \tag{33}$$

Using (31)–(33) and (28)–(30), the impedance of each terminal of the high-side MOSFET when n V is obtained is as follows:

$$Q=-Z_{21}^2+Z_{11}Z_{22}+Z_t\left(2Z_{21}+Z_{11}+Z_{22}\right) \tag{34}$$

$$W=-Z_{21}^2+Z_{11}Z_{22}-Z_{11}Z_{22_t}+Z_t\left(Z_{21}+Z_{22}-Z_{22_t}\right) \tag{35}$$

$$E=Z_t^2\,Z_{21_t}Z_{21}\left(2Z_{21}+Z_{11}+Z_{22}\right)-Z_tZ_{21_t}\left(Z_{21}^3-Z_{11}Z_{21}Z_{22}\right) \tag{36}$$

$$R=Z_{21}\,Z_tQ \tag{37}$$

$$T=Z_{11}\,Z_{22}Z_{11n}-Z_{11}Z_{11n}Z_{22n}+Z_t\left(Z_{21n}^2+Z_{21}Z_{11n}+Z_{22}Z_{11n}-Z_{11n}Z_{22n}\right) \tag{38}$$

$$Z_{dh}=\frac{Z_{11}Z_{21n}^2-Z_{21n}\left(\sqrt{Z_{21}Z_t\left(Q\right)}\right)-Z_{21}^2Z_{11n}+T}{W} \tag{39}$$

$$Z_{gh}=\frac{E}{\sqrt{R}W} \tag{40}$$

$$Z_{sh}=\frac{E+\sqrt{R}Z_t\left(-Z_{21}^2+Z_{11}Z_{22}-Z_{11}Z_{22n}-Z_{21}Z_{22n}\right)}{\sqrt{R}\left(Z_{21}^2-Z_{11}Z_{22}+Z_{11}Z_{22n}-Z_{21}Z_t-Z_{22}Z_t+Z_{22n}Z_t\right)}. \tag{41}$$

The capacitances under dynamic conditions can be obtained from (39)–(41). In conclusion, the proposed method can extract the device capacitance of a half-bridge MOSFET with one measurement per topology and one voltage case.

Unlike previously proposed methods, there is no need to change terminal wiring to measure a half-bridge MOSFET package forming module, and because the measurement steps are reduced, the time and cost of producing a test fixture are also reduced. Additionally, while existing research is based on two-port network methods for measuring half-bridge packages in static situations, it cannot measure dc bias characteristics. In a static state in previous studies, the reproducibility and stability of the measurement may decrease as the terminal wiring is changed and multiple test fixtures are used. Therefore, by using the proposed method, capacitances can be extracted simply and stably.

C. Summary

The proposed method is summarized, and the measurement sequence is organized. Fig. 6 shows the measurement flow chart using the proposed method. First, create a test fixture for measurement, as shown in Fig. 4, and then measure the two-port

$$Z_{sl}=-\frac{Z_{21}Z_t+Z_{22}Z_t-\sqrt{Z_{21}^2Z_t^2-2Z_t^2Z_{21}^2+Z_{11}Z_{22}Z_t^2+Z_{11}Z_t^3+Z_{22}Z_t^3}}{Z_{21}-Z_t} \tag{28}$$

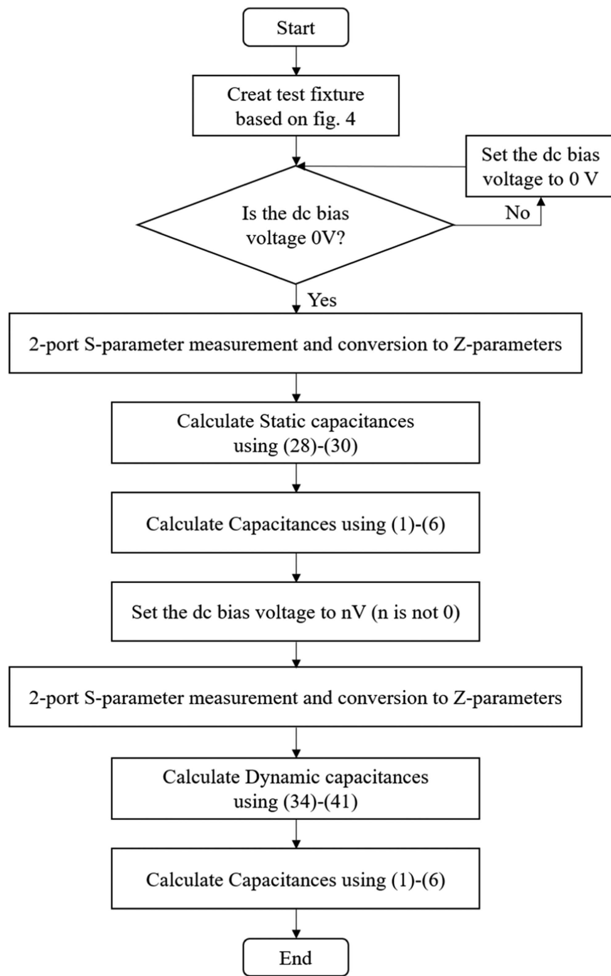


Fig. 6. Flow chart of the proposed method.

S-parameter when the dc voltage is 0 V. Find the Z parameter from the measured S-parameter, and use (28)–(30) to find the impedance in the static state. Afterward, the dc bias voltage is raised to n V to extract dynamic characteristics. Measure the two-port S-parameter with voltage applied and extract the impedance in the dynamic state using the converted Z parameter and (34)–(41). The capacitances of each state can be obtained through (1)–(6). In other words, using the proposed method, device capacitance can be extracted with one measurement per voltage condition.

The proposed method extracts capacitance based on the premise that the high-side and low-side impedances are identical under 0 V conditions, thereby avoiding any floating issues.

Initially, the capacitance is extracted under the 0 V condition by assuming equal impedance for both the high side and the low side. Subsequently, when a voltage is applied, the proposed topology is used where only the high side experiences the applied voltage. The previously extracted low-side impedance at 0 V is substituted into the model, and the impedance at each terminal of the high-side is measured under the applied voltage. This approach allows for the extraction of capacitance as a function of the applied voltage.

TABLE I
SIMULATION RESULT OF STATIC EXTRACTION

@1 MHz	C_{ds} [pF]	C_{dg} [pF]	C_{gs} [pF]
Datasheet [pF]	1850	274.9	1420
Simulation [pF]	1882.4	249.6	1397.6
Difference	1.75%	9.2 %	1.58%

IV. SIMULATION VERIFICATION

In this section, a test fixture is designed, and a 3-D EM simulation is performed to verify the proposed method. Based on the datasheet, the capacitances were imported into the 3-D model. Since the internal structure of the selected device is unknown, the test fixture alone was modeled to validate the effectiveness of the proposed method and fixture, with the device capacitances imported into the lumped port based on the datasheet. The two-port S-parameters were obtained through simulation, and the proposed method is applied using simulation results. The 3-D EM simulation tool is ANSYS HFSS, a well-known finite element solver.

A. Simulation Setup

The 3-D modeling was performed in the same form as the test fixture produced for the experiment, and the product verified in this article is an Infineon IAUC60N04S6N031H.

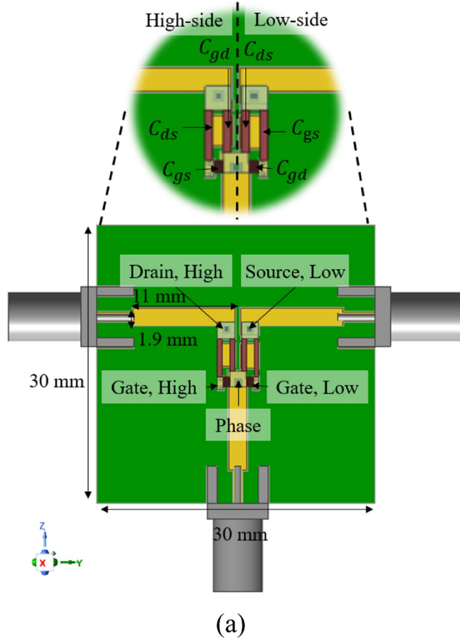
Fig. 7 shows the modeled simulation setup. An SMA connector was additionally modeled for a setup similar to the actual measurement environment. The test fixture was designed considering the package size and footprint of the target MOSFET, and the fixture size was modeled considering the measurement frequency. In general, the fixture size was selected to be sufficiently short compared to the wavelength according to the $\lambda/20$ rule of thumb, and it was designed to be 30 mm long, considering the maximum frequency of 30 MHz. The simulation was performed up to 30 MHz according to the measurement standards for conducted emissions in electronic devices [18].

As shown in Fig. 7(a) and (b), vias were used to ground the high-side and low-side gates.

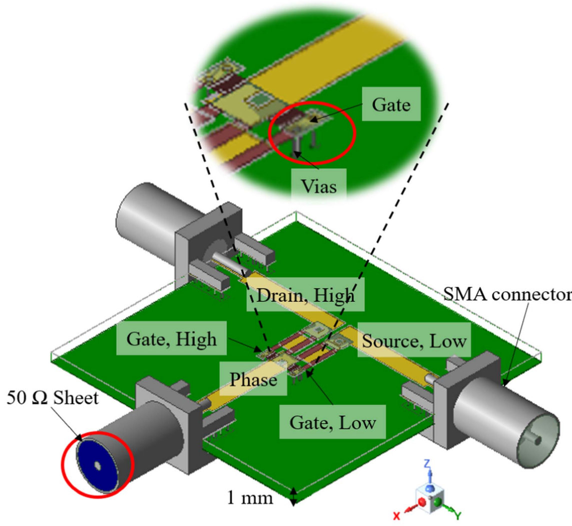
The measurability of the method was evaluated through 3-D simulations performed in a static situation with a dc voltage of 0 V. This simulation was conducted to determine the robustness of the test fixture when using the proposed method, so it was performed only for static conditions.

Referring to the datasheet, the capacitance between each terminal was set using the lumped *RLC* function of ANSYS HFSS, and the setup values are in Table I. As shown in Fig. 7, brown sheets were created between the yellow footprints, and the capacitances from the data sheet, as listed in Table I, were set. The impedances in Fig. 8 were then extracted from the S-parameters obtained from the connectors. Therefore, this simulation can be used to verify whether the fixture is suitable for the proposed method.

The lumped *RLC* boundary in HFSS is a modified impedance boundary. Unlike the impedance boundary, lumped *RLC* can be



(a)



(b)

Fig. 7. Three-dimensional EM Simulation setup of the proposed method. (a) Top view. (b) Perspective view.

used to specify a resistor, inductor, or capacitor value directly in an HFSS simulation [27].

In addition, to apply the proposed method, the phase terminal has to be connected to the ground through 50 Ω. During the experiment, a load calibration kit (Keysight, 85052D) was used to achieve the ideal 50-Ω condition, so to apply this, 50 Ω was connected using a lumped *RLC* boundary sheet between the signal pin and the ground of the SMA connector connected to the phase.

In Fig. 7, the connector is modeled with RF Korea end launch 1.0T dimension information, and the simulation frequency range is 300 kHz to 30 MHz.

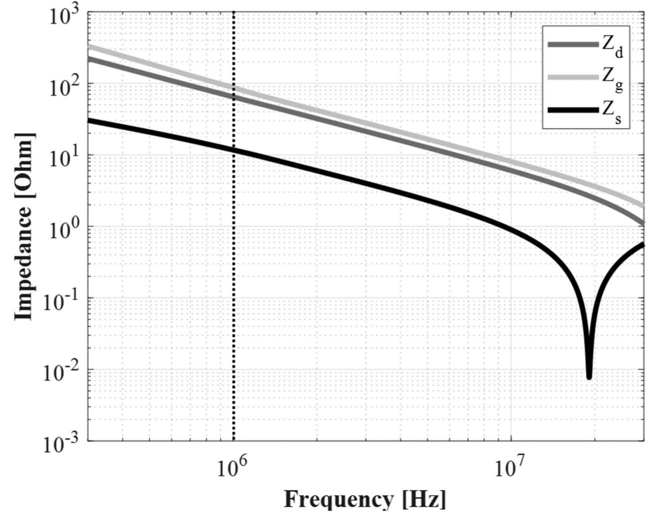


Fig. 8. Drain, gate, and source impedance simulation results of a half-bridge MOSFET.

B. Simulation Result

Two-port S-parameter results were obtained using ports connected to the high-side drain and low-side source, respectively. After converting the S-parameters to Z-parameters, the impedance of each terminal was calculated using (28)–(30). As mentioned in Section II, the simulations were performed under 0 V conditions, so the high-side and low-side impedances are the same.

The impedance calculated through the proposed method and the capacitances between each terminal are shown in Fig. 8 and Table I, respectively. Typically, manufacturers provide capacitance measured at 1 MHz, which is sufficiently capacitive and high frequency. The switching frequency of the power MOSFETs normally ranges from tens of kHz to hundreds of kHz, so 1 MHz is an appropriate frequency when considering the attenuation of noise generated during switching [15].

The capacitance of each terminal, obtained using the simulation results, was calculated using (4)–(6), as shown in Table I. C_{ds} and C_{gs} show a slight difference of less than 2%, but C_{dg} has a relatively significant difference of about 9%. This phenomenon occurs because C_{dg} has a relatively small capacitance, and there is usually an 8 to 10% difference [15], [16]. In addition, when the method is applied to a high-voltage half-bridge MOSFET with a relatively large capacitance, measurement sensitivity, and accuracy can be increased.

V. Experiment Verification

In this section, the proposed method was verified through experiments. Both static and dynamic properties were measured, and the results were compared with the datasheets. Using this method, the capacitances of the half-bridge MOSFET were extracted with one-step measurement per voltage condition in one case.

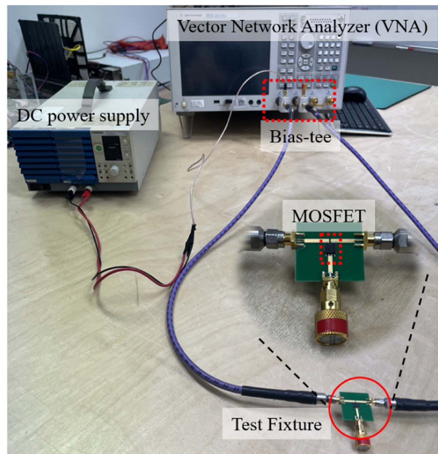


Fig. 9. Experimental setup for the proposed method.

TABLE II
EXPERIMENT RESULT OF THE PROPOSE METHOD

@1 MHz, 25 V	C_{iss} [pF]	C_{oss} [pF]	C_{rss} [pF]
Datasheet [pF]	1479	452	26
Measurement [pF]	1483.6	463.3	28.8
Difference	0.31%	2.5%	9.72%

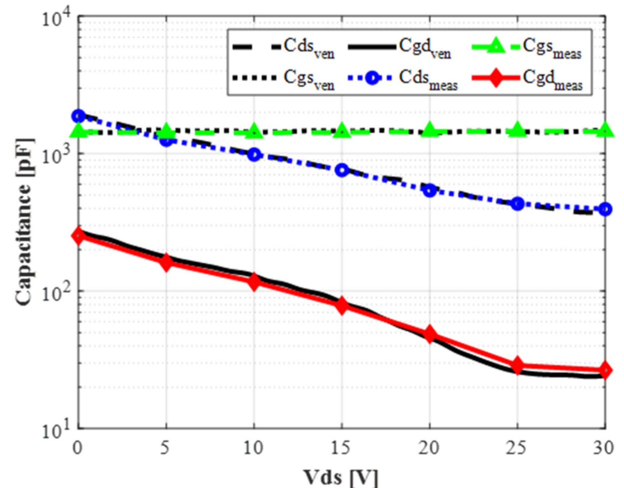
A. Experiment Setup

The experiment setup is shown in Fig. 9. To make the circuit shown in Fig. 4, a dc power supply, VNA (Keysight E5071C, 9 kHz-8.5 GHz), and bias-tees (Mini circuit ZFBT-6GW+, 0.1–6 GHz) were used. To short the port 2 side opposite to the dc voltage, a short calibration kit was connected to the dc terminal of the bias-tee, as shown in Fig. 4, and a load calibration kit was connected to the phase of the test fixture. To eliminate the influence of the bias-tee, calibration was performed after connecting the bias tee, and measurements were performed in 5 V steps from 300 kHz to 30 MHz.

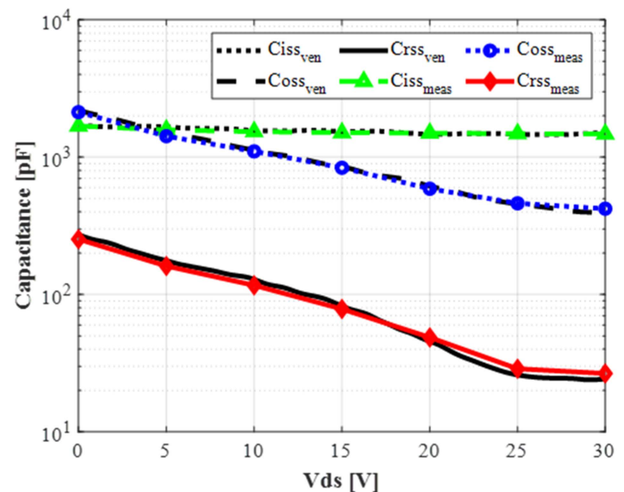
B. Experiment Result

The capacitance measured in 5 V steps from 0 V to 30 V using the proposed method is shown in Fig. 10. The maximum voltage between the drain and the source of the selected device is 40 V. The measured results were compared at 1 MHz, which is the datasheet standard, and show a difference of up to 9.7% at 25 V. This is because C_{rss} is a very small value to measure, tens of pF. For reference, data sheets are generally indicated as C_{iss}, C_{oss}, and C_{rss}, so the experimental results were compared. As shown in the experiment results, when the dc bias voltage of the MOSFET increases, the capacitance decreases due to the structure and channel characteristics of the MOSFET.

Therefore, knowing the capacitance depending on the operating conditions is important to determine the switching characteristics. Measured results were compared with the datasheet, and capacitance results were measured at 25 V using (7)–(9), as shown in Table II. The measurement results showed a difference of up to about 9.7% in C_{rss}, and the difference in results for C_{rss} with relatively small capacitance was large compared to the datasheet [15], [16].



(a)



(b)

Fig. 10. Drain, gate, and source capacitances experiment results of a half-bridge MOSFET. (a) C_{ds}, C_{gs}, and C_{gd}. (b) C_{iss}, C_{oss}, and C_{rss}.

The method proposed in this article was verified through experiments and compared with datasheets. In the next chapter, a switching EMI analysis using measurement results and circuit simulation is introduced.

VI. EMI ANALYSIS

In this section, to utilize the proposed method, a switching test is performed to analyze the correlation between the ringing phenomenon that occurs during switching due to capacitances. The ringing phenomenon is closely related to the device capacitances of the MOSFET, which demonstrates the importance of characterizing and extracting the device capacitances of the MOSFET. Therefore, this analysis was conducted to analyze EMI, a factor

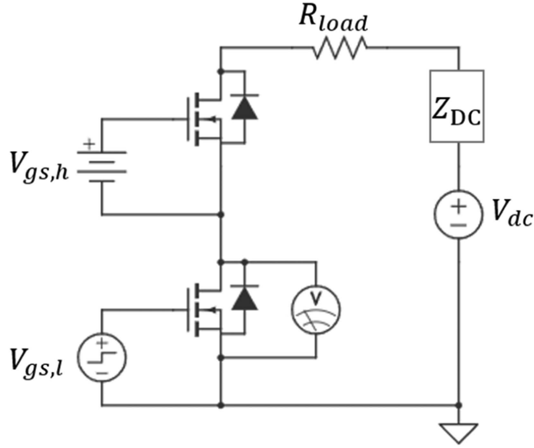


Fig. 11. Switching the test circuit for the EMI analysis.

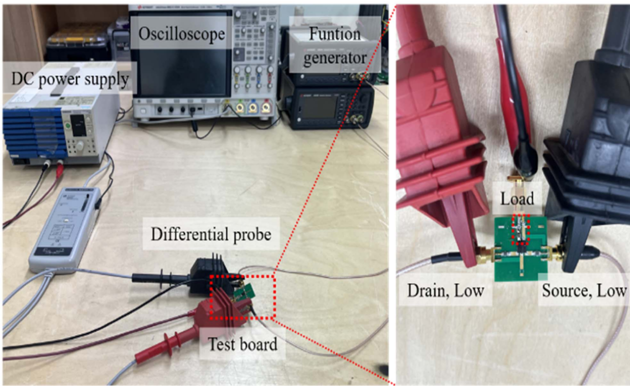


Fig. 12. Experiment setup for switching test.

to be considered when designing a power conversion system, and to confirm its correlation with capacitance extraction.

A. Switching Test Setup

As shown in Fig. 11, a circuit was designed to measure the switching characteristics of the power MOSFET. To prevent floating terminal issues, dc voltage is input to the gate and source of the high-side MOSFET, so the high-side MOSFET is continuously turned ON. Based on the circuit, the ringing phenomenon caused by loop inductance and device capacitance during switching was performed.

The test setup is shown in Fig. 12, and the measurement equipment used is shown in Table III. The test board in Fig. 12 was designed based on the circuit in Fig. 11, and the test conditions are shown in Table IV. For the load resistance and switching frequency, the switching frequency was assumed to be 20 kHz and the load resistance to be 20 Ω, referring to the inverter used for motor driving [28]. In reality, the motor is an inductive load. Still, in this research, resistance, which is relatively clear to analyze, was selected as the load condition to focus on ringing and EMI analysis.

TABLE III
MEASURING INSTRUMENTS

	Vendor	Model	Bandwidth
Dc power supply	KIKUSUI	PWR 800L	-
Oscilloscope	Keysight	MSO-X 4154A	1.5 GHz
Function generator	Keysight	33600 A	80 MHz
		33500 B	20 MHz
Differential probe	Keysight	N2691 A	70 MHz

TABLE IV
EXPERIMENT PARAMETERS OF SWITCHING TEST

	V_{dc}	$V_{gs,h}$	$V_{gs,l}$	R_{load}
Values	5 V	5 V (dc)	5 V, 20 kHz	20 Ω

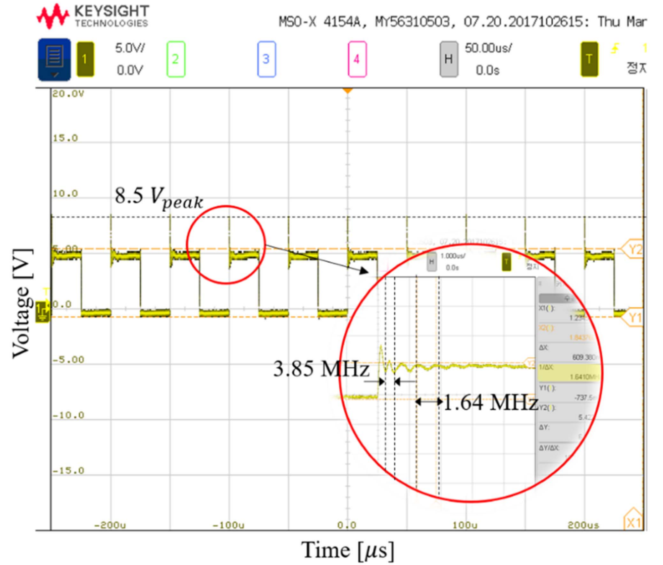


Fig. 13. Measurement result of low-side V_{ds}.

B. Test Result

During switching, the V_{ds} of the low-side MOSFET was measured to analyze the ringing phenomenon. Table IV shows the electrical parameter conditions used during measurement. At the moment of switch turn-ON/OFF, resonance occurs due to loop impedance and device capacitances between the drain and the source, and a ringing phenomenon with the corresponding resonance frequency occurs.

Fig. 13 shows the measured low-side V_{ds} results. The oscillation occurs when the switch turns OFF, ringing around 3.85 MHz and 1.64 MHz dominant.

To analyze the measurement results in Fig. 13, it is necessary to check the loop impedance of the switching circuit. Fig. 14 shows the switching circuit loop when turned OFF, and Z_{dc} is the equivalent impedance of the cable connected to the dc power

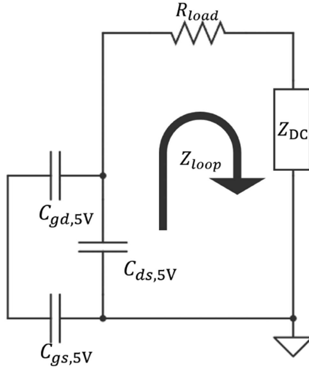


Fig. 14. Circuit loop when the MOSFET turns OFF.

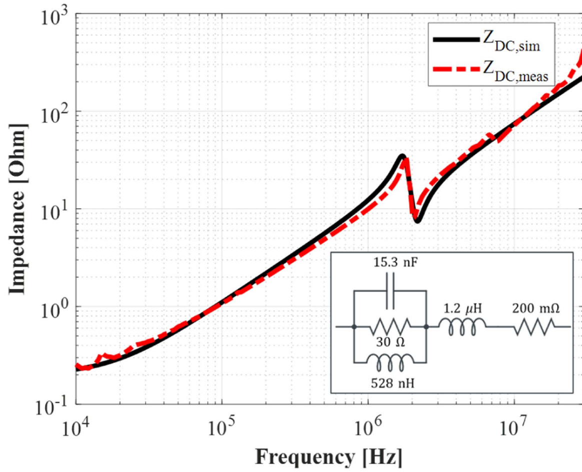


Fig. 15. Comparison of cable impedance measurement and equivalent circuit modeling result.

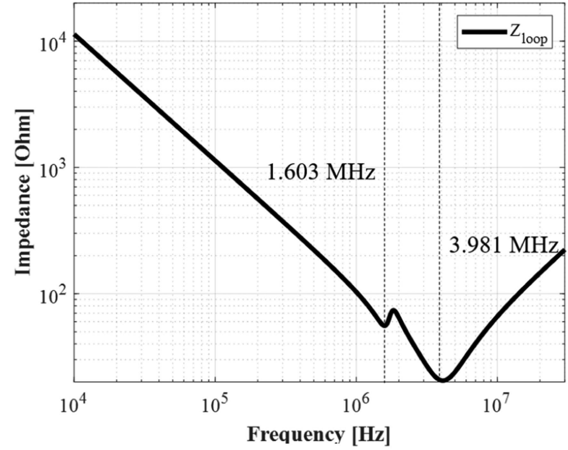


Fig. 16. Magnitude of the loop impedance of the circuit when the switch turns OFF.

supply used during the experiment. The device capacitances of the MOSFET constituting the circuit used the capacitances measurement result when the dc 5 V voltage was biased in Fig. 10. Z_{dc} was measured with the one-port method using a VNA, and the comparison of the measurement results and equivalent circuit modeling results is shown in Fig. 15. The loop impedance of the circuit in Fig. 14, including the impedance of the cable, is shown in Fig. 16 in the frequency domain, with resonance occurring at approximately 1.6 MHz and 4 MHz.

Through this, the ringing of approximately 4 MHz and 1.6 MHz occurs in the measurement results in Fig. 13, which confirms the correlation between switching noise and the device capacitances of the MOSFET. In other words, the device capacitances of the MOSFET change depending on the dc bias condition, and the loop impedance changes accordingly, thereby changing the ringing frequency.

Therefore, measuring the dynamic capacitance of the MOSFET as performed in this research is very essential.

C. Modeling and Analysis

SPICE modeling of the MOSFET was performed to model the measured phenomenon using circuit simulation and analyze EMI. A SPICE model, including capacitances change depending on the voltage, was designed based on the channel characteristics, and dynamic capacitances were measured in the SPICE model provided by Infineon. The capacitance change depending on the voltage was modeled as a diode [29]. Afterward, the circuit in Fig. 11 was modeled, and time domain circuit simulation was performed using Keysight Advanced Design System (ADS).

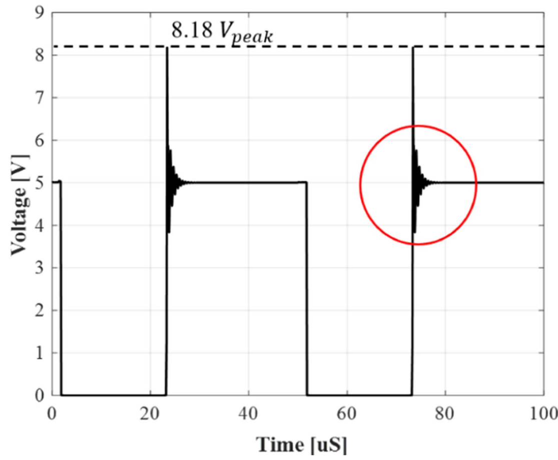
The simulations were conducted using two different cases: one with a modeled SPICE model based on the measured capacitances and the other with a vendor SPICE model. Figs. 17 and 18 show the simulation results using the modeled SPICE model and the vendor SPICE model, respectively.

The simulation results of the V_{ds} are shown in Fig. 17. When the ringing frequencies that appear were calculated from the time domain data, approximately 3.85 MHz and 1.67 MHz were dominant. Additionally, the voltage spike level that occurs due to the charging and discharging of the capacitor is also 8.18 V, which is about 3.9% different from the measurement result.

When using the vendor SPICE model, as shown in Fig. 18(a), the maximum voltage reached approximately 9.5 V, which is about 10% different from the measured results. The ringing frequencies are dominated by components at 3.45 MHz and 1.7 MHz, showing slight differences compared to the modeled SPICE model based on the measured capacitances.

To analyze the correlation between the time domain measurement results and EMI, a fast Fourier transform (FFT) was performed using V_{ds} data from circuit simulation and experiment. Fig. 19 shows the results of the FFT of V_{ds} using measurement data and simulation results. For the EMI analysis, FFT was calculated from 10 kHz to 30 MHz. As a result of the FFT, the harmonics are large at the ringing frequency that appears to be dominant in the time domain, which ultimately becomes a factor in increasing the switching noise at the ringing frequency.

To compare the consistency between measurement and simulation results, the peak envelope of the FFT results was extracted, as shown in Fig. 20, and feature selective validation (FSV) was performed with 2000 data. This method is adopted in the IEEE 1597.1 standard and is a method to quantitatively evaluate the similarity between two data sets [30]. This is divided into



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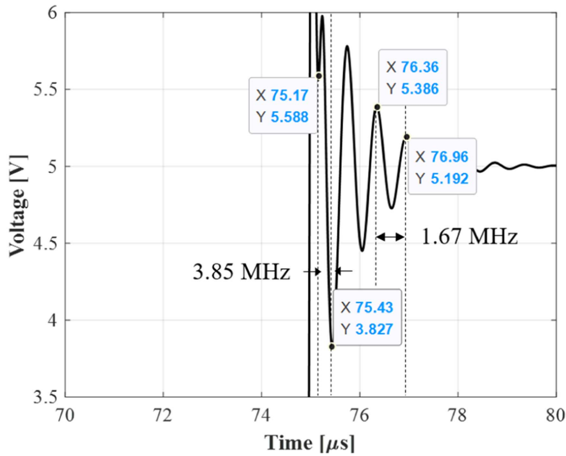
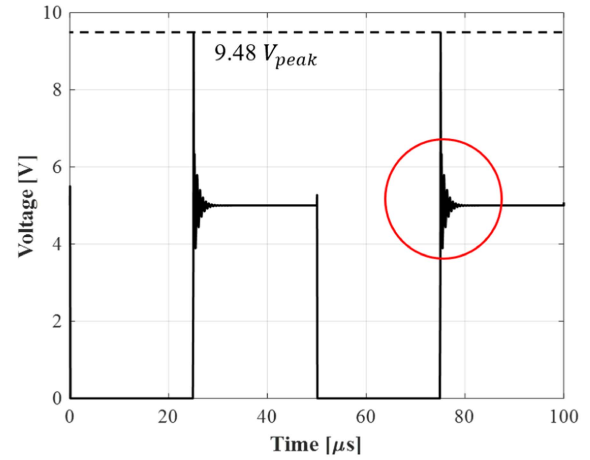
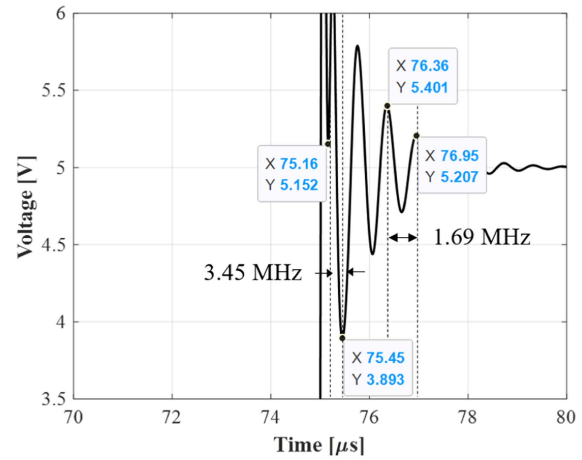


(b)

Fig. 17. Switching circuit simulation results using modeled SPICE model. (a) Low side V_{ds}. (b) Ringing frequencies.



(a)



(b)

Fig. 18. Switching circuit simulation results using vendor SPICE model (a) Low side V_{ds}. (b) Ringing frequencies.

amplitude difference measure (ADM), which compares trends between data sets, and feature difference measure (FDM), which compares differences in shapes or patterns between data sets. Also, the global difference measure (GDM) is a method for evaluating the comprehensive characteristics of ADM and FDM.

This method has the advantage of being able to quantitatively compare data that has commonly been qualitatively evaluated in the EMC field and better reflects the visual and structural characteristics of the data than traditional statistical indicators such as relative error or mean square error. It allows for a more intuitive interpretation of results [31].

In the peak envelope results shown in Fig. 20, the vendor SPICE model and the measurement-based SPICE model demonstrated a high degree of agreement. Therefore, the FSV results were compared only between the measurement results and the simulation results using the measurement-based SPICE model. Table V shows the results of evaluating simulation and measurement-based FFT data using the FSV technique using

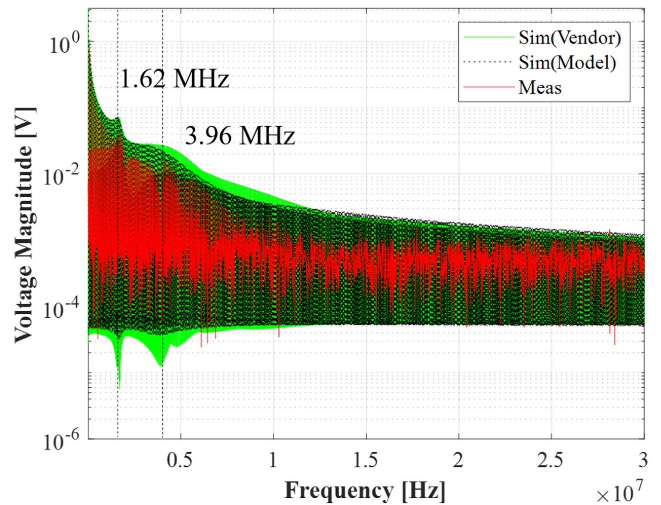


Fig. 19. Comparison of experimental and simulated FFT results for low-side V_{ds} magnitude.

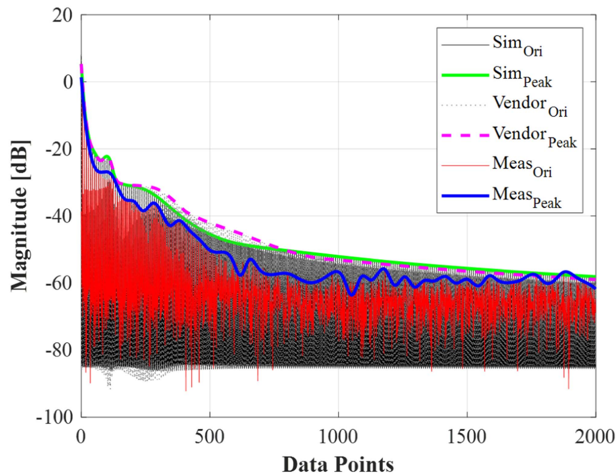


Fig. 20. Peak envelope results of low-side V_{ds} for FSV.

TABLE V
FSV RESULTS OF SIMULATION AND MEASUREMENT

	Average value	Interpretation
ADM	0.183	Very good
FDM	0.239	Good
GDM	0.335	Good

a web-based FSV tool, and it can be confirmed that results above "Good" were obtained [32], [33]. Generally, consistency is considered excellent in the EMC field when it exceeds "Fair" [30]. Thus, EMI performance can be predicted or analyzed by modeling MOSFETs through device capacitance extraction.

VII. DISCUSSION

The discussion section of this article highlights several key limitations and considerations for future research.

First, a limitation of the proposed method is its application in high-voltage environments. While the method effectively extracts capacitance at low voltages, its performance under high-voltage conditions remains unverified. High-voltage scenarios introduce additional challenges, such as insulation breakdown risks, which could compromise measurement accuracy and reliability. Previous research has demonstrated the measurement of inductor impedance up to 500 V and 30 A using bias tees and VNA [34]. However, as recent research increasingly focuses on power modules exceeding 10 kV, validating measurements under high-voltage conditions remains critical. Therefore, future work should focus on adapting the method for high-voltage applications and thoroughly validating its effectiveness in these conditions.

Second, this research primarily concentrates on extracting the capacitance values (C_{gs}, C_{dg}, C_{ds}) of the MOSFETs, without addressing the role of inductance. Stray inductance in power modules plays a critical role in power electronics, particularly in high-frequency ringing, where it significantly impacts circuit performance. In this research, a very small module with a rated voltage of 40 V and an approximate size of 5 mm was used, making the inductance of the device less significant compared to the inductance of the cables and dc power supply used in the measurement setup. However, in high-voltage power modules, the presence of larger bus bars and other structures can increase parasitic inductance, altering the ringing behavior [35], [36]. The proposed method allows for the theoretical extraction of inductance based on the resonant frequency identified from the impedance curve and the extracted capacitance. However, due to the small size of the selected device, the influence of the test fixture must be removed using a de-embedding process [37]. Thus, future research should explore methodologies for simultaneously extracting both capacitance and inductance from high-voltage power modules to provide a more holistic characterization of the device.

Finally, the EMI analysis conducted in this research is based on a device-focused analysis rather than a standard EMC test. In practical EMC testing, the EMI characteristics can vary greatly depending on the cable structure, system configuration, and load conditions. This study focused on modeling the switching device and conducting simple tests, which are one of the key factors influencing EMI characteristics. Previous studies have performed analyses of resonant frequency through simple switching circuits, such as double pulse tests, after extracting and modeling device characteristics [35], [36]. While the simple switching tests conducted in this research provide valuable insights into EMI analysis, it is challenging to fully understand how these measurements lead to system-level EMC performance without incorporating standard EMI tests. Future studies should include standard EMI tests to validate the effectiveness of the method and ensure compliance with industry standards.

These discussions underscore the need for further research and refinement of the proposed method to enhance its robustness and applicability across a broader range of scenarios in the field of power electronics.

VIII. CONCLUSION

In this article, research was conducted to extract the device capacitances of a SiC power MOSFET in a half-bridge package for switching EMI analysis. The device capacitances of a MOSFET change depending on dc bias voltage conditions, and therefore the EMI generated under operating conditions may vary due to changes in loop impedance. Therefore, extracting the dynamic capacitances of the MOSFET is essential for designing a stable power conversion system. With miniaturization and integration, half-bridge MOSFETs in the package are being developed. Therefore, the existing single MOSFET dynamic capacitances measurement method has limitations in that it requires multiple measurement steps and test fixtures and may cause floating issues. Therefore, this article proposed a method to extract the dynamic capacitances of a half-bridge MOSFET with one measurement per voltage condition. This method is based on the two-port network theory and has the advantage of extracting with only one test fixture and setup.

The proposed method was verified through 3-D EM simulation and measurement, and the measurement results showed a difference of up to about 9.7% from the datasheet. Additionally, to analyze the correlation with EMI, the voltage obtained through the switching test was analyzed in the frequency domain. Ringing occurs during switching depending on the loop impedance caused by device capacitances, and this was analyzed through experiment and simulation. To perform the circuit simulation, SPICE modeling of the MOSFET was performed using measurement data, and the correlation between measurement and simulation was confirmed using the FSV, which has been adopted in the EMC field as a standard to compare the results of simulation and measurement.

Using the proposed method, the dynamic capacitances of a half-bridge MOSFET can be extracted in one step, and the EMI, such as the ringing noise that occurs during switching, can be analyzed and modeled. Switching noise is an essential element that has to be evaluated when designing a power conversion system, and it is expected that the proposed method will help us design a system that is robust against noise generation in the future.

Acknowledgment

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