Modulation-Independent Initial Current Control of DAB-Based Single-Stage AC–DC Converter for DC Bias Elimination

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***Abstract*—In the dual active bridge-based single-stage (DAB-1S) ac–dc converter, the varying input power causes a variation in the phase shift ratios, resulting in varying initial current and the generation of dc-bias current (DCBC). The DCBC will aggravate current stress and increase conduction loss, etc. This article introduces an initial current control method of DAB-1S ac–dc converter to eliminate the DCBC. The introduction of control degrees of freedom that are independent of power control enables the initial current of each switching cycle to be controlled to zero in any modulation mode. In this manner, the currents of neighboring switching cycles are decoupled, thereby eliminating the DCBC. Moreover, the impact of nonideal parameters in practical DAB 1S ac–dc converters is analyzed, and corresponding compensation methods are proposed. Meanwhile, mathematical analysis of the switching cycles and grid cycles indicates that this method only changes the initial phase angle of the voltage and current for each switching cycle, leaving the harmonic content of the port current unchanged and the total harmonic distortion of the grid current unaffected. The experimental prototype has confirmed the effectiveness of the dc bias elimination method. Comparative experimentation with various other existing modulation methods highlights the superiority of this method.**

***Index Terms*—DABs, dc bias, phase shift modulation, signal-stage ac–dc converter.**

I. Introduction

With the rapid global popularity of electric vehicles and the widespread grid connection of energy storage systems and new energy power generation systems, isolated ac–dc converters, as crucial power interfaces, are attracting increasing research attention [1], [2], [3]. Currently, there are two main types of structures for isolated ac–dc conversion [4]: two-stage structures [5], which comprise a nonisolated ac–dc converter and an isolated dc–dc converter; and single-stage structures [6], which only consist of an isolated ac–dc converter. Among them, the dual active bridge-based single-stage (DAB-1S) ac–dc converters are a promising option for grid-connected energy storage systems due to their advantages [7], [8], [9], including buck-boost conversion, high efficiency, and high power density.

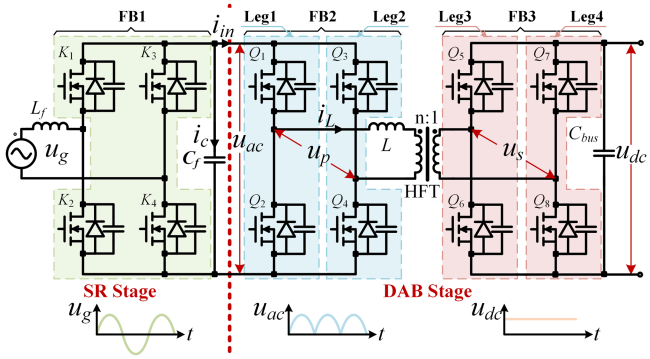

Fig. 1. DAB-1S AC–DC converter circuit.

Fig. 1 illustrates the topology of the DAB-1S ac–dc converter, which consists of a synchronous rectifier (SR) stage and a DAB stage. Similar to the DAB dc–dc converter, the fundamental principle of this converter is to adjust the phase shift, known as "D_f," between the primary- and secondary-side active bridge square wave voltages, "u_p" and "u_s," to achieve the free regulation of power transferred amplitude and direction [10]. To improve the performance of the converter, each active bridge incorporates an internal phase shift ratio, "D_p" and "D_s," respectively. Additionally, the transferred power can also be regulated by adjusting the switching frequency "f_s." These four degrees of freedom enable simultaneous control of the transmitted power and current characteristic, enhancing the efficiency and reliability of the converter [6], [8], [10], [11], [12].

The abovementioned modulation methods can generate an expected output waveform. However, they lack attention to the inductor current, and all of them default to the inductor current waveform being directly determined by the phase shift ratios, ignoring the effect of the initial current. In fact, this condition is only met when the transferred power of the DAB stage is constant, resulting in an inductor current with an average value of zero during one switching cycle. This is contrary to the operating characteristics of the ac–dc converter. The transferred

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power is equal to the input/output power of the ac port, both of which vary with time [13]. To change the transferred power, it is necessary to adjust the voltage across the series inductor and the current flowing through it. On the assumption that the inductor current is symmetric and unbiased, a definite initial current can be obtained, which is the desired value. However, the principle that the inductor current cannot change suddenly means that the actual initial current for a subsequent switching cycle is determined by the final current of the previous switching cycle. When the actual value differs from the desired value, the inductor current will have a nonzero average value, which will be referred to as the transient dc-bias current (DCBC) [13], [14], [15], [16]. The DCBC is directly related to the increase in transferred power, and its transient value can be significant. At worst, the transient inrush current can be several times the steady state current, subjecting the power device to greater current stress and leading to flux saturation of magnetic components. These issues will affect the safe operation of the converters [17]. Thus, this article focuses on the elimination of DCBC in DAB-1S ac–dc converter.

There are three categories of methods to eliminate DCBC in DAB converters: hardware-based, closed-loop control, and phase shift optimization. The most common hardware-based method is to connect the dc-blocking capacitor in series with the inductor. However, the use of a dc-blocking capacitor may lead to low-frequency oscillations in response to variations in transferred power [18]. Moreover, in high-power applications, a large number of capacitors are connected in parallel to handle high currents. This practice results in increased costs and reduced power density. To address these issues, a closed-loop control method has been proposed to enhance power density and eliminate DCBC simultaneously [19], [20]. The method regulates an average voltage with the opposite polarity of the bias current is applied to the series inductor to cancel it out. It can be achieved by precisely measuring the flux or current, which has minimal effect on power density. However, meeting this requirement necessitates high levels of current or flux sampling and monitoring, resulting in increased in system cost and complexity [21].

These methods can effectively eliminate DCBC, but they are passive elimination methods without considering the generation mechanism of DCBC. To achieve faster elimination of DCBC, phase shift optimization methods have been proposed. These methods originated from the DCBC model of DAB converters with phase shift modulation [18]. Optimizing the gate signals can eliminate the DCBC. These methods can be classified into four groups based on different optimization strategies.

1) *Peak current control:* The voltage across the inductor is adjusted when the transient current reaches the allowable current limit to reverse the slope of the current [22]. This method ensures that the current stress of the power device can be controlled without affecting dynamic performance of the converter. However, sensors are required to sample the current, and the DCBC still needs to be eliminated through the parasitic resistance, which typically requires several switching cycles.
2) *Piecewise linearly current control (PCC):* In [20], [22], and [23], the authors propose using PCC to eliminate DCBC. The method is accomplished by combining the phase shift ratios of the previous switching cycle and readjusting the phase shift ratios of the positive half-switching cycle in subsequent cycle. The DCBC can be eliminated within half-switching cycle. However, this method is only applicable in single phase shift (SPS) modulation. In order to improve the efficiency of the converter, multiple phase shift modulations are generally required. Thus, the authors in [24], [25], and [26] propose PCC applied to extended phase shift (EPS) modulation, double phase shift (DPS) modulation, and triple phase shift (TPS) modulation, respectively. However, these methods are not generalizable to each other. In [27], the authors propose a general analysis method that optimizes the phase shift ratio for each half-bridge instead of the full bridge. All of these methods eliminate the DCBC in half-switching cycle. However, altering the gate signal leads to fluctuations in the port current, causing the actual power to deviate from the target power.
3) *Linear current control:* Hou et al. [28] and Bu et al. [29] proposed a method to eliminate DCBC by adjusting the switching cycle length to compensate for the initial current difference between adjacent switching cycles. This method converts the segmented compensation current in PCC to linear compensation current, leading to a more streamlined and transparent calculation process. However, this approach still results in a bias in the actual power.
4) *Initial current control (ICC):* The DCBC is the result of coupling adjacent switching cycle currents. It can be naturally eliminated by decoupling the inductor current of adjacent cycles [31]. Current decoupling is achieved by ensuring that the initial currents of each switching cycle are equal. This approach optimizes current using only information from the current switching cycle, without considering phase shift ratios of the previous cycle. Moreover, this method does not suffer from power transfer error because there is no need to optimize the current by modifying the phase shift ratios obtained by solving the power equation. However, to achieve initial current control, the power equation is solved with the addition of initial current constraints. As there are two control objectives, two of the four control degrees of freedom (f_s, D_p, D_s, and D_f) must be used simultaneously to obtain a closed solution to the system of equations [30], [32]. This limitation prevents the application of existing control methods in constant frequency SPS modulation, which limits the maximum transferred power of DAB stage and output power of the converter. In [33], the concept of shifting switching pattern to realize zero initial current in each switching cycle is proposed. A natural transition between different modulation modes is achieved by optimizing the phase shift ratio offline and constructing a lookup table. This eliminates DCBC over the entire power range without affecting power transfer. In order to extend the applicability of this approach, in a subsequent work [34],

an online approach for determining the zero crossing point (ZCP) was introduced, along with an analysis of various commonly employed phase shift modulations. Although the literature [33] and [34] primarily focus on the analysis of SPS, the analysis of TPS is insufficient and does not provide a theoretical analysis of the impact of nonideal factors, such as line resistance and port voltage ripple, on the accuracy of the calculation of the ZCP. Nevertheless, the method offers a novel approach to addressing the DCBC issue of the DAB 1P1S ac–dc converter.

In order to resolve the reliability issue of the converter resulting from the current spike during the transient process, while simultaneously ensuring that the dc bias elimination method does not impact the steady-state operation of the converter, this article introduces a modulation-independent initial current control (MIICC) method. In light of the distinctive operational characteristics of the DAB 1P1S ac–dc converter, an in-depth analysis of the dead time, line resistance in the high-frequency loop, and port voltage ripple has led to the identification of the influence of these nonideal parameters on the ZCP of inductor current. Consequently, a method for compensating for nonideal parameters has been proposed in order to enhance the accuracy of the aforementioned method. Furthermore, the impact of the MIICC on the grid current harmonic content and converter efficiency is mathematically analyzed and experimentally compared. The results demonstrate that the MIICC method has a negligible effect on the converter's steady-state operation.

The rest of this article is organized as follows. First, the operational characteristics of the DAB topology applied to an ac–dc converter are analyzed in Section II, with an explanation of the reasons contributing to the generation of DCBC. In Section III, this article analyzes and presents MIICC to eliminate DCBC, along with the calculation of key variable under different modulation modes. In Section IV, an in-depth analysis is conducted on the impact of different nonideal factors present in DAB-based ac–dc converters on the utilization of the MIICC method, along with the provision of an error compensation technique. Furthermore, in Section V, the impact of MIICC on the port ripple characteristics is analyzed. In Sections VI and VII, the effectiveness of MIICC is verified through experiments and simulations. Finally, Section VIII concludes this article.

II. Principle of DAB-1S AC–DC Converter and DC Bias

A. Steady State Operation Analysis

Fig. 1 depicts the schematic circuit of a DAB-1S ac–dc converter. The SR stage consists of the full bridge FB1 and the *LC* low-pass filter, which is composed of L_f and C_f. The grid voltage is represented by u_g, and the grid current is represented by i_{ac}. u_{ac} is the voltage at both ends of C_f and serves as the input voltage of the DAB stage, which varies with u_g. The DAB stage consists of four half-bridges, namely Leg1 to Leg4, and a high-frequency transformer (HFT). L represents the series inductor, which includes the leakage inductance of HFT and the external auxiliary inductor. Consider the example of power flow from the ac side to the dc side under unity power factor and boost conditions. Assuming the converter loss and the influence of C_f

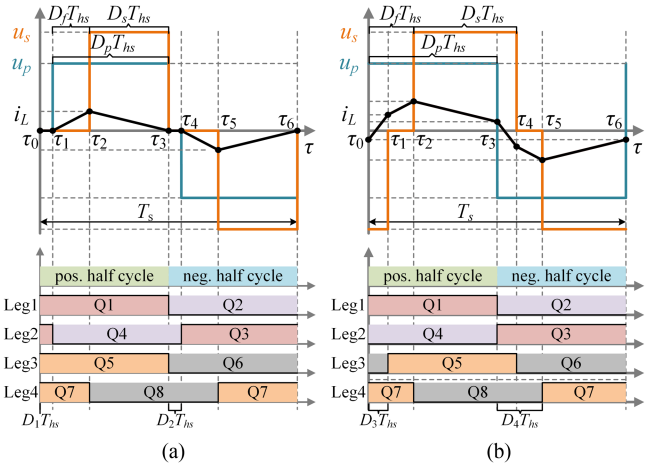

Fig. 2. Key operation waveforms of the optimal current stress modulation in the boost condition. (a) TDCM. (b) TCCM.

are disregarded, the input power can be expressed as follows:

$$P_{ac} = u_g \cdot i_{ac} = P_{dc} - P_{dc} \cos 2\omega_g t \tag{1}$$

where ω_g is the angle frequency of u_g and P_{dc} denotes the average output power. In steady state, P_{dc} remains constant. However, as stated in (1), P_{ac} remains time-varying under this condition. This phenomenon is exclusive to the application of the DAB topology in single-stage ac–dc converter. When the converter operates in rectifier mode, P_{dc} is greater than zero. Conversely, in inverter mode, P_{dc} is less than zero. The transferred power of the DAB stage is equal to the input power of the ac port. Therefore, in the following analysis, we will use "P_{ac}" to refer to the transferred power of the DAB stage.

B. Phase-Shift Modulation Method and DC-Bias Current

As stated in Section I, there has been extensive research on phase shift modulation methods for DAB-based converter. For instance, the optimal phase shift (OPS) modulation shown in Fig. 2, achieves the global minimum reactive power and minimum current stress [35]. Fig. 2 shows the modal diagram of the OPS modulation, which comprises two operating modes based on the continuity of the inductor current: triangular discontinuous conduction mode (TDCM) and trapezoidal continuous conduction mode (TCCM), as depicted in Fig. 2(a) and (b), respectively. Where T_s represents the switching cycle of the converter, and $T_{hs} = T_s/2$ denotes half-switching cycle. Depending on the operating state, this method exists in SPS, EPS, and TPS modulation modes. Therefore, this method is selected to verify the effectiveness of the proposed dc bias elimination method in Section III. Q1–Q8 are the gate signals for eight MOSFETs. The duty ratios of all gate signals are set to 0.5. D_1 and D_3 represent the phase shift ratios between the rising edge of Q1 and Q5 and the positive half-switching cycle, respectively. Similarly, D_2 and D_4 represent the phase shift ratios between the rising edge of Q3 and Q7 and the negative half-switching cycle, respectively. They are all labeled in Fig. 2. The relationship among several phase shift ratios can be expressed as (2).

The power depends only on the phase difference between D_1, D_2, D_3, and D_4, regardless of their specific values. Therefore, in Fig. 2, D_1 is set to zero, meaning that the phase shift between Q1 and the positive half-switching cycle is constant at zero, while the phase of Q3–Q8 is adjusted to generate the voltage waveform of the OPS modulation [28].

$$\begin{cases} D_p = 1 - D_2 + D_1 \\ D_s = 1 - D_4 + D_3 \\ D_f = D_4 - D_2 \\ D_1 = 0 \end{cases}. \tag{2}$$

Since the switching frequency f_s is much higher than the grid frequency, the dc-side voltages of the active bridges FB2 and FB3 are considered constant throughout a switching cycle. The amplitudes of u_p and u_s can be expressed in terms of the instantaneous values of u_{ac} and nu_{dc}, respectively, for each switching cycle. In TCCM, inductor current i_L can be defined as (3) during the positive half-switching cycle. Then, based on the symmetry of the inductor current, i_L at each switching action moment in the nth switching cycle can be derived as (4). According to Fig. 2 and (3) as well as (4), P_{ac} for a single switching cycle can be calculated as (5).

$$i_L = \begin{cases} i_L(\tau_0) + \frac{u_{ac}+nu_{dc}}{L}\tau, \tau \in [\tau_0, \tau_1) = (D_s + D_f - D_p)T_{hs} \\ i_L(\tau_1) + \frac{u_{ac}}{L}(\tau - \tau_1), \tau \in [\tau_1, \tau_2) = (D_p - D_s)T_{hs} \\ i_L(\tau_2) + \frac{u_{ac}-nu_{dc}}{L}(\tau - \tau_2), \tau \in [\tau_2, \tau_3] = (D_p - D_f)T_{hs} \end{cases} \tag{3}$$

$$\begin{cases} \langle i_L(\tau_0)\rangle_{T_{sn}} = -\langle i_L(\tau_3)\rangle_{T_{sn}} = \frac{nu_{dc}(2-D_s-2D_f)-u_{ac}}{4f_sL} \\ \langle i_L(\tau_1)\rangle_{T_{sn}} = \frac{u_{ac}(2D_s+2D_f-3)+nu_{dc}D_s}{4f_sL} \\ \langle i_L(\tau_2)\rangle_{T_{sn}} = \frac{u_{ac}(2D_f-1)+nu_{dc}D_s}{4f_sL} \end{cases} \tag{4}$$

$$\begin{aligned} P_{ac} &= \frac{1}{T_s}\int_0^{T_s} u_p i_L d\tau \\ &= \left[\left(D_s(3 - 2D_f - D_s) - 2(D_f - 1)^2\right) nu_{ac}u_{dc}\right] \Big/ 4f_sL \end{aligned} \tag{5}$$

$$\begin{cases} P_n = P_{ac}/P_b \\ P_b = du_{ac}^2/2f_sL \end{cases} \tag{6}$$

$$i_L(\tau_0) = \begin{cases} 0, & P_n \in \left[0, \frac{d-1}{2d^2}\right) \\ \frac{u_{ac}}{4f_sL}\left(d\sqrt{\frac{1-4P_n}{d^2-2d+2}} - 1\right), & P_n \in \left[\frac{d-1}{2d^2}, \frac{1}{4}\right] \end{cases} \tag{7}$$

$$\begin{aligned} &\langle i_L(\tau_0)\rangle_{T_{sn},\text{desired}} \neq \langle i_L(\tau_0)\rangle_{T_{sn},\text{actual}} = \langle i_L(\tau_6)\rangle_{T_{s(n-1)},\text{actual}} \\ &= \langle i_L(\tau_0)\rangle_{T_{s(n-1)},\text{actual}}. \end{aligned} \tag{8}$$

As per [35], the optimal phase shift ratios can be determined by solving (5) using objective functions, such as minimizing current stress and backflow power. To simplify the expression of phase shift ratio, input power is normalized as (6). Table I presents the optimal phase shift ratios in TCCM. In a similar manner, the optimal phase shift ratios in TDCM can be calculated, and are also shown in Table I. Where $d = nu_{dc}/u_{ac}$ denotes the voltage conversion ratio.

TABLE I
OPTIMAL PHASE-SHIFT RATIOS IN BOOST CONDITION ($d > 1$) [35]

Mode	Power range	Optimal control parameters
Rectifier	$P_n \in \left[0, \frac{d-1}{2d^2}\right]$	$\begin{cases} D_s = \sqrt{2P_n/(d-1)} \\ D_p = dD_s, D_f = (d-1)D_s \end{cases}$
	$P_n \in \left(\frac{d-1}{2d^2}, \frac{1}{4}\right]$	$\begin{cases} D_s = 1-(d-1)\sqrt{\frac{1-4P_n}{d^2-2d+2}} \\ D_p = 1, D_f = \frac{(2-d)D_s + 2d - 3}{2(d-1)} \end{cases}$
Inverter	$P_n \in \left[\frac{1-d}{2d^2}, 0\right]$	$\begin{cases} D_s = \sqrt{2P_n/(1-d)} \\ D_p = dD_s, D_f = 0 \end{cases}$
	$P_n \in \left[-\frac{1}{4}, \frac{1-d}{2d^2}\right)$	$\begin{cases} D_s = 1-(d-1)\sqrt{\frac{1+4P_n}{d^2-2d+2}} \\ D_p = 1, D_f = (1-dD_s)/(2d-2) \end{cases}$

By substituting the phase shift ratio expressions from Table I into (4), the initial current can be calculated as shown in (7). This is the desired initial current value. However, the actual initial inductor current is determined by the final current of the leading switching cycle. This coupling relationship can be expressed by (8).

Fig. 3 shows four successive cycles with a stepwise increase in transferred power. The red dotted line is calculated on the basis of the phase shift ratios under the assumption that the currents are symmetric. The solid black line represents the actual current waveform, taking into account the coupling relation of (8). The first two switching cycles are in TDCM. The initial current is equal to zero and no DCBC is generated. The third switching cycle operates in TCCM, and the initial current satisfies (8), resulting in the generation of DCBC, which is recorded as Δi_1. In the fourth switching cycle, the DCBC is labeled as Δi_3. Additionally, the difference between the desired initial current of the third switching cycle and that of the fourth switching cycle is recorded as Δi_2. These three values satisfy

$$\Delta i_3 = \Delta i_1 + \Delta i_2. \tag{9}$$

This indicates that the difference in initial current between adjacent switching cycles is the increment in bias current for the current switching cycle. The DCBC of different cycles can be superimposed. In effect, the amplitude of DCBC may decrease due to the parasitic resistance in high-frequency loop. However, in TCCM, DCBC cannot be completely eliminated by the parasitic resistors due to the initial current difference present in each switching cycle. Especially when a power-step change occurs, a significant initial current difference can result in current spikes. Therefore, an effective DCBC elimination method is necessary.

III. MIICC FOR DC-BIAS CURRENT ELIMINATION

To eliminate the DCBC caused by the change in input power, we propose MIICC to control initial current. This section presents the detailed mechanism and parameter calculation method.

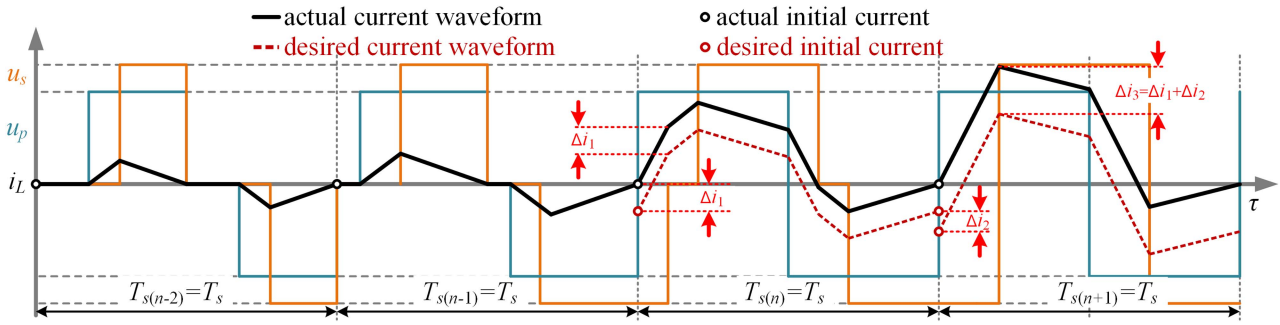

Fig. 3. Typical operation waveform in TCCM.

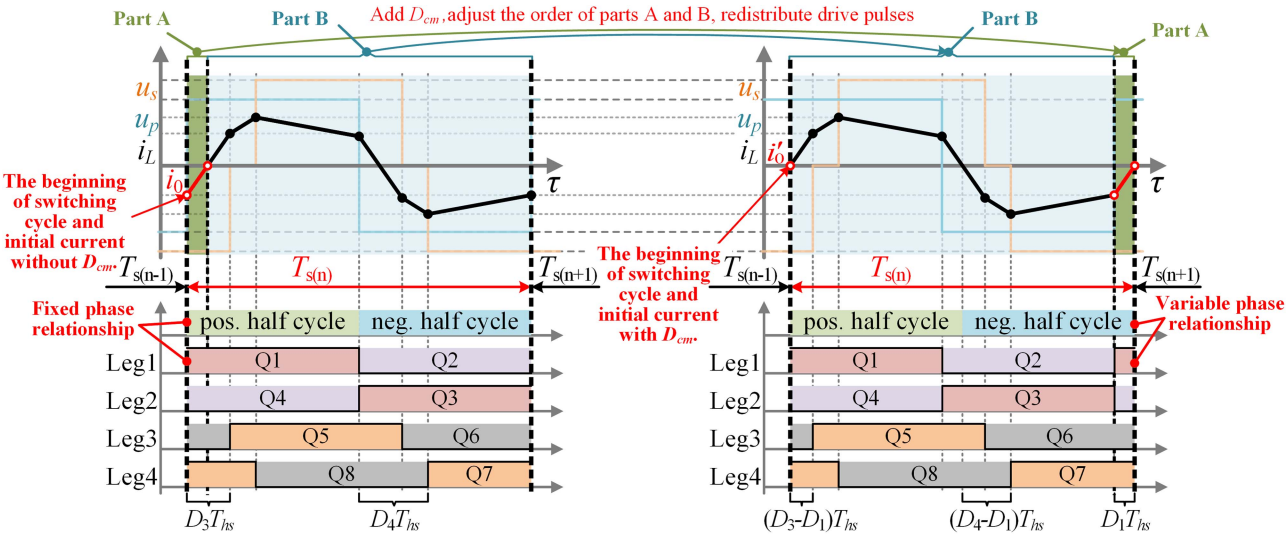

Fig. 4. Impact of D_{cm} on the voltage-current waveform.

A. Operating Principle of MIICC

In previous modulation methods, only the difference in phase shift ratios between the four half-bridges is of interest, not their reference phase, which is typically fixed to a constant angle [28]. In Fig. 4, adjusting the reference phase (selecting the phase of Leg1 as the reference) to be variable causes synchronous changes in the phase of u_p, u_s, and i_L. It makes the initial phase angle of i_L controllable and decoupled from the power control.

The main idea of MIICC is to identify the ZCP of the desired inductor current and add a same phase shift ratio (D_{cm}) to the voltage-current waveform and the gate signals simultaneously, thereby making the ZCP the initial current. Thus, (8) can be re-expressed as (10). This ensures current decoupling of adjacent switching cycles. In the MIICC algorithm, D_{cm} is the only control variable in the actual implementation. Fig. 4 illustrates how D_{cm} affects the voltage "u_p," "u_s" and the inductor current "i_L."

$$\begin{aligned}\langle i_L(\tau_0)\rangle_{T_{sn},\text{desired}} &= \langle i_L(\tau_0)\rangle_{T_{sn},\text{actual}} = \langle i_L(\tau_6)\rangle_{T_{s(n-1)},\text{actual}} \\ &= \langle i_L(\tau_0)\rangle_{T_{s(n-1)},\text{actual}} = 0. \end{aligned} \tag{10}$$

In Fig. 4, the ZCP of the positive half-switching cycle of the inductor current is used as the dividing line. The gate signal Q1–Q8 can be divided into two parts. MIICC optimizes OPS modulation by adjusting the order of these two parts. In this way, the duty ratio of the gate signal for each MOSFET remains constant at 0.5, but the initial inductor current is adjusted from i_0 to i'_0. Meanwhile, (2) should be modified to $D_1 = D_{\text{cm}}$.

B. Calculation Method of D_{cm} for OPS Modulation

In TDCM, the inductor current remains constant at zero between τ_0 and τ_1, as shown in Fig. 2(a). Therefore, any point within this interval can be optimized as the initial point, that is, D_{cm} ranges from 0 to 1-D_{p}. In practice, when the previous switching cycle operates in TDCM, D_{cm} is set to zero; when the previous switching cycle operates in TCCM, D_{cm} is set to 1 - D_{p} and 0 at the first and the second half-switching cycles, respectively. The reasons for this will be discussed in Section IV. In TCCM, the initial current of each switching cycle is not zero, as shown in Fig. 2(b). Therefore, it is crucial to implement active control to ensure that the initial current is controlled to zero. The partial derivative of $i_L(\tau_0)$ with respect to P_n can be expressed as (11).

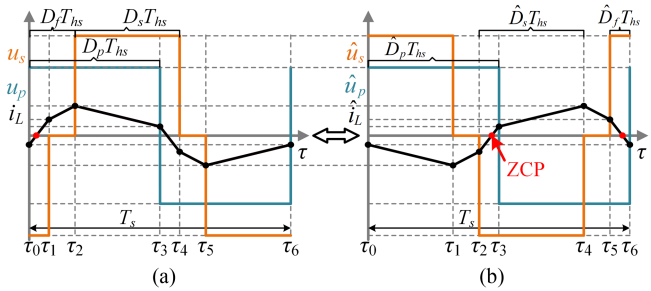

Fig. 5. Symmetrical transformation from forward to backward scenarios. (a) AC side to the dc side. (b) DC side to the ac side.

The aforementioned calculations can be easily performed with the assistance of Mathematica or any other similar software. The partial derivative is always less than zero, indicating that $i_L(\tau_0)$ is a decreasing function of P_n within the feasible region. Considering $P_n \in ((d-1)/2d^2, 1/4]$, the range of $i_L(\tau_0)$ in TCCM can be calculated as (12).

$$\frac{\partial i_L(\tau_0)}{\partial P_n} = -\frac{2du_{ac}}{4f_sL\left[(d-1)^2+1\right]\sqrt{\frac{1-4P_n}{2-2d+d^2}}} < 0 \tag{11}$$

$$-\frac{u_{ac}}{4f_sL} \le i_L(\tau_0) < 0. \tag{12}$$

By substituting the phase shift ratio expressions from Table I into (4), $i_L(\tau_1)$ can be expressed as follows:

$$i_L(\tau_1) = \frac{u_{dc}}{4f_sL}\left(1 - d\sqrt{\frac{1-4P_n}{d^2-2d+2}}\right). \tag{13}$$

The partial derivative of $i_L(\tau_0)$ with respect to P_n can be expressed as follows:

$$\frac{\partial i_L(\tau_1)}{\partial P_n} = \frac{2du_{dc}}{4f_sL\left[(d-1)^2+1\right]\sqrt{\frac{1-4P_n}{2-2d+d^2}}} > 0. \tag{14}$$

The partial derivative is always greater than zero, indicating that $i_L(\tau_1)$ increases as P_n increases. Considering $P_n \in ((d-1)/2d^2, 1/4]$, the range of $i_L(\tau_1)$ in TCCM can be calculated as follows:

$$0 < i_L(\tau_1) \le u_{dc}/4f_sL. \tag{15}$$

By combining (12) and (15), it can be seen that the maximum value of $i_L(\tau_0)$ and the minimum value of $i_L(\tau_1)$ are obtained at $P_n = (d-1)/2d^2$. This value serves as a boundary for TDCM and TCCM. Hence, the ZCP of inductor current during first half-switching cycle must be between τ_0 and τ_1. As shown in Fig. 2, the voltage across the inductor is constant during the interval τ_0–τ_1. This allows us to calculate the current slope λ using (16), and subsequently determine $D_{\rm cm}$ using (17).

$$\lambda = (u_{ac}+u_{dc})/L \tag{16}$$

$$D_{cm} = \frac{\Delta i/\lambda}{T_{hs}} = \frac{-i_L(\tau_0)}{\lambda T_{hs}} = \frac{1+d(D_s+2D_f-2)}{2(1+d)}. \tag{17}$$

Fig. 5 illustrates the voltage-current waveforms when an equal amount of transfer power using TCCM in two directions: from the dc side to the ac side (inverter mode) and from the ac side to the dc side (rectifier mode). Fig. 5(a) and (b) are constructed using the same parameters as follows:

$$\begin{cases} \hat{u}_{ac} = u_{ac}, \hat{u}_{dc} = u_{dc} \\ |\hat{P}_{ac}| = |P_{ac}| \end{cases}. \tag{18}$$

Based on Table I, the relationship of the optimal phase shift ratios of Fig. 5(a) and (b) can be expressed as follows:

$$\begin{cases} \hat{D}_p = D_p \\ \hat{D}_s = D_s \\ \hat{D}_f = D_f + D_s - 1 \end{cases}. \tag{19}$$

The inductor currents of Fig. 5(a) and (b) are mirror-symmetrical to each other. Thus, the current at each switching action moment during inverter mode can be expressed using the values obtained during rectifier mode. The specific correspondence can be expressed as follows:

$$\begin{cases} \hat{i}_L(\tau_0) = i_L(\tau_0) \\ \hat{i}_L(\tau_1) = -i_L(\tau_2) \\ \hat{i}_L(\tau_2) = -i_L(\tau_1) \end{cases}. \tag{20}$$

Combining (12), (15), and (20) with Fig. 5, when energy is transferred from the dc side to the ac side using TCCM, the ZCP between τ_2 and τ_3 is selected as the optimization objective. Based on Fig. 5(b), the current slope $\hat{\lambda}$ in this interval is equal to the slope in interval τ_0–τ_1. Therefore, $\hat{D}_{cm}$ can be calculated as follows:

$$\hat{D}_{cm} = 1 - D_{cm} = \frac{1-d(D_s+2D_f-4)}{2(1+d)}. \tag{21}$$

IV. Practical Design Consideration

Previous calculations of the ZCP have primarily relied on the theoretical circuit model of the DAB converter. Nevertheless, practical implementations are subject to nonideal elements like dead time, line resistance, capacitor ripple voltage, and time-varying ac port voltage, which can introduce inaccuracies in determining the ZCP. Enhancing the precision of calculating the phase-shift ratio D_{cm} necessitates a thorough analysis of the impacts of these nonideal factors and the addition of suitable compensatory strategies.

A. Effect of Dead Time

The effect of the dead time in DAB is analyzed in [7]. If the switching transient of the power devices Q1–Q8 in the DAB stage do not coincide within the same switching cycle, it may result in a deviation from the effective phase shift ratios. The modification of the gate drive signal phase by the MIICC will lead to an alteration in the initial switching state within the switching cycle. Therefore, when examining the impact of dead time, it is essential to take into account the operational mode of the preceding switching cycle. In OPS modulation, which encompasses a total of two modulation modes known as TDCM and TCCM. Thus, there exist four potential transition combinations to be taken into account when analyzing two successive switching cycles.

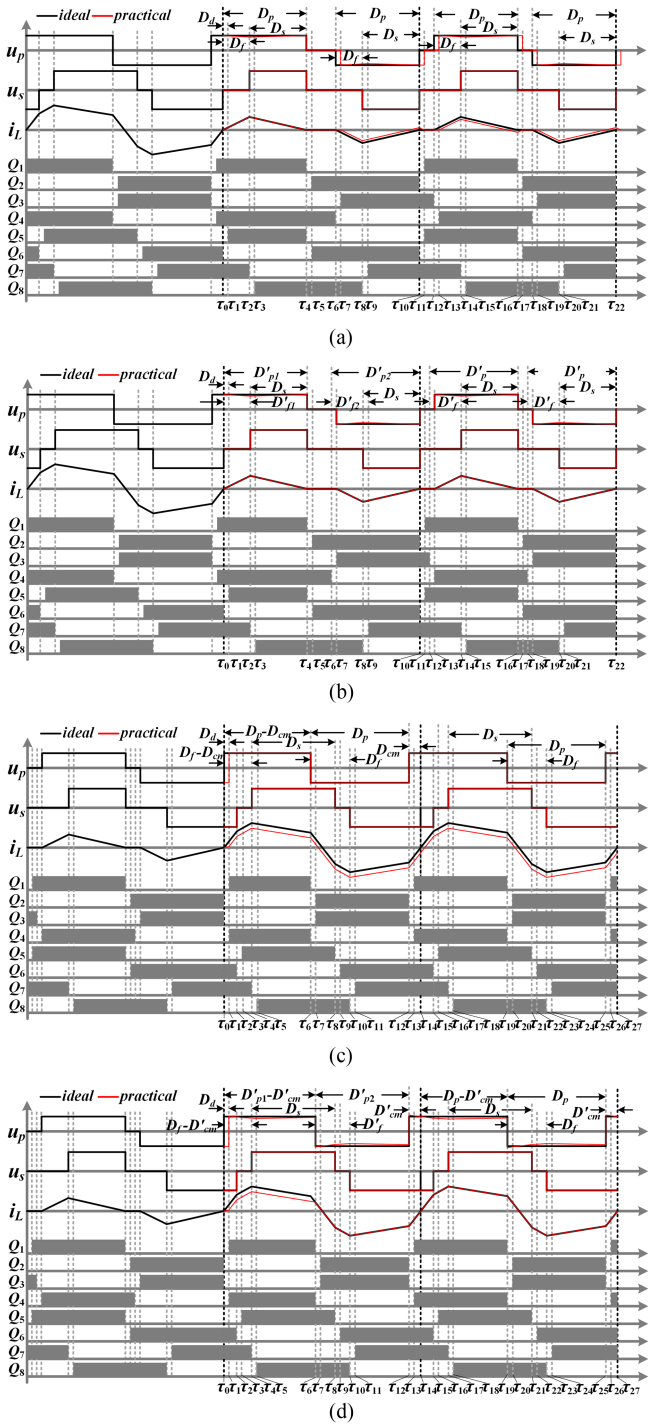

Fig. 6. Waveform of MIICC for different transition combinations. (a) High-frequency link waveform of TDCM without compensation. (b) High-frequency link waveform of TDCM with compensation. (c) High-frequency link waveform of TCCM without compensation. (d) High-frequency link waveform of TCCM with compensation.

1) TCCM-to-TDCM Transition: As illustrated in Fig. 6(a), the converter operates in the TCCM mode prior to time τ_0, transitioning to the TDCM mode within the time interval [τ_0, τ_{10}]. In order to prevent the switching operation of Q3 and Q4 at time τ_0, adjustments are made to the zero-level distribution of "u_p" and "u_s" within the time interval [τ_0, τ_6], resulting in an asymmetric distribution of "zero current region." This phenomenon is specific to the TCCM-to-TDCM transition. At time τ_0, the gate drive signal of Q6 is disabled and Q6 is turned OFF. Since "u_p" has already established a positive polarity voltage before time τ_0, the transformer's secondary-side current will be forced freewheeling through the parallel diode of Q5. At time τ_2, the gate drive signal of Q7 is disabled and Q7 is turned OFF, the transformer's secondary-side current will be forced freewheeling through the parallel diode of Q8 due to positive polarity of the inductor current. At time τ_4, Q1 and Q5 are turned OFF, as the volt-second products of "u_p" and "u_s" within the interval [τ_0, τ_4] are equivalent, the inductor's current reaches zero at time τ_4. Meanwhile, the voltage drop of the series inductor, that is, $u_L = u_p - u_s = 0$ during $\tau \in [\tau_4, \tau_5]$, and the inductor current remains constant. It can be proved that within interval [τ_0, τ_5], the operating process of the proposed MIICC with dead time is the same as that under the ideal condition. At time τ_6, the gate drive signal of Q4 is disabled and Q4 is turned OFF. Since the control signal of Q3 is not enabled yet, the transformer's primary-side current remains zero, resulting in the voltage "u_p" staying at zero in the interval [τ_6, τ_7]. This connection persists until the turn-ON of Q3 after the dead time. It shows that the dead time causes a reduction in the effective output level width of the active bridge on the ac side at the turn-ON time of power device Q3 by the duration of one dead time. At time τ_8, Q7 is capable of achieving ZVS turn-ON, similar to Q8 at time τ_2, thereby the dead time has no effect. At time τ_{10}, the inductor current is greater than zero as the volt-second product of "u_p" within the interval [τ_0, τ_4] is less than that of "u_s." This will lead to the failure of the zero-current control of the MIICC method. According to the previous analysis, this phenomenon is caused by the loss of effective duty cycle caused by the dead time of Q3. Hence, deadtime compensation is attained by advancing the timing of Q4 turn-OFF (Q3 turn-ON) by a single deadtime width. Once the deadtime of Q3 is compensated, the nonzero current at time τ_{10} will be eliminated naturally.

2) TDCM-to-TDCM Transition: In this scenario, the zero levels of "u_p" and "u_s" are symmetrically distributed, and the waveforms of the first and second half-switching cycles are symmetrical. Both are also similar to the second half-switching cycle in the TCCM-to-TDCM transition. Therefore, deadtime compensation is attained by advancing the timing of Q3(Q4) turn-OFF and turn-ON by a dead time width.

3) TDCM-to-TCCM Transition: As illustrated in Fig. 6(c), the converter operates in the TDCM prior to time τ_0, transitioning to the TCCM within the time interval [τ_0, τ_{14}]. At time τ_0, the gate drive signals of Q2 and Q3 are disabled. Since "u_s" has already established a negative polarity voltage before time τ_0, the transformer's primary-side current will be forced freewheeling through the parallel diode of Q2 and Q3, and the "u_p" still maintains a negative polarity voltage output. This indicates that the dead time of Q1 and Q4 reduces the effective level width of the positive voltage of "u_p." Therefore, at time τ_1, the actual inductor current value will be lower than the ideal inductance current value. This difference value between the practical and ideal values of the inductor current will present throughout the time interval [τ_1, τ_{14}]. This difference value is

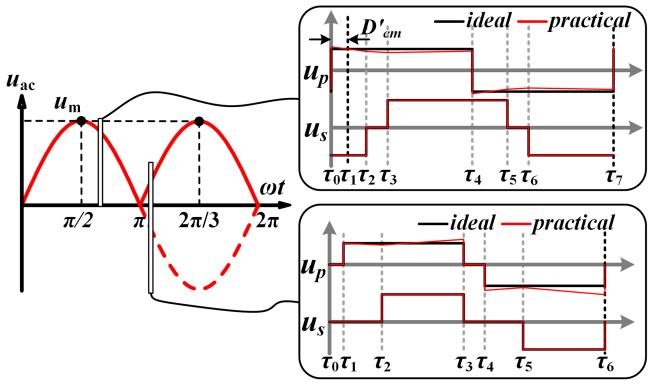

Fig. 7. Fluctuant ac voltage over the switching cycle.

typically not substantial due to the small proportion of dead time within the entire switching cycle. In general, the polarity of the inductor current within the interval $[\tau_1, \tau_{14}]$ remains unchanged, resulting in all switches staying in the ZVS turn-ON state, thereby eliminating the effect of dead time. To counteract the impact of dead time in the time interval $[\tau_0, \tau_1]$, it becomes imperative to extend the duration of the "u_p" positive level. Consequently, a delay in the turn-OFF timing of Q1 and Q4 by a width equivalent to the dead time is required.

4) TCCM-to-TCCM Transition: In this scenario, at the point when the inductor current reaches zero, there is no switching action present, allowing all power devices to attain ZVS turn-ON (which is the fundamental property of OPS). Consequently, the presence of dead time does not impact the operation under these conditions.

B. Effect of Voltage Ripple Caused

In the specific operational scenario of a single-stage ac–dc converter, the presence of a small filter capacitance (usually a few microfarads to a dozen microfarads) at the ac port combined with significant ripple currents at the DAB stage can result in notable ripple voltage across the filter capacitor. This effect is exacerbated by sinusoidal fluctuations in the grid voltage, causing variations in the ac port's steady-state voltage throughout the switching cycle [36], particularly evident at the ZCP of the grid voltage. This phenomenon becomes more pronounced as the ratio of the switching frequency to the grid frequency decreases. Furthermore, line resistances in the high-frequency loop lead to variations in the effective voltage applied to the inductor by the port voltage, impacting the precision of the ZCP calculation.

The high-frequency loop waveform, accounting for nonideal elements, is depicted in Fig. 7, with voltage fluctuations not depicted to scale for clarity. Taking the TDCM within the $[\pi, \frac{3\pi}{2}]$ range of the grid frequency cycle as an example, as outlined in the preceding discussion, the practical voltage waveform is expected to consist of four distinct terms.

1) Ideal Voltage Term: This term represents the voltage waveform derived from the simplified ideal model of the traditional DAB converter without considering nonideal parameters. In this model, the waveform is depicted as an ideal square wave with a consistent amplitude throughout the switching cycle, which is the grid voltage sampling value at the beginning of the switching cycle.

2) Sinusoidal Voltage Correction Term: To model the changing ac voltage over a switching period, a ramp function Δu_1 is used to represent the amount of change over the switching cycle. Through the utilization of a phase-locked loop, the grid voltage can be characterized as a sinusoidal waveform with identifiable frequency, phase, and amplitude attributes. Consequently, the rate at which the voltage changes can be articulated as a cosine function, as delineated by (22). The slope λ_g of the ramp function is the value of the cosine function corresponding to the current switching period.

$$\begin{cases} \lambda_g = \frac{du_{ac}}{dt} = u_m \omega_g \cos(\omega_g t), \omega_g t \in [0, \pi] \\ \Delta u_1 = \begin{cases} \lambda_g \tau, & \tau \in [0, T_{hs}] \\ -\lambda_g \tau, & \tau \in [T_{hs}, T_s] \end{cases} \end{cases}. \tag{22}$$

3) Capacitance Ripple Voltage Correction Term: The DAB stage can be modeled as a controlled current source, and in accordance with Kirchhoff's current law (KCL), the current passing through the ac port is the sum of the capacitive ripple current and the current flowing through the DAB stage. By disregarding the ripple component of the grid current, the magnitude of the grid current throughout the switching cycle can be represented by the constant i_{ref}, which is the reference current used to calculate the phase shift ratios. As shown in (23), there is a correlation between i_{ref} and the ac side port current of the DAB stage during the switching cycle.

$$i_{ref} = \frac{1}{T_{hs}} \int_0^{T_{hs}} i_{in}(\tau) d\tau. \tag{23}$$

The ripple current of the capacitor leads to the ripple voltage of the capacitor, and this component can be given by

$$\Delta u_2 = \frac{1}{C} \int (i_{ref} - i_{in}) d\tau. \tag{24}$$

During the intervals [0, T_{hs}] and [T_{hs}, T_s] of the switching cycle, the average value of the ripple voltage is zero. However, the average value is not zero for any time period within these intervals, such as the time period $[\tau_0, \tau_1]$ in the TCCM and the time period $[\tau_1, \tau_3]$ in the TDCM as shown in Fig. 7. In order to facilitate the subsequent calculations, this correction term is approximated by the average value of the ripple voltage over each time period, which can be calculated from the change in charge of the filter capacitor over a period of time. In the TCCM, the mean ripple voltage within the range [0, T_{hs}] is null, while within the range [0, $D_{cm}T_{hs}$], the mean ripple voltage can be represented by (25). This suggests that in this mode, this factor does not influence the magnitude of $i_L(\tau_0)$, but solely impacts the value of D_{cm}. Conversely, in the TDCM, the mean ripple voltage in the range [0, (1-D_p)T_{hs}] can be denoted by (26). Since the mean value within the range [0, T_{hs}] is zero, the mean value within the range [(1-D_p)T_{hs}, T_{hs}] can be given by (27). Where C denotes the capacitance value of the filter capacitor.

$$\overline{\Delta u_2} \approx \frac{\int_0^{D_{cm}T_{hs}} [i_{ref} - \lambda(\tau - D_{cm}T_{hs})] d\tau}{2C}$$

$$= \frac{(i_{ref} - \frac{i_L(\tau_0)}{2})D_{cm}T_{hs}}{2C} \tag{25}$$

$$\overline{\Delta u_2} \approx \frac{\int_0^{(1-D_p)T_{hs}} i_{ref}d\tau}{2C} = \frac{(1-D_p)T_{hs}i_{ref}}{2C} \tag{26}$$

$$\overline{\Delta u_2} \approx \frac{(1-D_p)T_{hs}i_{ref}}{2C} \cdot \left(-\frac{(1-D_p)}{D_p}\right)$$

$$= -\frac{(1-D_p)^2T_{hs}i_{ref}}{2CD_p}. \tag{27}$$

4) Resistance Voltage Drop Correction Term: Line resistances in the high-frequency loop encompass the on-resistance of power devices, winding resistances of inductors and transformers, and wiring resistances of printed circuit boards. To facilitate analysis, all resistances within the high-frequency loop are simplified and represented as the transformer primary-side resistance R_{tot}, in series with the inductor. From the perspective of circuit analysis, the line resistance can be regarded as the internal resistance of the voltage source "u_p." Consequently, the impact of the line resistance is reflected in a decrease in the effective voltage of the ac port applied to the inductor. The expression can be given by $\Delta u_3 = R_{tot}i_L$.

In TDCM, the duty cycle of "u_p" needs to be increased to compensate for this effect; in TCCM mode, this voltage difference needs to be taken into account to recalculate the ZCP.

C. Compensation Methods of D_{cm} Considering Nonideal Parameters

As indicated in Section IV-A, the dead time compensation necessitates the widening of the affected waveform by a width of one dead time interval (D_d). This is manifested in TDCM by advancing the point at which the "u_p" transition from zero voltage to positive or negative voltage occurs by D_d, and in TCCM by deferring the point at which the "u_p" transition from positive to negative voltage occurs by D_d. Where D_d represents the ratio of the dead time to the half-switching period, as defined in the following equation:

$$D_d = t_{dead}/T_{hs}. \tag{28}$$

As indicated in Section IV-B, in the TDCM, the impacts of nonideal factors manifest as alterations in the effective volt-second product of the "u_p" applied to the inductor, resulting in nonzero values of inductor current in the "zero current region" (e.g., intervals [τ_0, τ_1] and intervals [τ_3, τ_4] as illustrated in Fig. 2). As Δu_1 exhibits asymmetry between the first and second half-switching cycles, the phase shift ratios with compensation of these two half-switching cycles must be calculated separately. Referring to Fig. 6(b), (29) can be derived under the condition that the volt-second products of "u_p" and "u_s" during the interval [τ_{13}, τ_{16}] are equal.

$$\int_{\tau_{13}}^{\tau_{16}} (u_{ac} + \Delta u_1 + \Delta u_2 + \Delta u_3)d\tau = \int_{\tau_{13}}^{\tau_{16}} (nu_{dc})d\tau. \tag{29}$$

By associating (22)–(24) and (27)–(29), and neglecting second-order infinitesimal terms, the expression of the ac side active bridge internal phase shift ratio's compensation can be obtained as (30). Moreover, when the previous switching cycle of the TDCM operates in TCCM, the compensation value of Δu_1 changes due to the phase adjustment of the first half-switching cycle. Equation (29) is recalculated as (31).

$$\Delta D_{p1} = \frac{1}{u_{ac}}\left(\frac{i_{ref}(1-D_p)^2T_{hs}}{2CD_p} + i_{ref}R_{tot} - \frac{\lambda_g}{2}T_{hs}D_p(2-D_p)\right) \tag{30}$$

$$\Delta D_{p2} = \frac{1}{u_{ac}}\left(\frac{i_{ref}(1-D_p)^2T_{hs}}{2CD_p} + i_{ref}R_{tot} - \frac{\lambda_g}{2}T_{hs}{D_p}^2\right) \tag{31}$$

$$\Delta D_{p3} = \frac{1}{u_{ac}}\left(\frac{i_{ref}(1-D_p)^2T_{hs}}{2CD_p} + i_{ref}R_{tot} - \frac{\lambda_g}{2}T_{hs}D_p(4-D_p)\right). \tag{32}$$

The phase shift ratio's compensation of the second half-switching cycle can be calculated using the similar method. It can be given by (32).

In TCCM, it is essential to calculate the value of $i_L(\tau_0)$ following the influence of nonideal parameters, and subsequently determine the time width from $i_L(\tau_0)$ to the ZCP. Since the average value of Δu_2 is zero in the half-switching period, the variation of the initial current $i_L(\tau_0)$ only needs to consider the volt-second product of Δu_1 and Δu_3. The variation of $i_L(\tau_0)$ can be expressed as follows:

$$\Delta i_L(\tau_0) = \frac{1}{2L}\int_0^{T_{hs}} (\Delta u_1 + \Delta u_3)d\tau = \frac{i_{ref}R_{tot}T_{hs} + \frac{1}{2}\lambda_g T_{hs}^2}{2L}. \tag{33}$$

Consequently, the prediction equation for the ZCP can be adjusted as follows:

$$0 - (i_L(\tau_0) + \Delta i_L(\tau_0)) = \frac{1}{L}\int_0^{(D_{cm}+\Delta D_{cm})T_{hs}} (u_{ac} + nu_{dc} + \Delta u_1 + \overline{\Delta u_2} + \Delta u_3)d\tau. \tag{34}$$

By associating (22)–(25), and (34), and neglecting second-order infinitesimal terms, D_{cm} can be obtained as (35), shown at the bottom of the next page.

Upon the aggregation of all aforementioned compensation values for distinct items, the compensation values for disparate scenarios of TDCM and TCCM are presented in Table II. The numerical subscripts are utilized to distinguish between the first and second half-switching cycles. The symbol accompanied by a superscript "$'$" denotes the phase shift ratios with compensation.

TABLE II
COMPENSATION VALUES IN DIFFERENT SCENARIOS

Transition combinations	Phase shift ratio with compensation
TDCM-to-**TDCM**	$D'_{p1}=\Delta D_{p1}+D_d,\ D'_{f1}=D'_{p1}-D_s,\ D'_{cm}=0$ $D'_{p2}=\Delta D_{p3}+D_d,\ D'_{f2}=D'_{p1}-D_s,\ D'_{cm}=0$
TCCM-to-**TDCM**	$D'_{p1}=\Delta D_{p1},\ D'_{f1}=D'_{p1}-D_s,\ D_{cm}=1-D'_{p1}$ $D'_{p2}=\Delta D_{p3}+D_d,\ D'_{f2}=D'_{p1}-D_s,\ D_{cm}=0$
TDCM-to-**TCCM**	$D'_{p1}=1+D_d,\ D'_{p2}=1-D_d,\ D'_{cm}=D_{cm}+\Delta D_{cm}$
TCCM-to-**TCCM**	$D'_{cm}=D_{cm}+\Delta D_{cm}$

V. EFFECT OF MIICC METHOD ON WAVEFORM QUALITY OF GRID CURRENT

The previous sections describe the working principle of MIICC and the calculation of key parameters. This section will focus on analyzing the impact of MIICC on OPS modulation, including the port power and harmonic characteristics.

In one switching cycle without MIICC, when $0<\tau\le T_{hs}$, $i_{in}=i_L$, and when $T_{hs}<\tau\le T_s$, $i_{in}=-i_L$. i_{in} represents the dc bus current of the active bridge FB2. The asymmetry of the inductor currents in the two half-switching cycles due to the nonideal parameters is disregarded, as the proportion of nonideal terms in the inductor current is less than that of the ideal term. Consequently, the expression of the port current for the first half-switching cycle is identical to that of the second half-switching cycle, both of which can be represented by (3). In first half-switching cycle, according to the Fourier transform theory, $i_L(\tau)$ can be decomposed by trigonometric series, where "$2f_s$" is the fundamental frequency for Fourier expansion, and it can be expressed as follows:

$$\begin{cases} i_{\text{in}}(\tau)=A_0+\sum_{k=1}^{\infty}A_k\cos\left(k\cdot 4\pi f_s\tau+\varphi_k\right) \\ A_0=\int_0^{T_{hs}} i_{\text{in}}(\tau)d\tau \Big/ T_{hs} \\ a_k=\left(2\int_0^{T_{hs}} i_{\text{in}}(\tau)\cos\left(k\cdot 4\pi f_s\tau\right)d\tau\right)\Big/T_{hs} \\ b_k=\left(2\int_0^{T_{hs}} i_{\text{in}}(\tau)\sin\left(k\cdot 4\pi f_s\tau\right)d\tau\right)\Big/T_{hs} \\ A_k=\sqrt{{a_k}^2+{b_k}^2},\varphi_k=\operatorname{atan2}(b_k,a_k)\in(-\pi,\pi] \end{cases} \tag{36}$$

where $\varphi_k(k=1,2,\ldots)$ is the initial phase angle of each harmonic components, $A_k(k=0,1,\ldots)$ denotes the amplitude of each component contained in the input current (A_0 denotes the amplitude of the dc component related to the port power, $A_k(k=1,2,\ldots)$denotes the amplitude of the harmonic components associated with "$2f_s$."). This is related to the quality of port waveform the converter. Based on Section III, MIICC optimizes the initial current by adding a phase shift to i_L. Thus, the optimized inductor current and dc bus current can be expressed as follows:

$$\begin{cases} i'_L(\tau)=i_L(\tau+D_{cm}T_{hs}) \\ i'_{in}(\tau)=i_{in}(\tau+D_{cm}T_{hs}) \end{cases}. \tag{37}$$

Based on the shifting property of the Fourier transform, the Fourier coefficients of the input current using MIICC can be expressed as $A'_k=A_k\ (k=0,1,\cdots)$ and $\varphi'_k=\operatorname{mod}(\varphi_k+D_{cm}\cdot 2\pi,\pi),(k=1,2,\cdots)$. This indicates that MIICC does not affect the harmonic content, but only changes the initial phase angle of each harmonic. The same conclusions are reached in the analysis of the TDCM, which is not repeated in this article but is analyzed in the same way. The calculation of total harmonic distortion (THD) is based on the following equation:

$$\text{THD}=\sqrt{I_2^2+I_3^2+\cdots+I_k^2}\Big/I_1 \tag{38}$$

where I_1 is the root-mean-square (RMS) value of the fundamental component of input current, and I_{k} is the RMS value of the kth-degree harmonic. Equation (36) provides the harmonic components for a single switching cycle. The percentage of harmonics over the entire switching cycle can be calculated using (39). T_{g} represents the grid cycle. Therefore, $T_{\text{g}}/T_{\text{s}}$ represents the quantity of switching cycles within a grid cycle. The expression for THD is independent of φ_k when (27) is brought into (26). This demonstrates that the harmonic content of the port current is not altered by MIICC. An analysis of the dc-port ripple current supports the same conclusion. Furthermore, it can be noted that $A'_0=A_0$ results in $I'_1=I_1$, indicating that the input power remains unaffected.

$$\begin{cases} I_1=\sqrt{\frac{T_s}{T_g}\sum_{n=1}^{T_g/T_s}\int_0^{T_s}A_{0,n}^2d\tau} \\ I_k=\sqrt{\frac{T_s}{T_g}\sum_{n=1}^{T_g/T_s}\int_0^{T_s}\left(A_{k,n}\cos(k\cdot 4\pi f_s\tau+\varphi_k)\right)^2d\tau} \\ \quad=\sqrt{\frac{T_s}{T_g}\sum_{n=1}^{T_g/T_s}\frac{A_{k,n}^2}{2}} \end{cases}. \tag{39}$$

Therefore, MIICC does not affect the port waveform quality as well as the input power of the converter.

VI. SIMULATION EVALUATION

In order to verify the effectiveness of the theoretical analysis, a simulation evaluation was carried out in PLECS with the main converter parameters shown in Table III. The rated output power of the DAB converter is 10 kW. Fig. 8 shows the simulation waveforms of eight switching cycles when the instantaneous input power changes from 7.3 to 14.6 kW, with and without optimization using the proposed MIICC. The purple and red

$$\begin{aligned} \Delta D_{cm}&=\frac{D_{cm}^2\left(i_L(\tau_0)-2i_{ref}\right)T_{hs}-C\left(2D_{cm}i_L(\tau_0)R_{tot}+2i_{ref}R_{tot}+T_{hs}\lambda_g+2{D_{cm}}^2T_{hs}\lambda_g\right)}{-2D_{cm}\left(i_L(\tau_0)-2i_{ref}\right)T_{hs}+2C\left(2nu_{dc}+i_L(\tau_0)R_{tot}+2u_{ac}+2D_{cm}T_{hs}\lambda_g\right)} \\ &\approx\frac{D_{cm}^2\left(i_L(\tau_0)-2i_{ref}\right)T_{hs}}{4C\left(nu_{dc}+u_{ac}\right)-2D_{cm}\left(i_L(\tau_0)-2i_{ref}\right)T_{hs}} \end{aligned} \tag{35}$$

TABLE III
SIMULATION PARAMETERS

Parameter	Value	Parameter	Value
u_g	220 Vrms	n	1
C_{bus}	2.52 mF	L	14 μH
u_{dc}	400 V	L_f	80 μH
f_s	50 kHz	C_f	2 μF

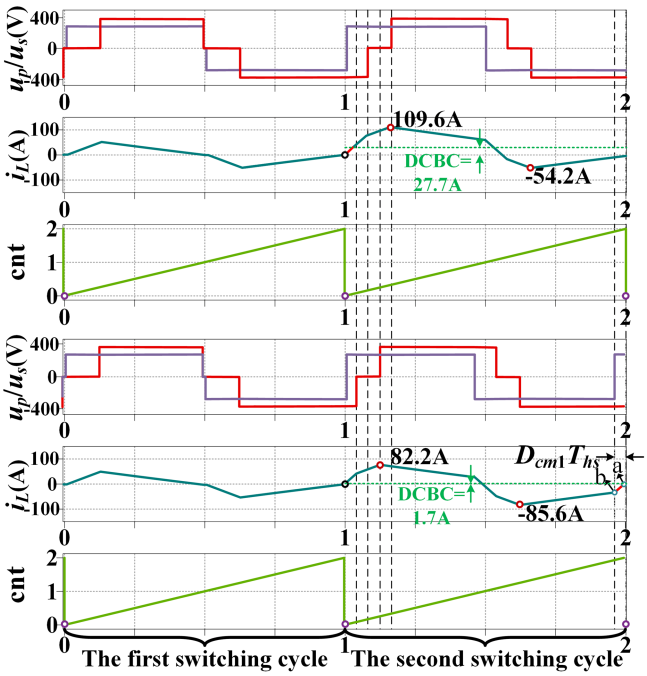

Fig. 8. Simulation results when the instantaneous input power changes from 7.3 to 14.6 kW. The upper half-part shows the waveform with 27.7 A DC bias obtained without MIICC and the lower half-part shows the waveform with 1.7 A DC bias obtained with MIICC.

lines show the output voltage waveforms of the ac and dc side active bridge, respectively. The inductor current is denoted by i_{L}, and the "cnt" value output by the controller is reset to zero at the beginning of each switching cycle.

In the upper half-part of Fig. 8, the initial current was not optimized using MIICC. As a result, the current of the first switching cycle couples with that of the second switching cycle after the power mutation, leading to a DCBC of 27.7 A in the second switching cycle. The peak current of the second switching cycle reaching as high as 109.6 A. The lower half-part of Fig. 8 illustrates that the MIICC-optimized inductor current is decoupled from the currents of adjacent switching cycles, the peak current of the second switching cycle is only 82.2 A with a DCBC of 1.7 A. The slight difference in positive and negative peak currents arises from the presence of the dead time of Q1 and Q4 at the beginning of the second switching cycle, as elucidated in Section IV-A. Based on the comparison of simulation results, MIICC reduces DCBC by 94%.

To label the value of D_{cm} on the simulation waveform, follow these steps: First, determine the ending moment of the second switching cycle based on "cnt," which corresponds to point "a" in Fig. 8. Then, locate the nearest moment of switching action

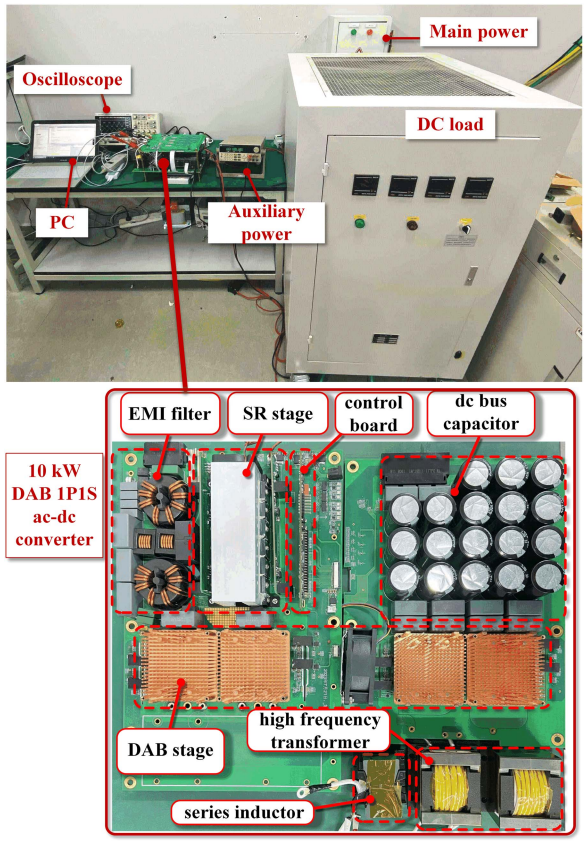

Fig. 9. Experimental platform.

TABLE IV
PROTOTYPE SETUP

Parameter	Value	Parameter	Value
u_{ac}	220 Vrms,50 Hz	n	0.59
C_{bus}	2.52 mF	L	10.8 μH
u_{dc}	200—650 V	L_{cm}	1.4 mH
f_s	50 kHz	L_{dm}	3.3 μH
C_x , C_y	0.33 μF, 4.7 nF	C_f	2 μF

within this cycle, which corresponds to point "b" in Fig. 8. Finally, calculate the ratio of the time length between "a" and "b" to "T_{hs}" to obtain the value of D_{cm}. However, observing "cnt" can often be challenging in practice. The approximation of point "a" can be determined by the ZCP of the inductor current. This method may introduce some errors, but they are within acceptable limits.

VII. EXPERIMENT VERIFICATION

A. Experimental Setup

A 10-kW experimental platform is illustrated in Fig. 9. The semiconductor devices used in the prototype are SiC MOSFET (CAB008M12GM3 for DAB stage and C3M0015065K for SR stage, both from Wolfspeed). The other parameters are the same as listed in Table IV for the DAB 1P1S ac–dc converter. L_{cm} is common mode choke (DKIH-3252-506J-NK, from Schurter). Its leakage inductance and L_{dm}, together with C_f, form an ac side

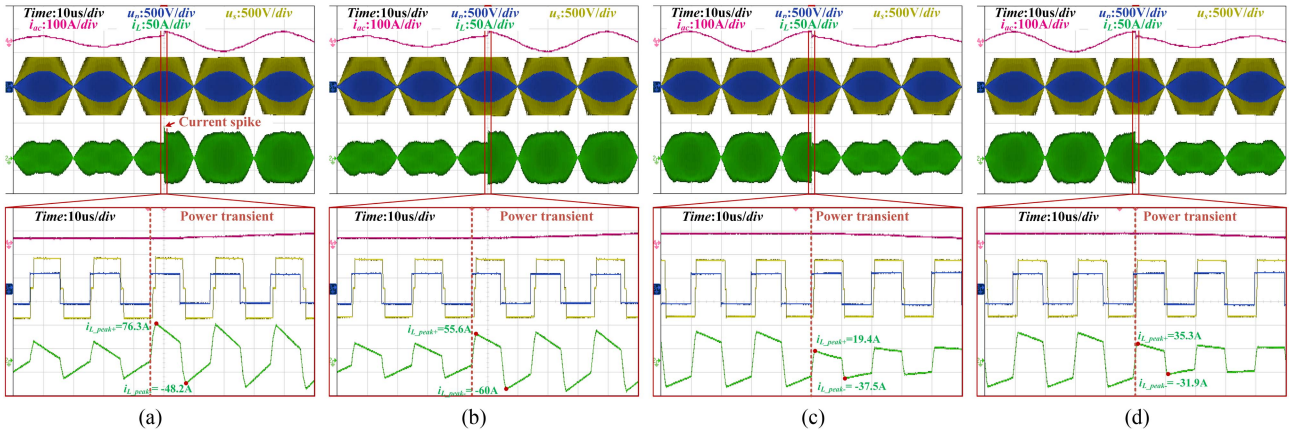

Fig. 10. Voltage-current waveforms of switching P_o between 3 and 6 kW when $u_{dc} = 560$ V and 90° phase angle of the grid voltage. (a) From 3 to 6 kW using OPS modulation without MIICC. (b) From 3 to 6 kW using OPS modulation with MIICC. (c) From 6 to 3 kW using OPS modulation without MIICC. (d) From 6 to 3 kW using OPS modulation with MIICC.

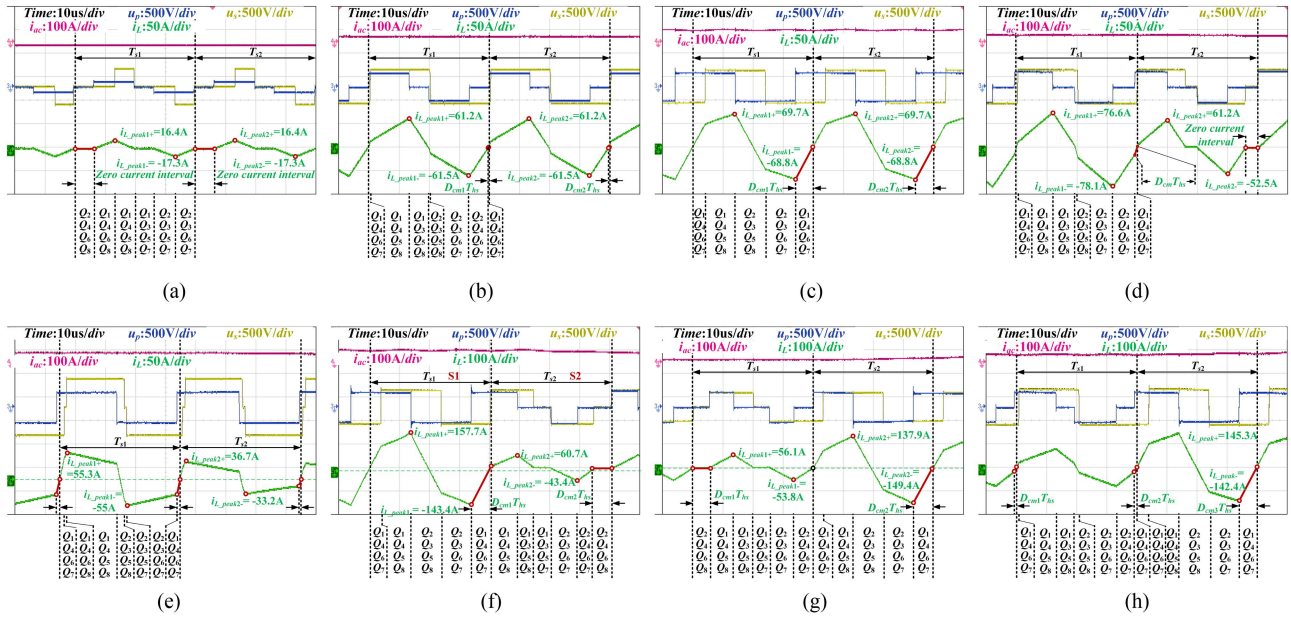

Fig. 11. Voltage-current waveforms of switching between different phase shift modulation modes when using MIICC. (a) TDCM to TDCM (TPS to TPS), boost condition. (b) TCCM to TCCM (EPS to EPS), buck condition. (c) TCCM to TCCM (SPS to SPS), buck condition. (d) TCCM to TDCM (EPS to TPS), buck condition. (e) TCCM to TCCM (EPS to EPS), boost condition. (f) TCCM to TDCM (SPS to TPS), buck condition. (g) TDCM to TCCM (TPS to SPS), buck condition. (h) TCCM to TCCM (EPS to SPS), buck condition.

filter to eliminate high-frequency ripple in the port current. C_x and C_y is used to form the electromagnetic interference (EMI) input filter. To absorb fluctuating power and reduce low-frequency voltage ripple, a large capacitor bank is placed on the dc bus. The control loop is implemented in a 32-bit 200-MHz digital signal processor TMS320F28377. The converter is controlled by closed-loop control of the output voltage. To improve the dynamic performance of the converter, load current feedforward compensation control has been added to the PI algorithm.

B. Experimental Results

Experiments were conducted on the DAB-1S ac–dc converter in rectifier mode to further demonstrate the validity of the proposed MIICC method. The experiments included sudden power increases, sudden power decreases, and other conditions. Fig. 10 displays the voltage-current waveforms for the input power mutation experiment with and without MIICC, respectively.

1) Power Increases: Fig. 10(a) shows that after the power increase, the inductor current of the OPS modulation without MIICC experiences a significant spike, reaching 76.3 A. The DCBC can be calculated as 14 A following the sudden power increase. In contrast, Fig. 10(b) displays the voltage and current waveform using MIICC, where the power naturally transitions into a new steady state without current spikes. DCBC was calculated to be −2.2 A, with a peak current of only −60 A. After optimizing the initial current using MIICC, the DCBC

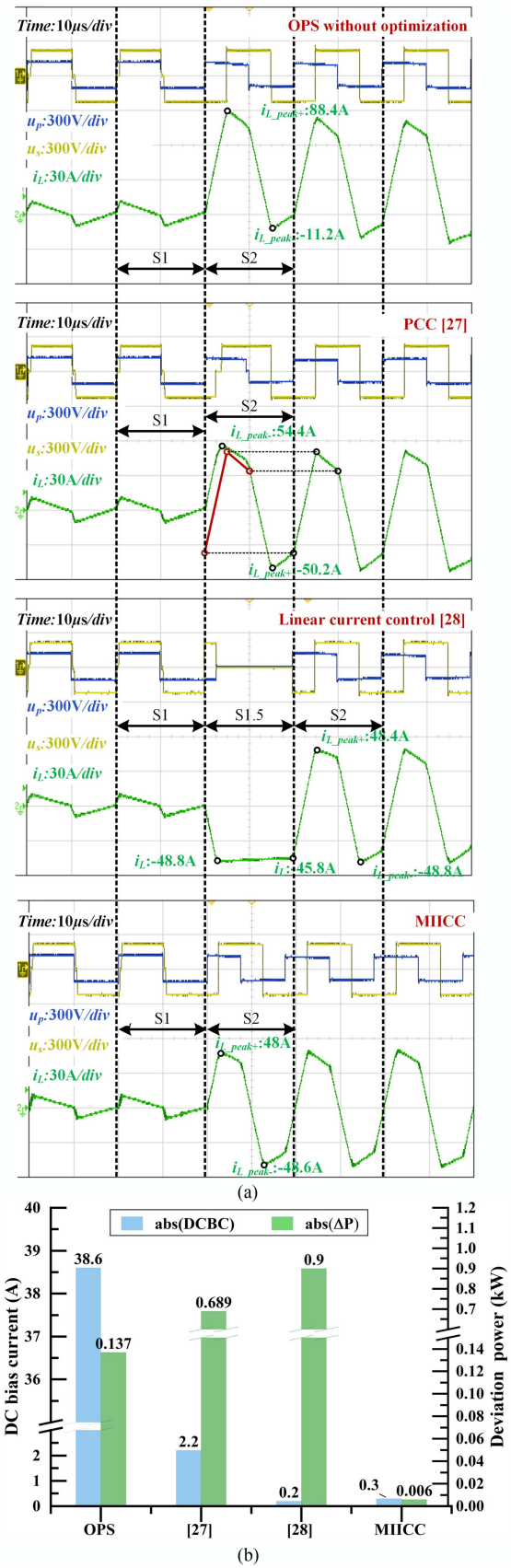

Fig. 12. Comparison of experimental results using different optimization methods. (a) Experimental contrast waveform. (b) Effect comparison of different methods.

and current peaks were significantly reduced under the same operating conditions. The experiments demonstrate that MIICC effectively eliminates DCBC when power increases.

2) Power Decreases: Fig. 10(c) illustrates that following the power decrease, the inductor current of the OPS modulation without MIICC exhibits an apparent asymmetry. The first switching cycle after the power change produced positive and negative peak currents of 19.4 and −37.5 A, respectively. These values were used to calculate the DCBC, which was determined to be −9.05 A. In contrast, the DCBC after using the MIICC was only 1.7 A, as shown in Fig. 10(d). Although Fig. 10(c) does not show a large current spike, the current waveform is highly asymmetric due to the DCBC. This asymmetry results in an increase in port ripple current and negatively affects the waveform quality. Furthermore, the DCBC leads to higher conduction losses. After optimizing the initial current using MIICC, the DCBC and current peaks were significantly reduced under the same operating conditions. The experiments show that MIICC effectively eliminates DCBC when power is reduced.

3) Other Conditions: When power flow direction changes, it is typically necessary to first reduce input power to zero before increasing power in the reverse direction due to the presence of inductor L_f in the main circuit. Therefore, this process can be represented as a combination of the two previous procedures. This article does not include experiments for this scenario.

Fig. 11 presents a detailed analysis of the observed and unobserved modulation mode combinations in the abovementioned experiments. Fig. 11(a), (b), and (c) show the steady-state operation waveforms after implementing the initial current control method proposed in this article to the TPS, EPS, and SPS, respectively. These are all the possible modulation mode in OPS modulation. In each switching cycle, the dark red lines indicate the portion of the current that is shifted by MIICC. It is evident that MIICC does not generate a narrow pulse during operation, indicating its applicability to all three modulation methods without affecting the switching frequency or number of switching actions.

The waveforms of dynamic switching between different phase shift modulation methods when using MIICC are displayed in Fig. 11(d)–(h). The width of D_{cm} is labeled using the method outlined in Section VI. Fig. 11(f) and (g) demonstrates the mutual switching between SPS and TPS in different directions, displaying the optimization results of the switching action times analysis in Section IV-A. Fig. 11(g) and (h) shows the experimental results obtained by switching from light load and medium load to full load, respectively. Following the switch, there is only a very small DCBC of −4.2 and 1.45 A. Based on the D_{cm} labeled in the figure, it can be deduced inversely that the peak current will be more than 280 A without MIICC. This current level is not tolerated by the power device and the magnetic components.

C. Compared With Other DCBC Elimination Methods

Fig. 12 compares the effectiveness of MIICC method proposed in this article with existing methods. The methods shown in Fig. 12(a) are MIICC proposed in this article, PCC [27], and

TABLE V
COMPARISON OF THE CONVENTIONAL METHODS AND THE PROPOSED METHOD

Method	Algorithm complexity	Required time	Current stress	Power coupling	Applicability
PCC [27]	**Low**	Less than half a switching cycle	High	Yes	Medium
LCC [28], [29]	Medium	Less than one switching cycle	**Low**	Yes	**Wide**
ICC [30]	High	**Zero**	**Low**	**No**	Narrow
ICC [31], [32]	**Low**	**Zero**	**Low**	**No**	Narrow
This article	Medium	**Zero**	**Low**	**No**	**Wide**

linear current control [28], respectively. Additionally, Fig. 12(a) includes a comparison of the experimental waveforms without the current optimization method. The experimental conditions were identical for all four control methods, with input port voltage and output port voltage set at 100 and 200 V, respectively. The transferred power was varied from 384 W to 2 kW. The two switching cycles before and after the power mutation are labeled as S1 and S2, respectively. Additionally, S1.5 represents the extra switching cycle inserted by the linear current control. The solid red line in Fig. 12(a) represents the steady-state current waveform of the PCC for the S2 cycle. Fig. 12(b) presents a detailed comparison of the experimental effects. The peak currents after applying the three DCBC elimination methods are −48.6, −48.8, and 54.4 A, while the peak current without current optimization is 88.4 A. It demonstrates that all three methods can effectively decrease current stress levels. Additionally, the current of the MIICC reaches a new steady state immediately, while that of the PCC takes half a switching cycle. Linear current control necessitates a full switching cycle. The input power for MIICC and PCC during S2 are calculated based on the acquisition parameters of oscilloscope, which are 2 and 2.7 kW, respectively. The input power of the linear current control method after power mutation is expressed as the average of the power of S1.5 and S2, which is calculated to be 1.1 kW. The experiments indicate that PCC and linear current control cause errors in the transferred power, while the transferred power of MIICC is mostly accurate. The current control methods discussed in literature [30] and [31] are not included in the comparison because their optimization cannot be applied to the SPS.

Fig. 13 shows the measured efficiency and THD using different dc bias elimination methods over the output power range from 10% to 100% for 600 V. The test results indicate that the THD of the grid current obtained by the PCC exhibits the highest values across the power range. This outcome is attributed to the dc bias elimination is coupled with the power transfer. Comparatively, the efficiency and THD levels of the MIICC and ICC show minimal disparity when the power is below 4 kW. As the power output surpasses 4 kW but remains under 8 kW, the THD of ICC slightly outperforms that of MIICC, while MIICC demonstrates slightly superior efficiency. This discrepancy arises from MIICC's capability to achieve ZVS turn-ON for all power devices during heavy-load conditions, whereas ICC can only enable ZVS turn-ON for some devices, with the remainder operating under ZCS turn-ON. Upon exceeding 8 kW power output, the THD of the grid current in ICC experiences a sudden increase, which is due to the fact that the transfer power demand exceeds the power limit of the method, resulting in severe distortion of the grid current. Furthermore, because the ICC limits the power transfer capacity of the converter, the output voltage cannot reach the set value under the constant resistance load condition, so this part of the efficiency data is discarded.

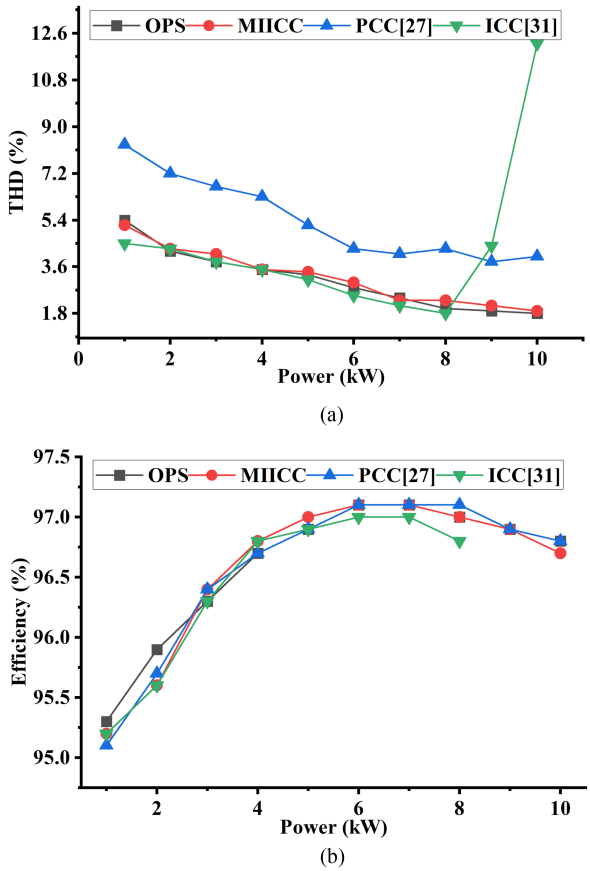

Fig. 13. Comparison of experimental results using different optimization methods at $u_{dc} = 600$ V. (a) THD of grid current with different methods. (b) Efficiency of experimental prototype with different methods.

The experiments demonstrate that MIICC has an excellent DCBC elimination effect comparable to that of the traditional method. Compared with PCC and linear current control method, MIICC can achieve the advantages of a smaller number of switching actions and higher power transfer accuracy. Furthermore, the use of MIICC can eliminate the current optimization process, reducing it from one full switching cycle [28] or half a switching cycle [27] to zero transient time. Comparing MIICC with ICC [13], [31], [32] and UCM [30], MIICC has an advantage in the SPS because it can work over the full power range. A more comprehensive comparison based on experimental phenomena is given in Table V.

VIII. Conclusion

This article introduces a method for optimizing the initial inductor current of the DAB 1P1S ac–dc converter with the objective of eliminating DCBC. The method introduces a control degree of freedom, designated as D_{cm}, which is independent of power control. This control degree of freedom is then used to establish a correlation with the initial current and to regulate the initial current by varying D_{cm}. The initial current control is decoupled from the power control in this manner, thus resolving the defect of the previous method that could not operate in the full power range. In addition, the influence of nonideal parameters, including dead time and port ripple voltage resulting from line resistance and filter capacitor, on practical DAB 1S ac–dc converters is analyzed, and corresponding compensation methods are proposed. Moreover, this study examines the influence of MIICC on the number of switching actions, transferred power, and port ripple current of OPS modulation under diverse operational conditions. The results indicate that MIICC is an effective means of eliminating the DCBC. The study validates the efficacy of the method through a series of experimental tests.

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