Modified Harmonic Current Control and Load Range Extension Method for Single-Stage Isolated DCM Boost AC–DC Converter

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***Abstract*—Single-stage discontinuous-conduction mode (DCM) boost ac–dc converters garnered significant attention for their low cost, high efficiency, and reduced bus voltage. However, the harmonic current control performance of the input current of these converters employing traditional schemes can still be improved. In addition, due to the DCM operation of the input inductor currents and the boost power factor correction (PFC) topology, this type of converter has an inherent power limitation. Exceeding the power threshold can lead to the bus voltage dropping below the input voltage, resulting in pronounced distortion in the input current. In this article, a single-stage two-switch ac–dc converter is introduced, and an input current PFC control method with variable feedforward parameter is proposed to suppress the odd harmonic current while facilitating soft-switching operation. Moreover, to address the power limitation of the traditional schemes, a load range extension method is proposed, in which a proper design of the input filter capacitance causes grid-side resonance in *LC* when the power is relatively high, and thus improves the operating load range, preventing the input current distortion due to excessive output power. Finally, a 500-W prototype is built to verify the feasibility and effectiveness of the proposed method.**

***Index Terms*—Interleaved discontinuous-conduction mode (DCM) boost, load range extension, power factor correction (PFC), single-stage ac–dc converter, soft-switching.**

I. Introduction

AS THE power conversion equipment between users and the power grid in applications, such as electric vehicle charging systems, data center power supply systems, energy storage systems, and lighting systems, ac–dc converters have attracted wide attention due to their cost, grid current control performance, and reliability [1], [2], [3], [4]. When high-frequency isolation and specific voltage conversion ratio are required in the application, traditional approaches to address high-frequency isolation and specific voltage conversion requirements typically involve a two-stage architecture, i.e., a single-phase rectifier equipped with power factor correction (PFC) at the front end, followed by an isolated dc–dc converter at the back end [5], [6], [7]. This structure, due to its decoupling power across the stages and allowing for adjustable bus voltage, generally achieves good input current quality, a wide output voltage range, and a wide operating load range [8]. However, the inherent efficiency of the dual-stage scheme is constrained by the two-stage power conversion steps, which require more active and passive power devices and more complex closed-loop control methods, thereby increasing the cost of the system [9]. In addition, the two-stage scheme usually requires the use of bulky electrolytic capacitors on the dc bus to buffer the energy flow between the two stages and decouple the control method of the two stages. However, the volume of the bus capacitors and their lifetime sensitivity to operation temperature will further affect the volume and reliability of the system [10], [11], [12].

Numerous cutting-edge single-stage ac–dc converters have been introduced as innovative alternatives to conventional two-stage solutions, aiming to address their inherent issues. Early iterations of single-stage ac–dc converters, such as boost-forward/-flyback [13], SEPIC [14], and half-bridge [15] types, simplify circuit topology and reduce costs by multiplexing power switches between boost or bridgeless PFC converters and dc–dc converters. These schemes feature the advantages of simple structure, low cost, and easy-implementation control method. However, the design of the magnetic devices in these converters is affected by unidirectional excitation, which limits the volume and power level of these schemes [16], [17]. In addition, achieving soft-switching operation in these configurations is challenging, and the power switches often endure considerable current stress, presenting significant limitations to their overall performance and efficiency.

In recent years, to improve the efficiency of single-stage converters, many researchers have paid attention to the scheme of adopting dc–dc converter, which is easy to realize soft-switching

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operation in back stage [5], [8], [17], [18], [19], [20], [21]. With the application of wide bandgap devices, the single-stage isolated ac–dc scheme, which adopts bidirectional switches in the ac side of the converter to replace the rectifier bridge in the traditional schemes, has gradually become a research hotspot [18], [19], [20]. In [19], a dual-active-bridge ac–dc converter is proposed, and the input current PFC function and zero-voltage switching (ZVS) operation are realized. In [20], a current-fed converter composed of bidirectional switches is adopted on the ac side, which can realize zero-current switching turn-OFF of the ac side and ZVS turn-ON operation of the dc side. The scheme with bidirectional switches does not need a diode bridge or PFC part, but its switches on the ac side operate at high frequency in the corresponding half cycle of the grid voltage, and the number of power switches seems to be not significantly reduced compared with other schemes.

Typically, in order to further reduce the cost and volume of the converter, schemes in which the bridgeless PFC converter with the dc–dc converter are integrated are proposed in [8], [22], [23], [24], and [25]. In [22], the totem-pole PFC converter and half-bridge *LLC* converter are combined for LED lighting applications. Its control method is easy to implement while realizing ZVS operation of the ac-side switches at full-load range. Yi et al. [23] propose a single-stage converter combining interleaved boost PFC and full-bridge *LLC* converter and limit the amplitude of bus voltage through a hybrid pulse frequency modulation (PFM)/pulsewidth modulation (PWM) control method. However, the control performance of input current in these schemes can still be modified. The interleaved totem-pole bridgeless PFC converter has been widely used due to its small size of filter inductor and good harmonic current control performance, and thus, it is integrated with dual-active-bridge (DAB) converter in [8], [24], and [25]. In this type of converter, generally, the six switches on the ac side operate with a duty cycle of 0.5, while an internal phase-shift angle that changes with the phase of the grid voltage is adopted in the modulation of the switches in the dc side and achieves PFC function. In [24], a single-stage ac–dc converter for a solid-state transformer is proposed, and the average current of the switches is minimized by an extended phase-shift control method to optimize the operation efficiency. In [8], the soft-switching operation in a wide load range is achieved by the proposed control method and the design of input inductance, and there is no zero-crossing current spike at the ac side of the converter by making the inductance current operate in continuous-conduction mode (CCM). Zhang et al. [25] proposed a structure without boost inductors, which further reduces the cost and volume of the converter. However, to achieve dc output voltage control and input current control, the corresponding control and modulation methods in this type of converter are relatively complex, and the phase-shifting schemes may cause loss of soft switching. At the same time, as the duty cycle of the switches on the ac side is fixed at 0.5, the maximum voltage stress of these switches is about twice the peak value of the grid voltage, which brings great restrictions to the selection of power devices, and thus, this type of converter is suitable for the applications with grid voltage limitation.

The discontinuous-conduction mode (DCM) boost single-stage ac–dc converter with two-phase interleaved has received widespread attention from researchers, featuring reduced bus voltage [17], [26], [27], [28]. These converters reduce the peak bus voltage by using two series-connected capacitors to divide the input voltage at the grid side or after the rectifier bridge so that the input voltage of the PFC is only half of the grid voltage [17]. Sadilek et al. [26] propose a two-switch single-stage ac–dc converter suitable for aviation applications and propose a control method with PFM and PWM to reduce the input harmonic current. In [27], a three-level TAIPEI rectifier is proposed, which reduces the voltage stress of the switches, and is beneficial for reducing the switching frequency range and improving operation efficiency at light load. However, these schemes are still nonisolated converters, in which soft-switching operation cannot be achieved over the full-load range, and additional control methods, such as PWM mode, are required. A series of topology schemes, including a DCM boost single-stage isolated ac–dc converter, as well as input current PFC performance, soft-switching operation, and resonant parameter design analysis, are derived in [17]. Lu et al. [28] further propose a scheme for integrated DCM boost PFC and *LLC* circuit, making the converter more suitable for applications with high grid voltage. However, in these schemes, the input current control performance can still be improved, and at the same time, this type of single-phase ac–dc converter generally has a maximum limitation on the output power. When the converter exceeds the power limitation, the operation mode of the input inductor current may change from DCM to CCM and the bus voltage will be lower than the input voltage, similar to the overmodulation problem of the boost PFC circuits, causing current distortion or even significant current overshoot, while making it difficult to maintain a stable output voltage. However, it is necessary to consider the working condition of the short-term overload of the system, which limits the application of this type of converter in a larger power-level range. With the traditional schemes, changing the circuit parameters, such as the input filter inductance, to avoid input current distortion caused by high power is required while resulting in the increasing of current harmonics and the bus voltage, i.e., the voltage stress of the switches.

To tackle the aforementioned problems, this article introduces a DCM boost single-stage isolated ac–dc converter, which advances a PFC control strategy featuring an adjustable feedforward parameter, alongside a method for extending the load range. With the converter's variable frequency control loop, the amplitude of the feedforward component is dynamically adjusted based on the value of the third-order harmonic current component, which is derived using a second-order generalized integrator (SOGI) at three times the gird frequency, effectively mitigating odd harmonics in the input current. Moreover, to overcome the load range limitations characteristic of traditional designs, a load range extension method that involves meticulous design of the input filter capacitance to make grid-side *LC* resonance at high power is proposed, avoiding current distortion. Finally, the feasibility and effectiveness of the proposed scheme are verified by experimental results in a 500-W prototype.

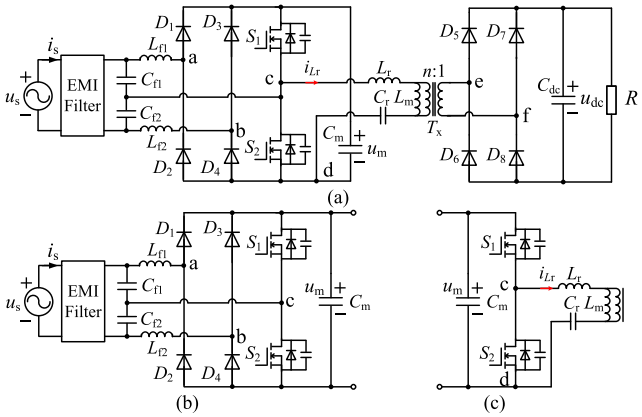

Fig. 1. Topology of the adopted single-stage isolated AC–DC converter and the topology breakdown of the ac part. (a) Adopted converter. (b) PFC part. (c) Primary side of the *LLC* circuit.

The rest of this article is organized as follows. In Section II, the topology and operation principle of the single-stage ac–dc converter with load range extendibility are described and clarified in detail. Section III shows the proposed control structure. In Section IV, the experimental results and analysis of the 500-W prototype are presented and discussed. Finally, Section V concludes this article.

II. Topology and Operation Principle

A. Structure of the Introduced AC–DC Converter

The topology of the single-stage isolated ac–dc converter adopted in this article is shown in Fig. 1(a), in which u_s and i_s represent the single-phase grid voltage and input current, respectively, and $u_{\rm dc}$ is the dc output voltage. The ac part of the converter consists of the PFC part and the half-bridge part of the *LLC* primary side, as shown in Fig. 1(b) and (c). The ac part includes the input filter inductors L_{f1} and L_{f2}, filter capacitors C_{f1} and C_{f2}, diodes D_1–D_4, power switches S_1 and S_2, bus capacitor C_m, and a resonant circuit composed of resonant inductor L_r, resonant capacitor C_r, and high-frequency transformer T_x excitation inductor L_m. The transformer ratio is n: 1. The dc side of the converter consists of diodes D_5–D_8, dc output capacitor $C_{\rm dc}$, and load R.

When the converter is operating under single-phase power grid input, the voltage on the filter capacitors C_{f1} and C_{f2} is about half of the instantaneous value of the grid voltage u_s. With the high-frequency switching of S_1 and S_2 and the diode bridge on the ac side, a pulsating voltage that changes with the grid voltage can be obtained on the input filter inductors L_{f1} and L_{f2}; thereby, the input current will change with the grid voltage, achieving input current PFC function. The ac-side diode bridge is adopted to converter grid voltage u_s to dc voltage u_m on C_m. Meanwhile, an *LLC* circuit is composed of S_1 and S_2, C_r, L_r, T_x, and the secondary diode bridge. The output voltage $u_{\rm dc}$ can track the dc voltage reference $u_{\rm dcref}$ with PFM, thereby achieving single-phase single-stage ac–dc conversion with galvanic isolation.

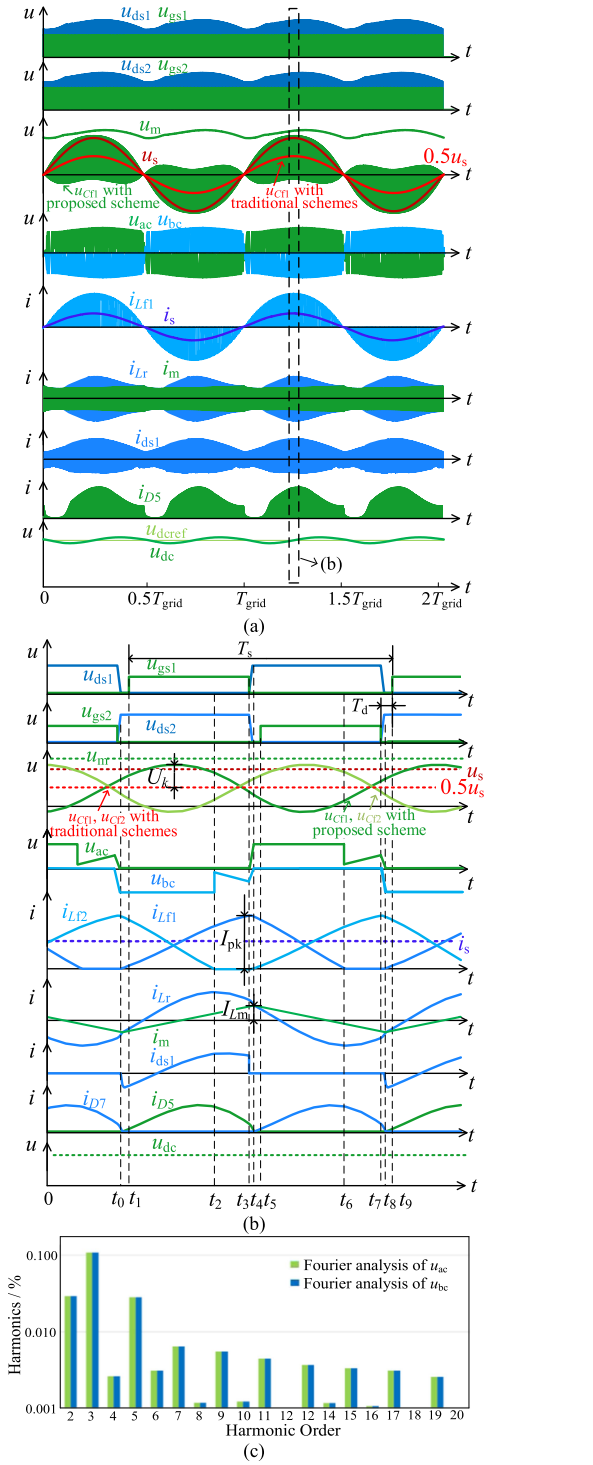

Fig. 2. Typical operation waveforms. (a) Operation waveforms under grid voltage cycle. (b) Operation waveforms under switching cycle when $u_s = U_s$. (c) Fourier analysis of u_{ab} and u_{bc}.

B. Operation Principle of the Converter

The operation waveforms of the adopted converter under the grid voltage cycle $T_{\rm grid}$ are shown in Fig. 2(a). The waveforms under the switching cycle T_s when $u_s = U_s$ are shown in Fig. 2(b), where the duty cycles of S_1 and S_2 are both 50% and f_s is the resonant frequency. Fig. 2(c) illustrates the Fourier

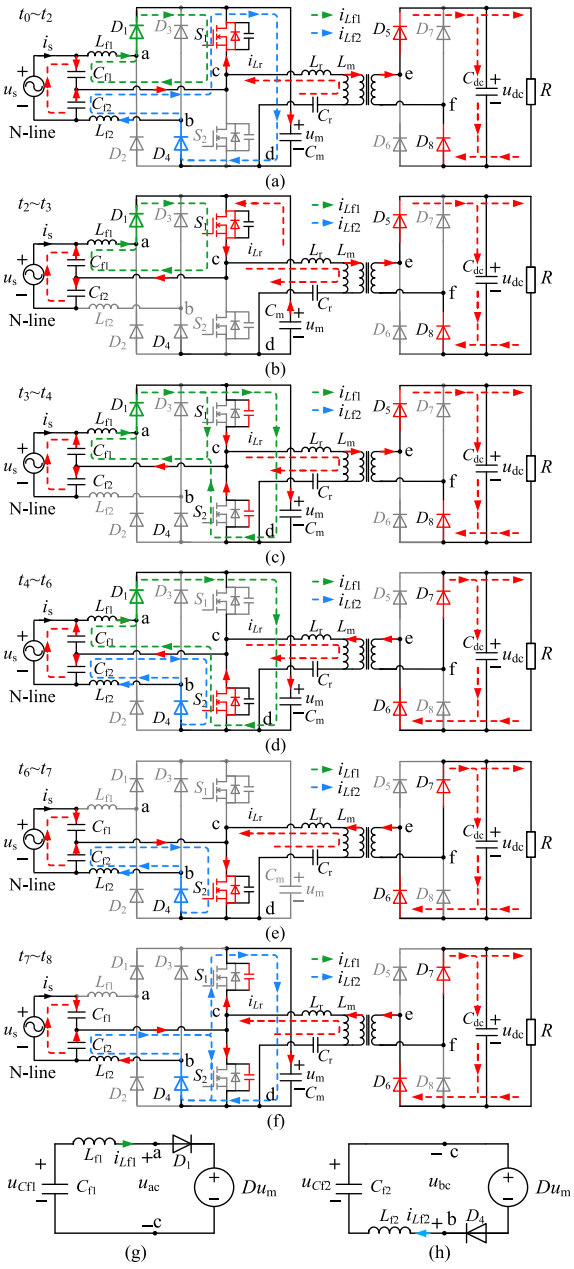

Fig. 3. Operation modes of the single-stage AC–DC converter with the time of (a) $[t_0 \sim t_2]$, (b) $[t_2 \sim t_3]$, (c) $[t_3 \sim t_4]$, (d) $[t_4 \sim t_6]$, (e) $[t_6 \sim t_7]$, (f) $[t_7 \sim t_8]$, (g) equivalent circuit of i_{Lf1} when $u_g > 0$, and (h) equivalent circuit of i_{Lf2} when $u_g > 0$.

analysis of the pulsating voltages u_{ab} and u_{bc}, in which except the second-order voltage ripple from the bus voltage, odd harmonics account for the majority. The corresponding operation modes and the equivalent circuits of the filter inductor currents i_{Lf1} and i_{Lf2} of the converter when $u_s > 0$ are presented in Fig. 3, where T_d is the deadtime added in the modulation part of the converter. In traditional schemes of the DCM boost ac–dc converters, the capacitance of C_f is relatively large, and thus, it is considered that the voltage of C_f remains unchanged within one switching cycle. Therefore, it can be obtained that $u_{Cf1} = u_{Cf2} \approx 0.5u_s$. The detailed working principles are as follows.

$[t_0 \sim t_2]$: With the turn-OFF of S_2, the diode of S_1 is conducted for freewheeling. As the gate-drive signal of S_1, u_{gs1}, changes to positive, both the inductor current i_{Lf2} and the resonant current i_{Lr} provide the reverse current, thereby achieving ZVS turn-ON of S_1. In the grid-side diode bridge, D_1 conducts, and the input filter capacitor C_{f1} charges L_{f1} forward through D_1 and S_1, resulting in an increase in i_{Lf1}, while L_{f2} discharges to the bus capacitor C_m through C_{f2}, D_4, and S_1, and the i_{Lf2} gradually decreases to 0. At this point, the voltage between points c and d is equal to the bus voltage u_m.

$[t_2 \sim t_3]$: i_{Lf1} is charged forward to the peak current $I_{\rm pk}$, while i_{Lf2} is zero; therefore, D_4 is turned OFF. The power grid and C_m discharge to the resonant circuit through the grid-side diode bridge and S_1. D_5 in the secondary side conducts, converting power from the primary side to the secondary side.

$[t_3 \sim t_4]$: i_{Lf1} and i_{Lr} are both positive, causing the drain–source voltage of S_1, $u_{\rm ds1}$, to rise to u_m, while the drain–source voltage of S_2, $u_{\rm ds2}$, drops to 0. During this process, when $u_{\rm ds2}$ is less than u_{Cf2}, D_4 withstands a reverse voltage and conducts, and i_{Lf2} increases in reverse. The excitation inductor L_m is still clamped, and the excitation current gradually decreases from the peak I_{Lm}.

The following operation modes are similar to the previous ones.

It is noted that during the operation of the converter, the operation mode of the input inductor current is DCM, and both the inductor currents and the resonant current can provide the reverse current for the ZVS operation of S_1 and S_2. Due to the symmetry of the converter topology, the filter inductance and the filter capacitance at the grid side can be designed in the same value, i.e., $L_{f1} = L_{f2} = L_f$ and $C_{f1} = C_{f2} = C_f$. According to Figs. 2 and 3, the voltage equation of the grid side is given as follows:

$$\begin{cases} u_{Cf1} = L_{f1}\frac{di_{Lf1}}{dt}, & t_0 < t < t_3 \\ u_{Cf1} = L_{f1}\frac{di_{Lf1}}{dt} + u_m, & t_4 < t < t_6 \\ 0 = L_{f1}\frac{di_{Lf1}}{dt}, & t_6 < t < t_7. \end{cases} \tag{1}$$

With the traditional schemes of the DCM boost ac–dc converters, $u_{Cf1} = u_{Cf2} \approx 0.5u_s$. After substituting this in (1), the expression of i_{Lf1} can be deduced as follows:

$$\begin{cases} i_{Lf1} = \frac{u_s}{2L_f}t, & t_0 < t < t_3 \\ i_{Lf1} = \frac{2u_m - u_s}{2L_f}\left(\frac{T_s}{2} + T_{\rm down} - t\right), & t_4 < t < t_6 \\ i_{Lf1} = 0, & t_6 < t < t_7 \end{cases} \tag{2}$$

where $T_{\rm down}$ is the falling time of i_{Lf1} from $I_{\rm pk}$ to 0. During the switching process of the switches, it follows that

$$2C_{\rm ds}\frac{du_{\rm ds}}{dt} = 2C_{\rm ds}\frac{u_m}{t_4 - t_3} = i_{Lf1} + i_{Lf2} + i_{Lr} \approx I_{\rm pk} + I_{Lm} \tag{3}$$

where $C_{\rm ds}$ is the drain–source parasitic capacitance of S_1 and S_2. It is worth noting that due to $C_{\rm ds}$ being relatively small, the turn-ON or turn-OFF time of the switches is ignored in the analysis, and the duration from t_0 to t_3 can be considered as $0.5T_s$. Therefore, it can be obtained that

$$I_{\rm pk} = \frac{u_s}{2L_f}(t_3 - t_0) = \frac{T_s u_s}{4L_f}. \tag{4}$$

According to (2), it follows that $i_{Lf1} = I_{\rm pk}$ when $t = t_4$, and $i_{Lf1} = 0$ when $t = t_6$, it can be deduced that

$$T_{\rm down} = t_6 - t_4 = \frac{u_s T_s}{4u_m - 2u_s}. \tag{5}$$

To further simplify the theoretical analysis, it can be approximately considered that the ripple component of the input filter inductor current is fully absorbed by the filter capacitor, so the average value of the input current and the filter inductor current i_{Lf1} in one switching cycle is equal, and thus, it follows that

$$i_s = \frac{1}{T_s}\int_0^{T_s} i_{Lf1}(t)dt = \frac{T_s}{16L_f}\cdot\frac{2u_m u_s}{2u_m - u_s}. \tag{6}$$

With the traditional variable frequency control method, the bandwidth of the dc voltage loop is relatively low, and the variation of the switching frequency in one grid voltage cycle can be ignored. According to (6), it can be obtained that

$$P_{\rm in} = 2\int_0^{0.5T_{\rm grid}} u_s i_s dt = \frac{T_s U_s^2}{8L_f}\int_0^{0.5T_{\rm grid}} \frac{a\sin^2\omega t}{a - \sin\omega t}dt \tag{7}$$

where $a = 2u_m/U_s$, U_s and ω are the amplitude and angular frequency of the grid voltage, respectively. Due to the limitation of the converter topology, $u_m > U_s$, and thus, $a > 2$. According to the authors in [29] and [30], the expression of input power can be approximately obtained as $P_{\rm in} = 0.06T_s{U_s}^2/[(a-0.92)L_f]$. Thus, the expression of bus voltage u_m can be derived as follows:

$$u_m = \frac{0.03T_s U_s^3}{L_f P_{\rm in}} + 0.46U_s. \tag{8}$$

When the operation loss of the converter is ignored, it can be obtained that $P_{\rm in} = P_{\rm out} = {u_{\rm dc}}^2/R$. Considering the voltage gain $M_{\rm dc}$ of the *LLC* circuit in the converter, it can be deduced that

$$u_m = \frac{u_{\rm dc}}{M_{\rm dc}} = \frac{2\sqrt{\left[1 + \frac{1}{K}\left(1 - \frac{f_r}{{f_s}^2}\right)\right]^2 + Q^2\left(\frac{f_s}{f_r} - \frac{f_r}{f_s}\right)^2}u_{\rm dc}}{n} \tag{9}$$

where Q and K are the quality factor and inductance ratio of the *LLC* circuit, respectively, and it follows that $Q = (L_r/C_r)^{1/2}/R_{\rm eq}$ and $K = L_m/L_r$. In addition, f_r is the resonant frequency of L_r and C_r, and $R_{\rm eq}$ is the equivalent load in the *LLC* output side, and it satisfies that $f_r = 1/[2\pi(L_r C_r)^{1/2}]$ and $R_{\rm eq} = 8n^2R/\pi^2$. By adopting the output voltage closed loop in the control method of the converter, $u_{\rm dc}$ will track the reference $u_{\rm dcref}$ with no static error. Therefore, the steady-state operating points of the converter at different powers can be obtained from (8) and (9), as shown in Fig. 4. The blue and green lines correspond to the curves obtained from (8) and (9), respectively, of which the colors change from light to dark corresponding to an increase in Q of the *LLC* circuit, i.e., an increase in the input power. It can be seen that, with the increase of the input power $P_{\rm in}$, the bus voltage u_m of the converter will decrease in the steady state, and the switching frequency f_s will also decrease. At the same time, the changing trend is relatively mild with low operating power and high switching frequency, while near the resonant frequency, the changing trend of the operating point with $P_{\rm in}$ is relatively rapid, while at the operating point with high power and low switching frequency, the trend will tend to ease. The operating

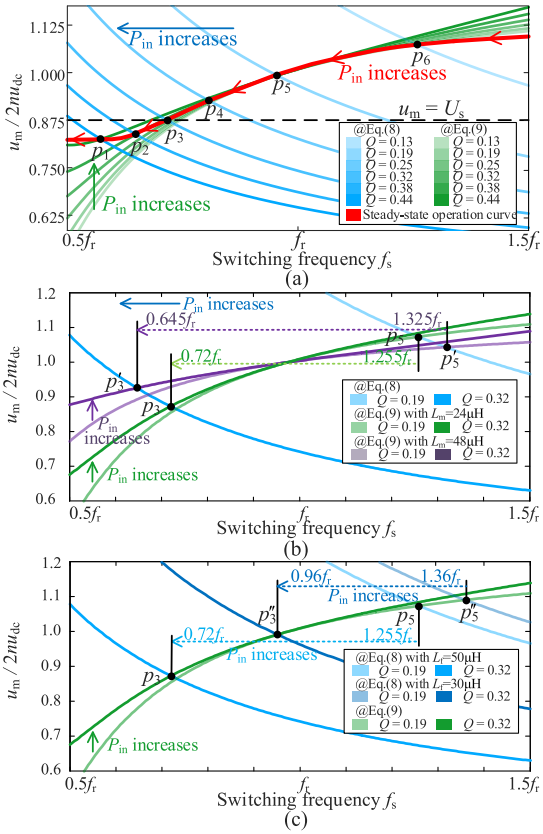

Fig. 4. Steady-state operating points of the converter. (a) With rated circuit parameters. (b) With different L_m. (c) With different L_f.

points of the converter with different L_m can be obtained, as shown in Fig. 4(b), which shows that with a high power, the larger the value of L_m, the lower the switching frequency, and u_m is higher. Fig. 4(c) presents the operating points with different L_f, and it can be found that as L_f decreases, the operating point at the same power level will move toward the upper right, i.e., f_s increases and u_m rises. Therefore, when using the traditional method in the adopted converter, it is necessary to increase the bus voltage u_m at the same operating power by changing the circuit parameters, such as L_m or L_f to avoid input current distortion caused by high power.

However, it is worth noting that the grid side of the converter is a DCM boost-type circuit, which generally needs to meet the requirement that u_m is not less than U_s. The operation power limitation of the converter can be obtained by substituting $u_m \geq U_s$ to (7) as follows:

$$P_{\rm in} \leq \frac{T_s U_s^2}{18L_f}. \tag{10}$$

When $P_{\rm in} = {T_s U_s}^2/(18L_f)$, it corresponds to the static operating point p_3 in Fig. 4, and $u_m = U_s$. If $P_{\rm in}$ further increases, the rms value of the input current will increase and the peak value of the filter inductor current $I_{\rm pk}$ will also increase. Meanwhile, the instantaneous value of the bus voltage u_m will be lower than the grid voltage u_s, and the switching of S_1 and S_2 cannot control the waveform of the input current, which is similar to the

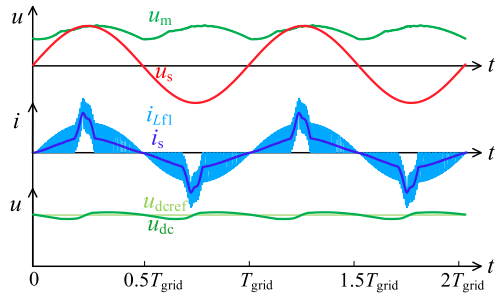

Fig. 5. Operation waveforms of the traditional single-stage DCM boost AC–DC converter when it exceeds the operation load range.

overmodulation in the PFC circuit, resulting in the distortion of the input current, and the operation mode of the filter inductor current will change from DCM to CCM at the peak of the input current waveform. The corresponding operation waveforms are shown in Fig. 5. It can be seen that the load range limitation will not only affect the input current control performance and increase the input current harmonics but also may cause the overcurrent damage to the switches due to serious distortion of the current waveform.

C. Load Range Extension With Design of Input Capacitor

The load range limitation of the converter will make the circuit design and component parameter design more complex, and affect the reliability of the system. Moreover, as shown in Fig. 4(a), with the increase of P_{in}, the switching frequency decreases, which will also bring difficulties to the design of the high-frequency transformer. Therefore, it is necessary to extend the operating load range of the converter. According to (1), (4), and (7), under the same switching frequency and input and output voltages, to expand the operating load range, it is necessary to increase I_{pk} when $u_m = U_s$. Therefore, it demands either reducing the input filter inductance of the inductance L_{f1} or increasing the voltage of the filter capacitor u_{Cf1} during t_0–t_3. However, a small input filter inductance is prone to cause the increase of ripple current and harmonic current components, which not only affects the operation efficiency but also affects the steady-state current control performance. Therefore, in the proposed scheme, the voltage of the filter capacitor u_{Cf1} during t_0–t_3 is increased by reducing the filter capacitance C_{f1} to make grid-side LC resonance at high power and increase I_{pk} while i_{Lf1} maintains DCM, thus avoiding the distortion of the input current of the converter caused by high power, and extending the operation load range of the converter.

During t_0–t_2, integrating both sides of (1), it follows that

$$\int_{t_0}^{t_3} u_{Cf1}dt = L_f i_{Lf1}\big|_{t_0}^{t_3} = L_f I_{\text{pk}}. \tag{11}$$

According to Kirchhoff's current law, the current of the filter capacitor C_{f1}, i_{Cf1}, can be deduced as follows:

$$i_{Cf1} = C_{f1}\frac{du_{Cf1}}{dt} = i_{Lf1} - i_s. \tag{12}$$

It can be seen from Fig. 2(b) that the high-frequency ripple component of the filter capacitor voltage u_{Cf1} is the voltage ripple at the switching frequency. Therefore, similar to the fundamental equivalence analysis of the LLC converter, u_{Cf1} can be expressed as follows:

$$u_{Cf1} = \frac{u_s}{2} + U_k \sin\theta \tag{13}$$

where U_k is the amplitude of the high-frequency ripple component of u_{Cf1}, and θ is the phase of the ripple component. From Fig. 2(a), it can be approximated that $\theta = 2\pi f_s(t-t_0)$. After substituting (13) into (11), when $u_s = U_s$, it can be obtained that

$$I_{\text{pk}} = \frac{T_s U_s}{4L_f} + \frac{T_s U_k}{\pi L_f}. \tag{14}$$

Due to the grid-side LC resonance, the voltage of C_{f1} is greater than $0.5U_s$ in the increasing process of the filter inductor current from t_0 to t_3. Therefore, comparing (4) and (14), it can be seen that $T_s U_k/\pi L_f$ is added to the peak current expression with the traditional scheme, and its size is proportional to U_k. Considering the situation when the filter inductor current is operating in critical-conduction mode, it can be obtained that $t_6 - t_4 = T_s/2$. By integrating both sides of (1), it follows that

$$\begin{aligned}\int_{t_4}^{t_6} u_{Cf1}dt &= \frac{T_s}{2\pi}\int_{\pi}^{2\pi}\left(\frac{u_m}{2} + U_k\sin\theta\right)d\theta \\ &= -L_f I_{\text{pk}} + \frac{T_s}{2}u_m.\end{aligned} \tag{15}$$

As $i_{Cf1} = C_f du_{Cf1}/dt$, during the process of C_{f1} charged from $0.5u_s$ to $(0.5u_s + U_k)$, it can be deduced that

$$U_k = \frac{1}{2C_f}\int_0^{\frac{T_s}{4}} i_{Cf1}dt \approx \frac{T_s}{4\pi C_f}\int_0^{\frac{\pi}{2}}\frac{I_{\text{pk}}}{2}\cos\theta d\theta = \frac{T_s I_{\text{pk}}}{4\pi C_f}. \tag{16}$$

By combining (15) and (16), the expression of I_{pk} can be derived as

$$I_{\text{pk}} = \frac{\pi^2 T_s C_f U_s}{4\pi^2 L_f C_f - T_s^2}. \tag{17}$$

It can be seen that when I_{pk} approaches infinity, it follows that

$$2\pi\sqrt{L_f C_f} = T_s. \tag{18}$$

According to (17) and (18), the relationship between I_{pk} and the input filter capacitor C_f, filter inductor L_f, and switching frequency f_s can be obtained, as shown in Fig. 6. It can be seen that, within the traditional selection range of filter capacitors and inductors [17], [26], [27], [28], C_f is relatively large. With the decrease of L_f, the maximum current ripple I_{pk} of the converter at the critical operation condition will increase linearly and slowly. When C_f decreases to around 0.1 μF, the resonant frequency of L_f and C_f gradually approaches the switching frequency. At this time, with the decrease of L_f, I_{pk} increases significantly, and so does the corresponding maximum operation power of the converter. In addition, with the decrease of the switching frequency, I_{pk} also increases. It can be seen that the operation load range of the converter can be extended by the design of the filter capacitance through LC resonance at the grid side, thereby reducing the nonlinear distortion of the input current at high

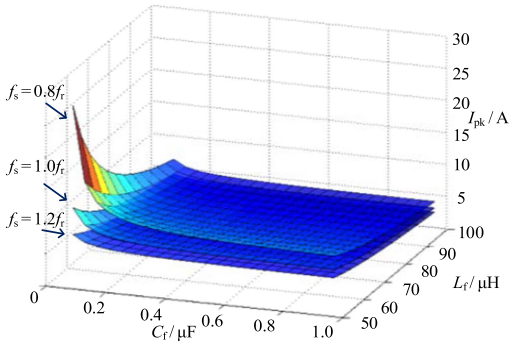

Fig. 6. Relationship between $I_{\rm pk}$, the input filter capacitor C_f, input filter inductor L_f, and switching frequency f_s.

power. Meanwhile, with the proposed scheme, the inductor current waveform is nonlinear compared to that with the traditional scheme, which is beneficial for reducing the conduction loss of the power switches and improving the efficiency of the converter.

The expression for the maximum peak voltage stress of the filter capacitor $U_{Cf\rm pk}$ can be derived from (14) as

$$U_{Cf\rm pk} = \frac{U_s}{2} + U_k = \frac{2-\pi}{4}U_{\rm s} + \frac{\pi L_f I_{\rm pk}}{T_s}. \tag{19}$$

It can be seen that with the increase of $I_{\rm pk}$ and operation power, and the decrease of C_f, the voltage stress $U_{Cf\rm pk}$ of the filter capacitor will be higher. Therefore, a boundary condition $U_{Cf\rm pk} \le U_s$, i.e., $U_k \le 0.5U_s$ is selected in this article, and it is obvious that the converter still needs to meet the following requirement:

$$I_{\rm pk} \le \frac{(2+\pi)T_s}{4\pi L_f}U_s. \tag{20}$$

Meanwhile, considering the circuit component parameter variation caused by operating conditions, such as temperature, it is necessary to further leave margin for the selection of C_f and L_f. In this article, the resonant frequency of C_f and L_f is selected as $0.65f_r$. Meanwhile, as shown in Fig. 6, this selection can ensure that under a light-load operation, it will not cause grid-side *LC* resonance due to the increase of the switching frequency in the *LLC* circuit. Therefore, the operating point with the proposed scheme under a light load is basically the same as traditional schemes. In addition, the minimum switching frequency needs to be set to limit the current stress of the transformer and resonant circuit. As shown in Fig. 6, under the same switching frequency and L_f, $I_{\rm pk}$ increases with the decrease of C_f. Therefore, it is noted that, under the full load, the smaller the filter capacitance, the higher the switching frequency of the converter in the steady state will be. The selection of filter capacitance not only helps to expand the operating load range but also facilitates the design of the converter.

III. Analysis of the Control Structure

A. PFC Realization of the Converter

Assuming that the grid voltage u_s is an ideal sinewave, i.e., $u_s = U_s\sin\omega t$. Similar to (6), the expression of the input current

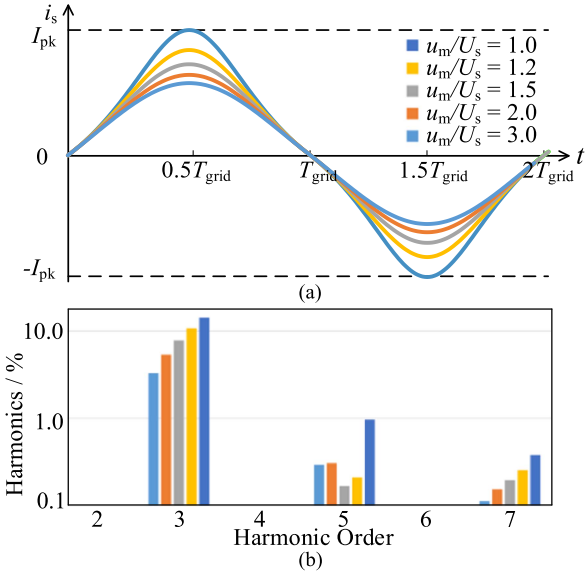

Fig. 7. Relationship between the input current i_s and u_m/U_s. (a) Input current waveforms. (b) Fourier analysis of the input current.

i_s can be derived as

$$i_s = \frac{u_m U_s T_s \sin\omega t}{16L_f u_m - 8L_f U_s|\sin\omega t|} = \frac{U_s\sin\omega t}{16L_f}\cdot\frac{T_s}{1-\frac{U_s|\sin\omega t|}{2u_m}}$$
$$= \frac{U_s\sin\omega t}{16L_f}\cdot\frac{T_s}{1-\frac{nU_s|\sin\omega t|}{4u_{\rm dc}\sqrt{\left[1+\frac{1}{K}\left(1-\frac{f_r}{f_s}^2\right)\right]^2+Q^2\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)^2}}}. \tag{21}$$

From (21), the relationship between the input current i_s and u_m/U_s can be obtained, as shown in Fig. 7. As u_m/U_s decreases, i.e., the input power increases, the distorted components of the input current rise, while the third-order component has the highest proportion of the input current harmonics. It can be seen from (21) that, to suppress the harmonic current, the ripple component of the switching frequency f_s should be proportional to $1/(1-|u_s|/2u_m)$. Taking the current waveform when $u_m/U_s = 1$ in Fig. 7(a) as an example, at the peak of the input current waveform, f_s should be increased, while near the zero-crossing points, f_s should be reduced to suppress the harmonic current. According to (10), the higher the f_s at the peak of the input current cycle, the lower the power limitation of the converter is. Therefore, the proposed load range extension method is suitable to be adopted in combination with the current control method and applied over a wider load range.

If the power loss of the converter is ignored, that is, $P_{\rm in} = U_s i_{sd}/2 = P_{\rm out}$, where i_{sd} is the *d*-axis component in the *d–q* rotation coordinate system of the input current obtained by second-order generalized integral phase-locked loop (SOGI-PLL) [31], [32]. It can be derived that

$$R_{\rm eq} = \frac{8n^2}{\pi^2}R = \frac{4n^2U_s i_{sd}}{\pi^2 u_{\rm dc}^2}. \tag{22}$$

Then, the value of Q can be obtained as

$$Q = \frac{1}{R_{\rm eq}}\sqrt{\frac{L_r}{C_r}} = \frac{\pi^2 u_{\rm dc}^2}{8\pi n^2 f_r C_r U_s i_{sd}}. \tag{23}$$

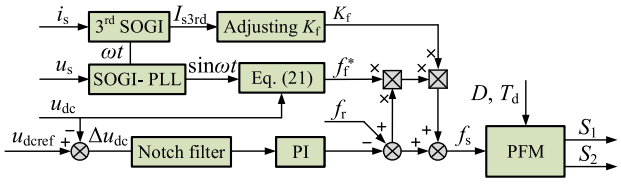

Fig. 8. Block diagram of the proposed control method.

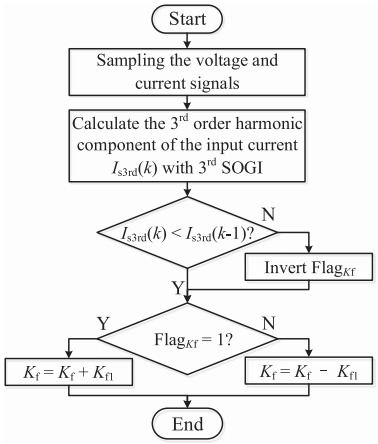

Fig. 9. Flowchart of the adjusting process of K_f.

It can be seen that both Q and K in (21) are related to the resonant parameters of the converter, while different operation temperatures, powers, and manufacturing processes will cause parameter mismatches, thereby affecting the control performance. In addition, the calculation of the corresponding feedforward parameters in (21) is relatively complex, which will bring a computation burden to the control loop. Therefore, this article adopts a variable frequency control method with an adjustable feedforward parameter K_f. The control block diagram is shown in Fig. 8. A notch filter and a proportional-integral (PI) controller are adopted in the dc voltage control loop to make the output voltage $u_{\rm dc}$ track the reference value $u_{\rm dcref}$ with no steady-state error while filtering out the harmonic component twice the grid frequency in $u_{\rm dc}$ of the single-phase charging system, avoiding its impact on the input current control performance. In the input current control loop, a third-order SOGI is used to calculate the third-order harmonic component of the input current and adjust the feedforward parameter K_f, thereby reducing the inherent odd harmonic components of the input current, improving the power quality at the grid side. f_f^* is the per-unit feedforward value by f_r, calculated through (21), and f_f is the feedforward component of the switching frequency f_s.

The adjusting process of K_f is shown in Fig. 9, which is similar to the maximum power point tracking method for solar applications. The initial value of K_f is set as 0, and K_{f1} is the step size, while Flag$_{Kf}$ is the perturbing direction. The amplitude of the third-order harmonic component of the input current is obtained by the third-order SOGI, while $I_{s3\rm rd}(k-1)$ and $I_{s3\rm rd}(k)$ represent its values at the $(k-1)$th and kth sampling time, respectively. If the variation is positive, then a step size of K_{f1} is moved in the same direction; otherwise, the perturbing direction will be changed. Finally, the feedforward component obtained from the current loop is added with the resonant frequency f_r and the voltage loop output to obtain the switching frequency f_s of the converter. The switching signals of S_1 and S_2 are generated through the PFM part.

However, (21) cannot represent the input current when using the proposed scheme with a small C_f. To obtain the expression of i_s, first, it is required to solve $T_{\rm down}$. According to (1), it can be derived that

$$\int_{t_4}^{t_6} u_{Cf1}dt = L_f i_{Lf1}\Big|_{t_4}^{t_6} + t_{\rm down}u_m = -L_f I_{\rm pk} + t_{\rm down}u_m. \tag{24}$$

Based on the analysis above, it is assumed that $u_{Cf} \approx u_s/2 + U_k\sin\theta$. Substituting it into (24), it follows that

$$\left(u_m - \frac{u_s}{2}\right)T_{\rm down} + \frac{T_s U_k}{2\pi}\left(1 - \cos\frac{2\pi T_{\rm down}}{T_s}\right) = L_f I_{\rm pk}. \tag{25}$$

Considering that $0 < T_{\rm down} < 0.5T_s$, and the cosine term in (25), i.e., $[1-\cos(2\pi T_{\rm down}/T_s)]$, has a positive value, it can be obtained that

$$T_{\rm down} = \frac{2K_T L_f I_{\rm pk}}{2u_m - u_s} \tag{26}$$

where K_T is a coefficient that is less than or equal to 1, and apparently, its value reduces with the decrease of C_f. It also decreases with the increase of the operating power. At light load and half load, due to the small U_k in u_{Cf}, K_T is close to 1. According to (14) and (16), $I_{\rm pk}$ can be obtained as follows:

$$I_{\rm pk} = \frac{T_s U_s}{4L_f}\cdot\frac{1}{1 - T_s^2/4\pi^2 L_f C_f} = \frac{T_s U_s}{4AL_f} \tag{27}$$

where A is a proportional coefficient, i.e., $1-T_s^2/(4\pi^2 L_f C_f)$, and i_s can be obtained by (26) and (27), which is shown as follows:

$$i_s = \frac{1}{T_s}\int_0^{T_s} i_{Lf1}(t)dt = \frac{T_s}{16L_f}\cdot\frac{[2u_m A + (K_T - A)u_s]u_s}{(2u_m - u_s)A^2}. \tag{28}$$

Due to the inclusion of T_s in A, A will decrease with the increase of the operating power. The resonant frequency of C_f and L_f is selected as $0.65f_r$, so A is also close to 1 at light load and half load. Therefore, it can be seen that, when adopting the proposed scheme, $(K_T - A)$ approaches 0 in most operating power ranges, and (28) can be further simplified as

$$i_s = \frac{T_s}{16L_f}\cdot\frac{2u_m u_s}{(2u_m - u_s)A}. \tag{29}$$

It is noted that the expression of i_s at this time differs by a coefficient A from (21). The above calculation process adopts certain equivalent calculations. Meanwhile, (21) uses fundamental analysis to calculate the voltage gain of the *LLC* circuit, which is more accurate only when f_s is near f_r. Therefore, in the proposed control scheme, the amplitude of the feedforward component is adjusted by $I_{s3\rm rd}$ to optimize the harmonic suppression performance.

The simulation results of adjusting K_f are shown in Fig. 10. It can be seen that a very small K_{f1} is selected to avoid significant overshoot in the transient process of decreasing the amplitude

TABLE I
COMPARISON BETWEEN THE TRADITIONAL SINGLE-STAGE AC–DC CONVERTERS WITH THE INTRODUCED CONVERTER

Aspects \ Schemes	[9]	[26]	[27]	[34]	[35]	[17]	[28]	Proposed Scheme
Topology type	CCM Boost PFC, DAB	DCM Boost PFC	DCM Boost PFC	DCM/CCM Sepic/Cuk PFC	DCM/BCM Boost PFC, *LLC*	DCM/BCM Boost/ Buck–Boost PFC, *LLC*	DCM Boost PFC, *LLC*	DCM Boost PFC, *LLC*
Number of switches	8	2	4	2	2	2/2/2	2	2
Number of diodes	0	4	8	4	8	6/6/8	6	8
Transformer center tap	No	--	--	--	Yes	Yes	Yes	No
Full range soft switching	No	No	No	No	Yes	Yes	Yes	Yes
Input current control	Good	Good	Good	Good	Moderate	Moderate	Moderate	Good
Circuit parameter mismatch Effect for current control	Yes	Yes	No	--	--	No	No	No
Load range extendibility	--	No	No	--	--	No	No	Yes
Control and modulation complexity	High	High	High	Moderate	Moderate	Moderate	Moderate	Moderate

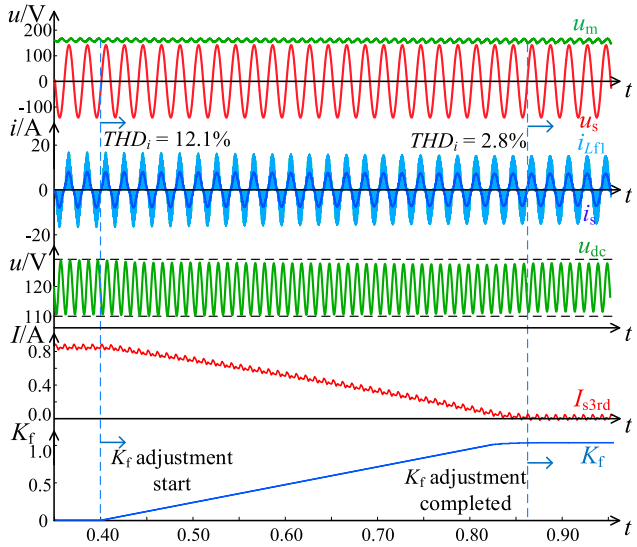

Fig. 10. Main simulation waveforms of the transient process of adjusting K_f.

of the third harmonic I_{s3rd}, and the THD_i of the input current can be improved after the adjustment is completed in several hundred milliseconds.

B. Comparison Between the Existing Single-Stage AC–DC Schemes and the Proposed Scheme

A detailed comparison between the traditional single-stage ac–dc schemes and the proposed scheme has been listed in Table I, mainly including the following nine aspects.

1) Topology type: The adopted topology is a combination of DCM boost PFC with a two-phase interleaved and *LLC* circuit.

2–4) Component composition: The adopted converter structure requires two switches and eight diodes to achieve ac–dc power conversion with galvanic isolation.

5) Full range soft switching: To achieve ZVS turn-ON of the switches of the converter, from Figs. 2(b) and 3, it follows that

$$I_{Lm} + I_{\text{pk}} \approx \frac{u_{\text{dc}}}{4nL_m f_s} + \frac{T_s u_s}{4L_f} + \frac{T_s U_k}{\pi L_f} \geq \frac{2C_{\text{ds}} u_m}{T_d} \tag{30}$$

where C_{ds} is the parasitic capacitance of the drain–source of the power switch. The PFC and *LLC* parts of the converter both provide a soft turn-ON reverse current for the switches; thus, the higher the input power, the easier it is to achieve ZVS turn-ON of the switches and improve the operation efficiency [33]. Therefore, under the light load, it demands that $L_m \leq T_d/(8C_{\text{ds}}f_s)$ to achieve full range soft-switching operation of the converter.

6) Input current control: Single-stage ac–dc converters can generally achieve unity power factor (PF) operation in the grid side by topology design or grid voltage feedforward control methods, but the input current still needs to be indirectly controlled to suppress its harmonic components, thereby improving the grid-side power quality.

7) Circuit parameter mismatch effect for current control: In traditional schemes, the control method with input current harmonic suppression function generally adopts circuit parameters, and thus, its control performance is affected by parameter mismatch. To mitigate the effect of the circuit parameter mismatch and reduce the computational burden of the controller, this article proposes an indirect input current control method with an adjustable feedforward parameter K_f.

8) Load range extension: The traditional DCM boost single-stage ac–dc converters have power limitations. Facing transient conditions, such as short-term overload, the filter inductor current will change to CCM, causing severe current distortion. The design of filter capacitance in the proposed scheme ensures the converter to maintain DCM operation of the filter inductor current at high power, thereby improving the load range and enhancing the reliability of the converter.

9) Control and modulation complexity: The proposed control method is a variable frequency control method with an adjustable feedforward parameter, which achieves PFC function with harmonic current suppression and no-static-error tracking of the

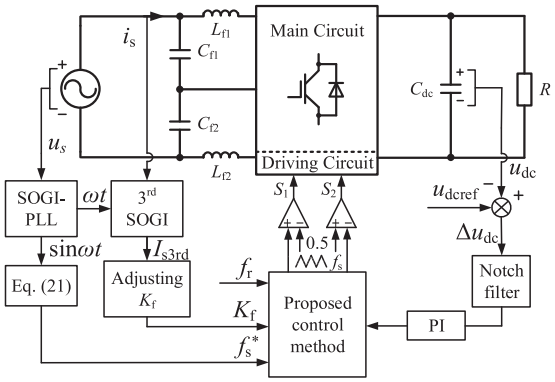

Fig. 11. Block diagram of the proposed scheme.

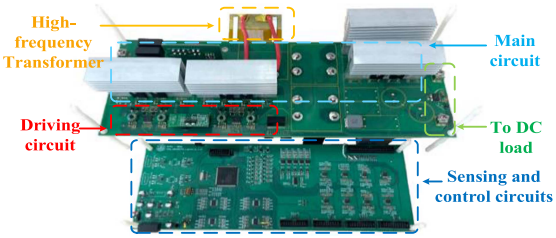

Fig. 12. Prototype of the single-stage AC–DC converter.

TABLE II
EXPERIMENTAL PARAMETERS

Parameters	Values
AC voltage RMS U_{srms}/V	100
AC voltage frequency f_{grid}/Hz	50
DC voltage reference u_{dcref}/V	120
Input filter inductors L_{f1}, L_{f2}/μH	50
Input filter capacitors C_{f1}, C_{f2}/nF	120 (Proposed method), 3300 (Traditional method)
DC capacitor C_m/μF	10
Resonant capacitor C_r/nF	320
Resonant inductor L_r/μH	8
Magnetizing inductor L_m/μH	24
Resonant frequency f_r/kHz	99.5
Switching frequency range f_s/kHz	70–180
Transformer ratio n	2 : 3
DC output capacitor C_{dc}/μF	400
Rated output power P_{out}/W	500 (Proposed method), 300 (Traditional method)

dc bus voltage reference. The calculation burden is relatively small, and the modulation method is relatively simple without any phase-shift methods.

IV. EXPERIMENTAL RESULTS AND ANALYSES

In order to validate the feasibility and effectiveness of the converter and the proposed scheme in this article, as shown in Fig. 11, a 500-W prototype is developed. The control method is implemented in the microcontroller TMS320F28377 of Texas Instruments. The experimental platform is shown in Fig. 12, and the experimental parameters are presented in Table II.

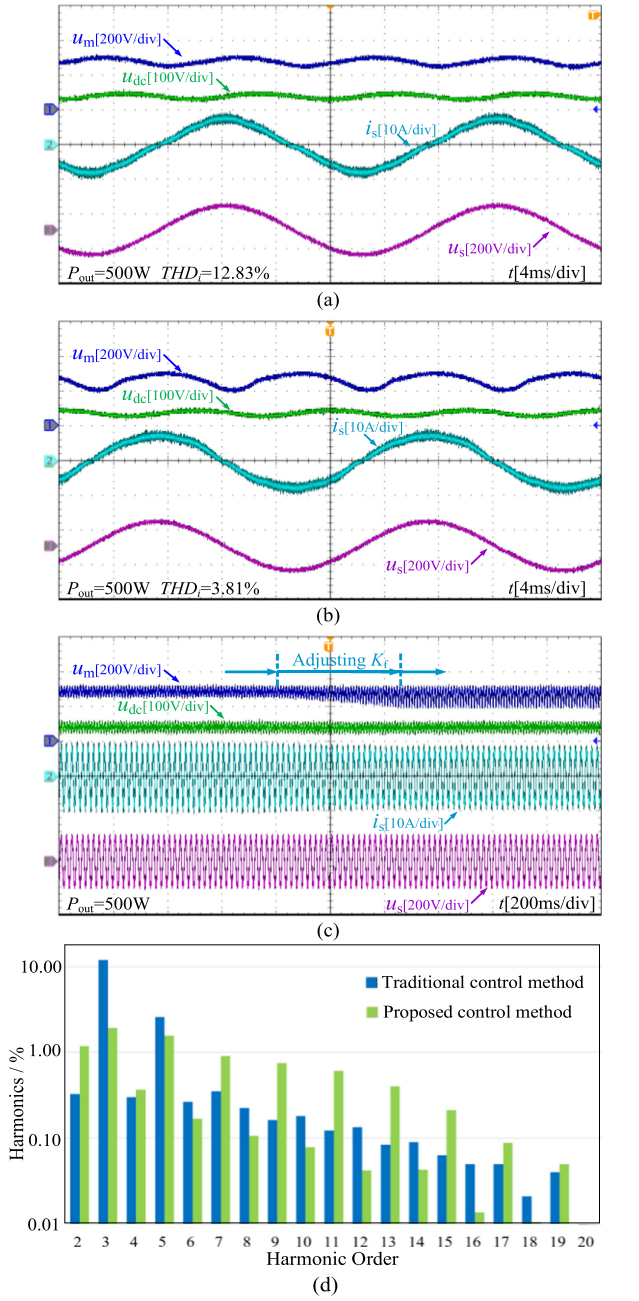

Fig. 13. Experimental waveforms of the input currents and DC output voltages (a) with traditional control method, (b) with proposed control method, (c) transient process of adjusting K_f, and (d) Fourier analysis of the input currents when $P_{out} = 500$ W and $C_f = 120$ nF.

A. Harmonic Current Control With Adjustable Feedforward Parameter

Fig. 13 illustrates the waveforms of grid voltage, input current, bus voltage u_m, and output voltage u_{dc} when $P_{out} = 500$ W and $C_f = 120$ nF with the traditional current control method or the proposed method, and the Fourier analysis diagram. When the converter is operating without the proposed feedforward control method, the distortion of the input current is larger, the THD_i of the input current is 12.83%, and the PF is 0.994. With the proposed control method, as shown in Fig. 13(b), the distortion

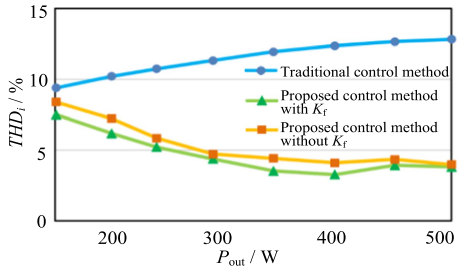

Fig. 14. Input current THD$_i$ curves at different operation powers.

of the input current is significantly suppressed, the THD$_i$ of the input current decreases to 3.81%, and the PF increases to 0.999.

The dynamic waveforms of the converter with feedforward parameter K_f adjustment are shown in Fig. 13(c). With the gradual increase of K_f, the harmonic component of the input current is reduced, while the peak value of the input current also slightly decreases. On the other hand, the low-frequency ripple component of bus voltage u_m will increase with the change of switching frequency caused by the increase of K_f. However, according to the power conservation law and the fact that $C_{\rm dc}$ is much greater than C_m, and the ripple power at twice the grid frequency is also the same, the ripple component of the output voltage $u_{\rm dc}$ almost does not change during the adjustment of K_f. In addition, according to the Fourier analysis of the input current in Fig. 13(d), the THD$_i$ of the input current under the rated load is reduced by 9.02%, and the third and fifth harmonic components are reduced by 88.56% and 39.60%, respectively. Finally, from the curves of THD$_i$ of the input current at different operation powers, as shown in Fig. 14, it can be seen that, with the increase of the operation power, the THD$_i$ of the input current with the traditional control method increases to more than 10%, while with the proposed control method, the THD$_i$ of the input current is lower than that with the traditional method and can be reduced to less than 5% at 0.6 times the rated load.

It is noted that with the adjustable K_f, a lower input current THD$_i$ can be obtained. However, from (28), when $P_{\rm out}$ approaches the rated load, f_s will be closer to the resonant frequency of C_f and L_f, and the value of A will decrease significantly. Therefore, it can be seen from Fig. 14 that THD$_i$ slightly rises when $P_{\rm out}$ is close to 500 W, rather than continuously decreasing with the increasing of power, as measured in other topologies [5], [8].

B. Load Range Extension Function

In the traditional DCM boost single-stage ac–dc converters, the filter capacitor C_f is generally large, while high operation power may result in input current distortion. In order to extend the operation load range of the converter, the capacitance of C_f in the proposed scheme is reduced to achieve LC resonant at high power, and the corresponding experimental verification is carried out, where the same input filter inductance and LLC circuit parameters are used in both methods. Fig. 15 shows the dynamic and steady-state experimental waveforms of the converter with load mutation with the traditional scheme and C_f = 3300 nF. It can be seen that the output voltage can track the

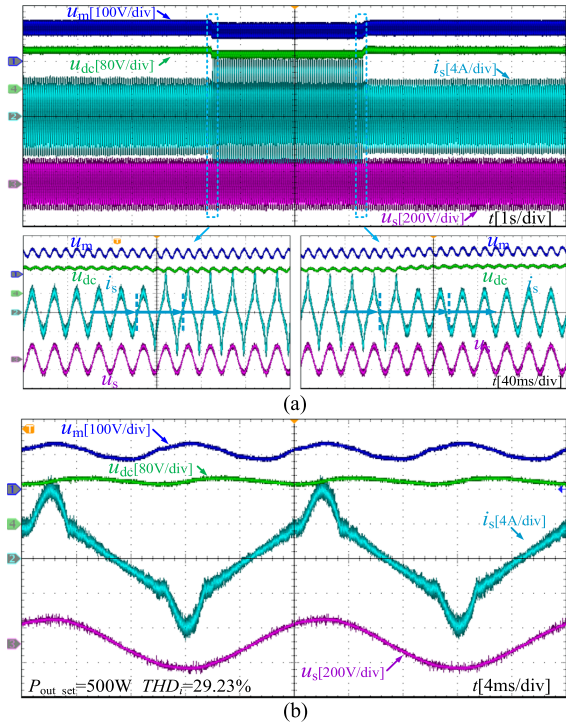

Fig. 15. Experimental waveforms of the input currents and DC output voltages with the load mutation from 250 to 360 W when C_f = 3300 nF, (a) transient process, and (b) steady state when $P_{\rm out}$ = 360 W.

reference when $P_{\rm out}$ = 250 W, but when the load is switched up to 1.2 times the rated load of the traditional method, due to the current distortion and switching frequency limitation, the output voltage drops 18 V from the reference value in the steady state. At the same time, as shown in Fig. 15(b), there is obvious distortion at the peak of the input current, and the THD$_i$ increases to 29.23%, which is 25.42% higher than that with the proposed scheme. With the proposed scheme, in order to cause grid-side LC resonance and obtain higher $I_{\rm pk}$ while maintaining the filter inductor current operation in DCM, C_f is selected as 120 nF, and the experimental results are shown in Fig. 16. In the dynamic process of load mutation, the output voltage can track the reference value. When the load steps up, the system reaches the steady state within 68 ms, and the output voltage drops about 10 V in the transient. When the load steps down, the system reaches the steady state within 80 ms and the output voltage rises about 12 V, which shows that the converter has a fair dynamic performance. It is worth noting that the current overshoot in this process results in the peak of the input current reaching 122% of the rated amplitude, and the waveforms of the bus voltage and grid voltage of the converter are tangent at the rated load and the dynamic process, so there is no current distortion caused by exceeding the power limitation, which further validates the effectiveness and necessity of the proposed load extension method.

Fig. 17 presents the waveforms of filter inductor current i_{Lf1}, filter capacitor voltage u_{Cf1}, and input/output voltages. When the converter operates at half load and C_f = 3300 nF, the inductor current is still DCM at the peak of the grid voltage cycle, while

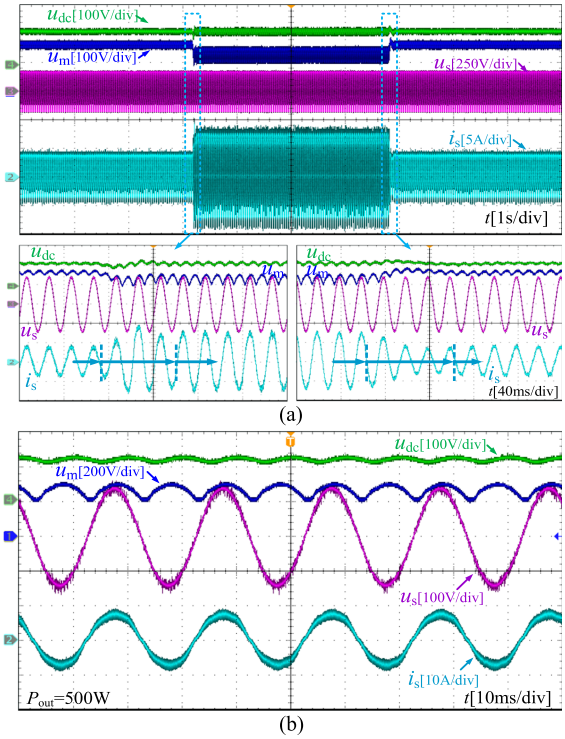

Fig. 16. Experimental waveforms of the input currents and DC output voltages with the load mutation from half load to rated load when C_f = 120 nF, (a) transient process, and (b) steady state at full load.

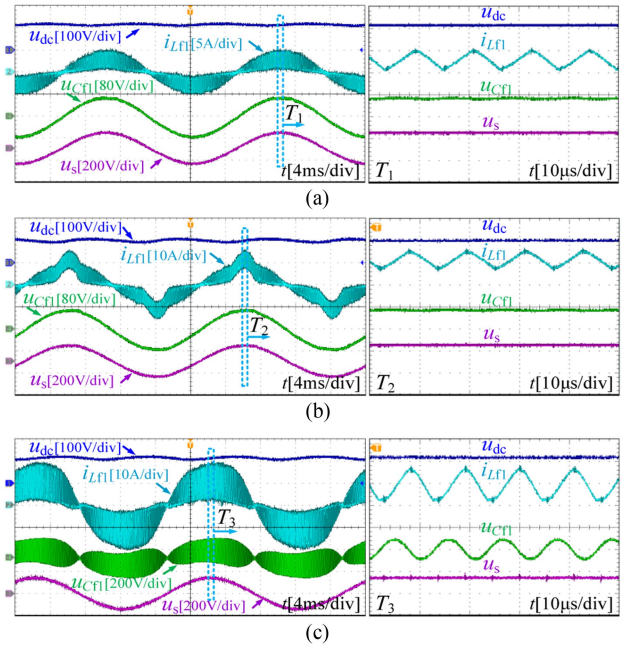

Fig. 17. Experimental waveforms of the grid voltages, input currents, and output voltage, (a) when P_{out} = 250 W and C_f = 3300 nF, (b) when P_{out} = 360 W and C_f = 3300 nF, and (c) under full load when C_f = 120 nF.

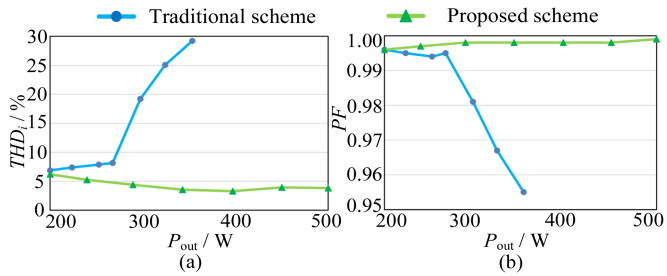

Fig. 18. THD_i and PF curves at different output powers. (a) THD_i and (b) PF.

the inductor current will be converted from DCM to CCM at the peak when P_{out} = 360 W, resulting in serious current distortion. In the above processes, the instantaneous value of the filter capacitor voltage is equal to half the grid voltage and will not change with the switching state of S_1 and S_2, and thus, the inductor current changes linearly in each switching state. As shown in Fig. 17(c), when adopting the proposed scheme, C_f = 120 nF and at full-load operation, C_f and L_f can be resonant during the switching cycle, i_{Lf1} remains in DCM at the peak of the grid voltage cycle, but different from Fig. 17(a) and (b), its waveforms under different switching states are curves, and the instantaneous value of u_{Cf1} is the sum of half of the grid voltage at the fundamental frequency and a sinusoidal ripple component at the switching frequency. Since the *LC* resonance makes that $L_{f1}di_{Lf1}/dt = u_{Cf1} > 0.5u_s$ at the rising stage of i_{Lf1}, higher input current peaks can be obtained at the same switching frequency.

The curves of THD_i and PF at different powers adopting the traditional scheme and the proposed scheme are shown in Fig. 18. It can be seen that, with the traditional scheme, as the input current distortion at the peak of the grid voltage cycle gradually increases with the operation power, the THD_i rises, while the PF will decrease significantly after more than 260 W, which affects the power quality at the grid side. When adopting the proposed scheme, the THD_i of the input current of the converter is less than 4% when close to the rated load, and the PF is higher than 0.995. Compared with the traditional scheme, the input current control performance of the converter has been improved, and it can operate at a higher power range.

It is worth noting that according to (10), when the lower limit of switching frequency is 70 kHz, the power limitation of the converter with the traditional scheme, L_f = 50 μH and C_f = 3300 nF, is about 315 W. However, in order to optimize the current control performance, after adding the feedforward component in the control scheme, the switching frequency at the peak of the grid voltage cycle will be increased to more than 85 kHz, so the power limitation with the traditional scheme will be further reduced to 260 W. Therefore, the operation load range extension method is suitable for implementation with the proposed input current control method, which is based on the variable frequency modulation.

Compared with the proposed scheme, when using the traditional method, it is necessary to increase u_m by changing the circuit parameters, such as L_f, to avoid input current distortion caused by high power. Therefore, an experimental comparison is carried out when adopting the traditional scheme with C_f = 3300 nF, and reducing L_f to 30 and 20 μH, as shown in Fig. 19. In Fig. 19(a), when L_f = 30 μH, and the load is set to 500 W, the dc output voltage u_{dc} is slightly lower than the reference due to the lower limitation of the switching frequency. In Fig. 19(b),

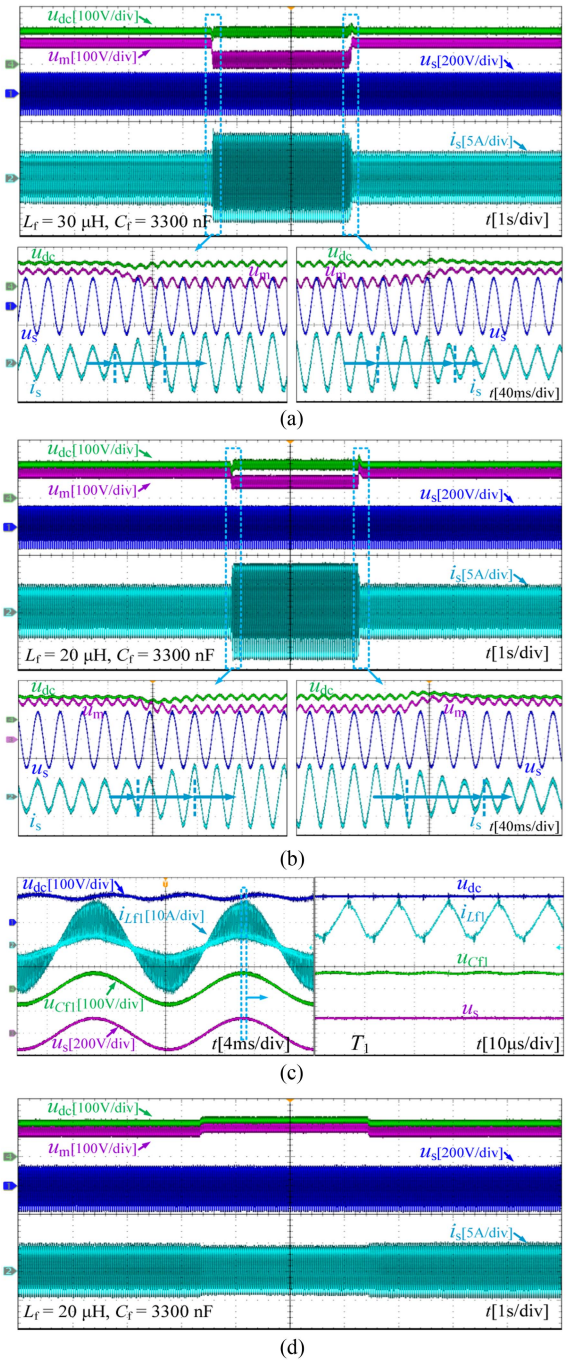

Fig. 19. Experimental waveforms with traditional method and $C_f = 3300$ nF. (a) Transient process when $L_f = 30$ μH and load steps from 250 to 500 W. (b) Transient process when $L_f = 20$ μH and load steps from 250 to 500 W. (c) When $L_f = 20$ μH and $P_{\rm out} = 500$ W. (d) Transient process when $L_f = 20$ μH and load decreases from 250 to 200 W.

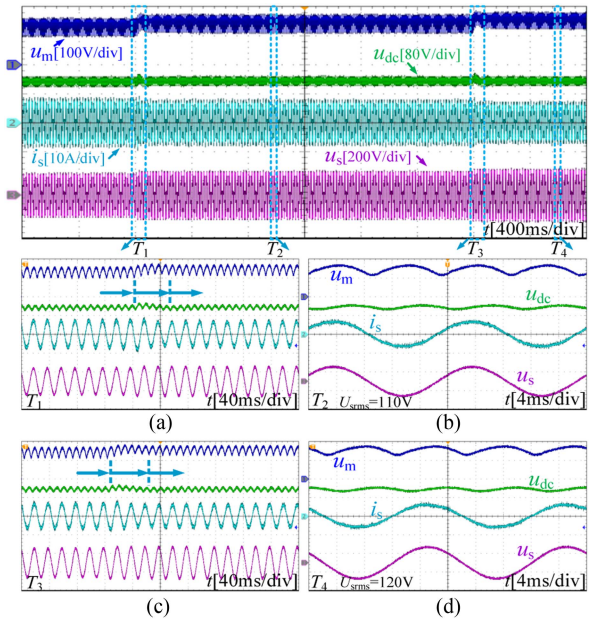

Fig. 20. Experimental waveforms of the input currents and DC output voltages at full load with $C_f = 120$ nF. (a) Transient process when U_{srms} steps from 100 to 110 V. (b) Steady state when $U_{srms} = 110$ V. (c) Transient process when U_{srms} steps from 110 to 120 V. (d) Steady state when $U_{srms} = 120$ V.

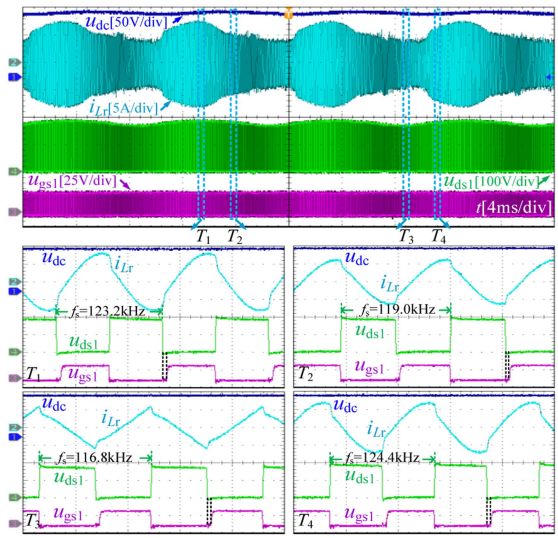

Fig. 21. ZVS waveforms for S_1 of the AC–DC converter under half load with the proposed control method and $C_f = 120$ nF.

when $L_f = 20$ μH, the converter can operate under 250 and 500 W, and as shown in Fig. 19(c), there is no distortion in the waveform of the filter inductor current when $u_s = U_s$. However, it is worth noting that, as shown in Fig. 19(d), when L_f is reduced to 20 μH and the load is decreased from 250 to 200 W, due to the maximum switching frequency limitation of the converter (200 kHz), $u_{\rm dc}$ is higher than the reference value, resulting in overvoltage problems. It can be seen from Figs. 16 and 19 that adopting the proposed scheme can reduce the bus voltage u_m, i.e., the voltage stress of the switches at the same output power, without reducing the input filter inductance, while expand the operating load range at the same switching frequency limitation.

C. Input Voltage Variation and Efficiency Analysis

In this article, the rated U_{srms} is selected as 100 V to validate the harmonic current control performance and load range extension function of the proposed scheme. To further verify the dynamic response and steady-state control performance of the converter, experimental results with grid voltage variation when

TABLE III
EXPERIMENTAL COMPARISON BETWEEN THE TRADITIONAL CONVERTERS WITH THE PROPOSED SCHEME

Aspects \ Schemes	[9]	[26]	[27]	[34]	[35]	[17]	[28]	Proposed scheme
Power (W)	500	320	6000	300	102.96	104	114	500
Peak PF	>0.99	>0.99	0.9955	0.998	0.986	0.994/ 0.972/ 0.992	0.994	0.999
Minimum input current *THD*	1.60%	<3.3%	2.54%	4.4%	<12.0%	9.9%/ 23.6%/ 8.71%	<10.0%	3.25%
Peak efficiency	94.6%	>96.5%	97.4%	93.58%	93.1%	93.41%/ 93.30%/ 91.85%	93.75%	94.31%

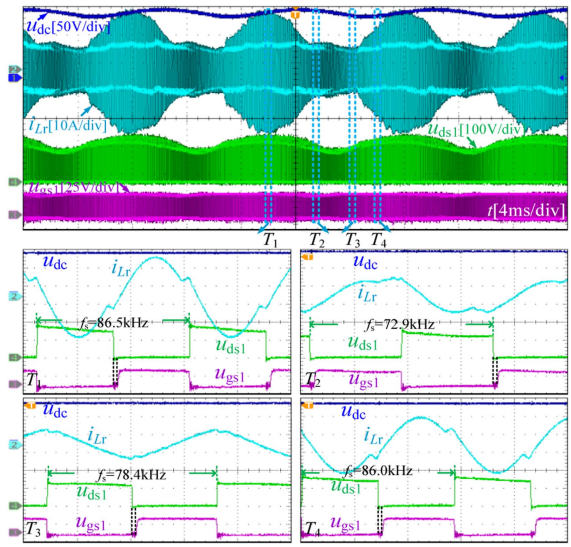

Fig. 22. ZVS waveforms for S_1 of the AC–DC converter under the rated load with the proposed control method and $C_f = 120$ nF.

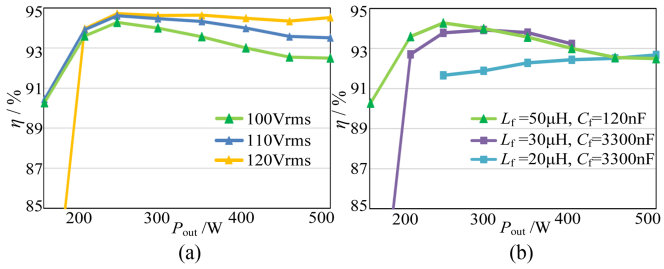

Fig. 23. Efficiency of the converter at different output powers. (a) With proposed scheme and different $U_{\rm rms}$. (b) With different L_f and C_f.

using the proposed method are presented in Fig. 20. It can be seen that the converter can maintain stable operation with the gird voltage mutation, with a response time of less than 56 ms and an output voltage overshoot of less than 8 V.

The experimental results, as shown in Figs. 21 and 22, are obtained to further verify the soft-switching operation of the proposed scheme. The proposed control method does not require additional phase-shifting control, and thus will not affect the soft-switching characteristics of the converter. At the peak of the grid voltage, the converter converts higher power from the grid side to the output side, while i_{Lf1} and i_{Lr} both provide soft turn-ON reverse current for S_1; at the zero-crossing point of the grid voltage, for example, at T_3, the transmission power from ac to dc side is close to 0, and only i_{Lr} provides the reverse current of soft turn-ON of S_1. It can be seen that, under different powers and switching frequencies, the switch of the converter can realize ZVS turn-ON operation.

The efficiency of the converter under different grid voltages when adopting the proposed scheme is shown in Fig. 23(a). It can be seen that as U_{srms} rises, the efficiency also increases. When $U_{srms} = 120$ V, the maximum operating efficiency of the converter is 94.72%, and the operating efficiency at the rated power reaches 94.53%, while the peak efficiency of the proposed converter is 94.31%, while the efficiency at full load is 92.52% at the rated U_{srms}. A comparison of the efficiency when the output voltage of the converter can maintain the reference value with the traditional method and proposed method is listed in Fig. 23(b). Compared with the operating points when the traditional method is adopted and the input filter inductance is reduced, using the proposed method results in higher efficiency and a wider operating load range. The experimental comparison of the traditional converters with the proposed scheme under the rated circuit parameters and grid voltage is listed in Table III, which shows a fair efficiency and steady-state control performance of the scheme.

V. CONCLUSION

This article introduces a modified PFC control strategy with an adjustable feedforward parameter and a method to broaden the load range of the single-stage DCM boost ac–dc converter, targeting the mitigation of input current harmonics and overcoming the load range constraints inherent in conventional designs. The employed converter inherently facilitates unity PF operation, and the third-order harmonic component of the input current is obtained by the third-order SOGI to adjust the feedforward component. The introduced control methodology significantly attenuates odd harmonics in the input current, thereby enhancing power quality on the grid side. In addition, to tackle the power limitation of the traditional schemes, a load range expansion design is executed through the precise engineering of filter capacitance, causing grid-side *LC* resonance under high power. With the proposed scheme, the current distortion caused by high power is avoided, and the operating load range of the converter is improved so that the converter can deal with load mutation and short-term overload conditions. In addition, while

maintaining the soft-switching operation, the bus voltage with the proposed scheme is reduced at the same operating power, and thus, a better efficiency curve compared with the traditional scheme is achieved. Finally, the feasibility and effectiveness of the proposed scheme are verified by experiments, with which the converter achieves a peak efficiency of 94.31% and a minimum THD_i of 3.25%.

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