Modified Back-Stepping Sliding Mode Controller With Robust Observer-Less Disturbance Rejection for DC Microgrid Applications

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***Abstract*—The proportional-integral-based double-integral sliding mode control suffers from linearization issues, restricted eigenvector-based state trajectory placement, and reduced robustness. To address these issues, this article describes a reduced-order dual-loop adaptive feed-forward double-integral back-stepping sliding mode control technique for a dc–dc converter used in dc microgrids. The proposed technique enables an observerless mitigation of unmodeled uncertainties using an adaptive feed-forward compensation. An ultimate compensatory feed-forward term is introduced to circumvent overall unmodeled converter uncertainties. The compensatory term also ensures a chattering-free faster reaching condition, that is selected based on a nonlinear pseudo sliding manifold (PSM). PSM is a non-singular extended-order fixed-time convergent manifold. The proposed technique uses double-integral back-stepping method to derive the control signal and PSM to mitigate the uncertainties. ADC and sensor uncertainties are corrected using a higher-order generalized polynomial weighted least squares convex optimization. To further support the compensation action, feed-forward constants of the proposed control loop are tuned online using a hybrid controller design approach considering loop shaping analysis, boundary conditions of parameter variations and small-signal closed-loop stability analysis. Experimental verification of the proposed control technique is carried out along with simulation analysis to ascertain the proposed technique against different test conditions, and comparisons are drawn with conventional techniques.**

***Index Terms*—Adaptive feed-forward, back-stepping control (BSC), compensatory term, dc microgrid, dc–dc converter, fixed-time convergence (FTC), observer-less, sliding mode control (SMC).**

NOMENCLATURE

δ_1, δ_2	Overall uncertainty representing terms.
Γ_j, $a_{k,j}$	Sensor weights, polynomial coefficients.
λ_k, p_{il}	Eigenvalues, participation factors.
$\mathbf{\Psi}$, $\mathbf{\Phi}$	Left and right eigenvector matrices.
$\mathbf{A}$, $\vec{\mathbf{B}}$	State matrix, control vector.
$\mathbf{P}$, $\vec{\mathbf{E}}$	Equilibrium point transformation matrix, input vector.
ρ_1, ρ_2	Terminal constants.
$\vec{\mathbf{\Delta}}$, $\mathbf{R}$	Uncertainty vector, covariance matrix.
$\vec{\hat{m}}$, $\mathbf{G}$	Estimated sensor vector, ADC gain matrix.
$\vec{\mathbf{a}}$, $\vec{\mathbf{o}}$	ADC calibrated voltage vector, ADC offset vector.
$\vec{\mathbf{e}}$, i_{off}	State error vector, offset dc current.
$\vec{\mathbf{f_0}}$, $\vec{\mathbf{f_{eq}}}$, $\vec{\mathbf{f}}$	State dynamic vectors.
$\vec{\mathbf{H}}$	Compensatory vector.
$\vec{\mathbf{J}}$	Sliding constant vector.
Ξ	Ultimate compensatory term.
d_{eq}, d'_{eq}	Equivalent control terms or PWM signals.
f_i, g_i	Scalar recursive functions.
$g_{o,i}$, $R_{2,i}/R_{1,i}$	Isolation Op-Amp gain, Op-Amp dc gains.
$N_{p,i}/N_{s,i}$, $R_{b,i}$	Hall-effect CT gains, burden resistors.
$R_{m,i}/\sum_j R_{j,i}$	Potential divider gain.
$T_s^{\max}$	Maximum settling time.
V_i	Lyapunov candidate energy functions.
$V_{\text{cal},i}$, $X_{\text{cal},i}$	Calibrated ADC and sensor values.
$V_{\text{off},i}$, n	Sensor dc offset, ADC no. of bits.
$X_{\text{act},i}$, $V_{\text{adc},i}$	Sensor signal, ADC sensed voltages.
ADI-BSM	Adaptive double-integral back-stepping sliding mode.
CI-SEPIC	Coupled-inductor SEPIC.
DI-SMC	Double-integral sliding mode control.
FOT-SMC	Fractional-order terminal SMC.
I-BSC	Integral back-stepping control.
NEO-FTC	Non-singular extended-order fixed-time convergent.
PSM	Pseudo sliding manifold.
PWLSQ	Polynomial weighted least squares.

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I. INTRODUCTION

DC–DC power converters are increasingly popular due to their wide range of applications in dc microgrids. They are also used in other applications such as electric vehicle (EV) charge controllers, battery management systems (BMS), hybrid renewable energy storage systems including photovoltaic (PV), wind, fuel cell, battery, supercapacitor (SC), etc. Linear control technique including proportional-integral (PI) control method is widely used in the industry due to its ease of implementation,

improved dynamics, and robustness to a certain range of parameter variations. PI technique uses small-signal perturbation analysis around a state equilibrium point by deriving control-to-state, state-to-state, and input-to-state transfer functions. The PI parameters of these transfer functions are tuned using time domain or frequency domain analysis using pole placement and loop-shaping analysis. The plant transfer function poses a limitation on controller parameter tuning using loop-shaping analysis. Also, the closed-loop response is stable up to a certain range of the parameter variations. Another crucial limitation of the linear control approach is the lack of flexibility in state trajectory shaping due to restricted eigenvectors. As the state trajectory is determined by the plant transfer function (placement of eigenvectors), there is no flexibility in positioning the state trajectory with these fixed eigenvectors [1].

Nonlinear control methods such as SMC offer the benefits including: modeled uncertainty rejection, mitigation of input disturbances, flexible state trajectory placement, asymptotic stability, simplified closed-loop dynamics, and finite-time convergence. SMC is based on a state space representation of a system in terms of the states or state errors. Further, an equivalent control law in terms of equivalent duty ratio, d_{eq} is derived by assuming a linear invariant sliding manifold or surface, which is a linear combination of the eigenvectors [2], [3]. Dual-loop control of a dc–dc converter with a PWM-based or PI-based DI-SMC technique helps to subdue the issues of high frequency chattering, steady-state error, variable switching frequency, and enables enhanced control of the inductor current [4]. The hitting condition for SMC guarantees that the state trajectory in a state space reaches the sliding manifold starting from any initial condition. Existence condition makes sure that the trajectory cuts the manifold from either side in a plane orthogonal to the manifold until a steady-state is achieved at an equilibrium point. To overcome the model-matched uncertainties, the disturbance term should be modeled as a function of the states and the control vector by using the equivalent sliding dynamics of the SMC technique. Further, DI-SMC technique cannot handle nonlinear controller tuning for complex plant models. Last, there is no well-defined methodology that can be adapted for tuning parameters of the PI-based dual-loop DI-SMC technique, as the controller gains result in high chattering. Section II-B describes the above mentioned disadvantages of the conventional PI-based DI-SMC technique in detail.

In order to overcome the above challenges of the DI-SMC technique, BSC is proposed in the literature [5], [6]. I-BSC is a recursive state-space control technique where nonlinear equations representing complex systems are broken into simpler single-input-single-output subsystems and are solved recursively [7], [8], [9]. This approach involves calculation of intermediate equivalent control variables with stabilization of the subsystems under consideration. These are then used for solving the next subsystems until a final equivalent control variable is generated. I-BSC is a robust control technique used for complex nonlinear equations with unmodeled uncertainties, and is also widely used in industries for spacecraft, chemical plants, robotics, and PV systems. [10].

Nonlinear feedback controlled systems can be represented in the state-space representation in different forms, such as pure-feedback systems, strict-feedback systems, output-feedback systems, etc. Most of the dc–dc converters are pure-feedback systems [17]. In pure-feedback systems, all the system states can be measured or estimated simultaneously and used to derive the control variables. In strict-feedback systems, each of the dynamic equation is solved recursively and separately for intermediate outputs or states, that are input to the next subsystems. BSC or I-BSC control methods necessitate that the system should be transformed into a recursive, simultaneous strict-feedback state-space dynamic model as outlined in (3). There are different ways in which pure-feedback systems are represented as strict-feedback systems including change of variable and state-feedback linearization approaches. Due to errors in the linearization process and variable set-point or operating point, there is a possibility of model uncertainties. Further, a Boost-derived dc–dc converter includes a noninvertible or nonminimal phase component with right-half plane zero in the output voltage-to-duty small-signal transfer function, which poses a restriction in representing the system in the required strict-feedback form. To address this issue, Wu et al. [17] and Ghosh et al. [19] proposed a SMC-based I-BSC technique that includes a linear transformation of the system states using a Brunovsky canonical linearized representation. However, this linear transformation uses power error to represent the sliding manifold equation. This does not guarantee zero steady-state errors for all the system states.

Alam et al. [20] described a dual-loop PWM-based composite robust BSC and Terminal SMC (T-SMC) technique with a modified integral sliding surface for fast convergence and reduced chattering, where the BSC enhances the voltage tracking accuracy. However, the parameter tuning approach presented here is purely based on user defined constants, where the best suited parameters are selected from different test cases, which may not be optimum. Yin et al. [21] described disturbance observer-based single-loop BSC and dual-loop SMC-based control techniques. Sarrafan et al. [16] described a fast fixed-time convergent observer with back-stepping control for a boost converter using the Brunovsky transformation. However, the maximum fixed-time expression is a logarithmic expression, where the observer delay is not considered. Active disturbance rejection technique for dc microgrid is proposed in Aliamooei et al. [22]. Xu et al. [23] described an extended disturbance-based load stabilization using nonlinear control technique for dc microgrids. Observer-based disturbance rejection suffers from delayed response, no well-defined rule for parameter tuning, high frequency chattering, prone to plant parameter variations, etc. Thus, there is a need to eliminate the observer. On the basis of the exhaustive literature survey mentioned above, it is evident that there is a need for an observerless fixed-time convergent nonlinear control technique.

This article describes observer-less disturbance mitigation with fixed-time convergence that uses a pseudo nonlinear sliding manifold without the need of disturbance estimation. CI-SEPIC converters have the advantages over conventional Boost

TABLE I
COMPARISON OF THE EXISTING TECHNIQUES WITH THE PROPOSED TECHNIQUE

Ref.	SMC+I-BSC Control	Singularity Suppression	Fixed-Time Convergence	Pseudo Sliding Manifold	Observer-less Operation	Chattering Reduction	Extended-Order State Terms	Adaptive Feed-Forward	Sensor Error Mitigation
[11]	Yes	No	No	No	No	No	No	No	No
[12]	Yes	No	No	No	No	No	Yes	No	No
[13]	No	Yes	No	No	No	Yes	Yes	No	No
[14]	Yes	No	No	No	No	Yes	No	Yes	No
[15]	No	No	No	No	No	No	No	No	Yes
[16]	Yes	No	Yes	No	No	No	No	No	No
[17]	Yes	No	No	No	No	Yes	No	Yes	No
[18]	No	No	Yes	No	No	No	No	Yes	No
Proposed	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**

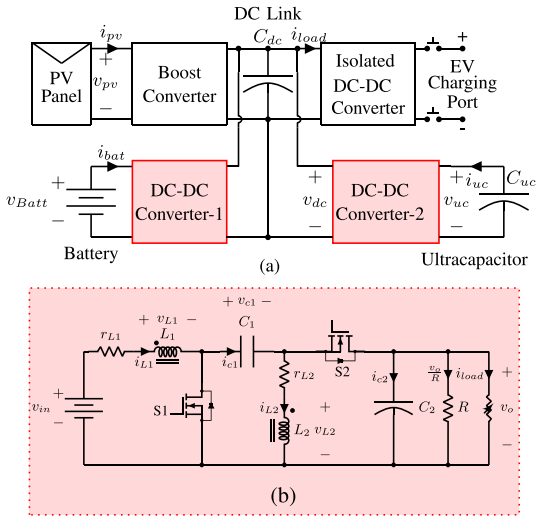


Fig. 1. (a) DC microgrid. (b) Synchronous CI-SEPIC DC–DC converter.

converter, including: better handling of the nonminimal phase component, ease of scalability for deriving higher-order isolated converters, reduced leakage inductance and improved efficiency and form factor. Owing to the above advantages, CI-SEPIC converter is selected for the dc–dc converter depicted in Fig. 1(a). Table I summarizes some of the significant existing research in the literature, where the text highlighted indicates the original contributions of this article. The literature does not report any studies on observer-less PSM-based approaches in dc–dc converters. In order to circumvent all the aforementioned disadvantages in the literature, the explicit contributions of this article are summarized as follows.

1) The I-BSC method is combined with the PWM-based DI-SMC technique to propose an adaptive feed-forward PI-based dual-loop ADI-BSM technique.
2) Additional double-integral term is added to the I-BSC error states to derive the equivalent control signal d_{eq} using the error state feedback-linearization approach.
3) Unmodeled uncertainties in the converter are overcome without an observer using an ultimate compensatory term designed using a NEO-FTC PSM.
4) The ADC and sensor values are corrected using PWLSQ approximation using calibrated ADC and sensor values.
5) Hybrid approach for controller parameter tuning includes using loop shaping analysis, SMC existence condition with parameter boundary values and closed-loop stability criterion.

Following are the advantages of the proposed technique over the state-of-the-art methods.

1) The proposed technique handles unmodeled uncertainties in a power converter without the need of an observer.
2) The proposed technique improves the dynamic voltage response of a dc–dc power converter in terms of reduced peak overshoots, faster settling time, and fixed-time convergence.
3) The proposed technique enables reduced order control for higher order dc–dc converters.
4) The proposed technique is resilient to sensor uncertainties and momentary faults with reduced sensor requirement using WLSQ state estimation techniques.

Boost derived dc–dc converter is the basic building block of higher order converters including CI-SEPIC converter, used in applications like solar MPPT controllers, battery-fed dc EV charging stations for dc microgrids as shown in Fig. 1(a). The proposed ADI-BSM+NEO-FTC control logic is easily scalable to higher-order isolated and nonisolated boost-derived converters as a reduced order technique. This is explained in Section III-E using the eigenvalue sensitivity, participation factor, and modal analysis. The subsequent sections of the article describe in detail the functionality of the proposed technique. Section II describes the conventional DI-SMC technique and its extension to the modified I-BSC method, which is described in Section III. Controller parameter tuning is described in Section IV. The technique is validated using simulation and hardware analysis in Sections V and VI, respectively. Finally, Section VII concludes this article.

II. CONVENTIONAL DI-SMC CONTROL TECHNIQUE

This section includes modeling and analysis of the error dynamics of the converter using the conventional DI-SMC technique.

A. Modeling and Analysis of the System

Fig. 1(a) describes the overall architecture of a dc microgrid including a common dc link and hybrid energy sources, such as

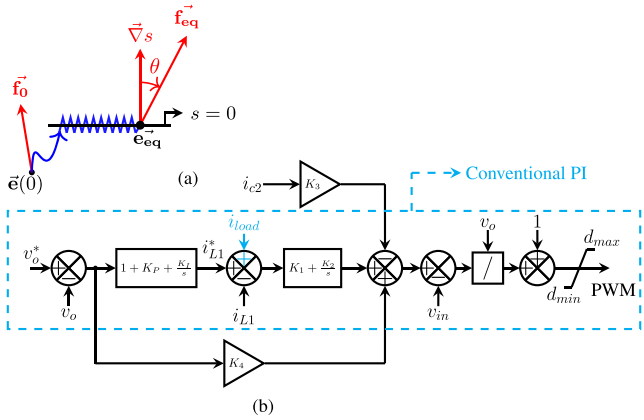


Fig. 2. (a) 2-D sliding manifold. (b) Conventional DI-SMC control loop.

solar PV, battery, and ultracapacitor and an EV charging station. Fig. 1(b) describes the synchronous CI-SEPIC converter, which is operated in the boost mode. This converter can be used as the dc–dc Converter-1 and II in Fig. 1(a) for integrating the hybrid energy storage systems with loads. The converter includes an input voltage source v_{in}, common-core coupled inductors L_1, L_2 with their series resistances r_{L1}, r_{L2}, series capacitor C_1, output capacitor C_2, MOSFETs S_1, S_2 and an equivalent load resistor R. The time-averaged reduced-order dynamic equations of the converter are given in (1). The states i_{L1} and v_o significantly contribute to the eigenvalue sensitivity of the converter. The other states i_{L2} and v_{c1} can be indirectly controlled by controlling these significant states thereby assuring stable closed-loop operation.

$$\left.\begin{aligned}\frac{di_{L1}}{dt} &= \frac{v_{in}-i_{L1}r_{L1}-d'v_{c1}-d'v_o}{L_1}+\delta_1\\ \frac{dv_o}{dt} &= \frac{d'i_{L1}-d'i_{L2}-\frac{v_o}{R}-i_{\text{load}}}{C_2}+\delta_2\end{aligned}\right\}. \tag{1}$$

The reduced-order dynamic representation of the converter is mentioned in (1), where d and $d'=1-d$ are the duty ratios or modulation signals for the switches S_1 and S_2, respectively. Constant switching frequency PWM scheme is employed for the control, where the modulation signals are compared with a triangular carrier signal and the resulting switching pulses are given to the respective switches. The terms δ_1 and δ_2 are the unmodeled terms representative of the overall model uncertainties due to parameter variations ($\Delta L_1, \Delta L_2$) and model mismatch.

B. Description of the Conventional DI-SMC Technique

This section describes analysis of the equivalent control law [d_{eq} and $d'_{\text{eq}}(1-d_{\text{eq}})$] using the conventional dual-loop PI-based DI-SMC technique, and the need to adopt the I-BSC technique. Errors e_1 (=i_{L1}^*-i_{L1}) and e_2 (=v_o^*-v_o) are defined as the new states for the dynamic state-space representation. Two more error terms, $e_3=\int(\sum_{i=1}^{2}e_i)dt$ and $e_4=\int e_3 dt$ are essential for overcoming steady-state errors. For implementing a PWM-based and PI-derived nested dual-loop control technique, the inner loop current reference is $i_{L1}^*=(K_P+\frac{K_I}{s})e_2$. Fig. 2(a) describes a particular linear sliding manifold mathematically represented by $s=\vec{\mathbf{J}}^T\vec{\mathbf{e}}=0$, where $\vec{\mathbf{J}}^T=[\alpha_1 \quad \alpha_2 \quad \alpha_3 \quad \alpha_4]$ is the sliding constant vector and $\vec{\mathbf{e}}=[e_1 \quad e_2 \quad e_3 \quad e_4]^T$ is the instantaneous state error vector. $\vec{\mathbf{e}}(0)$ and $\vec{\mathbf{e_{eq}}}$ are the initial and steady-state error vectors, respectively. The blue line in Fig. 2(a) describes the error state trajectory, and the red vectors define the state dynamic vectors $\vec{\mathbf{f_0}}$ and $\vec{\mathbf{f_{eq}}}$ ($\vec{\mathbf{f}}$), respectively, that represent tangent to the state trajectory in an Euclidean plane with $\vec{\mathbf{f}}=\dot{\vec{\mathbf{e}}}$. The state error trajectory starts from the initial point $\vec{\mathbf{e}}(0)$ and approaches the manifold, which is given by hitting or reaching condition, expressed as $s\dot{s}<0$. The existence condition of SMC elicits that the error state trajectory oscillates and cuts the manifold in an orthogonal plane (where the vector $\vec{\nabla}s$ lies), in a bounded region across the manifold $s=0$.

The error state-space representation of the system as per (1) is: $\dot{\vec{\mathbf{e}}}=\vec{\mathbf{f}}=\mathbf{A}\vec{\mathbf{e}}+\vec{\mathbf{B}}d'+\vec{\mathbf{E}}+\dot{\vec{\mathbf{H}}}$, where $\vec{\mathbf{f}}$, $\vec{\mathbf{H}}$, $\vec{\mathbf{e}}$, $\vec{\mathbf{B}}$, $\vec{\mathbf{E}}$ and $\vec{\mathbf{\Delta}}\in\mathbb{R}^4$, $\vec{\mathbf{\Delta}}=[\delta_1 \quad \delta_2 \quad 0 \quad 0]^T$ is the uncertainty vector, $\vec{\mathbf{H}}=\left[h_1(\vec{\mathbf{\Delta}}) \quad h_2(\vec{\mathbf{\Delta}}) \quad h_3(\vec{\mathbf{\Delta}}) \quad h_4(\vec{\mathbf{\Delta}})\right]^T$ is a compensatory vector, $\mathbf{A}\in\mathbb{R}^{4\times4}$ is the state matrix, $\vec{\mathbf{B}}$ and $\vec{\mathbf{E}}$ are the control and input vectors, respectively. To derive the equivalent law of d_{eq}, $\dot{s}=0$ is used, that yields $d'_{\text{eq}}=-[\vec{\mathbf{J}}^T\vec{\mathbf{B}}]^{-1}[\vec{\mathbf{J}}^T(\mathbf{A}\vec{\mathbf{e}}+\vec{\mathbf{E}}+\dot{\vec{\mathbf{H}}})]$, mathematically represented in Fig. 2(b) [24]. A linear transformation matrix $\mathbf{P}=\mathbf{I}-\vec{\mathbf{B}}[\vec{\mathbf{J}}^T\vec{\mathbf{B}}]^{-1}\vec{\mathbf{J}}^T=0$ is used to transform the state-space representation to the equilibrium point, where $\mathbf{I}$ is an identity matrix. The equivalent transformed error dynamics are: $\mathbf{P}\vec{\mathbf{f}}=\mathbf{PA}\vec{\mathbf{e}}+\mathbf{P}\vec{\mathbf{B}}d'_{eq}+\mathbf{P}\vec{\mathbf{E}}+\mathbf{P}\dot{\vec{\mathbf{H}}}$. In order to induce immunity against uncertainties, or $\mathbf{P}\dot{\vec{\mathbf{H}}}=0$, the compensatory vector should be expressed as some function of the error vector and the control vector, as: $\vec{\mathbf{H}}=\vec{\mathbf{B}}\chi(\vec{\mathbf{e}})$. This means that DI-SMC provides resilience to only modeled uncertainties, or SMC mitigates model matched uncertainties. For this, the function $\chi(\vec{\mathbf{e}})$ can be an unknown function, but $\vec{\mathbf{H}}$ should include the control vector term $\vec{\mathbf{B}}$. Thus, there is a need to have adaptive dynamic nonlinear control technique to handle unmodeled uncertainties, as not all disturbance terms can be modeled accurately. Additional compensatory functions can be added to the state-space representation, however, DI-SMC alone cannot assure complete disturbance rejection. Fig. 2(b) describes the control loop implemented using the conventional DI-SMC principle, where $K_3=\frac{L_1K_P}{C_2}$, $K_4=L_1K_I$ and the PI terms K_P, K_I, K_1, and K_2 can be selected using Bode plots analysis. From Fig. 2(b), it is evident that the control loop of d_{eq} or d using the DI-SMC technique is a super-set of that derived using conventional PI-based dual-loop technique.

III. Proposed ADI-BSM Control Technique

This section describes the proposed DI-SMC+I-BSC observer-less operation with a PSM, its fixed-time convergence verification and the ADC sensor uncertainties handling. To surmount the disadvantages of the unmodeled uncertainties, BSC is combined with the DI-SMC technique. In order to handle unmodeled disturbances, an adaptive ADI-BSM (DI-SMC+I-BSC) technique is proposed. This ADI-BSM technique includes a modified I-BSC technique where an additional double-integral term $-K_i'\int(\int e_1 dt)dt$ is added to e_4. This term is essential to derive the equivalent duty signal d_{eq} similar to that derived using a PWM-based DI-SMC technique. The innovative aspect

of the ADI-BSM technique is not solely the inclusion of the double-integral term, but also the introduction of an observer-less NEO-FTC term designed to manage these uncertainties. The state error vector according to the modified I-BSC methodology is given as follows:

$$\vec{\mathbf{e}} = \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \end{bmatrix} = \begin{bmatrix} i^*_{L1} - i_{L1} \\ v^*_o - v_o \\ \int (e_1 + e_2) dt \\ \int e_3 dt - K'_i \int \int e_1 dt dt \end{bmatrix} - \begin{bmatrix} h_1(\vec{\mathbf{\Delta}}) \\ h_2(\vec{\mathbf{\Delta}}) \\ h_3(\vec{\mathbf{\Delta}}) \\ h_4(\vec{\mathbf{\Delta}}) \end{bmatrix}. \quad (2)$$

Terms $h_i(\vec{\mathbf{\Delta}})$, $h_i(\mathbb{R}^4) \in \mathbb{R}$, where $i = 1, 2, 3, 4$, are compensatory functions appearing in the strict-feedback linearized state-space representation. A fourth-order recursive I-BSC technique is implemented to derive the ultimate equivalent control signal d_{eq}. The error state linearization representation defines a sequential chain of equations denoting four independent error subsystems given as follows.

$$\dot{e_i} = f_i\left(e_4, \ldots, e_i\right) + g_i\left(e_4, \ldots, e_i\right) e_{i-1} - \dot{h_i}(\vec{\mathbf{\Delta}}) \quad (3)$$

where $i = 4, 3, 2, 1$ and $e_0 = d'_{\text{eq}}$ is the ultimate control variable. The scalar recursive functions f_i and g_i are continuous, smooth, and differentiable functions with $g_i \neq 0$. The functions f_i $(i = 4, 3, 2, 1)$ are different from the state dynamic vectors $\vec{\mathbf{f}}$ $(\vec{\mathbf{f_o}}, \vec{\mathbf{f_{eq}}})$. Lyapunov candidate energy functions V_i are selected for each of the subsystems to ensure their stability

$$V_i = \sum_{j=i+1}^{4} V_j + \frac{e_i^{*2}}{2} \Rightarrow \dot{V}_i = \sum_{j=i+1}^{4} \dot{V}_j + e_i^* \dot{e}_i^*, \text{ where } i = 4, 3, 2, 1$$

$$\dot{V}_i = \sum_{j=i+1}^{4} \dot{V}_j + e_i^* \underbrace{\left[f_i + g_i e_{i-1}^* - \dot{h_i}(\vec{\mathbf{\Delta}})\right]}_{-K_i e_i^*}, e_{i-1}^*$$

$$= -g_i^{-1}\left[f_i - \dot{h_i}(\vec{\mathbf{\Delta}}) + K_i e_i^*\right]$$

where e_{i-1}^* and e_i^* are the reference state values for the ith and $i+1$th subsystems, respectively. The constants K_i represent Lyapunov positive constants. The assumption of $\dot{e_i^*} = -K_i e_i^*$ is considered to get $\dot{V}_i = \sum_{j=i+1}^{4} \dot{V}_j - K_i e_i^{*2}$. This implies that the Lyapunov functions $V_i > 0$ $(\because e_i^{*2} > 0)$ and their differentiation $\dot{V}_i < 0$ $(\because K_i > 0)$ for asymptotic stability. Equation (5) represents the detailed strict-feedback linearized reduced-order state-space representation of the CI-SEPIC converter. The above chain equations are solved sequentially to derive the ultimate control variable d'_{eq}, given in (4) and (6)

$$d'_{\text{eq}} = -g_1^{-1} \times \left[f'_1 - K_1 g_2^{-1} \left\{ f'_2 - K_2 g_3^{-1} \left(f'_3 - K_3 g_4^{-1} [f'_4 + K_4 e_4^*] \right) \right\} \right] \quad (4)$$

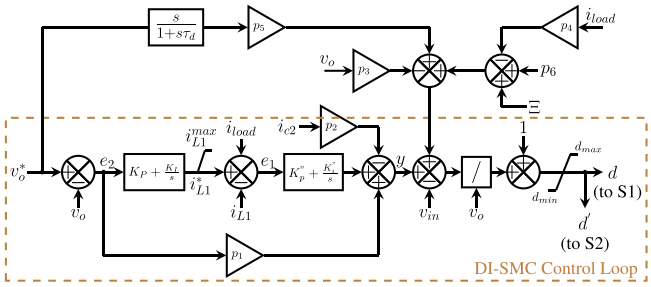


Fig. 3. Proposed ADI-BSM+NEO-FTC control strategy.

where $f'_i = f_i - \dot{h}_i(\vec{\mathbf{\Delta}})$ and $e_4^* = 0$.

$$\left.\begin{aligned} \dot{e_4} &= \overbrace{-K_i \int e_1 dt}^{f_4} + \overbrace{1}^{g_4} e_3 - \dot{h_4}(\vec{\mathbf{\Delta}}) \\ \dot{e_3} &= \overbrace{e_1}^{f_3} + \overbrace{1}^{g_3} e_2 - \dot{h_3}(\vec{\mathbf{\Delta}}) \\ \dot{e_2} &= \overbrace{\dot{v_o^*} + \frac{v_o}{RC_2} + \frac{i_{\text{load}}}{C_2} - \frac{D' I_{L1}}{C_2} + \delta_2}^{f_2} + \overbrace{\frac{D'}{C_2}}^{g_2} e_1 - \dot{h_2}(\vec{\mathbf{\Delta}}) \\ \dot{e_1} &= \overbrace{K_p\left(\dot{v_o^*} - \frac{i_{c2}}{C_2}\right) - \frac{v_{\text{in}}}{L_1} + K_i e_2 + \delta_1}^{f_1} + \overbrace{\frac{v_o}{L_1}}^{g_1} e_0 - \dot{h_1}(\vec{\mathbf{\Delta}}) \end{aligned}\right\} \quad (5)$$

In (6), $p_1 = L_1 K_I$, $p_2 = \frac{L_1}{C_2} K_P$, $p_3 = \frac{L_1 K_1}{D' R}$, $p_4 = \frac{L_1 K_1}{D'}$, $p_5 = L_1(K_P - \frac{K_1 C_2}{D'})$, $p_6 = L_1 K_1 I_{L1}$, $K''_p = \frac{L_1 K_1 K_2 C_2}{D'}$, $K''_i = K''_p K_3 K'_i$ and $\Xi = \sum_{j=1}^{4} c_j \dot{h_j}(\vec{\mathbf{\Delta}})$ $c_1 = -L_1, c_2 = \frac{L_1 K_1 C_2}{D'}, c_3 = -\frac{L_1 K_1 K_2 C_2}{D'}, c_4 = \frac{L_1 K_1 K_2 K_3 C_2}{D'}$, where D and D' $(= 1 - D)$ are the steady-state duty ratios and $I_{L1} = i^*_{L1}$ is the steady-state inductor current. The control loop of the proposed ADI-BSM technique given in Fig. 3 is a super-set of that derived using the DI-SMC technique. The term I_o in Fig. 3 is the steady-state value of the load current that is used to control the load current to mimic a battery charging characteristics. The unknown compensatory functions $h_i(\vec{\mathbf{\Delta}})$ are added in (2) in order to compensate for the effect of the uncertainty vector $\vec{\mathbf{\Delta}}$ in f_i. The compensatory term Ξ in (6) is selected independent to the plant parameters and described in the next Section III-A.

A. NEO-FTC Principle

A pseudocompensatory nonlinear sliding manifold (PSM) is introduced to derive Ξ as the control term for the robust observer-less operation. This pseudo surface $s_1 = 0$ is a combination of a nonlinear function and the main linear sliding surface $s = 0$. Nonlinear FOT-SMC demonstrated a better dynamic response than linear sliding manifold-based DI-SMC as per

$$d'_{\text{eq}} = \frac{-\left(K''_p + \frac{K''_i}{s}\right) e_1 - p_1 e_2 + p_2 i_{c2} + p_3 v_o + p_4 i_{\text{load}} - p_5 \dot{v_o^*} - p_6 + v_{\text{in}} - \Xi}{v_o}. \quad (6)$$

the literature [1]. Singularity in the equivalent control signal is a prominent problem with FOT-SMC, and thus nonsingular FOT-SMC techniques were proposed [13]. FO-SMC was proposed that showcased better dynamic performance due to the inclusion of all the state terms in the control signal [12]. An extended-order SMC is, therefore, needed where expressions of all the powers of the states are present along with their different order derivative and integral terms. PSM is selected as $s_1 = s - \left(\dot{e_3}^{\frac{\rho_2}{\rho_1}} - \rho_2 \dot{e_3}^{\frac{\rho_1}{\rho_2}}\right) - e_4$, where the terminal constants are: $\rho_2 = 2(n+2)\rho_1, \rho_1 = 2n$, for $n = 1, 3, 5, 7, \ldots$. The derivative of the PSM is: $\dot{s_1} = \dot{s} - \underbrace{\left[\frac{\rho_2}{\rho_1}\dot{e_3}^{(\frac{\rho_2}{\rho_1}-1)} - \rho_1 \dot{e_3}^{(\frac{\rho_1}{\rho_2}-1)}\right]}_{NEO-FTC\ Term\ \ddot{e}_3} \ddot{e_3} - e_3$. The NEO-FTC term is assumed equal to $\ddot{e}_3$, which will be substituted later in the next section for deriving fixed-time convergence. On solving $\dot{s_1} = 0$ for $\ddot{e}_3$ by substituting $\dot{s_1} = \dot{s} = 0$, $\ddot{e_3} = \frac{-e_3}{\left[\frac{\rho_2}{\rho_1}\dot{e_3}^{\left(\frac{\rho_2}{\rho_1}-1\right)} - \rho_1 \dot{e_3}^{\left(\frac{\rho_1}{\rho_2}-1\right)}\right]}$.

Lemma 1: Ξ is assumed as the new control variable in terms of the uncertainties, and d_{eq} is solved without considering uncertainties. By ignoring all other terms other than the uncertainties, $\dddot{e_3} = \dot{e_1} + \dot{e_2} = \dot{\delta_1} + \dot{\delta_2}$, as per (1). This implies that Ξ is chosen in the following manner to address uncertainties.

$$\Xi = \frac{\rho_1 \rho_2 e_3}{\left[\frac{\rho_2}{\rho_1}\dot{e_3}^{\left(\frac{\rho_2}{\rho_1}-1\right)} - \rho_1 \dot{e_3}^{\left(\frac{\rho_1}{\rho_2}-1\right)}\right]}. \tag{7}$$

Whenever uncertainties affect the error dynamics, the action of Ξ is effective. The compensatory term Ξ in (7) is used for the robust observer-less operation for handling the disturbances. It is independent of the system parameters similar to a conventional observer-based implementation.

It is found that the effect of the unknown disturbances appears as a scalar feed-forward term Ξ as shown in (6). Thus, instead of calling Ξ the effect of the unknown overall unmodeled disturbances, it is identified as the known overall compensatory term. Ξ is a function of known terminal constants ρ_1, ρ_2 and the error terms e_1, e_2, and this choice of selection of Ξ is based on the fixed-time convergence principle defined in (7). In case of uncertainty in the system, its effect appears in the error terms. Hence, irrespective of the level of the uncertainty, the NEO-FTC principle brings the state error trajectory back to the steady-state condition in a given fixed settling time irrespective of the initial state error conditions. It is very well known in the literature that feed-forward compensation improves the dynamic response of the system for change in the system parameters and test conditions. In this case, Ξ is an active feed-forward term that depends on the system errors, and thus based on the measure of the disturbance (need not be estimated using observer), the state trajectory returns to the steady-state in the fixed settling time. The overshoots in the voltage response are controlled based on the limits used for the control signal d_{eq} to avoid failure. Thus, the observer is not needed for this implementation. The terminal constants are selected as per the expected maximum settling time $T_s^{\max}$.

B. NEO-FTC Fixed-Time Convergence Analysis

This section describes the verification of the fixed-time convergence of the proposed NEO-FTC principle using the assumptions described as follows.

Lemma 2: It is assumed that the solution of the equation $\dot{w} = -\left[\frac{\rho_2}{\rho_1} w^{(\frac{\rho_2}{\rho_1}-1)} + \rho_1 w^{(\frac{\rho_1}{\rho_2}-1)}\right]$, where $w = \dot{e_3}$, gives the required settling time t_s. This is because the nonlinear NEO-FTC term $\dot{w}$ majorly governs the dynamics of the manifold s_1 compared to the linear DI-SMC manifold $s = 0$.

Lemma 3: A new Lyapunov candidate energy function $V_5 = \frac{w^2}{2}$ is considered.

$\dot{V_5} = w\dot{w} = -\frac{\rho_2}{\rho_1} w^{(\frac{\rho_2}{\rho_1})} - \rho_1 w^{(\frac{\rho_1}{\rho_2})}$

$\dot{V_5} = -(2V_5)^{(\frac{\rho_1}{2\rho_2})}\left[\frac{\rho_2}{\rho_1}(2V_5)^{(\frac{\rho_2}{2\rho_1}-\frac{\rho_1}{2\rho_2})} + \rho_1\right]$

$\frac{2\rho_2}{2\rho_2-\rho_1}\frac{d}{dt}\left\{V_5^{\frac{2\rho_2-\rho_1}{2\rho_2}}\right\} = (2)^{(\frac{\rho_1}{2\rho_2})}\left[\frac{\rho_2}{\rho_1}(2V_5)^{(\frac{\rho_2}{2\rho_1}-\frac{\rho_1}{2\rho_2})} + \rho_1\right]$.

$\frac{da}{dt} = \sigma_1 a^b + \sigma_2 \Rightarrow \int_0^{T_s^{\max}} dt = \int_0^{\infty} \frac{da}{\sigma_1 a^b + \sigma_2}$;

$T_s^{\max} = \int_0^1 \frac{da}{\sigma_2} + \int_1^{\infty} \frac{da}{\sigma_1 a^b} \Rightarrow \mathbf{T_s^{max}} = \frac{\boldsymbol{\sigma_1(1-b)-\sigma_2}}{\boldsymbol{\sigma_1\sigma_2(1-b)}}$. where $\sigma_1 = \left[\frac{2\rho_2-\rho_1}{2\rho_1}\right]2^{(\frac{\rho_2}{2\rho_1})}, \sigma_2 = \left[\frac{2\rho_2-\rho_1}{2\rho_2}\right]2^{(\frac{\rho_1}{2\rho_2})}, a = V_5^{\frac{2\rho_2-\rho_1}{2\rho_2}}$ and $b = \frac{\rho_2^2-\rho_1^2}{\rho_1(2\rho_2-\rho_1)}$. It is observed that the maximum settling time $T_s^{\max}$ is independent to the initial vector $\vec{\mathbf{e}}(0)$ thereby ensuring the fixed-time convergence. The overall settling time t_s, which includes effects from both the nonlinear NEO-FTC and the linear DI-SMC terms, consistently remains below $T_s^{\max}$. The expression for $T_s^{\max}$ in [16] involves computing a complex integral that includes a logarithmic term. However, $T_s^{\max}$ is a simplified and linear expression in the proposed technique. The fixed-time convergence of the proposed technique is verified in Section V, and where it is also compared with the conventional asymptotic convergent DI-SMC technique and finite-time convergent technique presented in [17].

C. Robustness Against Sensor Uncertainties

This section describes the sensor correction logic due to the overall sensor and ADC disturbances. Typically, these disturbances occur in the auxiliary power units, temperature variations of the Op-Amp signal conditioning resistors, sensor nonlinearities, noise from SMPS due to common grounds, quantization, etc. It is assumed that the ADC signal conditioning unit in the present application includes potential dividers, isolation Op-Amps, and noninverting Op-Amps. The dc relation between any sensed signal $X_{\text{act}}(V_{\text{act}}/i_{\text{act}})$ and their respective calculated ADC voltage signals V_{adc} is

$$V_{\text{adc},i} = \frac{g_{o,i} R_{m,i}}{\sum_j R_{j,i}} \left(\frac{N_{p,i} R_{b,i}}{N_{s,i}} X_{\text{act},i} \pm i_{\text{off}}\right) \frac{R_{2,i}}{R_{1,i}} + V_{\text{off},i} \tag{8}$$

where for an ith sensor (i is the sensor index): $g_{o,i}$ is the isolation Op-Amp fixed gain, $R_{m,i}/\sum_j R_{j,i}$ is the potential divider gain. For the current sensors, $N_{p,i}/N_{s,i}$ represents the CT gain for hall-effect sensors and $R_{b,i}$ is the burden resistor. $V_{\text{off},i}$ is the dc offset for ac sensed quantities like i_c. $R_{2,i}/R_{1,i}$ is the dc gain of the noninverting Op-Amp, and i_{off} is the offset dc current. The sensor calibration using a DSO and probes may give different

ADC calibrated values $V_{\text{cal},i}$ due to the nondifferential probe and calibration errors, and thus different calibrated sensor values $X_{\text{cal},i}$. The aim is to correct and represent the calculated ADC values $V_{\text{adc},i}$ using an nth order generalized polynomial function $\sum_{k=0}^{n} a_{k,i} X_{\text{act},i}^{k}$ for each sensor. The coefficients $a_{k,i}$ are to be tuned for this approximation for the hardware implementation. A PWLSQ optimization method is adopted using an error cost function OBJ defined in (9), considering the errors between the calibrated ADC data $V_{\text{cal},i}$ and the polynomial functions. Weights Γ_j $(j = 1, 2, .., 5)$ for each of the sensors are selected based on the error probability on the different ADCs, satisfying: $\sum_{j=1}^{5} \Gamma_j = 1$

$$\text{OBJ} = \min \sum_{j=1}^{5} \Gamma_j \sum_{i=0}^{N} \left(V_{\text{cal},i,j} - \sum_{k=0}^{n+1} a_{k,j} X_{\text{cal},i,j}^{k} \right)^2 \quad (9)$$

where N+1 is the total number of calibrated signal values for each of the sensors (different for each sensors). If any ADC uncertainties occur during the operation, the ADC values are corrected using the originally calibrated values using the same microcontroller. The proposed control loop action in Fig. 3 then resumes with the corrected ADC values without the need of an additional high-end DSPs. This is because the calibrated sensors values are captured during the open-loop operation, and only the polynomial coefficients are retuned for the uncertainties reducing the computational burden. In this way, the overall uncertainties due to the system linearization, parameter variations, and sensors are addressed.

D. State Estimation for Sensor Failure

This section describes the operation of the proposed technique in case of sensor failure, missing sensor data or reduced sensor operation. The state estimation technique using the WLSQ approximation is proposed where the weights are the error variances of different sensors. The state estimation based on the Gauss–Newton method with Taylor's series expansion is used to estimate the actual sensor quantities in the case of sensor failure [25]. Equation (8) can be rewritten as: $\vec{\mathbf{a}} = \mathbf{G}\vec{\mathbf{m}} + \vec{\mathbf{o}}$, where $\vec{\mathbf{a}}$ is a 5×1 known ADC calibrated voltage vector, $\mathbf{G}$ is a 5×5 gain matrix of ADC, $\vec{\mathbf{m}} = [v_{in} \quad v_o \quad i_{L1} \quad i_{\text{load}} \quad i_{c2}]^T$ is the actual measurement vector of the quantities to be estimated, and $\vec{\mathbf{o}}$ is the known respective offset vector of $\vec{\mathbf{m}}$.

Using the iterative WLSQ optimization for the Gauss–Newton method for state estimation, the actual sensor measurement estimation vector is given as follows:

$$\vec{\hat{m}}^{k+1} = \vec{\hat{m}}^{k} \underbrace{-(\mathbf{G}^{\mathbf{T}}\mathbf{R}^{-1}\mathbf{G})^{-1} \times (\mathbf{G}^{\mathbf{T}}\mathbf{R}^{-1}[\vec{\mathbf{a}} - \mathbf{G}\vec{\hat{m}}^{k}])}_{\Delta\vec{\hat{m}}^{k}} \quad (10)$$

where k is the iteration index, $\mathbf{R}^{-1} = \text{diag}(1/\sigma_1^2, 1/\sigma_2^2, \ldots, 1/\sigma_5^2)$ is the covariance inverse or weight matrix and σ_i (i = 1,2,...,5) are the variances of the measurements. The convergence criterion of (10) is: $\Delta\vec{\mathbf{m}}^{k} \leq \zeta$ where $\zeta = 0.01$. If any of the sensor(s) fail among the available sensors, those measurements are estimated based on the index of the row of the estimated sensor vector $\vec{\mathbf{m}}^{k+1}$ given in (10). Using the above recursive analysis in (10), the state estimation response for the feed-forward signals v_{in} and i_{load} is simulated. Fig. 4 describes the response of the estimated input voltage $\hat{v_{\text{in}}}$ and load current $\hat{i_{\text{load}}}$ using the state estimation technique at different converter operating conditions. The converter operating conditions include different values of actual v_{in} and i_{load}. Thus, the proposed technique can operate with reduced number of sensors, and also in sensor failure conditions, using the state estimation technique.

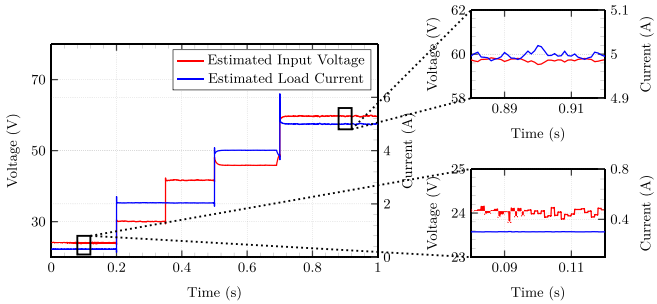


Fig. 4. Sensor state estimation graphs for input voltage and load current.

E. Scalability of the Proposed Control Technique for Higher-Order Boost-Derived Converters

In order to generalize the implementation of the proposed technique to other higher-order boost-derived topologies, eigenvalue sensitivity analysis, and modal analysis with participation factor are employed. For an nth order error state-space linearized system, the sensitivity of an eigenvalue λ_k with respect to a state matrix element A_{ij} is $\frac{\partial \lambda_k}{\partial A_{ij}} = \psi_{ki} \times \phi_{jk}$, where ψ_{ki} and ϕ_{jk} are the (k,i)th and (j,k)th elements of the left eigenvector matrix $\mathbf{\Psi}$ and the right eigenvector matrix $\mathbf{\Phi}$, respectively, for $1 \leq i, j, k \leq n$. And $\frac{\partial \lambda_k}{\partial c} = \frac{\partial \lambda_k}{\partial A_{ij}(c)} \frac{\partial A_{ij}(c)}{\partial c} = \sum_{i=1}^{n} \sum_{j=1}^{n} \psi_{ki}\phi_{jk} \frac{\partial A_{ij}(c)}{\partial c}$ gives the eigenvalue sensitivity with respect to the parameter c, where $c = L_1, L_2, C_1, C_o, r_{L1}, r_{L2}$. Based on the nature of the eigenvectors being real or complex conjugate pairs, they are divided into different modes. The complex conjugate eigenvectors are placed in the same mode. The number of modes, m is less than n. The modal analysis entails calculating participation factors that indicate, which states are influenced by these modes, meaning that every state will have a corresponding participation factor for each mode. The participation factor is given as $p_{il} = \phi_{il} \times \psi_{li}$, where i describes the ith state and l represents the lth mode. Higher the participation factor of a state, the more it is affected by a given mode or the respective eigenvectors in that mode. Thus, the participation factors for all the states of a higher (nth) order system is calculated for each eigenvectors. The sensitivity of eigenvectors to plant parameters can be estimated from eigenvalue sensitivities to the state matrix. This analysis identifies the two most affected states, enabling the control of a higher-order plant using the reduced-order principle.

In the case of CI-SEPIC converter, the proposed reduced-order control primarily considers the input inductor current and the output voltage, as these are largely influenced by the plant parameters and the system eigenvectors. Thus, using the above sensitivity and modal analysis, any higher-order dc–dc converter

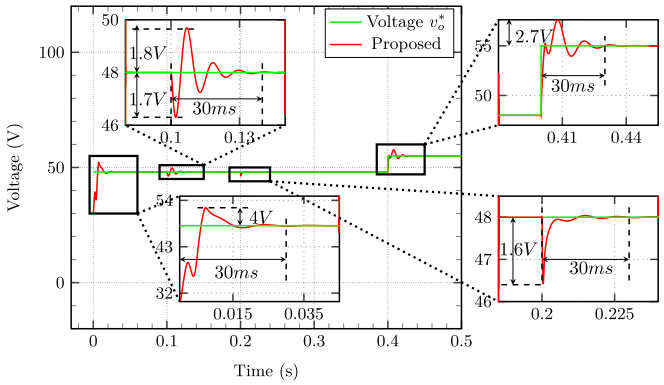


Fig. 5. Output voltage response of a Cuk converter using the proposed technique.

can be reduced to a second-order system for the proposed dual-loop implementation using the technique by considering the two most affected states. Equation (6) can be generalized as per topology. For example, the proposed control technique can be easily applied to a simple boost converter or a Cuk converter by using $L_1 = L$ and $C_2 = C$ in (6), where L and C are the input inductor and the output capacitor of the boost and Cuk converters, respectively. Fig. 5 describes the simulated output voltage response of a Cuk converter using the proposed technique, with a similar simulation test conditions-1 as that for CI-SEPIC converter mentioned in Section V.

The design procedure for the equivalent control law d_{eq} for each dc–dc converters will be similar using the I-BSC approach defined in (4) for the dc microgrid depicted in Fig. 1(a). Further, the design of the ultimate compensatory term for these dc–dc converters will also be similar as defined in (7). The effect of disturbances due to other dc–dc converters on a dc–dc converter under consideration will appear in the overall uncertainty terms δ_1, δ_2 in (1).

F. Application of the Proposed Control Technique for Solar PV MPPT

The proposed technique is scalable, and it is implemented on a boost converter for MPP extraction of PV panels as shown in Fig. 1(a). The only change that needs to be done is that the boost converter should control its input voltage i.e., the PV panel voltage for the MPP extraction. In many solar PV applications, the dc link voltage is already regulated by another converter (e.g., VSC or CI-SEPIC converter in the present case). The MPP control for the boost converter using the proposed ADI-BSM+NEO-FTC technique is a dual-loop control where the inner loop regulates the boost inductor current, which is the PV current, and the outer loop regulates the boost input voltage or the PV voltage corresponding to a value equal to MPP voltage for a given temperature and irradiance. In (2), the modifications needed are: $e_2 = v_{\text{in}}^* - v_{\text{in}}$, where v_{in}^* and v_{in} are the reference and actual boost input voltage or PV panel voltage, respectively. Model-based heuristic or meta-heuristic MPP extraction techniques are used to generate v_{in}^*. Based on this modification, the further steps to design the control loop are similar as described in Section III. This article does not discuss MPPT algorithms, as they are beyond the scope of the present study.

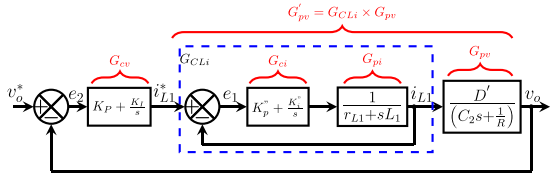


Fig. 6. Dual-loop structure for loop-shaping analysis.

TABLE II
CONTROLLER AND SYSTEM PARAMETERS

S. No.	Parameter	Value	S. No.	Parameter	Value
1	r_{L1}, r_{L2}	6 $m\Omega$, 10 $m\Omega$	10	ρ_1, ρ_2	2, 6
2	L_1	390 μH	11	C_1	1470 μF
3	L_2	780 μH	12	C_2	820 μF
4	K_P	1.65	13	f_{sw}	40 kHz
5	K_I	463	14	p_3	2.6×10^{-5}
6	K_p''	7.54	15	p_4	6×10^{-4}
7	K_i''	34391	16	p_5	5×10^{-4}
8	p_1,p_2	0.14,0.73	17	p_6	2.6×10^{-3}
9	PM_i, PM_v	85^o, 80^o	18	$\omega_{gc,i}, \omega_{gc,v}$	25 133, 1260

IV. Controller Parameter Selection

This section describes the controller parameter tuning of the control loop for the proposed technique. As described in the (6), all the parameters of d_{eq} depend on the plant parameters L_1, L_2, C_1, C_2. For enhanced robustness, a hybrid approach is adopted for parameter tuning, including the following.

1) For the PI parameters (K_p, K_i, K_p'' and K_i''), loop-shaping analysis is used.
2) For the feed-forward gains $p_1, p_2, \ldots, p_6$, adaptive feed-forward analysis is used along with-
   a) Existence condition of SMC is used with system boundary conditions to tune p_1 and p_2.
   b) Closed-loop stability analysis is used to tune remaining gains p_3, p_4, p_5, p_6.

A. Loop-Shaping Analysis

A dual-loop transfer function-based control loop for the controller tuning is described in Fig. 6. In Fig. 6, G_{pv}, G_{pi} are plant transfer functions and G_{cv}, G_{ci} are the PI controller transfer functions of the outer voltage and inner current loops, respectively. $G_{\text{CLi}} = \frac{G_{\text{ci}}G_{\text{pi}}}{1+G_{\text{ci}}G_{\text{pi}}}$ is the closed loop transfer function of the inner loop and G'_{pv} is the plant transfer function for the outer loop. The phase margins and cross-over frequencies of the inner loop ($\text{PM}_i, \omega_{\text{gc},i}$) and the outer loop ($\text{PM}_v, \omega_{\text{gc},v}$) are mentioned in the Table II. The PI parameters K_p, K_i, K_p'', and K_i'' are tuned using loop-shaping analysis with sufficient bandwidth and phase margins given in Table II.

B. Existence-Boundary Case Condition

The existence condition (11) is combined with boundary value condition, representative of the maximum and minimum variation of the converter states and inputs, given in (12) [4]. Simultaneous inequalities in (12) are solved for p_2 and p_1

$$\lim_{s\to 0} s\frac{ds}{dt} < 0 = \begin{cases} \frac{ds}{dt}_{s\to 0^+} < 0, & \mathrm{d}=0 \\ \frac{ds}{dt}_{s\to 0^-} > 0, & \mathrm{d}=1 \end{cases} \tag{11}$$

$$\left.\begin{aligned} -p_2 i_{c2}^{\min} + p_1 e_2^{\max} + K_1(e_1^{\max}+e_2^{\max}) + K_2 e_3^{\max} > v_{in}^{\min} \\ p_2 i_{c2}^{\max} - p_1 e_2^{\min} - K_1(e_1^{\min}+e_2^{\min}) - K_2 e_3^{\min} > v_{in}^{\max} - V_o \end{aligned}\right\} \tag{12}$$

C. Stability Analysis

1) Routh-Hurwitz Criterion: To further enhance disturbance rejection, the feed-forward gains of (6) are tuned adaptively. The closed-loop small-signal stability analysis is performed to tune the parameters p_3, p_4, p_5, and p_6 [4]. In the small-signal analysis, $d = d_{\mathrm{eq}}$ is substituted in (1) using (6). Also, the inputs and the error states are replaced by their steady-state and small-signal values, respectively, by ignoring disturbances. Equation (13) describes the dynamic equilibrium small-signal analysis

$$b_{21} = \frac{I_{L1}(K_P + K_p'') + p_3 V_o + p_4 I_{\mathrm{load}} - p_5 \dot{V}_o^* - p_6 + V_{ian}}{C_2(V_o - p_2 I_{L1})},$$

$$b_{23} = \frac{I_{L1} K_i''}{C_2(V_o - p_2 I_{L1})},$$

$$b_{22} = \frac{I_{L1}(K_p K_p'' + p_1 + p_3) - \frac{2V_o}{R} - I_{\mathrm{load}}}{C_2(V_o - p_2 I_{L1})},$$

$$b_{24} = \frac{I_{L1}(K_i K_p'' + K_p K_i'')}{C_2(V_o - p_2 I_{L1})},$$

$$b_{12} = -\frac{K_p K_p'' + p_1 + p_3 + p_2 C_2 b_{22}}{L_1},$$

$$b_{14} = -\frac{K_i K_p'' + K_p K_i'' + p_2 C_2 b_{24}}{L_1}$$

$$b_{11} = -\frac{r_{L1} + K_p + p_2 C_2 b_{21}}{L_1}, b_{13} = -\frac{K_i'' + p_2 C_2 b_{23}}{L_1},$$

$$b_{15} = -\frac{K_i K_i'' + p_2 C_2 b_{25}}{L_1}$$

$$b_{31} = b_{42} = b_{54} = 1, b_{32} = b_{33} = b_{34} = b_{35} = b_{41} = b_{43} = b_{44} = b_{45} = b_{51} = 0$$

$$b_{52} = b_{53} = b_{55} = 0, b_{25} = b_{23} K_i.$$

The characteristic equation of (13) is given as follows:

$$\begin{vmatrix} l - b_{11} & -b_{12} & -b_{13} & -b_{14} & -b_{15} \\ -b_{21} & l - b_{22} & -b_{23} & -b_{24} & -b_{25} \\ -b_{31} & -b_{32} & l - b_{33} & -b_{34} & -b_{35} \\ -b_{41} & -b_{42} & -b_{43} & l - b_{44} & -b_{45} \\ -b_{51} & -b_{52} & -b_{53} & -b_{54} & l - b_{55} \end{vmatrix} = 0 \tag{14}$$

where term l resembles the frequency term ($l = j\omega$). To ensure stability of the closed-loop system, the coefficients of all the powers of l in (14) must have the same sign, i.e., positive. The determinant in (14) is of the fifth order, where the coefficients of l^5 and l^0 are 1 and 54.86, respectively. The remaining four coefficients of l^4, l^3, l^2, l^1 are functions of the four unknown controller parameters p_3, p_4, p_5, p_6. Thus, these remaining four controller parameters are solved by using the four simultaneous inequalities given by solving the determinant in (14). In case the converter parameters vary, the PI loop-shaping analysis takes care of the desired converter response up to a certain extent based on the plant transfer functions, selected cross-over frequencies and the phase-margins. However, the converter performance is deteriorated for the parameter variations beyond a certain limit. Thus, the adaptive tuning of the feed-forward gains takes care of these abnormalities along with the compensatory functions to derive the proposed control technique.

2) Lyapunov Criterion: This section describes the Lyapunov stability analysis of the system considering PSM and NEO-FTC terms. Another Lyapunov candidate energy function V_6 is considered as $V_6(s_1) = \frac{s_1^2}{2}, \Rightarrow \dot{V}_6 = s_1 \dot{s_1}$. For stability, $\dot{V}_6 < 0 \Rightarrow s_1 \dot{s_1} < 0$ or s_1 and $\dot{s_1}$ should have opposite signs.

$$\dot{s_1} = \frac{ds_1}{dt} = \underbrace{\frac{\partial s_1}{\partial \vec{\mathbf{e}}} \cdot \frac{d\vec{\mathbf{e}}}{dt}}_{\text{Dot Product}} = |\cancel{\frac{\partial s_1}{\partial \vec{\mathbf{e}}}}|^{1} |\frac{d\vec{\mathbf{e}}}{dt}| \cos\theta = |\vec{\mathbf{f}}| \cos\theta$$

$$\Rightarrow \dot{s_1} = \begin{cases} \dot{s_1} > 0, & \text{for } s_1 < 0, \because |\theta| < 90^o \\ \dot{s_1} < 0, & \text{for } s_1 > 0, \because |\theta| > 90^o \end{cases}$$

This implies that s_1 and $\dot{s_1}$ always have opposite signs. This ensures reaching condition and stability of the state trajectory irrespective of any initial conditions [4]. This can be verified from Fig. 7 that the state trajectory hitting the manifold $s_1 = 0$ from the either sides always ensure $s_1 \dot{s_1} < 0$.

V. Simulation Results

The proposed observer-less ADI-BSM+NEO-FTC technique is validated using MATLAB simulation and the results are provided in this section. Table II describes the system parameters

$$\left.\begin{aligned} \frac{d\tilde{i_{L1}}}{dt} &= b_{11}\tilde{i_{L1}} + b_{12}\tilde{v_o} + b_{13}\int \tilde{i_{L1}} dt + b_{14}\int \tilde{v_o} dt + b_{15}\int\int \tilde{v_o} dt dt \\ \frac{d\tilde{v_o}}{dt} &= b_{21}\tilde{i_{L1}} + b_{22}\tilde{v_o} + b_{23}\int \tilde{i_{L1}} dt + b_{24}\int \tilde{v_o} dt + b_{25}\int\int \tilde{v_o} dt dt \\ \frac{d[\int \tilde{i_{L1}} dt]}{dt} &= b_{31}\tilde{i_{L1}} + b_{32}\tilde{v_o} + b_{33}\int \tilde{i_{L1}} dt + b_{34}\int \tilde{v_o} dt + b_{35}\int\int \tilde{v_o} dt dt \\ \frac{d[\int \tilde{v_o} dt]}{dt} &= b_{41}\tilde{i_{L1}} + b_{42}\tilde{v_o} + b_{43}\int \tilde{i_{L1}} dt + b_{44}\int \tilde{v_o} dt + b_{45}\int\int \tilde{v_o} dt dt \\ \frac{d[\int\int \tilde{v_o} dt dt]}{dt} &= b_{51}\tilde{i_{L1}} + b_{52}\tilde{v_o} + b_{53}\int \tilde{i_{L1}} dt + b_{54}\int \tilde{v_o} dt + b_{55}\int\int \tilde{v_o} dt dt \end{aligned}\right\} \tag{13}$$

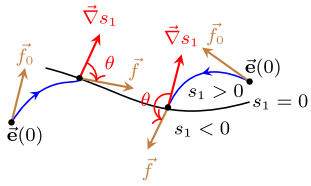


Fig. 7. Sliding manifold.

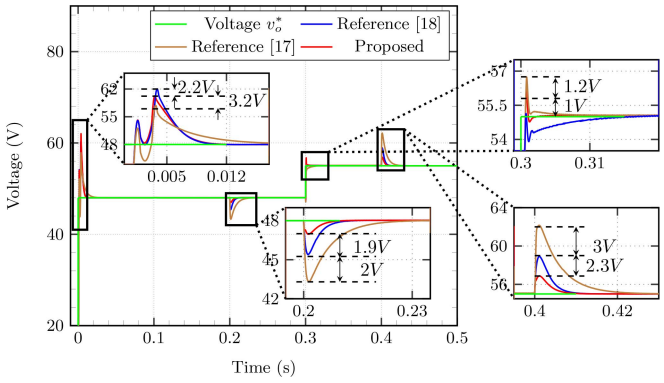


Fig. 8. Comparison of the output voltage response of the CI-SEPIC converter for the test conditions-1: proposed technique versus control techniques mentioned in [17] and [18].

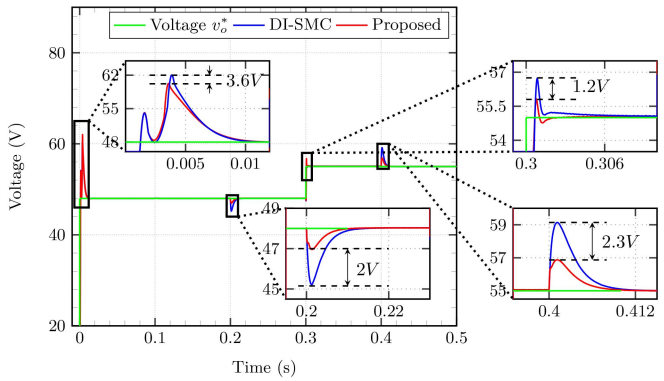


Fig. 9. Comparison of the output voltage response of the CI-SEPIC converter for the test conditions-1: proposed control technique versus conventional DI-SMC technique.

and the controller tuned parameters considered for the simulation analysis. The simulation was done for two sets of test conditions as benchmark settings, named test conditions-1 and test conditions-2. Test conditions-1 are given as follows:

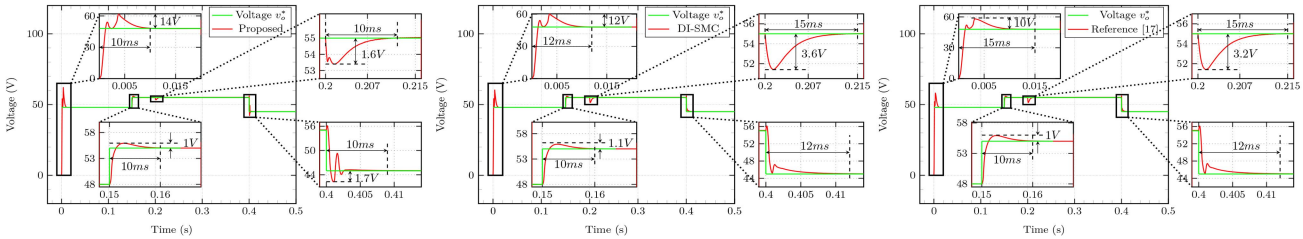
1) At $t = 0.1$ s, v_{in} is changed from 24 to 30 V.
2) Load $i_{\text{load}} = 4.1$ A for $v_o^* = 48$ V is added at $t = 0.2$ s and is removed at $t = 0.4$ s for $v_o^* = 55$ V.
3) At $t = 0.3$ s, v_o^* is changed from 48 to 55 V.
4) At $t = 0.2$ s and at $t = 0.3$ s, ΔL or L_1 and L_2 are increased by 20% and ΔC or C_2 is decreased by 30%, respectively.

Fig. 8 describes the output voltage response of CI-SEPIC converter for the test conditions-1 using the proposed technique and the control techniques mentioned in [17] and [18]. Fig. 9 describes the response of the output voltage v_o for the test conditions-1 by using the proposed technique and the conventional DI-SMC control technique. Fig. 10 describes the simulation verification of the fixed-time convergence in the proposed technique of the CI-SEPIC for test conditions-2 mentioned as follows:

1) v_{in} changes from 24 to 30 V at $t = 0.1$ s.
2) i_{load} changes from $i_{\text{load}}^{\text{min}} = 0.2$ A to 4.5 A, 1.13 A, and 2.3 A at $t = 0.2$ s, $t = 0.3$ s and $t = 0.4$ s, respectively.
3) v_o^* is changed from 48 to 55 V and 48 V at $t = 0.15$ s and $t = 0.4$ s, respectively.

The simulation test conditions 1 and 2 are varied to demonstrate the performance of the proposed method against traditional techniques and to confirm fixed-time convergence. Fig. 10 describes the output voltage response of CI-SEPIC using the proposed technique, the conventional DI-SMC technique, and the control technique defined in [17] for the test conditions-2. The proposed technique in Fig. 10(a) has a constant settling time of 10ms despite the load and reference changes thereby proving the fixed-time convergence. Fig. 10(b) and (c) illustrates the output voltage response of CI-SEPIC using the traditional DI-SMC technique, which shows asymptotic convergence, and the finite-time convergent control method detailed in [17], correspondingly. Table III describes the analytical comparison of the proposed technique and the control technique described in key references for the output voltage dynamics for the same test conditions as in Figs. 8 and 9. It is observed that the proposed technique outperforms the conventional DI-SMC technique and method given in [17], for all the test conditions. The method presented in [18] exhibited a slight enhancement in overshoot during the initial transient and when the reference changes, but it required a longer settling time. The proposed method achieves a notable decrease in both overshoot and undershoot, ensuring fixed-time convergence despite changes in load and parameter variations. It is thus concluded that the response of the converter using the proposed ADI-BSM+NEO-FTC technique is superior than that of the conventional PI-based technique and the control methods mentioned in the key references, in terms of the dynamic performance.

Figs. 11(a)–13(b) are the simulation results of CI-SEPIC using test conditions-1. Fig. 11(a) describes the input side inductor current response of the converter using the proposed ADI-BSM+NEO-FTC control technique. It can be seen from the figure that the average value of the inductor current tracks the reference inductor current generated by the outer output voltage control loop. The load current and output voltage responses of the converter using the proposed technique are depicted in Fig. 11(b). Fig. 11(c) describes the duty ratio signal response of the converter. The input side inductor current error and the output voltage error waveforms of the converter are described in Fig. 12(a). Waveform of the integral error term e_3 is given in Fig. 12(b). Fig. 12(c) describes the response of the control signal y, as shown in Fig. 3. Fig. 13(a) and (b) describes the ultimate compensatory term Ξ and the outer voltage loop Bode plots, respectively. From the simulation results, it is evident that the converter showcases the desired control characteristics.

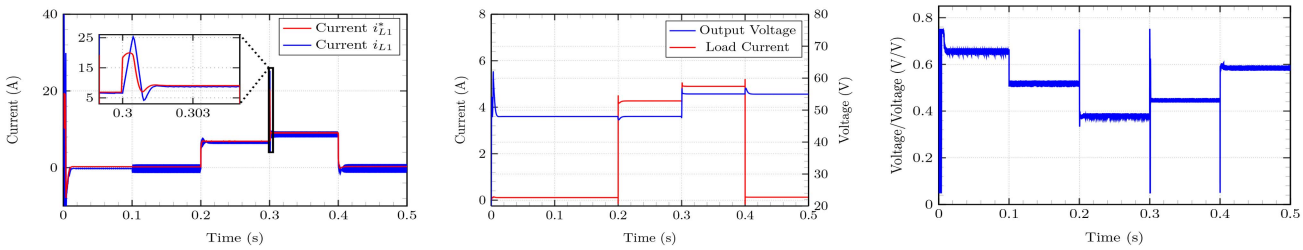


(a) (b) (c)

Fig. 10. Verification of the fixed-time convergence in the output voltage response for the test conditions-2. (a) Proposed technique. (b) Conventional DI-SMC technique. (c) Control technique in [17].

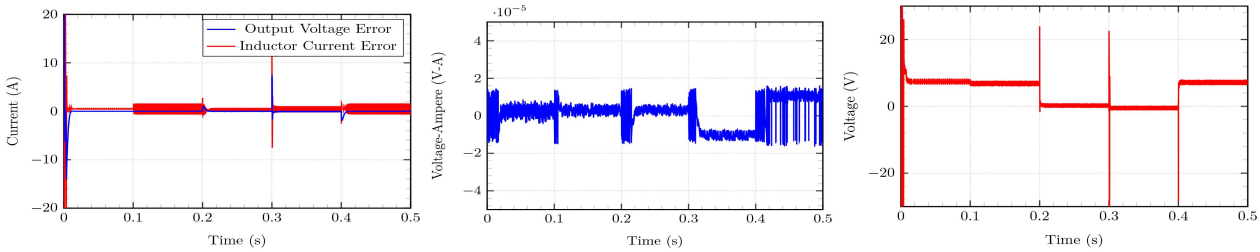
TABLE III
SIMULATION COMPARISON OF VARIOUS CONTROL TECHNIQUES

Test Conditions	Reference	Rise Time t_r(ms)	Settling Time t_s(ms)	Overshoot or Undershoot $M_p(V)$
Initial Condition (at $t = 0$s): $i_{\text{load}} = 0.25$A, at $V_{in} = 24V$, $v_o^* = 48V$.	Conventional DI-SMC	5	15	15.6
	Reference [18]	7	35	8.8
	Reference [17]	5	15	14.2
	Proposed	**5**	**10**	**12**
Load addition: $i_{load} = 0.25A$ to $4.1A$ at $t = 0.2s$, L increased by 20%, at $V_{in} = 24V$, $v_o^* = 48V$.	Conventional DI-SMC	2	30	4.9
	Reference [18]	3	20	2.9
	Reference [17]	3	25	3
	Proposed	**3**	**10**	**1**
Reference change: $v_o^* = 48V$ to $55V$ at $t = 0.3s$, C decreased by 30%, at $V_{in} = 30V$, and $v_o^* = 48V$.	Conventional DI-SMC	2	20	2.2
	Reference [18]	5	35	0.8
	Reference [17]	2.5	15	3.5
	Proposed	**3**	**10.2**	**1.2**
Load removal: $i_{load} = 0.41A$ to $0.25A$ at $t = 0.4s$, at $V_{in} = 30V$, at $v_o^* = 55V$.	Conventional DI-SMC	5	27	7.3
	Reference [18]	2	20	4.3
	Reference [17]	2	22	4.3
	Proposed	**2**	**10**	**2**



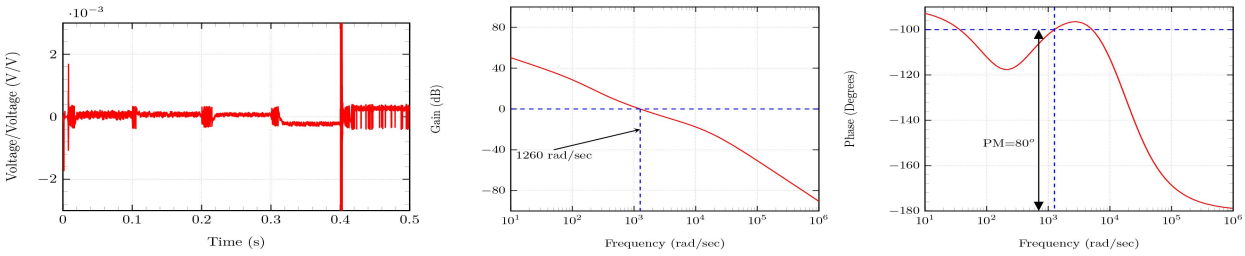
(a) (b) (c)

Fig. 11. Simulation results of the converter using the proposed technique for the test conditions-1. (a) Input-side inductor current. (b) Load current and output voltage. (c) Duty ratio.



(a) (b) (c)

Fig. 12. Simulation Results of the converter using the proposed technique for the test conditions-1. (a) Input-side inductor current and output voltage error. (b) Integral error e_3. (c) Control signal y.



(a) (b)

Fig. 13. Simulation results of the converter using the proposed technique for the test conditions-1. (a) Ultimate compensatory term Ξ . (b) Output voltage loop bode plots.

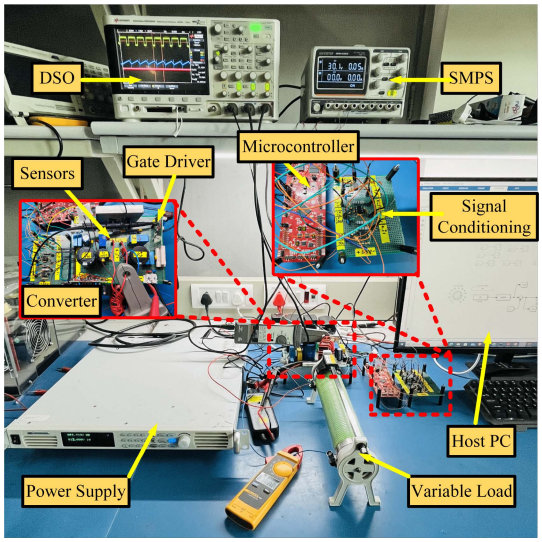


Fig. 14. Hardware setup.

TABLE IV
HARDWARE SYSTEM PARAMETERS

S. No.	Component Description	Part No./Rating
1	SiC MOSFET	NTHL080N120SC1: 200 V, 20 A
2	Hyperfast Diode	STTH2002DI: 200 V, 20 A
3	Dual OP-Amp, Isolated Gate Driver	MCP6477: 2 V 350 μA, TLP350: 24 V, 20 mA
4	MOSFET Snubbers	R=23 Ω 10 W, C=1 nF
5	Linear Regulator ICs	LM 7815, LM 7915: 0–30 V
6	SMPS-1, SMPS-2	0–30 V, 2 A and 0-5 V, 1 A
7	LEM Current Sensor	LA 25-P: $\pm$15 V, 100Ω burden, 1:1000 turns CT
8	TI Delfino Microcontroller	F28379D: 200 MHz dual C28$\times$CPU, 16/12-bit ADC
9	Programmable dc Power Supply	150V, 10 A

TABLE V
STEADY-STATE TEST RESULT DESCRIPTION

Cases \ Fig.	15(a)	15(b)	15(c)	15(d)	15(e)	15(f)
V_{in} (V)	32	43	65	16	49	56
$V_o^*(V)$	30	55	20	48	45	48
i_{load} (A)	4.8	11	0.33	0.17	7	6.6

VI. HARDWARE RESULTS

The proposed DI-SMC technique is implemented on a hardware prototype of a 1 kW CI-SEPIC converter developed in the lab. The hardware is developed on PCBs and are classified as follows: 1) Power and Sensing Board. 2) Signal Conditioning Board. 3) Gate Driver Card 4) Power Supply Units. 5) Microcontroller Unit. 6) Coding Platform. Fig. 14 showing the overall hardware setup. The power board includes the CI-SEPIC PCB board with sensors, heat sink, NTC, fuse, MOSFET and snubbers, etc. Isolated box-type CT hall-effect current transducers LA-25P are used for sensing all the currents. The signal conditioning board includes MCP6477 dual Op-Amp ICs operating in noninverting amplifier mode with capacitive filters used to process the signals sensed from the power board and sent to the microcontroller. The output of the current sensor employed for the output capacitor is dc shifted using differential Op-Amp configuration to match the ADC sensing range (0–3.3 V). The gate driver card includes TLP350 with provision of the negative bias supply for driving the MOSFETs of the power board by amplifying the ePWM signals from the microcontroller.

The power supply units include a 1.5 kW dc power supply for powering the converter. The microcontroller unit includes Texas Instruments' F28379D in single ended mode (12-bit ADC) digital controller. The coding platform-Embedded coder support package in MATLAB is used for programming the microcontroller using the host PC. Table IV provides the parameters of the hardware system and their ratings. The converter is tested for a constant power load of 1 kW to implement battery charging characteristics as per Fig. 1(a), by regulating the output voltage and the load current using I_o.

A. Steady-State Hardware Results Analysis

Fig. 15(a)–(e) describes the closed-loop steady-state hardware results of the converter using the proposed control technique for six different test cases described in Table V. The CI-SEPIC converter is tested in the buck mode ($D^{\min} \leq D < 0.5$), boost mode ($0.5 < D \leq D^{\max}$) and transition mode ($D = 0.5$) upto 600 W. Table VI describes the comparison of the measured system parameters of the converter with the calculated system parameters using the mathematical values.

B. Transients Hardware Results Analysis

The hardware is excited with various transient test conditions with load variations, change in the reference output voltage, change in the input voltage, and change in inductances using

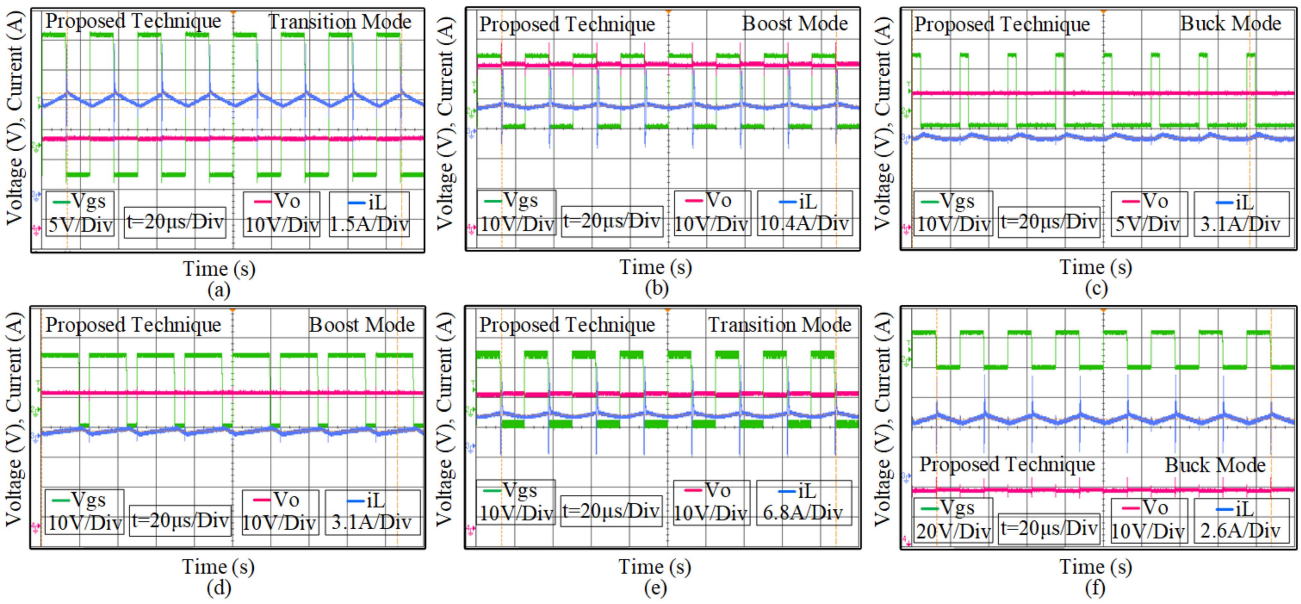


Fig. 15. Steady-state hardware results using the proposed technique for: (a) $V_{\text{in}} = 32$ V, $V_o^* = 30$ V, $i_{\text{load}} = 4.8$ A; (b) $V_{\text{in}} = 43$ V, $V_o^* = 55$ V, $i_{\text{load}} = 11$ A; (c) $V_{\text{in}} = 65$ V, $V_o^* = 20$ V, $i_{\text{load}} = 0.33$ A; (d) $V_{\text{in}} = 16$ V, $V_o^* = 48$ V, $i_{\text{load}} = 0.17$ A; (e) $V_{\text{in}} = 49$ V, $V_o^* = 45$ V, $i_{\text{load}} = 7$ A; (f) $V_{\text{in}} = 56$ V, $V_o^* = 48$ V, $i_{\text{load}} = 6.6$ A.

TABLE VI
STEADY-STATE HARDWARE RESULTS ANALYSIS

Fig. No.	Measured Value			Calculated Value		
	D (V/V)	I_{L1} (A)	Δi_{L1} (A)	D= $\frac{V_o}{V_{\text{in}}+V_o}$	I_{L1}= $\frac{DI_{\text{load}}}{(1-D)}$	Δi_{L1}= $\frac{V_{\text{in}}\,D}{f_{\text{sw}}\,L_1}$
15(a)	0.495	4.71	0.8	0.5	4.5	0.97
15(b)	0.562	9.36	1.04	0.6	9.5	0.982
15(c)	0.23	0.062	1.2	0.2	0.1	1.1
15(d)	0.75	0.47	1.7	0.75	0.5	1.78
15(e)	0.49	7	1.67	0.485	6.5	1.2
15(f)	0.462	5.2	1.3	0.46	5.7	1.035

a switched-resistor auxiliary winding. Fig. 16(a)–(f) describes the output voltage transient response of the converter for six different worst case test conditions in boost mode to verify the proposed technique. For the transient and steady-state hardware testing, the bandwidth of the outer loop voltage controller for the proposed and the conventional technique is kept slower than that of the simulation results for better analysis of the responses in the hardware results.

Case-1: Sudden Load Addition: The converter is loaded with $i_{\text{load}} = 4.5$ A from $i_{\text{load}}^{\text{min}} = 0.2$ A with $v_o^* = 48$ V at $V_{\text{in}} = 25$ V. It can be seen in Fig. 16(a) that the undershoot is almost 5 V with settling time of 0.16 s. A minimum load of $i_{\text{load}}^{\text{min}} = 0.2$ A is kept for the converter to avoid uncontrolled phase of output voltage, as the CI-SEPIC converter is a boost-derived dc–dc converter.

Case-2: Sudden Load Removal: In this case, i_{load} is reduced from 4.5 to 0.2 A with $v_o^* = 48$ V at $V_{\text{in}} = 35$ V. From Fig. 16(b), it can be seen that the maximum overshoot is 5.5 V with settling time of 0.165 s.

Case-3: Sudden Load Addition and Input Change: This condition is used to evaluate the converter performance for a sudden change in the input supply side, which closely mimics the momentary external fault in the dc microgrid depicted in Fig. 1(a). The converter is loaded to $i_{\text{load}} = 5$ A from $i_{loaad}^{\text{min}} = 0.2$ A followed by reduction in V_{in} from 20 to 10 V at $v_o^* = 60$ V. It can be seen from Fig. 16(c) that the maximum undershoot is 8 V for the load addition. As the minimum input voltage $V_{\text{in}}^{\text{min}} = 12$ V (due to $D^{\text{max}} = 0.75$), the converter safely operates in open loop mode with D^{max} without huge transients and with a settling time of around 0.17 s.

Case-4: On-Load Reference Change: v_o^* is increased from 45 to 60 V. The input voltage V_{in} is 26V with $i_{\text{load}} = 4.5$ A. It can be seen in the Fig. 16(d) that the overshoot is 6 V for the v_o^* change on-load and the settling time is around 0.16 s.

Case-5 and 6: Change in Parameters and Reference Change: Case-5 and case-6 primarily define the converter performance in case of internal faults including the converter parameter changes. These cases describe the comparison for the proposed technique versus the DI-SMC technique for the sudden output reference voltage change and reduction in the coupled inductances L_1 and L_2. In order to show sudden reduction in the coupled inductances, an additional coil is wound across the common inductor core and connected to a resistor using an another controlled MOSFET [26]. The resistance value and power rating of this resistor are selected in such a way that the current induced in the coil reduces the required magnetizing current and the inductances by 25%–30%. The converter is supplied with $V_{\text{in}} = 25$ V with $i_{\text{load}} = 2A$. v_o^* is increased from 51 to 60 V and the additional MOSFET is turned ON simultaneously. It can be seen that the proposed technique demonstrates better dynamic performance as in Fig. 16(e) than the conventional DI-SMC

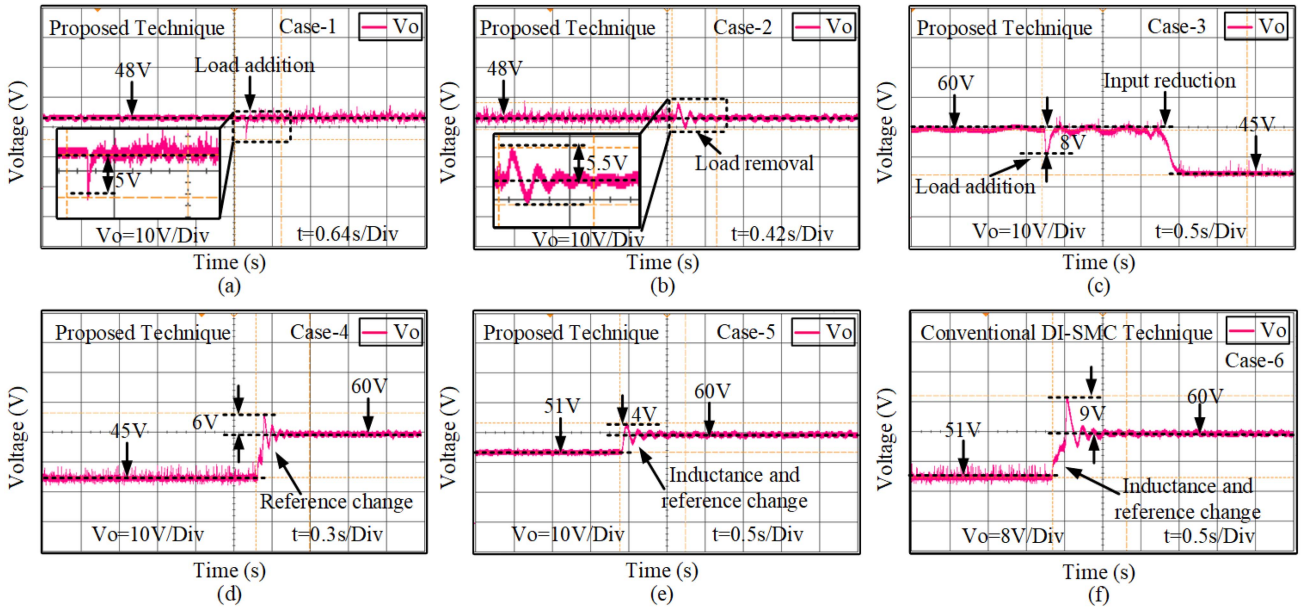


Fig. 16. Transient hardware results of the CI-SEPIC converter using the proposed technique for (a) Case-1: Load addition i_{load} from 0.2 A to 4.5 A at $v_o^* = 48$ V and $v_{\text{in}} = 25$ V; (b) Case-2: Load removal i_{load} from 4.5 A to 0.2 A at $v_o^* = 48$ V and $v_{\text{in}} = 35$ V; (c) Case-3: Load addition with input change i_{load} from 0.2 A to 5 A and v_{in} from 20 V to 10 V at $v_o^* = 60$ V; (d) Case-4: On-load reference change v_o^* from 45 V to 60 V at $v_{\text{in}} = 26$ V and $i_{\text{load}} = 4.5$ A; Case-5: Change in Reference v_o^* from 51 V to 60 V and parameters $\Delta L_1 = \Delta L_2 = 20\%$ decrease at $v_{\text{in}} = 25$ V and $i_{\text{load}} = 2$ A using (e) Proposed technique and (f) Conventional DI-SMC technique.

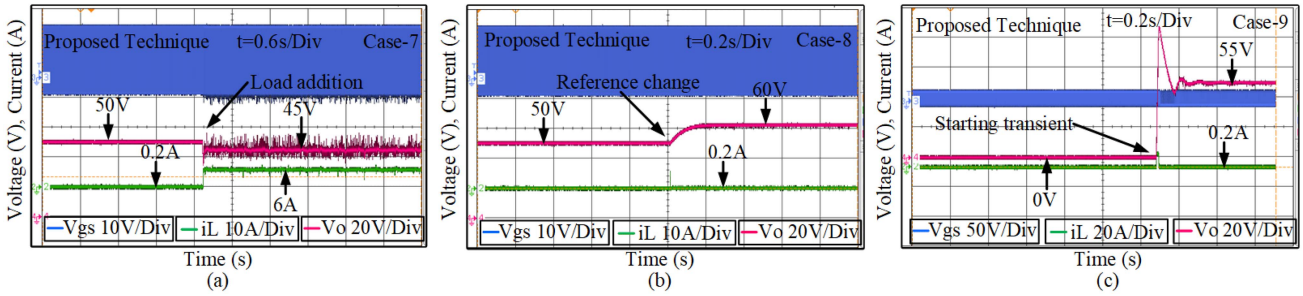


Fig. 17. Transient hardware results of the CI-SEPIC converter using the proposed technique for (a) Case-7: Huge load addition $i_{\text{load}} = 0.25$ A to $i_{\text{load}} = 6$ A and at reference $v_o^* = 50$ V and $v_{\text{in}} = 17$ V; (b) Case-8: Reference change $v_o^* = 50$ V to $v_o^* = 60$ V at $v_{\text{in}} = 33$ V and $i_{\text{load}} = 0.25$ A; (c) Case-9: Starting transients $v_o^* = 0$ V to $v_o^* = 55$ V at $v_{\text{in}} = 25$ V and $i_{\text{load}} = 0.2$ A.

method as in Fig. 16(f) for the same operating conditions. The proposed technique achieves an output voltage response settling time of approximately 0.17 s, whereas the conventional DI-SMC technique takes about 0.6 s.

Case-7: Load Addition Beyond the Rating: This case is used to depict the converter performance in case of load side external short circuit faults. The load is increased from $i_{\text{load}} = 0.25$ A ($R = 19.5\ \Omega$) to $i_{\text{load}} = 6$ A at the output voltage reference of $v_o^* = 50$ V and $v_{\text{in}} = 17$ V. As the maximum input current rating of the programmable power supply is set to 6 A and the load demands 7.6 A ($D = 0.67$, $i_{\text{load}} = 2.6$ A and $i_{L1}^* = 7.6$ A), the programmable power supply provides reduced power to the converter. It is observed in Fig. 17(a) that the input inductor current rises from 0.2 A to the maximum current of 6 A and v_o reaches 45 V using the proposed ADI-BSM+NEO-FTC technique with a settling time of around 0.16 s. Thus, the output voltage falls due to reduced power and the input current is limited to maximum current rating 6 A. Thus, in case of fault at the load side or external faults, the CI-SEPIC converter safely operates at the reduced power. The blue waveform in Fig. 17 and the green waveform in Fig. 15 show the gate driver pulses V_{gs} supplied to the MOSFET, which varies from $+19$ to -5 V.

Case-8: Reference Output Voltage Change on No-load: In this case, the converter is tested using the proposed technique for increase in the output voltage reference. v_o^* is increased from 50 to 60 V at $v_{\text{in}} = 33$ V and at the minimum load of $i_{\text{load}} = 0.25$ A. It is seen in Fig. 17(b) that the settling time is around 0.17 s.

Case-9: Starting Transient: This case represents the starting transient of the CI-SEPIC converter, where the input voltage is applied as step change from 0 to 25 V with $v_o^* = 55$ V. The converter takes around 0.18 s to reach steady state as seen in Fig. 17(c).

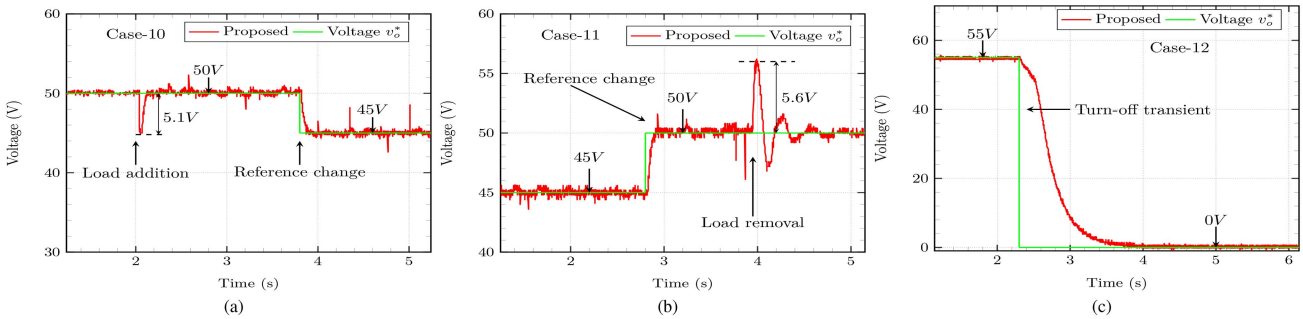


Fig. 18. Hardware results for the CI-SEPIC converter using the proposed control techniques for (a) Case 10: Load addition $i_{\text{load}} = 0.25$ A to $i_{\text{load}} = 3.5$ A, reference change $v_o^* = 50$ V to $v_o^* = 45$ V at $v_{\text{in}} = 33$ V; (b) Case 11: Reference change $v_o^* = 45$ V to $v_o^* = 50$ V, load removal $i_{\text{load}} = 3.5$ A to $i_{\text{load}} = 0.25$ A at $v_{in} = 33$ V; and (c) Case 12: Converter turn OFF $v_o^* = 55$ V to $v_o^* = 0$ V at $i_{\text{load}} = 0.25$ A and $v_{\text{in}} = 33$ V.

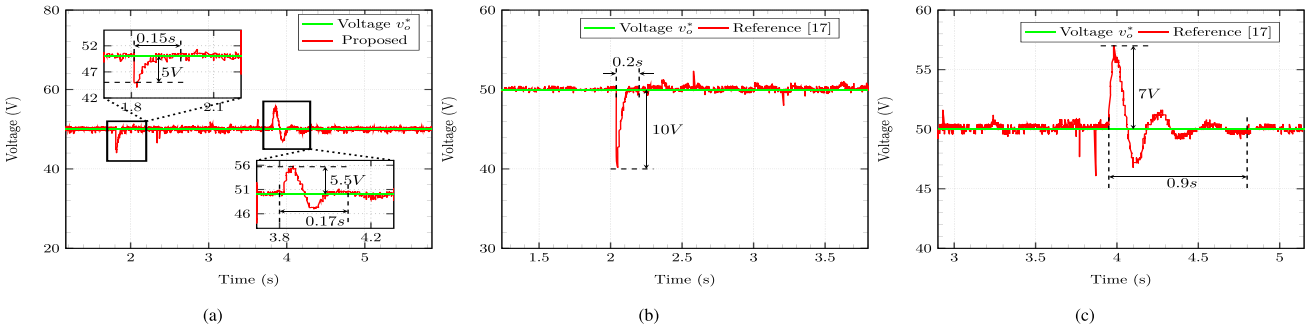


Fig. 19. Hardware comparison of the control techniques for $v_o^* = 50$ V, $v_{\text{in}} = 33$ V and $i_{\text{load}} = 3.5$ A addition and removal: (a) Proposed technique; (b) and (c) Conventional technique in [17].

Hardware results in Figs. 18–19(c) are plotted using the DSO exported CSV data to show the comparison of the proposed technique with state of art on a similar scale for ease of dynamic response comparison.

Case-10: Load Addition and Reference Change: In this case i_{load} is increased from 0.2 to 3.5 A followed by reference change $v_o^* = 50$ V to $v_o^* = 45$ V at $v_{ian} = 33$ V. It can be seen in Fig. 18(a) that the settling time for both the transients is around 0.16 s.

Case-11: Load Removal and Reference Change: In this case i_{load} is reduced from 3.5 to 0.2 A followed by reference change from $v_o^* = 45$ V to $v_o^* = 50$ V at $v_{\text{in}} = 33$ V. It can be seen in Fig. 18(b) that the converter takes around 0.17 s to reach the new steady states.

Case-12: Turn-Off Transients: This case in Fig. 18(c) includes the turn-OFF transients of the converter when v_o^* is reduced as step change from 55 to 0 V at $i_{\text{load}} = 0.25$ A and $v_{\text{in}} = 33$ V. This scenario evaluates the converter's performance under fault conditions that require disconnection from the dc microgrid. In case the CI-SEPIC converter is turned OFF due to some faults, the other converters of the dc microgrid in Fig. 1(a) share the currents according to the droop characteristics to supply the load.

Fig. 19 illustrates the transient output voltage waveforms of the CI-SEPIC converter examined with the proposed technique depicted in Fig. 19(a) as well as the control method detailed in [17] shown in Fig. 19(b) and (c), for comparison purpose. The test condition includes: addition and removal of load of $i_{\text{load}} =$ 3.5 A from 0.2 A at $v_o^* = 50$ V and $v_{\text{in}} = 33$ V. It can be seen in Fig. 19(a) that the proposed technique takes around 0.15 s with 5 V undershoot for the load addition, and 0.17 s with 5.5 V overshoot for the load removal. The control technique in [17] takes around 0.2 s with 10 V undershoot for the load addition and 0.9 s with 7 V overshoot for the load removal, respectively.

Thus, it is concluded that the converter demonstrated the desired steady-state and dynamic response during all test conditions and parametric variation disturbances. Moreover, the proposed control method enhances the dynamic response relative to the traditional DI-SMC approach, also broadening the operational range of the converter. Further, the settling time of the proposed technique for the hardware results is mostly 0.15–0.17 s irrespective of the test conditions, thereby ensuring fixed-time convergence.

VII. Conclusion

A hybrid dual-loop ADI–BSM control technique is described in this article with observer-less mitigation of uncertainties using a pseudo nonlinear sliding manifold. The PSM is a nonsingular extended-order fixed-time convergent manifold. Further, the ADC and sensor uncertainties are handled using a PWLSQ convex optimization technique. An adaptive feed-forward hybrid controller tuning approach is also described that involves loop-shaping analysis, boundary value conditions, and

closed-loop stability analysis. CI-SEPIC converter demonstrated significantly improved dynamic response against parameter variations and changes in load, input, and reference values. Hardware and simulation test results demonstrated the claimed advantages of the proposed technique for different test conditions compared to the conventional PI-based DI-SMC control technique. In addition, the proposed approach is a scalable, reduced-order method that can be applied to higher-order dc–dc converters, utilizing the WLSQ iterative state estimation in the event of sensor failure. The proposed control technique improves the dynamic response of the CI-SEPIC converter but at the expense of increased computations and complexity. Potential directions for future research could involve broadening the proposed control method to encompass hierarchical control of dc microgrids incorporating multiple dc–dc converters, without relying on observers.

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