Modeling and Design of Load Current Based Adaptive Voltage Positioning (AVP) Control for Multiphase Buck Converter Using Digital Current Estimation Algorithm

Lingyun Li, Shen Xu, Haiqing Zhang, Yijie Qian, and Weifeng Sun, *Senior Member, IEEE*

***Abstract*—This article proposes a load current-based adaptive voltage positioning (AVP) control scheme, which applies the load current as the current injection information directly instead of the inductor current feedback of the existing research, the proposed architecture does not need the inner current loop and the entire loop bandwidth only depends on the voltage loop, so the control bandwidth is increased and the transient speed is enhanced. The small signal model is proposed, including the modelling of the closed-loop output impedance and the design process of the loop compensators. Besides, since the load current is hard to sample in the high-power system, the digital load current estimation algorithm is proposed, to calculate the load current by digital controllers and used in the proposed AVP control. The proposed algorithm is constructed in field-programmable gate array (FPGA) and is applied on the 4-phase buck system, the maximum load step of 100 A is tested with the current slew rate of 370 A/μs, the voltage tolerance window is 40 mV ($R_{LL} = 0.4$ mΩ) and the system recovery time is only 3 and 7 μs under the load step-up and step-down respectively. The proposed algorithm is compared with the commonly used active droop AVP control and AVP in constant ON-time control, to prove its fast transient response.**

***Index Terms*—Adaptive voltage positioning (AVP), constant output impedance, digital control, load current estimation, voltage regulator module (VRM).**

I. INTRODUCTION

NOWADAYS, the rapid development of artificial intelligence, 5G, etc. has caused the power consumption of datacentre servers to become increasingly large, the current and transient speed of the processors become higher and higher. To reduce the voltage spike and decrease the system recovery time when the load step transient occurs, adaptive voltage positioning (AVP) control is applied in the voltage regulator controller [1]. The concept is to control the output voltage level according to the load current that is higher than the minimum value at the heavy load and lower than the maximum value at the light, and then construct a voltage tolerance window. Fig. 1 shows the comparison of AVP and non-AVP control, the entire voltage tolerance window is utilized for the voltage undershoot or overshoot during load step transient, thus reducing the requirement of the output capacitors [2].

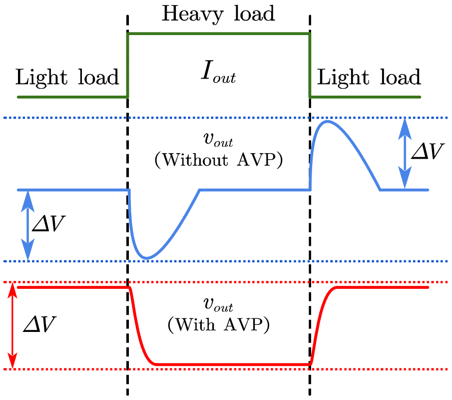

Fig. 1. Transient performance of the output voltage without and with AVP control.

The essence of the output voltage level variation is to follow the change of the load current. However, due to the inefficient and complicated load current sensing technique, the inductor current is used to construct the AVP control loop in the existing research. In [3], [4], and [5], the active droop AVP control is proposed which still be popularly used in the nowadays' research and products. It uses the feedback inductor current to construct the inner current loop, and realises the constant closed loop output impedance by the proper compensation. Although the active droop method is an efficient and stable approach to achieve the AVP control, the entire loop bandwidth is limited by the inductor current feedback scheme, it is hard to realise the high bandwidth control. The limitation of its loop bandwidth is analysed in detail in Section II. In [6], the time-optimal control (TOC) is combined with the active droop method to achieve the

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fast transient control. This method uses the active droop AVP control loop in the steady state and switches to TOC control in the transient state, so it requires complex nonlinear control logic. In addition, this combination of linear and nonlinear solutions does not fundamentally optimize the response performance of the AVP control loop. The peak current AVP control is proposed in [7] and the corresponding on-chip solution is proposed in [8]. However, this approach needs the extra offset-cancellation loop, which makes the loop design complicated. Besides, the peak current mode control is not good for high bandwidth design because of its complex poles at half switching frequency. Although the slope compensation is often applied to solve the complex poles issue, it is a compromise between the transient response and the slope of the slope compensation, and therefore the transient response speed may be affected. In [9], [10], and [11], the AVP scheme for constant ON-time (COT) control is proposed, but it utilizes the nonlinear characteristic of COT control for AVP design, which is not suitable for pulsewidth modulation (PWM) controlled voltage regulator module (VRM) system. Also, as in the case of the inductor current-based AVP in PWM control, the inductor current information is fed back to realise the AVP function, the slope of the inductor current limits the response speed. The AVP control based on input current is proposed in [12], which uses the sensed input current for loop compensation to construct the constant closed-loop output impedance. However, the extra input current sensing circuit is needed which increases the design complexity and reduces the system efficiency, the entire loop bandwidth is also limited, so it has not been widely used.

To increase the loop bandwidth and enhance the transient speed, this article proposes a load current-based AVP control scheme, which applies the load current as the current injection information directly instead of the inductor current feedback, so the proposed load current-based AVP does not need the inner current loop and the entire loop bandwidth only depends on the voltage loop, the high bandwidth control can be realised. Some works research the load current injection strategies, as which presented in [13], [14], [15], and [16]. Those methods are based on the analog sampling approaches, the difference between [13] and [14], [15], [16] is that a resistor is used to sample the capacitor current in [13] while the operation amplifier circuit is used in [14], [15], and [16]. However, the analog sampling-based injection strategies require extra complex sampling circuits, which increase the design complexity and decrease the power density, the extra parasitic components are introduced which impact the estimation accuracy. Besides, the noise is a serious issue under the sampling approach, which makes the load current injection strategy have poor stability. Also, the strategy in [14], [15], and [16] fails to consider the effect of capacitors' equivalent series inductance (ESL) when using the operation amplifier to sample the capacitor current. However, the effect of ESL cannot be ignored at the large load step with a fast slew rate transient. Although the ESL effect can be taken into account by using the resistor in series in [13], the power loss on the resistor is huge in the high-power application. Therefore, to solve the issue that it is difficult to sense the load current in the high-power VRM, this article proposes a digital load current estimation algorithm. The proposed current estimation algorithm only requires sampling the input, output voltage and the switching node voltage level, and estimates the load current through a digital filter, which has higher compatibility and can be well applied in high-power VRM system. The measurement of the switching node voltage is an important part of digital current estimation and it affects the estimation accuracy of the inductor current. In [17], the voltage at the switching node is directly sampled by an analog-to-digital converter (ADC). However, the switching node voltage has serious issues with noise which are not good for the current estimation, Besides, sampling the switching node voltage requires the ADC with a very fast sample rate. Otherwise, the switching ON and switching OFF moments cannot be sampled accurately. In [18], it is giving up to sample the switching node voltage directly but to use the PWM signal inside the digital controller. This approach avoids the use of high-speed ADCs and has no impact on noise, but the duty cycles of the PWM signal and the actual switching node voltage are not exactly the same because of Miller's platform, which results in the estimation error. The most effective way so far is to use a comparator to convert the switching node voltage to a one-bit digital signal, and input it to the digital controller [19], [20], which has been also applied in this article. In conclusion, the proposed load current-based AVP control has a high control bandwidth to achieve a fast transient response, and the load current estimation eliminates the need for complex current sampling, which can be easily implemented by digital controllers. The overall structure of the proposed load current-based AVP control is shown in Fig. 2.

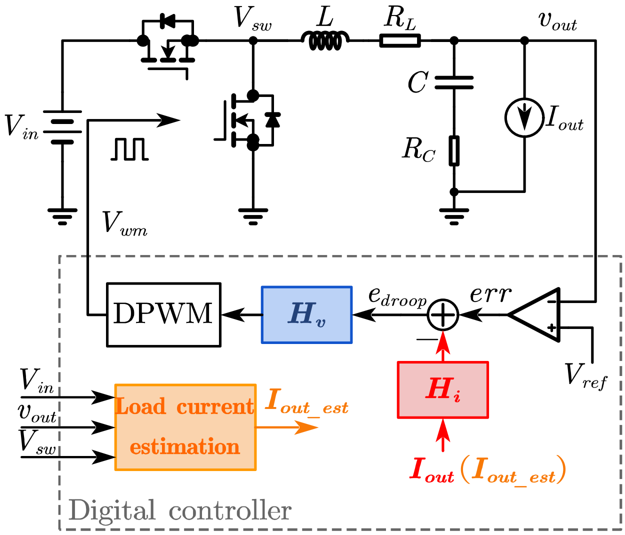


Fig. 2. Overall structure diagram of the proposed load current-based AVP control.

The rest of this article is organized as follows. Section II analyses the bandwidth limitation of active droop AVP control. Section III presents the small-signal model of the proposed load current-based AVP control loop, including the modelling of the closed-loop output impedance and the design process of the loop compensators. Section IV describes the proposed digital load current estimation algorithm. Section V shows the experimental

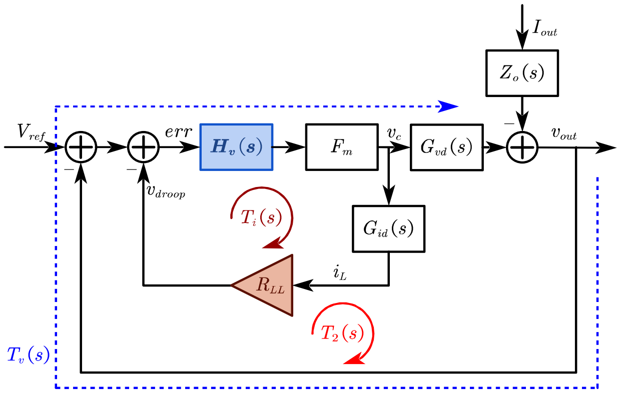


Fig. 3. Block diagram of active droop AVP control.

TABLE I
SYSTEM TRANSFER FUNCTIONS

<table>
<tr><th>Transfer function</th><th colspan="2">Expression</th></tr>
<tr><td>$G_{vd}(s)=\frac{v_{out}(s)}{v_c(s)}$</td><td colspan="2">$V_{in}\cdot\frac{1+s/\omega_{esr}}{1+\frac{s}{Q\cdot\omega_o}+\frac{s^2}{\omega_o^2}}$</td></tr>
<tr><td>$G_{id}(s)=\frac{i_L(s)}{v_c(s)}$</td><td colspan="2">$V_{in}\cdot\frac{C\cdot s}{1+\frac{s}{Q\cdot\omega_o}+\frac{s^2}{\omega_o^2}}$</td></tr>
<tr><td>$Z_o(s)=\frac{v_{out}(s)}{I_{out}(s)}$</td><td colspan="2">$r\cdot\frac{(1+s/\omega_L)\cdot(1+s/\omega_{esr})}{1+\frac{s}{Q\cdot\omega_o}+\frac{s^2}{\omega_o^2}}$</td></tr>
<tr><th colspan="3">Parameter</th></tr>
<tr><td>$\omega_o=1/\sqrt{L\cdot C}$</td><td>$\omega_{esr}=1/(R_C\cdot C)$</td><td>$\omega_L=r/L$</td></tr>
<tr><td>$Q=\frac{\sqrt{L/C}}{r+R_C}$</td><td>$r=R_{ds\_on}+R_L$</td><td></td></tr>
</table>

verification, the transient performance with the fast slew rate load step is tested, and the proposed control method is compared with the widely used active droop AVP control. Also, the load current estimation algorithm is verified in this section. Finally, Section VI concludes this article.

II. BANDWIDTH LIMITATION ISSUE OF EXISTING INDUCTOR CURRENT-BASED AVP CONTROL

In this section, the commonly used active droop method is analysed as an example of inductor current-based AVP control, to describe the limitation of the control loop bandwidth.

Fig. 3 is the block diagram of active droop AVP control, where $H_v(s)$ is the loop compensator, R_{LL} is the equivalent load line resistor, $T_i(s)$ is the inner current loop, $T_v(s)$ is the voltage loop and $T_2(s)$ is the entire loop. $H_v(s)$ is a type II compensator which has one zero and two poles. One of the poles is placed at the origin to eliminate the steady-state error and boost the low-frequency gain, another pole is placed near the half of the switching frequency to attenuate the high-frequency noise. A compensation zero is placed at the resonance frequency to compensate for the phase lag of the complex poles of the buck power stage. The system transfer function is given in Table I.

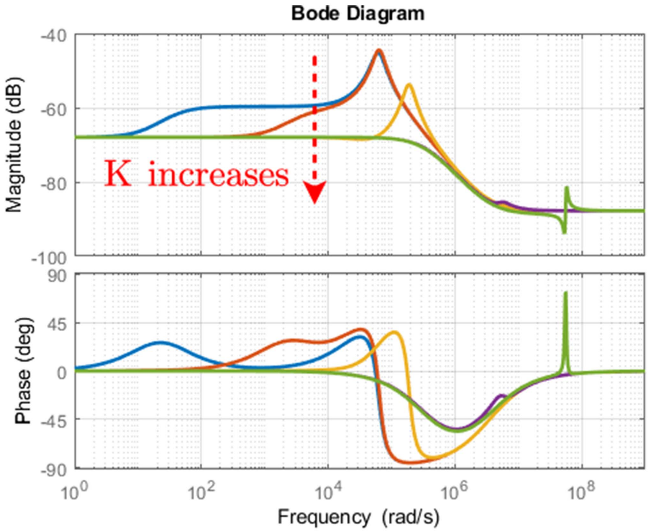


Fig. 4. Bode diagram of the closed-loop output impedance $Z_{oc}(s)$ with different values of K of active droop AVP control.

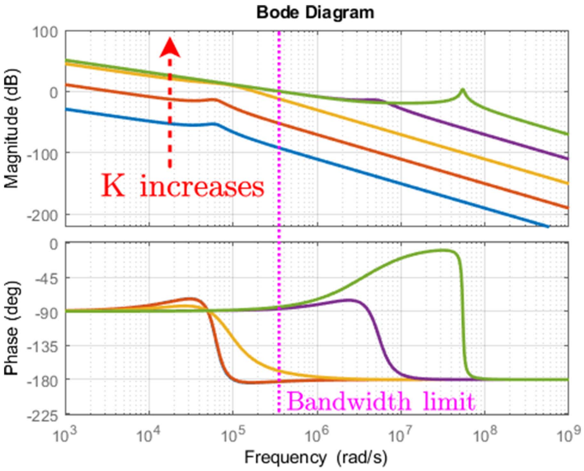


Fig. 5. Bode diagram of the entire loop $T_2(s)$ with different values of K of active droop AVP control.

According to the concept of active droop control, the transfer function of $T_v(s)$ and $T_i(s)$ are given in (1) and (2) respectively, then the entire loop $T_2(s)$ and the closed-loop output impedance $Z_{oc}(s)$ are expressed in (3) and (4). In order to make $Z_{oc}(s)$ equal the constant R_{LL} within the bandwidth, the loop $T_2(s)$ and $T_i(s)$ should satisfy $T_2(s)>>1$ and $T_i(s)>>1$ at that range. Figs. 4 and 5 are the frequency response of $T_2(s)$ and $Z_{oc}(s)$ under different values of K, respectively, where K is the gain of the loop compensator $H_v(s)$. It can be seen that if $H_v(s)$ is not able to provide sufficient loop gain, the loop $T_2(s)$ and $T_i(s)$ cannot meet the condition that far greater than 1 within the bandwidth, then $Z_{oc}(s)$ cannot be approximated to R_{LL}, and fail to achieve a proper AVP control. Within this range, the bandwidth of $T_2(s)$ increases as K increases (as shown by the blue to yellow curves in Fig. 5.

When both $T_2(s)$ and $T_i(s)$ satisfy that far greater than 1, then $Z_{oc}(s)$ can be approximated to R_{LL}. In this situation, $T_2(s)$ can be approximated to $T_v(s)/T_i(s)$, and the expression is given in (5). It can be seen that the transfer function of $T_2(s)$ is not determined by $H_v(s)$, so its bandwidth is basically constant. The bandwidth can be calculated by letting the magnitude of $T_2(s)$ equals 1 that $|T_2(j\omega)| = 1$, which is expressed in (6). BW in (6) is the limitation of the $T_2(s)$ bandwidth with the unit of hertz. If K further increases, the phase margin of $T_i(s)$ becomes small, and the amplitude of $1+T_i(s)$ near the crossover frequency of $T_i(s)$ becomes large, resulting in a resonance peak on $T_2(s)$, as shown by the green curve in Fig. 5. In this condition. the amplitude-frequency characteristic of $T_2(s)$ crosses 0 dB multiple times, which seriously affects system stability, but its first crossover frequency is still approximately equal to BW. For the multiphase system with the parameters in Section V, the maximum achievable bandwidth is only 64 kHz.

As well as in COT controlled converter, the slope of the inductor current is limited by the inductance value, which cannot respond quickly to the fast load transient, so the system can only return to a steady state through a longer time. Both the active droop AVP method and the AVP in COT control are compared with the proposed method, which is given in Section V.

Overall, under the inductor current-based AVP control, the output voltage takes a longer time to reach the new steady-state value during the load step because the inductor current cannot reflect the change of load current quickly. Also, in frequency domain, the maximum bandwidth is limited because of the inner current loop, which limits the response speed. From Section III onward this article proposes the load current-based AVP control strategy, and proposes to obtain the load current most efficiently by digital current estimation, so that the output voltage can be switched from the original steady state to the new steady state at the time of load step with the fastest speed

$$T_v(s) = H_v(s)\, F_m G_{vd}(s) \tag{1}$$

$$T_i(s) = H_v(s)\, F_m G_{id}(s)\, R_{LL} \tag{2}$$

$$T_2(s) = \frac{T_v(s)}{1+T_i(s)} = \begin{cases} \frac{T_v(s)}{T_i(s)} = \frac{G_{vd}(s)}{G_{id}(s)R_{LL}}, & \text{if } T_i(s) \gg 1 \\ T_v(s), & \text{if } T_i(s) \ll 1 \end{cases} \tag{3}$$

$$Z_{oc}(s) = \frac{Z_{oi}(s)}{1+T_2(s)} = \begin{cases} R_{LL}, & \text{if } T_2(s) \gg 1 \\ Z_{oi}, & \text{if } T_2(s) \ll 1 \end{cases} \tag{4}$$

$$T_2(s) \approx \frac{1}{C \cdot R_{LL}} \cdot \frac{1 + s/\omega_{\text{esr}}}{s} \tag{5}$$

$$\text{BW} \approx \frac{1}{2\pi \cdot C\sqrt{{R_{LL}}^2 - {R_C}^2}} \quad (\text{Hz}). \tag{6}$$

III. PROPOSED LOAD CURRENT-BASED AVP CONTROL

To achieve the high bandwidth AVP control and then enhance the transient speed, the load current-based AVP control scheme is proposed in this section. The load current is used to replace the inductor current in the proposed scheme and a novel compensation loop is designed. Compared to the existing inductor current-based AVP loop, the inner current loop is eliminated, so the high bandwidth control can be easily achieved. The load current is obtained by the digital current estimation algorithm, which is presented in Section IV.

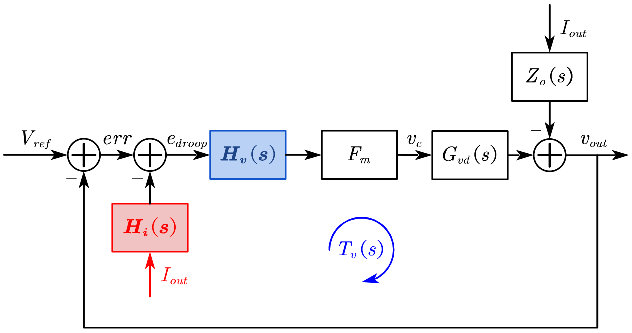


Fig. 6. Equivalent block diagram of proposed load current-based AVP control.

Based on Fig. 2, the equivalent control block diagram is shown in Fig. 6, where $H_v(s)$ is the voltage loop compensator. The load current I_{out} is injected into the loop after being compensated by a load current compensator $H_i(s)$ to achieve the constant closed-loop output impedance. The system transfer functions are given in Table I, and F_m is the modulation gain of digital PWM. It should be noticed that in multiphase application, the multiphase power stage is equivalent to the single phase by parallel the per phase inductor and MOSFET. Hence, the value of L and r in Table I should be the per-phase value divided by N, where N is the number of phases.

A. Entire Loop Transfer Function

In the proposed scheme, the voltage loop $T_v(s)$ is also the entire loop. Since the load current I_{out} is an independent signal which does controlled by any other loop signals, there is no inner current loop used to feedback the current information, which makes the loop design clearer. According to Fig. 6, the entire loop $T_v(s)$ is expressed in (7). $H_v(s)$ is a second order compensator, which has two zeros and two poles, as expressed in (8). One of the poles is placed at the origin to eliminate the steady-state error and boost the low-frequency gain, another pole ω_{p1} is placed near the half of the switching frequency to adjust the phase margin and attenuate the high-frequency noise. A compensation zero ω_{z1} is placed at the resonance frequency ω_o to compensate for the phase lag of the complex poles of the buck power stage, and another zero ω_{z2} is placed between the origin and ω_o to compensate for the phase lag introduced by the pole at the origin. The proportional gain K of $H_v(s)$ is calculated according to the desired bandwidth of $T_v(s)$

$$T_v(s) = H_v(s)\, F_m G_{vd}(s) \tag{7}$$

$$H_v(s) = \frac{K\left(1 + {}^{s}/_{\omega_{z1}}\right)\left(1 + {}^{s}/_{\omega_{z2}}\right)}{s\left(1 + {}^{s}/_{\omega_{p1}}\right)}. \tag{8}$$

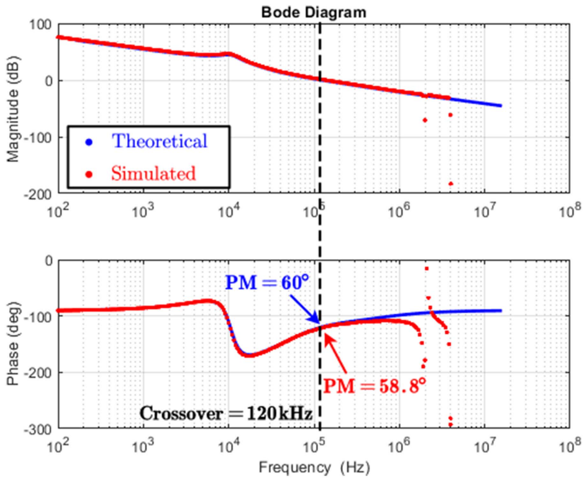


Fig. 7. Frequency response of the entire loop (blue: modelled; red: SIMPLIS simulated).

The compensator is converted to z-domain by the bilinear transformation and then implemented on the digital controller. To achieve a fast response, the finite state machines are designed to calculate multiple times per switching cycle to reduce the digital calculation delay. Fig. 7 is the frequency response of the entire loop $T_v(s)$, where the blue curve is the modelled result and the red dotted curve is the SIMPLIS ac simulation result, the time delay in digital control is considered in the SIMPLIS model. The bandwidth of 120 kHz is designed. It is verified that in the proposed load current-based AVP control loop, the current feedback does not affect the system bandwidth and the entire loop is equivalent to the voltage loop. In the digital implementation, although the time delay affects the frequency response at high frequency and causes phase lag, but has few effects within the bandwidth under the multiple calculations per switching cycle.

B. Modeling of the Open and Closed Loop Output Impedance

In this section, the closed loop output impedance $Z_{oc}(s)$ is finally derived according to the proposed control loop in Fig. 6, which is used in Section III-C to design the output constant impedance.

The open loop output impedance is calculated when the voltage loop is open, according to Fig. 6, the output voltage is expressed as

$$\begin{aligned} v_{\text{out}}(s)\,|_{V_{\text{ref}}=0} &= e_{\text{droop}}(s)\,T_v(s) - I_{\text{out}}(s)\,Z_o(s) \\ &= \left[-I_{\text{out}}(s)\,H_i(s)\right]\cdot T_v(s) - I_{\text{out}}(s)\,Z_o(s). \end{aligned} \tag{9}$$

Based on (9), the open loop output impedance is derived as

$$\begin{aligned} Z_{oi}(s) &= \frac{v_{\text{out}}(s)}{-I_{\text{out}}(s)} \\ &= H_i(s)\,T_v(s) + Z_o(s). \end{aligned} \tag{10}$$

The closed-loop output impedance is calculated when the voltage loop is closed, and the expression of $v_{\text{out}}(s)$ becomes (11). Based on Fig. 6 and (10) and (11), the closed-loop output impedance is expressed in (12)

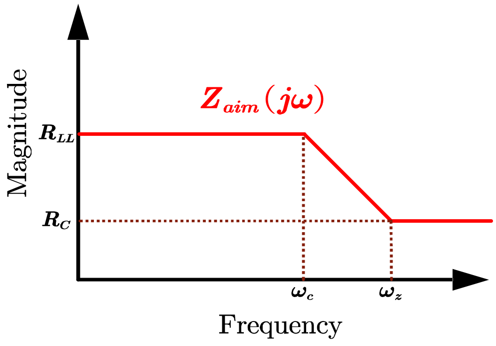


Fig. 8. Frequency response of the target impedance $Z_{\text{aim}}(j\omega)$.

$$\begin{aligned} v_{\text{out}}(s)\,|_{V_{\text{ref}}=0} &= \left[\text{err}(s) - I_{\text{out}}(s)\,H_i(s)\right]\cdot T_v(s) \\ &\quad - I_{\text{out}}(s)\,Z_o(s) \\ &= -v_{\text{out}}(s)\,T_v(s) - I_{\text{out}}(s)\,H_i(s)\,T_v(s) \\ &\quad - I_{\text{out}}(s)\,Z_o(s) \end{aligned} \tag{11}$$

$$\begin{aligned} Z_{oc}(s) &= \frac{v_{\text{out}}(s)}{-I_{\text{out}}(s)} \\ &= \frac{H_i(s)\,T_v(s) + Z_o(s)}{1 + T_v(s)} \\ &= \frac{Z_{oi}(s)}{1 + T_v(s)}. \end{aligned} \tag{12}$$

According to (12), $Z_{oc}(s)$ is associated with the load current compensator $H_i(s)$ and the entire loop $T_v(s)$. The entire loop should be taken into consideration in $H_i(s)$ design. $H_i(s)$ is designed according to the target impedance, to ensure $Z_{oc}(s)$ remains constant within the bandwidth.

C. Modeling of the Constant Output Impedance

In the frequency domain, recall (10) and (12), $T_v(j\omega) << 1$ if ω approaches infinity, so $Z_{oc}(j\omega)$ equals $Z_o(j\omega)$ which magnitude is R_C if ω approaches infinity. As a result, the target impedance should be designed to approach R_C when ω approaches infinity to make sure the designed system is causal. Besides, to achieve the constant output impedance within the bandwidth, the target impedance should equal a constant value R_{LL} in this range, where R_{LL} is the desired dc load line. Hence, the frequency characteristic of the target impedance $Z_{\text{aim}}(j\omega)$ should be designed as shown in Fig. 8, which is expressed as

$$Z_{\text{aim}}(j\omega) = R_{LL}\cdot\frac{1+\frac{j\omega}{\omega_z}}{1+\frac{j\omega}{\omega_c}}. \tag{13}$$

In (13), ω_c is the desired system bandwidth frequency (120 kHz) and ω_z is the zero frequency which controls the magnitude of $Z_{\text{aim}}(j\omega)$ reaches R_C beyond the bandwidth. The magnitude of $Z_{\text{aim}}(j\omega)$ when ω approaches infinity is calculated in (14), so the value of ω_z can be determined by solving the

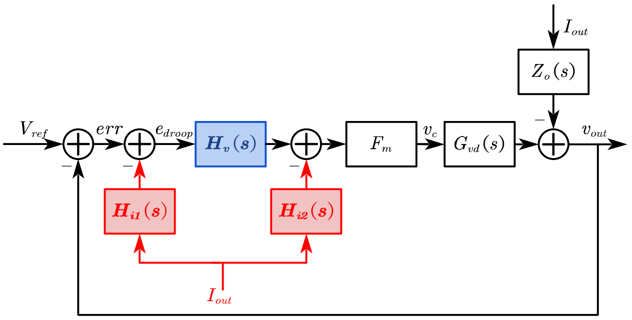


Fig. 9. Block diagram of the optimised equivalent control loop.

equation that (14) equals R_C, which is shown in (15). In this way, the target impedance as shown in Fig. 8 is modelled, and the transfer function in s-domain is given in (16)

$$\lim_{\omega\to\infty} |Z_{\text{aim}}(j\omega)| = R_{LL}\sqrt{\frac{1}{{\omega_z}^2}}\Big/\sqrt{\frac{1}{{\omega_c}^2}} \tag{14}$$

$$\omega_z = \frac{\omega_c R_{LL}}{R_C} \tag{15}$$

$$Z_{\text{aim}}(s) = R_{LL}\cdot\frac{1+\frac{s}{\omega_c R_{LL}/R_C}}{1+\frac{s}{\omega_c}}. \tag{16}$$

Based on (12) and (16), the transfer function of the load current compensator H_i(s) is solved by letting $Z_{oc}(s) = Z_{\text{aim}}(s)$, which is expressed as

$$\begin{aligned} H_i(s) &= \frac{R_{LL}T_v\left(1+\frac{s}{\omega_z}\right)+R_{LL}\left(1+\frac{s}{\omega_z}\right)-Z_o(s)\left(1+\frac{s}{\omega_c}\right)}{T_v(s)\left(1+\frac{s}{\omega_c}\right)} \\ &= Z_{\text{aim}}(s) + \frac{Z_{\text{aim}}(s)-Z_o(s)}{T_v(s)}. \end{aligned} \tag{17}$$

Although the compensator $H_i(s)$ in (17) is enough to model the constant $Z_{oc}(s)$ within the bandwidth, its order is too high to be implemented. However, it can be seen from (17) that $H_i(s)$ is a function of $T_v(s)$, so it is possible to break H_i(s) into several parts and inject the compensated load currents to the loop from different nodes, to achieve the equivalent compensation of $H_i(s)$. The analysis is as follows.

The output voltage $v_{\text{out}}(s)$ is expressed in (18) by substituting (17) into (11). Combining Fig. 6 and (18), the expression of $v_{\text{out}}(s)$ can be considered as the subtraction of two subsystems multiplied by $F_m G_{vd}(s)$, only the first subsystem has the component of $H_v(s)$. Hence, the high order compensator H_i(s) can be broken into two parts and injecting the compensated load currents prior to and behind the voltage loop compensator H_v(s), respectively. According to (18), the 2 load current compensators are named $H_{i1}(s)$ and $H_{i2}(s)$, the transfer function is shown in (19), and the control block diagram in Fig. 6 is optimised to that in Fig. 9. The transfer function of $H_{i1}(s)$ is the same as $Z_{\text{aim}}(s)$, which is a 1st order system. In $H_{i2}(s)$, the complex poles in $G_{vd}(s)$ and $Z_o(s)$ are cancelled, which makes $H_{i2}(s)$ a 2nd order system, and easy to be implemented by digital controllers with a simple finite-state machine (FSM). The transfer functions of H_v(s), H_{i1}(s) and H_{i2}(s) are converted to z-domain impulse transfer function by the bilinear transformation in digital implementation

$$\begin{aligned} &v_{\text{out}}(s) \\ &= \left[\text{err}(s) - \left(Z_{\text{aim}}(s) + \frac{Z_{\text{aim}}(s)-Z_o(s)}{T_v(s)}\right) I_{\text{out}}(s)\right]\cdot T_v(s) \\ &= F_m G_{vd}(s)\,[H_v(s)\,(\text{err}(s) - Z_{\text{aim}}(s)\cdot I_{\text{out}}(s)) \\ &\quad \left.- \frac{Z_{\text{aim}}(s)-Z_o(s)}{F_m G_{vd}(s)} I_{\text{out}}(s)\right] \end{aligned} \tag{18}$$

$$\begin{cases} H_{i1}(s) = Z_{\text{aim}}(s) \\ H_{i2}(s) = \frac{Z_{\text{aim}}(s)-Z_o(s)}{F_m G_{vd}(s)} \end{cases}. \tag{19}$$

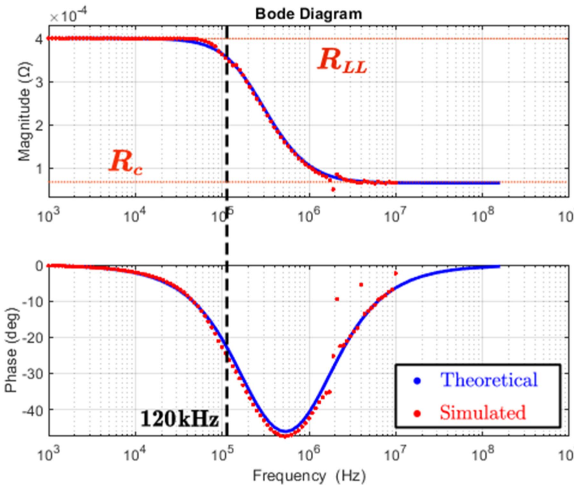


Fig. 10. Bode diagram of $Z_{oc}(s)$ under the proposed control scheme (blue: modelled; red: SIMPLIS simulated).

The model of $Z_{oc}(s)$ is verified using SIMPLIS ac simulation. Fig. 10 is the Bode diagram of $Z_{oc}(s)$ under the proposed control scheme, where the blue curve is the modelled result of (9), and the red dotted curve is the SIMPLIS ac simulation result under the control structure of Fig. 9. The dc load-line R_{LL} is designed to 0.4 mΩ. It can be seen that $Z_{oc}(s)$ is modelled to the constant R_{LL} within the bandwidth, and the SIMPLIS ac simulation result proves the correction of the equivalent control loop in Fig. 9.

IV. DIGITAL LOAD CURRENT ESTIMATION ALGORITHM

In this section, the digital load current estimation algorithm is proposed, to provide the load current information for the proposed AVP control. The proposed algorithm is a pure digital control, only the voltage signals need to be sampled, which has no requirement for the complex current sampling circuit. Besides, the digital estimation algorithm is not sensitive to the sampling noise, which stabilises the loop control. The block diagram is shown in Fig. 11, where the input and output voltages are sampled by the ADC, and the switching node voltage level is input to the digital controller as a one-bit digital signal. It should be noted that, since the switching node voltage V_{sw} has a

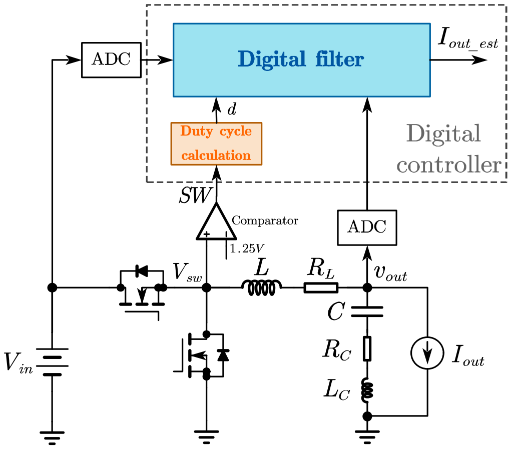


Fig. 11. Block diagram of the proposed digital load current estimation.

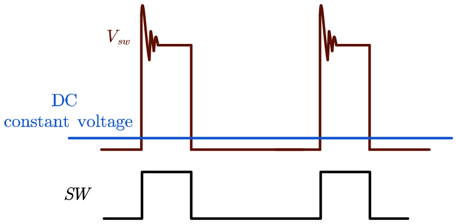


Fig. 12. Sampling of the switching node voltage using the analog input and digital output comparator.

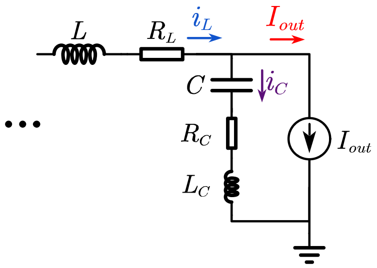


Fig. 13. Basic concept of the proposed load current estimation.

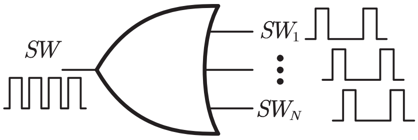


Fig. 14. Switching node voltage level sensing in multiphase applications.

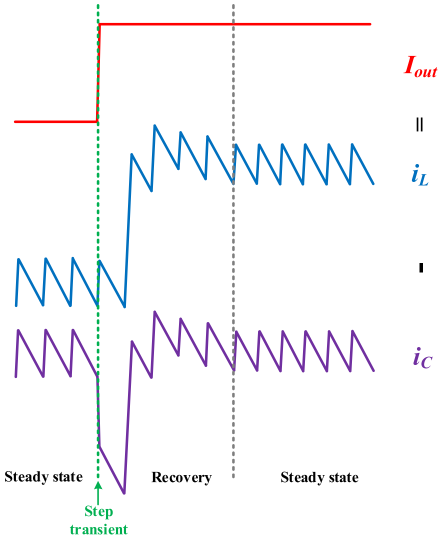


Fig. 15. Schematic diagram of the load current estimation concept.

serious ringing effect and switching noise, an analog input and digital output comparator is used to compare V_{sw} with a constant dc voltage, so the output signal SW is a digital signal without the impact of the noises. The waveform schematic is shown in Fig. 12.

The concept of the load current estimation is shown in Fig. 13. The load current can be expressed as the difference between the inductor current and the capacitor current, which is denoted in (20). Hence, the load current estimation is comprised of the inductor current and capacitor current estimation, both estimations are realised by the digital controller. In a multiphase system, the summed phase inductor current should be estimated as i_L, SW should represent the interleaved switching node signal. As shown in Fig. 14, SW is obtained by an OR logic of each phase's switching node signal SW_1 to SW_N, this operation is performed in the digital controller. So the summed inductor current can be estimated under the multiphase interleaving. In the steady state, the average value of the inductor current equals the load current while that of the capacitor current is 0, and the ripples of both are cancelled. During the load transient, the inductor current cannot change immediately, the load step moment is presented by the capacitor current. The schematic diagram is shown in Fig. 15. To estimate more accurate information, the ESL L_C of the capacitor is considered when designing the digital filter. The details are as follows:

$$I_{\text{out}} = i_L - i_C. \tag{20}$$

The inductor current is estimated according to the input voltage V_{in}, the output voltage v_{out} and the duty cycle value d, and calculated by the digital filter. The high-resolution inductor current estimation algorithm is applied to calculate the duty cycle value d, which is proposed in [21], to get a more accurate inductor current information by the delay-line-based structure, including the average and peak-to-peak value, the circuit diagram is shown in Fig. 16. Besides, the capacitor current is estimated according to the output voltage, the transfer function expression corresponding to $i_c(s)$ is shown in (21). Based on the estimation of the inductor and capacitor currents, the expression of the load current I_{out} in the z-domain is given in (22), which is discretised by the bilinear transformation. The corresponding parameters are given in Table II, where T_s is the discretization period of the digital filter. In (22), the first polynomial is the inductor current estimation and the second is the capacitor

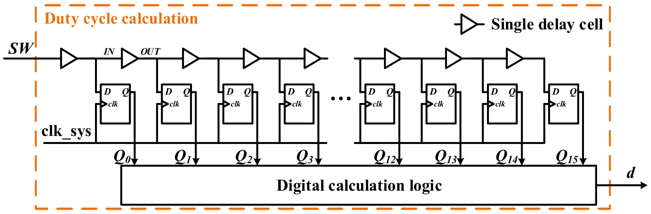


Fig. 16. Circuit diagram of the delay line-based high-resolution structure.

TABLE II
PARAMETERS OF THE LOAD CURRENT ESTIMATION ALGORITHM

Parameter	Expression
N_1	$\frac{2T_sC}{(2R_cT_s+4L_c)C+T_s^2}$
N_2	$\frac{T_s}{rT_s+2L}$
D_1	$\frac{(4L_c-2R_cT_s)+T_s^2}{(4L_c+2R_cT_s)+T_s^2}$
D_2	$\frac{-8CL_c+2T_s^2}{(2R_cT_s+4L_c)C+T_s^2}$
D_3	$\frac{rT_s-2L}{rT_s+2L}$

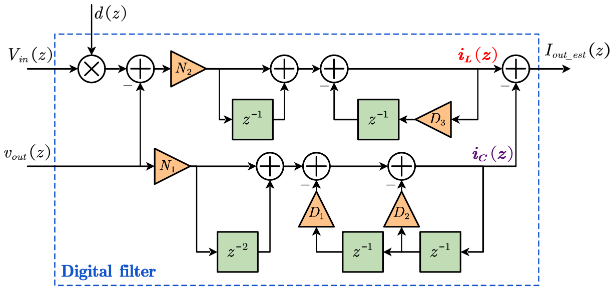


Fig. 17. Block diagram of the digital filter.

current estimation. The expression in (22) can be realised by the digital filter, which is shown in Fig. 17. The accuracy of the estimated digital load current is verified in Section V.

$$i_C(s) = \frac{v_{\text{out}}(s)}{\frac{1}{C\cdot s}+R_C+L_C\cdot s}$$
$$= v_{\text{out}}(s)\cdot\frac{C\cdot s}{1+\frac{s}{1/(R_CC)}+\frac{s^2}{1/(L_CC)}} \quad (21)$$

$$I_{\text{out\_est}}(z) = [d(z)\cdot V_{\text{in}}(z) - v_{\text{out}}(z)]\frac{N_2(1+z^{-1})}{1+D_3z^{-1}}$$
$$- v_{\text{out}}(z)\frac{N_1(1-z^{-1})}{1+D_2z^{-1}+D_1z^{-2}}. \quad (22)$$

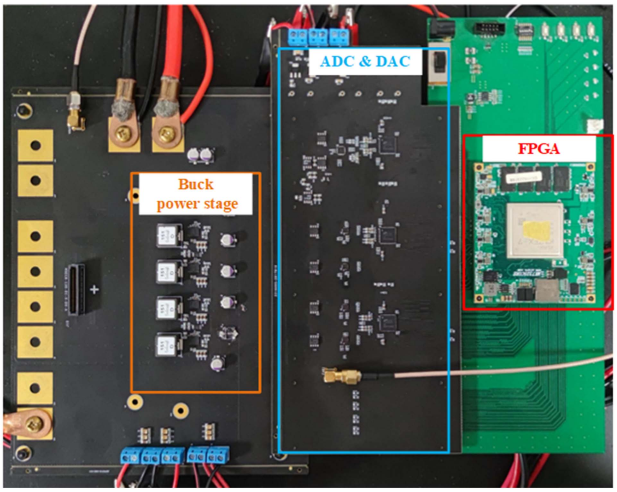
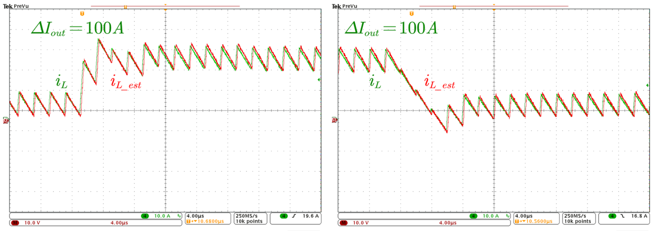


Fig. 18. Multiphase buck test system.

TABLE III
SYSTEM PARAMETERS

	Value	Remark	Part number
Input /output voltage	12V/1V		
DC Load line	$R_{LL} = 0.4\text{m}\Omega$		
Phase number	4		
Switching frequency	500 kHz		
Power MOSFET			MP86945
Inductor	$L = 150$ nH	$R_L = 150\ \mu\Omega$	SLC1480-151MLD
Output capacitor	6.6 mF	$R_C = 133\ \mu\Omega$	GCM32ED70E227ME36L



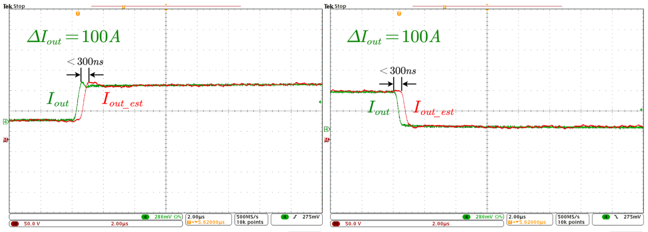
(a) (b)

Fig. 19. Inductor current estimation in load step transient: (a) Step-up. (b) Step-down.

V. EXPERIMENTAL RESULTS

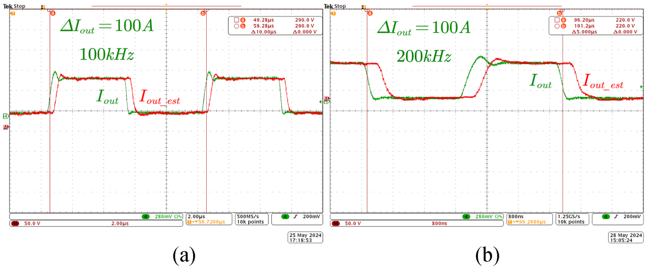
In this section, the proposed load current-based AVP control algorithm is tested on the four-phase buck system, the prototype is shown in Fig. 18. The input and output voltages are sampled by ADCs. The estimated load current is converted to the analog signal by a digital to analog converter (DAC) and is observed on the oscilloscope to verify its accuracy. The load transient response is tested using LOADSLAMMER PRO 1000RS electronic load, the maximum load step of 100 A is tested and the slew rate is 370 A/μs. The dc load line R_{LL} is designed to be 0.4 mΩ. The system parameters are given in Table III.

Fig. 19 shows the test results of the phase's estimated inductor current, the high-resolution algorithm guarantees the estimation accuracy of the inductor currents, which is the foundation of the proposed load current estimation. Fig. 20 is the test results of the load current estimation algorithm, where the green signal



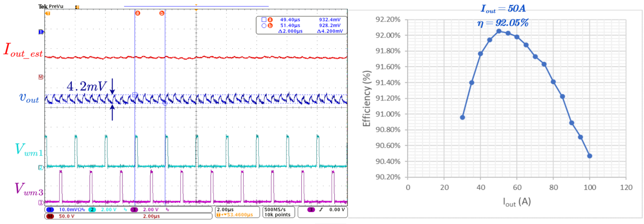
(a) (b)

Fig. 20. Load current estimation in load step transient. (a) Step-up. (b) Step-down.



(a) (b)

Fig. 21. Load current estimation in high-frequency load step transient. (a) 100 kHz. (b) 200 kHz.



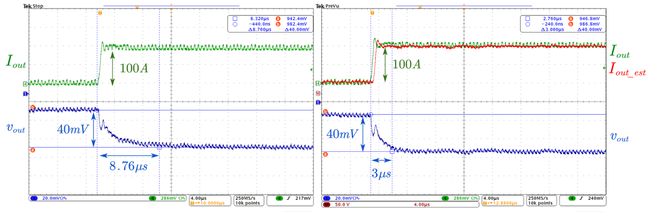
(a) (b)

Fig. 22. Stead- state operation of the proposed load current AVP control. (a) Steady-state waveforms. (b) Efficiency curve.

is the actual load current and the red signal is the estimated load current. It can be seen that the estimated current has an accurate steady-state value, and the transient slope has also been accurately estimated. The time delay between the actual and estimated signal in Fig. 20 is around 300 ns, which is determined by the ADC conversion delay when sampling the input & output voltage, the calculation delay of the digital controller and the DAC conversion delay.

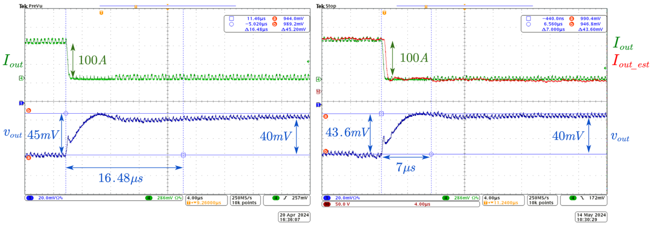
Besides, the estimated load current is accurate not only in the single load step but also in the high-frequency load step transient. Fig. 21 is the estimated load current under the load step frequency of 100 and 200 kHz, respectively, which proves that the load current-based control can be effectively applied in the controller to respond to the high-frequency load step transient.

Fig. 22 is the steady state-operation of the proposed. Fig. 22(a) is the steady-state waveforms, where V_{wm1} and V_{wm3} are the PWM pulses of phase 1 and phase 3, respectively, and the voltage ripple is around 4.2 mV. Fig. 22(b) is the efficiency curve under the load current range of 30–100 A, and the peak efficiency is 92.05% at the load current of 50 A. The test results in Fig. 22 prove the stability of the proposed scheme, and the system still has high efficiency under the control of the estimated load current injection.



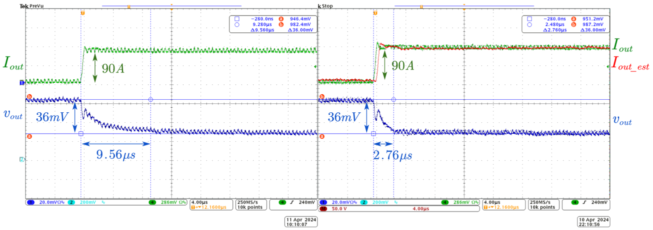
(a) (b)

Fig. 23. Load step-up transient with $\Delta I_{\text{out}} = 100\text{A}$. (a) Active droop method. (b) Proposed load current-based method.



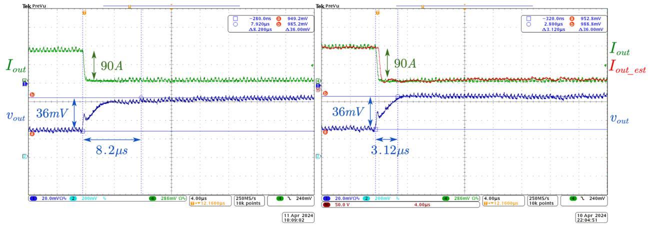
(a) (b)

Fig. 24. Load step-down transient with $\Delta I_{\text{out}} = 100\text{A}$. (a) Active droop method. (b) Proposed load current-based method.



(a) (b)

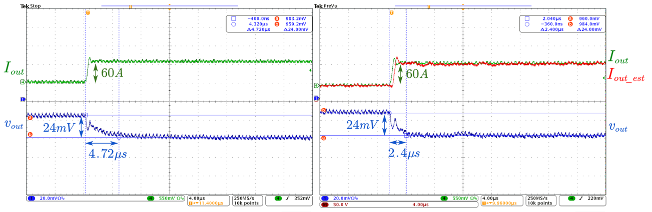
Fig. 25. Load step-up transient with $\Delta I_{\text{out}} = 90$ A. (a) Active droop method. (b) Proposed load current-based method.



(a) (b)

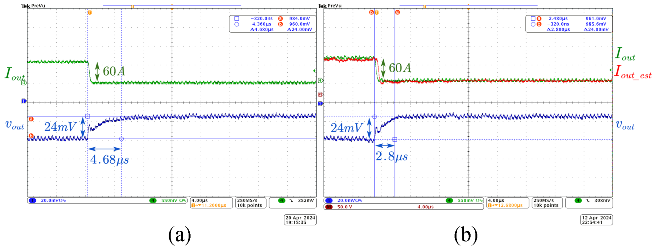
Fig. 26. Load step-down transient with $\Delta I_{\text{out}} = 90$ A. (a) Active droop method. (b) Proposed load current-based method.

The transient response of the proposed load current-based AVP control is compared with the commonly used active droop AVP control, the active droop AVP control has also been implemented by the prototype system. Figs. 23–28 are the load step-up and step-down transient responses of them, respectively, the load



(a) (b)

Fig. 27. Load step-up transient with $\Delta I_{\text{out}} = 60\text{A}$. (a) Active droop method. (b) Proposed load current-based method.



(a) (b)

Fig. 28. Load step-down transient with $\Delta I_{\text{out}} = 60\text{A}$. (a) Active droop method. (b) Proposed load current-based method.

TABLE IV

COMPARISON OF THE PROPOSED AND THE ACTIVE DROOP AVP

		Active droop AVP	The proposed
ΔI_{out} = 100 A	step-up	40 mV/8.76 µs	40 mV/3 µs
	step-down	45 mV/16.48 µs	43.6 mV/7 µs
ΔI_{out} = 90 A	step-up	36 mV/9.56 µs	36 mV/2.76 µs
	step-down	36 mV/8.2 µs	36 mV/3.12 µs
ΔI_{out} = 60 A	step-up	24 mV/4.72 µs	24 mV/2.4 µs
	step-down	24 mV/4.68 µs	24 mV/2.8 µs

steps of 100, 90, and 60 A are tested. The green and red signals are the actual and estimated load current respectively, the blue signals are the output voltage, the comparison results are given in Table IV. It can be seen that the proposed load current-based AVP control responds quickly to the load step transient, which significantly reduces the system recovery time.

To further verify the advancement of the load current-based AVP control, the proposed method is also compared with the AVP in COT control, as proposed in [9], [10], and [11]. Another four-phase buck system is developed which is controlled by TPS536C7 [22] of Texas Instruments, the prototype is shown in Fig. 29. TPS536C7 is a multiphase step-down controller, it applies the D-CAP+ [23], [24] control architecture, which is one of the advanced COT control schemes. The buck power stage parameters of Fig. 29 are totally the same as that of Fig. 18, the dc load line is also configured to 0.4 mΩ, which is a fair comparison.

The transient response of the TPS536C7 controlled system is presented in Fig. 30, where the green waveforms are the load current and the blue waveforms are the output voltage. The load step of 100 A is tested and the slew rate is 370 A/μs. The comparison results between the proposed load current-based AVP control and TPS536C7 controlled system are given in Table V. It can be seen that the output voltage takes 5.72 and 12 μs to recover to the steady state from the load step-up and step-down transient respectively, but it only takes 3 and 7 μs, respectively, under the control of the proposed control algorithm, which further proves the fast response performance of the proposed.

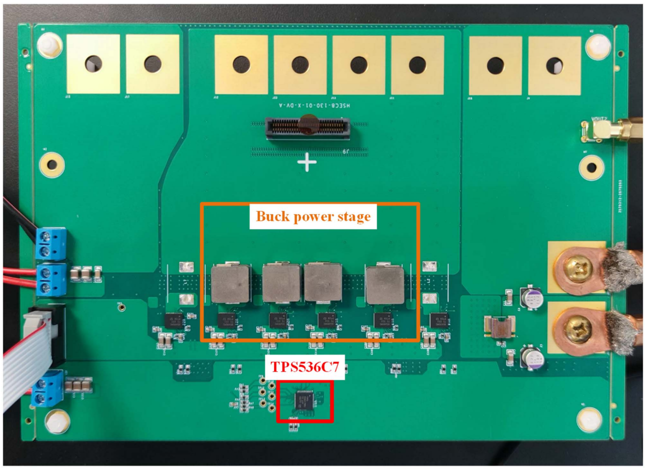
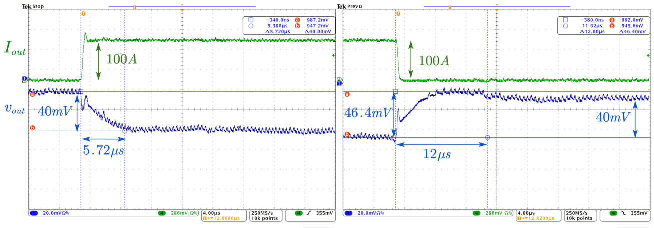


Fig. 29. Multiphase buck system with the TPS536C7 controller.



(a) (b)

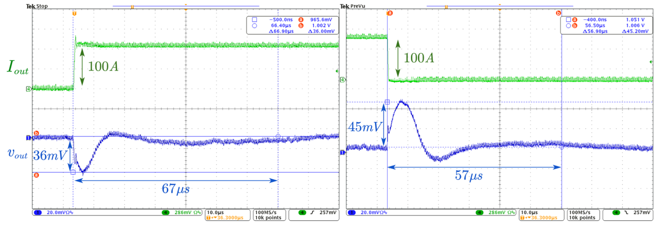
Fig. 30. Load step transient of TPS536C7 controlled system. (a) Load step-up. (b) Load step-down.

TABLE V

COMPARISON OF THE PROPOSED AND THE TPS536C7 CONTROLLER

	TPS536C7	The proposed
Load step (slew rate)	100A (370 A/µs)	
DC load-line	0.4 mΩ	
Undershoot/recovery time	40 mV/5.72 µs	40 mV/3 µs
Overshoot/recovery time	46.4 mV/12 µs	43.6 mV/7 µs

The enable or disable of the AVP function can be controlled. As shown in Fig. 9, if the outputs of $H_{i1}(s)$ and $H_{i2}(s)$ are disconnected from the loop, the AVP is disabled and it becomes a conventional PID control. The test results are shown in Fig. 31, the load step of 100 A is tested and the slew rate is 370 A/μs. The comparison results between the proposed load current-based AVP control and the PID control are given in Table VI. Compared to AVP control, PID control does not construct the constant output impedance, so the over-regulation occurs during the load step transient, and the system recovery time is significantly increased.



(a) (b)

Fig. 31. Load step transient when AVP is disabled (PID control). (a) Load step-up. (b) Load step-down.

TABLE VI
COMPARISON OF THE PROPOSED AND THE PID CONTROL

	PID	The proposed
Load step (slew rate)	100A (370 A/µs)	
DC load-line	Disabled	0.4 mΩ
Undershoot/recovery time	36 mV/67 µs	40 mV/3 µs
Overshoot/recovery time	45 mV/57 µs	43.6 mV/7 µs

VI. CONCLUSION

This article proposes a load current-based AVP control algorithm to improve the load transient performance. The load current is used as the current information instead of the inductor current, which makes it easy to realise high bandwidth control and respond quickly to the load step transient. The small signal model is developed for buck converters using this scheme. Based on the model, the load current compensation design process is proposed to construct the constant closed-loop output impedance. Besides, the digital load current estimation algorithm is proposed, to get the load current by only sampling the input and output voltage and the switching node level and does not need the complex and inefficient current sampling approach. The estimated load current is used in the proposed AVP control loop. The load current-based AVP control is verified on the multiphase buck system, the maximum load step of 100 A is tested and the slew rate reaches 370 A/μs. Compared with the active droop AVP control and the AVP in COT control, the proposed scheme has faster transient performance, which significantly reduces the system recovery time. The proposed algorithm is fully digital control, the cost and complexity of the implementation are not a challenge for developing a digital integrated circuit (IC). Furthermore, the proposed scheme can be applied to the multiphase system with an arbitrary number of phases. In the future, the current estimation algorithm under converter parameter variations will be investigated based on current research to further increase the estimation accuracy.

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