Modeling and Design Guideline of Optimal Split Inductance Range for Split-Output Power Module Considering Normal and Fault Conditions

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***Abstract*—Split-output structure outperforms the common half-bridge structure for silicon carbide (SiC) applications in terms of operation efficiency increasing, crosstalk voltage suppression, and zero dead time. An appropriate split inductance is the key to fully exploiting the potentials of the split-output structure. However, the split inductance design is empirical and lacks a theoretical guideline. Therefore, in this article, models in the s-domain are established to quantitatively illustrate the effects of the split inductance on the characteristics of normal operation and short-circuit faults, respectively. The accuracy of the models is verified by experiments. The lower limit of the split inductance is determined to obtain the lowest switching loss and safe crosstalk voltage. It is also observed that the upper limit also exists to avoid undesirable oscillation and excessive short-circuit thermal stress. As a result, a general design guideline is presented to determine the optimal split inductance range, relying only on the application conditions and datasheet parameters.**

***Index Terms*—Design guideline, short-circuit stress, silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET), split-output.**

I. Introduction

SILICON carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) is generally utilized in a common half-bridge configuration, where the two active switches are connected directly. The common structure has natural drawbacks, which limit the full use of the advantages of SiC MOSFET. First, when the active device turns ON, the capacitive current induced by the complementary OFF-state device is injected into the active device, which leads to turn-ON current overshoot and increased turn-ON loss. Second, a high voltage variation rate *dv/dt* causes undesirable gate voltage (crosstalk phenomenon) on the power device, which results in false turn-ON and gate oxide degradation [1]. A dead time is required to avoid the shoot-through fault at the expense of the output current quality.

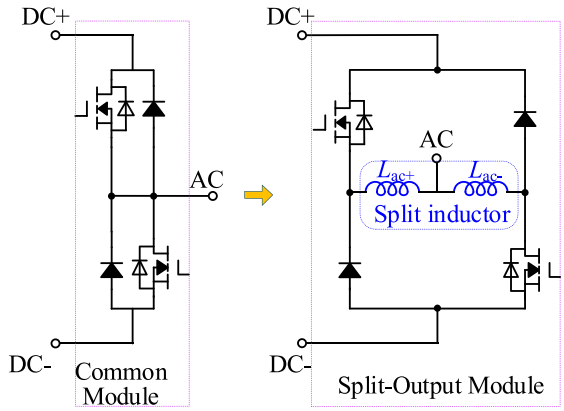

Fig. 1. Schematic diagram of common and split-output half-bridge structure.

To overcome the constraints induced by the common half-bridge structure, the split-output structure is proposed in [2], as shown in Fig. 1. The inductors L_{ac+} and L_{ac-} are introduced and called "split inductors," which decouple the complementary devices and attenuate the voltage variation rate of the OFF-state device. As a result, the split-output power module possesses the potential for increased operation efficiency [3], [4], suppressed crosstalk voltage [5], and zero dead time [6], [7].

Split inductance is the key to achieving the potential advantages [8]. The methods of equipping the split inductors to the power module can be divided into two types. Type I utilizes the internal subcomponents of the power module to build the split inductor. As shown in Fig. 2(a) [9], the split inductance is imported by the self and mutual inductance of the ac terminals. However, the split inductance is limited by the geometry of the power terminal. Type II connects external split inductors to the split-output power module [4], [10], [11], as shown in Fig. 2(b). However, because of lacking the theoretical guidance, the split inductance is determined by plenty of time-consuming experiments or empirically selected to be high [12], [13]. Besides, the negative effects of the too-high split inductance have not yet been noticed and explored.

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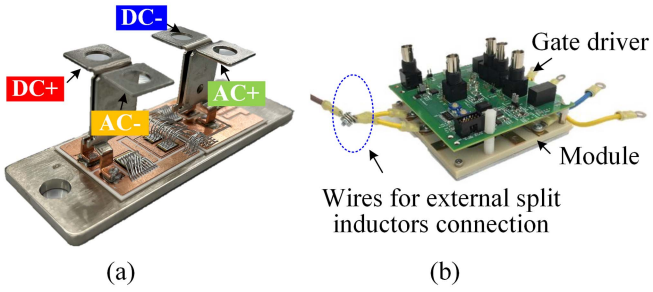


Fig. 2. Two types of split inductors equipping methods. (a) [9]. (b) [10].

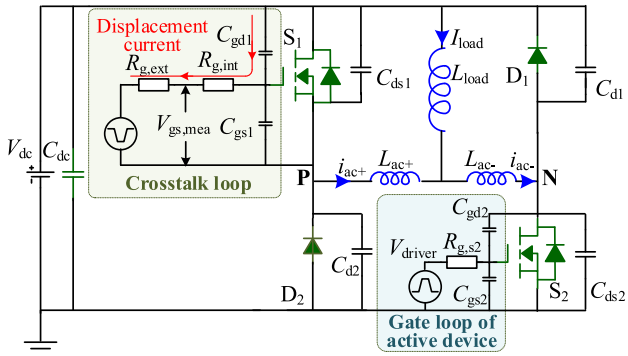


Fig. 3. Equivalent circuit of split-output power module.

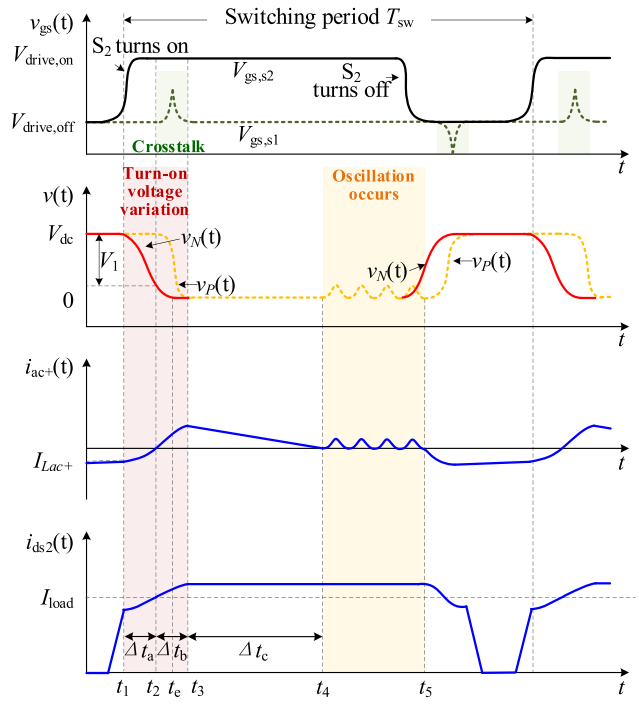


Fig. 4. Switching waveforms of split-output power module during normal operation.

This article proposes the models describing the normal operation and short-circuit fault of the split-output power module. Then, the effects of the split inductance on the switching loss, crosstalk voltage, oscillation, and short-circuit thermal stress are analyzed. A quantitative calculation flowchart is proposed to determine the optimal split inductance quickly and accurately and is only based on the application conditions and datasheet parameters. The lower limit of the split inductance is determined by the lowest switching loss and safe crosstalk voltage. The upper limit of the split inductance also exists to avoid undesirable oscillation [14] and excessive short-circuit thermal stress, which degrades the EMI characteristics and device life [15].

The rest of this article is organized as follows. Section II establishes equivalent models in stages to analyze the effects of the split inductance on the characteristics of the normal operation and short-circuit fault. In Section III, the flowchart for obtaining the optimal split inductance as well as the parameters extraction is demonstrated. Section IV introduces the test bench, verifies the models by experiments, and shows an example of determining the optimal range of the split inductance based on application conditions. Finally, Section V concludes the article.

II. Modeling of Split-Output Power Module

Transient normal switching and short-circuit fault processes of the split-output power module are analyzed. The voltage and current waveforms are depicted to illustrate the sequence of the turn-ON loss, crosstalk voltage, and oscillation. Equations and calculation routines are also derived to reveal the effects of the split inductance on the device's electrical and thermal stresses under normal operation and short-circuit fault.

A. Normal Operation Analysis of Split-Output Power Module

As shown in Fig. 3, the equivalent circuit of the split-output power module driving an inductive load is established, which considers the crucial elements including gate drive loop, load inductor, and junction capacitance. The S_2 is regarded as the active device, while S_1 keeps OFF-state. The switching process is illustrated in Fig. 4 and studied stage by stage. The regions corresponding to the turn-ON process, crosstalk voltage, and oscillation are highlighted.

The turn-ON and turn-OFF processes are symmetrical and the split inductors reduce switching loss only by impacting the voltage variation phase. Thus, while revealing the effects of the split inductance on the switching loss, only the turn-ON loss during the voltage variation phase is modeled and divided into two phases ($[t_1$-$t_2]$, $[t_2$-$t_3]$). When S_2 turns ON, the voltage at node N starts to drop at t_1 after the current commutation. The variation of voltage across the active device is modeled as a piecewise function as shown in (1), whose slope is represented by k. The k can be calculated as (2) [16]. To concisely represent the equations, some variables are predefined, as shown in (3)

$$V_N(t) = \begin{cases} V_{\rm dc} - k \cdot (t - t_1) & t_1 \le t < t_e \\ 0 & t \ge t_e \end{cases} \tag{1}$$

$$k = \frac{dV_{ds2}}{dt} = \frac{d(V_{gd2} + V_{gs2})}{dt} = \frac{dV_{gd2}}{dt} = \frac{|V_{\rm miller} - V_{\rm driver}|}{R_{g,s2} \cdot C_{gd2}} \tag{2}$$

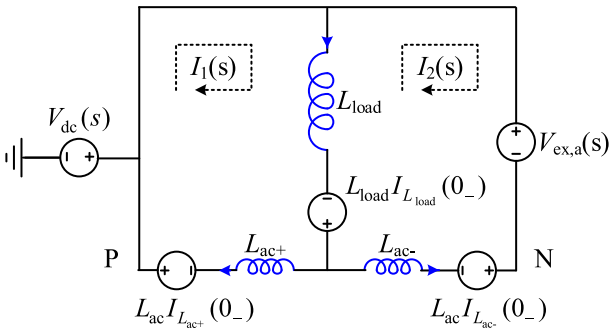


Fig. 5. Equivalent circuit during i_{ac+} freewheeling through S_1 body diode.

$$\begin{cases} C_{\text{iss}} = C_{gd1} + C_{gs1} \\ C_{\text{eq}} = C_{ds1} + C_{d2} \\ L_a = 2L_{\text{load}} + L_{\text{ac}} \\ L_b = L_{\text{load}} + L_{\text{ac}} \\ R_g = R_{g,\text{int}} + R_{g,\text{ext}} \\ \omega_{\text{eq}} = \sqrt{L_b/(L_a L_{\text{ac}} C_{\text{eq}})} \end{cases} \tag{3}$$

where V_{ds2}, V_{gd2}, and V_{gs2} are the voltage across the S_2 junction capacitors, C_{gd1}, C_{gs1}, and C_{ds1} are the S_1 junction capacitance, respectively, V_{miller} is the miller plateau voltage, V_{driver} is the gate driver voltage, $R_{g,s2}$ is the S_2 gate resistance, C_{gd2} is the gate-drain junction capacitance, and t_e is the moment when the voltage at N decreases to zero. $R_{g,\text{int}}$, $R_{g,\text{ext}}$ are the internal and external gate resistance of S_1.

1) [t_1-t_2] S_1 Body Diode Freewheeling Current Falling Phase: The current on the L_{ac+} is freewheeling through the S_1 body diode and the voltage at node P is clamped at V_{dc}. Thus, the L_{ac+} withstands the reverse voltage and the current through L_{ac+} attenuates to zero gradually. The equivalent circuit in the s-domain is shown in Fig. 5 and can be represented as (4). The voltage variation at node N is regarded as the excitation. Then, the voltage and current of S_2 during [t_1-t_2] can be calculated as shown in (5) by solving

$$\begin{cases} (sL_{\text{load}} + sL_{\text{ac}})I_1(s) - sL_{\text{load}}I_2(s) \\ = L_{\text{load}}I_{\text{load}} + L_{\text{ac}}I_{Lac+} \\ -sL_{\text{load}}I_1(s) + (sL_{\text{load}} + sL_{\text{ac}})I_2(s) \\ = -V_{\text{ex},a}(s) - L_{\text{ac}}(I_{\text{load}} - I_{Lac+}) - L_{\text{load}}I_{\text{load}} \\ V_{\text{ex},a}(s) = \frac{k}{s^2}(e^{-t_1 s} - e^{-t_e s}) \end{cases} \tag{4}$$

where I_{Lac+} is the current through L_{ac+} at t_1

$$\begin{cases} V_{ds2}(t) = V_{\text{dc}} - k \cdot (t - t_1) \\ I_{ds2}(t) = -\mathcal{L}^{-1}\{I_2(s)\} - C_{d1}\frac{dV_{\text{ds2}}(t)}{dt} \\ E_{\text{on},a} = \int_{t_1}^{t_2} V_{ds2}(t) \cdot I_{ds2}(t)dt \\ \Delta t_a = t_2 - t_1 = \sqrt{\frac{2L_{\text{ac}}L_a I_{Lac+}}{k \cdot L_{\text{load}}}} \\ V_1 = V_{\text{dc}} - V_{ds2}(t_2) = k \cdot \Delta t_a \end{cases} . \tag{5}$$

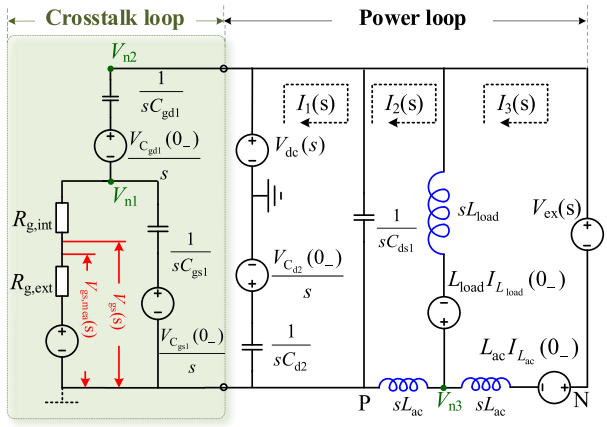


Fig. 6. Equivalent circuit including crosstalk loop and power loop during node P voltage falling in s domain.

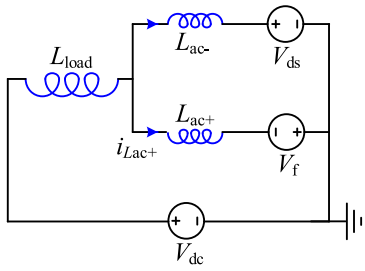


Fig. 7. Equivalent circuit during D_2 freewheeling phase.

2) [t_2-t_3] Voltage at Node P Falling Phase: At t_2, the voltage at node N is represented as (V_{dc}-V_1). If V_1 does not reach V_{dc} at t_2, the loss of [t_2-t_3] should also be included in the turn-ON loss. The S_1 body diode stops freewheeling and the voltage at node P starts to drop at t_2. Then the displacement current generates and flows into S_1 gate loop because of the voltage variation across the S_1 as shown in Fig. 3. The positive crosstalk spike occurs on the gate-source voltage of the S_1 and raises the shoot-through fault risk.

As shown in Fig. 6, the equivalent circuit in the s domain is divided into a power loop and a crosstalk loop. The turn-ON loss and crosstalk are calculated in sequence. Given that the crosstalk loop does not affect the turn-ON loss, only the power loop is considered while analyzing the turn-ON loss. The voltage variation of node N is the excitation. With the loop current analysis method, the power loop can be described as

$$\begin{cases} \left(\frac{1}{sC_{ds1}} + \frac{1}{sC_{\text{d2}}}\right) I_1(s) - \frac{1}{sC_{ds1}} I_2(s) = 0 \\ -\frac{1}{sC_{ds1}} I_1(s) + \left(\frac{1}{sC_{ds1}} + sL_{\text{ac}} + sL_{\text{load}}\right) I_2(s) \\ -sL_{\text{load}} I_3(s) = L_{\text{load}} I_{\text{load}} \\ -sL_{\text{load}} I_2(s) + (sL_{\text{load}} + sL_{\text{ac}})\, I_3(s) \\ = -V_{\text{ex},b}(s) - L_{\text{ac}} I_{\text{load}} - L_{\text{load}} I_{\text{load}} \\ V_{\text{ex},b}(s) = \frac{k}{s^2}\left(e^{-t_2 s} - e^{-t_e s}\right) + \frac{V_1}{s} e^{-t_2 s} \\ V_p(s) = \frac{1}{sC_{d2}} I_1(s) + \frac{V_{\text{dc}}}{s} \\ I_{\text{ac+}}(s) = -I_2(s) \end{cases} . \tag{6}$$

Then, the turn-ON loss of S_2 during node P voltage falling phase and the [t_2-t_3] duration can be calculated as shown in (7). Besides, the duration of the Δt_b and peak current through the L_{ac+} are also demonstrated in (14) and (15) shown at the bottom of the next page. The total turn-ON loss during S_2 voltage variation phase is represented as (8)

$$\begin{cases} V_{ds2}(t) = V_{\rm dc} - V_1 - k \cdot (t - t_2) \\ I_{ds2}(t) = -\mathcal{L}^{-1}\{I_3(s)\} - C_{d1}\frac{dV_{ds2}}{dt} \\ E_{{\rm on},b} = \int_{t_2}^{t_3} V_{ds2}(t) \cdot I_{ds2}(t)dt \end{cases} \tag{7}$$

$$E_{\rm on} = E_{{\rm on},a} + E_{{\rm on},b}. \tag{8}$$

The crosstalk loop is considered when calculating the crosstalk voltage. The node P voltage is regarded as the reference point for calculation simplification as shown in Fig. 6. With the node-voltage analysis method, the equivalent circuit can be described as (9). The initial voltage of the C_{d2} is $V_{\rm dc}$. The initial current of load inductor $IL_{\rm load}$(0-) and N-side split inductor $IL_{\rm ac}$(0-) is $I_{\rm load}$. The initial voltage of the gate driver, C_{gs1} and C_{gd1} is $V_{\rm driver}$, $V_{\rm driver,}$ and -$V_{\rm driver}$, respectively. Given that the gate driver voltage does not affect the amplitude of the crosstalk voltage, the $V_{\rm driver}$ is set to zero to simplify the calculation. Then, the gate-source voltage of the off-state device can be derived from (9) as (16) shown at the bottom of the next page. Given that only the $V_{gs,{\rm mea}}$(s) outside the device can be measured by experiments, $V_{gs,{\rm mea}}$(s) is also calculated by (17) shown at the bottom of the next page, and used to compare with experimental results

$$\begin{cases} \left(\frac{1}{R_g} + sC_{gs1} + sC_{gd1}\right) V_{n1}(s) - sC_{gd1}V_{n2}(s) = 0 \\ \left(sC_{d2} + sC_{gd1} + sC_{ds1} + \frac{1}{sL_{\rm load}} + \frac{1}{sL_{\rm ac}}\right) V_{n2}(s) \\ -sC_{gd1}V_{n1}(s) - \left(\frac{1}{sL_{\rm load}} + \frac{1}{sL_{\rm ac}}\right) V_{n3}(s) = \frac{V_{{\rm ex},b}(s)}{sL_{\rm ac}} \\ \left(\frac{1}{sL_{\rm load}} + \frac{1}{sL_{\rm ac}}\right) V_{n2}(s) - \left(\frac{1}{sL_{\rm load}} + \frac{2}{sL_{\rm ac}}\right) V_{n3}(s) = \frac{V_{{\rm ex},b}(s)}{sL_{\rm ac}} \end{cases} \tag{9}$$

3) [t_3-t_4] i_{ac+} (Current Through L_{ac+}) Falling Stage: At t_3, the voltage at node P drops to zero and the current $i_{\rm ac+}$ through $L_{\rm ac+}$ reaches the peak value. Then, $i_{\rm ac+}$ freewheels through D_2 and attenuates gradually. The equivalent circuit is depicted in Fig. 7. The changing rate of the current through $L_{\rm ac+}$ can be described by (10). Then, the time interval of $i_{\rm ac+}$ from the peak value falling to zero can be represented by (11). The whole duration $\Delta t_{L{\rm ac+}}$ of the $i_{L{\rm ac+}}$ after the active device turns ON can be calculated by (12)

$$\frac{di_{L{\rm ac+}}(t)}{dt} = \frac{V_{\rm dc}}{L_a} + \frac{L_{\rm load} \cdot V_{ds} + L_b \cdot V_f}{L_{\rm ac} \cdot L_a} \tag{10}$$

$$\Delta t_c = t_4 - t_3 = \frac{i_{{\rm ac+},{\rm peak}}}{di_{L{\rm ac+}}/dt} \tag{11}$$

$$\Delta t_{L{\rm ac+}} = \Delta t_a + \Delta t_b + \Delta t_c \tag{12}$$

where V_{ds} and V_f are the conduction voltage of the S_2 and D_1, respectively.

4) [t_4-t_5] Node P Voltage Oscillation Analysis: At t_4, the current $i_{\rm ac+}$ through $L_{\rm ac+}$ decreases to zero and triggers the undesirable oscillation at node P. The equivalent oscillation loop

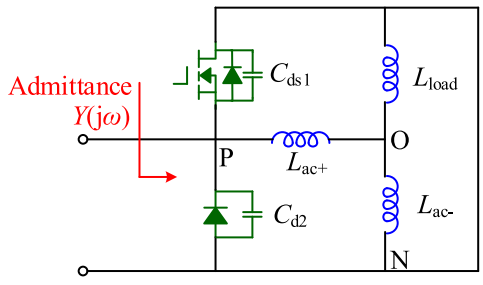


Fig. 8. Equivalent oscillation circuit.

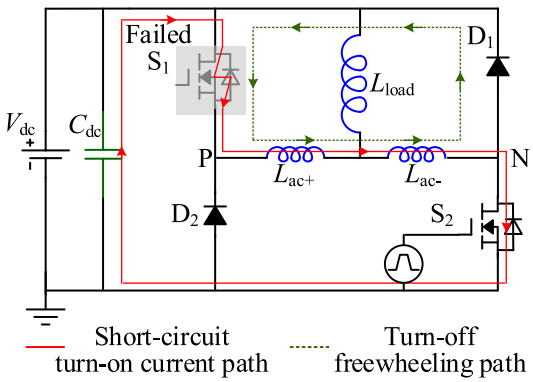


Fig. 9. Schematic diagram of short-circuit turn-ON and turn-OFF current paths.

is depicted in Fig. 8, which is utilized to derive the equivalent admittance $Y(j\omega)$ and oscillation frequency $f_{\rm os}$ as shown in (13). The oscillation continues until the S_2 turns OFF. The parasitic capacitor and resistor of the load inductor are neglected. Because although the parasitic capacitor of the load inductor introduces a higher frequency oscillation, it does not affect the original lower frequency capacitor. Besides, the amplitude of the higher frequency oscillation is very low and can be neglected. In addition, the parasitic resistance of the load inductor does not affect the oscillation frequency

$$\begin{cases} Y(j\omega) = j\omega(C_{ds1} + C_{d2}) + \frac{1}{j\omega[L_{\rm ac+} + (L_{\rm load}//L_{\rm ac-})]} \\ f_{os} = \frac{1}{2\pi\omega_0} = \frac{1}{2\pi\sqrt{(C_{ds1}+C_{d2})[L_{\rm ac+} + (L_{\rm load}//L_{\rm ac-})]}} \end{cases} \tag{13}$$

where ω_0 is the resonance angular frequency

B. Short-Circuit Fault Analysis of Split-Output Power Module

The short-circuit turn-ON and turn-OFF current paths of the split-output power module are illustrated in Fig. 9. The upper device S_1 is assumed to be the failed device and out of control. When S_2 turns ON, the shoot-through fault occurs and the short-circuit current rises. After the short-circuit current reaches the protection threshold, the S_2 turns OFF and the short-circuit current freewheels through D_1 and split inductors. The voltage and current waveforms during the short-circuit fault are illustrated in Fig. 10 and analyzed stage by stage. The equivalent circuits during the turn-ON and turn-OFF processes are given in Table I. In the equivalent circuits, the $R_{\rm loop}$ represents the lumped loop resistance, which is omitted in Fig. 9.

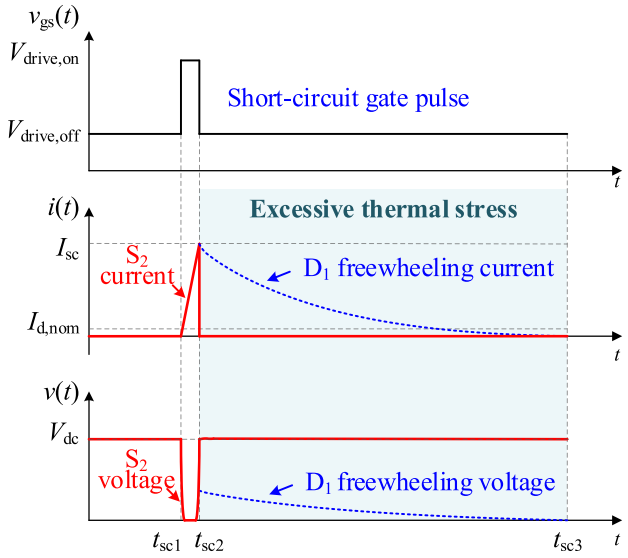
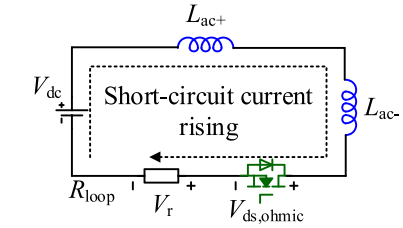
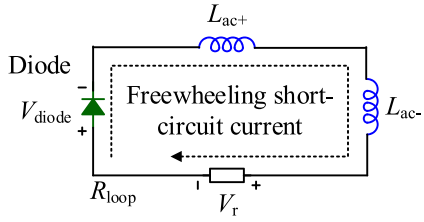


Fig. 10. Switching waveforms of split-output power module in a short-circuit fault.

TABLE I
EQUIVALENT CIRCUITS AND CURRENT EXPRESSIONS DURING SHORT-CIRCUIT FAULT

Phase	Equivalent circuit and current variation rate
$[t_{sc1}$-$t_{sc2}]$	 $\frac{di_d}{dt} = \frac{V_{DC} - V_{ds} - V_r}{L_{SC}} \approx \frac{V_{DC}}{2L_{ac}}$ (18)
$[t_{sc2}$- $t_{sc3}]$	 $\frac{di_d}{dt} = \frac{V_{diode} + V_r}{2L_{ac}}$ (19)

1) [t_{sc1}-t_{sc2}] Short-Circuit Turn-On Process: At t_{sc1}, a short-circuit fault occurs. The short-circuit turn-ON loop inductance is composed of the split inductance. Because of the split inductors, the SiC MOSFET first enters the ohmic region at the beginning of the short-circuit fault [17], as shown in Fig. 10. The voltage drop across the R_{loop} and $V_{ds,ohmic}$ are negligible compared to the dc-bus voltage. Thus, the short-circuit current rising rate can be expressed as (18). It can be seen that the short-circuit rising rate and energies can be suppressed in the split-output power module compared to the common half-bridge structure.

2) [t_{sc2}- t_{sc3}] Short-Circuit Turn-Off Process: At t_{sc2}, the short-circuit current reaches the protection threshold, and then the S_2 is shut down. The shut-down current I_{sc} is several times the device's nominal current. Then, the short-circuit current freewheels by the upper diode D_1 as shown in Fig. 9. It is worth noting that owing to the conducting diode, the turn-OFF overvoltage of S_2 is not affected by the split inductance, as shown in Fig. 10. The equivalent circuit and current changing rate during the D_1 freewheeling phase are given in Table I. Given that the sum of the V_{diode} and V_r is far lower than the V_{dc}, the current changing rate during the turn-OFF process is much slower than that of the turn-ON process. As a result, the freewheeling duration [t_{sc2}-t_{sc3}] is much longer than that of short-circuit duration [t_{sc1}-t_{sc2}], as shown in Fig. 10. At t_{sc3}, the short-circuit energy stored in the split inductors totally dissipates in the diode D_1 until the freewheeling phase ends, which causes the D_1 to withstand extreme thermal stress and even failure. Thus, it is important to monitor the junction temperature of diode D_1 during the short-circuit freewheeling phase, given that the short-circuit protection method can only prevent the SiC MOSFET failure from short-circuit faults [18].

The thermal impedance network method is utilized to calculate the diode junction temperature [19]. As shown in Fig. 11, the diode can be modeled as a voltage source and a resistor in series, which are all junction temperature dependent. Then, the diode conduction voltage V_d(t) can be represented as (20). $V_T(T_j)$, $R_T(T_j)$, and $i_d(t)$ represent the voltage source, resistance, and diode current, respectively. Then, the time-varying heat power P_d(t) can be calculated by multiplying V_d(t) and i_d(t), as shown

$$\Delta t_b = t_3 - t_2 = \frac{1}{\omega_{eq}} \arccos\left[\frac{k}{V_1}\left(t_e - t_2 - \frac{1}{\omega_{eq}}\sin\left(\omega(t_e - t_2)\right) + 1 - \frac{V_{dc}}{V_1}\frac{L_b}{L_{load}}\right]\right. \tag{14}$$

$$i_{ac+,peak} = i_{ac} + (t_3) = \frac{kL_{load}C_{eq}}{L_b}[2 - \cos\omega_{eq}(t_3 - t_2) - \cos\omega_{eq}(t_3 - t_e)] + V_1 L_{load}\sqrt{\frac{C_{eq}}{L_a L_b L_{ac}}}\sin\omega_{eq}(t_3 - t_2) \tag{15}$$

$$V_{gs}(s) = \frac{sL_{load}R_g C_{gd1} V_{ex,b}(s)}{s^3\left(L_a L_{ac} R_g\left(C_{iss}C_{eq} + C_{gs1}C_{gd1}\right)\right) + s^2\left(L_a L_{ac}\left(C_{eq} + C_{gd1}\right)\right) + s(C_{iss}R_g L_b) + L_b} \tag{16}$$

$$V_{gs,mea}(s) = V_{gs}(s) \cdot \frac{R_{g,ext}}{R_{g,ext} + R_{g,int}}. \tag{17}$$

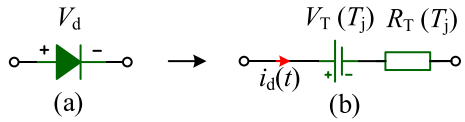


Fig. 11. (a) Diode. (b) Equivalent circuit.

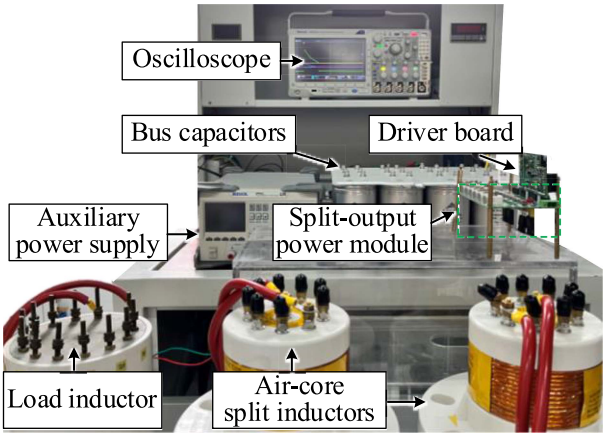


Fig. 12. Experimental test bench for split-output power module.

in (21)

$$V_d(t) = V_T(T_j) + i_d(t) \cdot R_T(T_j) \tag{20}$$

$$P_d(t) = V_T(T_j) \cdot i_d(t) + i_d^2(t) \cdot R_T(T_j). \tag{21}$$

The diode thermal impedance is fitted to a partial fraction model can be expressed as (22). Then, the diode junction temperature can be calculated as

$$Z_{\text{th}}(t) = \sum_{i=1}^{n} R_{\text{th},i}(1 - e^{-t/\tau_i}) \tag{22}$$

$$\begin{aligned} T_j(t) &= P_d(t) * Z_{\text{th}}(t) + T_a \\ &= \int_0^{\infty} P_d(\tau) \cdot Z_{\text{th}}(t-\tau)d\tau + T_a \end{aligned} \tag{23}$$

where T_a is the ambient temperature.

III. Application of Models Considering Normal Operation and Short-Circuit Fault

The flowchart to determine the optimal split inductance range is illustrated in Fig. 13. The optimal split inductance is strongly related to the application scenarios. Thus, the parameters of the power loop, devices, and gate driver should be extracted first. Then, with the above expressions, the effects of the split inductance on the switching loss, crosstalk voltage, undesirable oscillation, and short-circuit thermal stress can be depicted, respectively. The lower limit of the split inductance is obtained considering the lowest switching loss and safe crosstalk voltage, while the upper limit is determined to avoid undesirable oscillation and excessive junction temperature.

TABLE II
Charge Equivalent Capacitance of Devices

$C_{\text{gs,eq}}$	$C_{\text{gd,eq}}$	$C_{\text{ds,eq}}$	$C_{\text{d,eq}}$
5987pF	18pF	491pF	288pF

TABLE III
Fitting Coefficients of Relationship Among Diode Forward Voltage, Junction Temperature, and Current

α_1	β_1	α_2	β_2
0.9276	-0.001746	0.02078	0.000161

TABLE IV
Coefficients of Five-Order Partial Fraction Model

i	1	2	3	4	5
$R_{\text{th},i}$ [K/W]	0.0154	0.0432	0.1475	0.0954	0.5681
$C_{\text{th},i}$ [W·s/K]	0.0018	0.0221	0.0448	0.6394	1.3961

Taking the CREE C3M0016120K and C4D40120D as examples, the devices operate with $V_{\text{dc}} = 600$ V, ambient temperature $T_a = 25$ °C, and gate driver voltage +15 V/-5 V. The parameters extraction of the devices is illustrated in the following.

1) *Junction Capacitance*: Given that the junction capacitances of the MOSFET and diode are voltage-dependent, the charge equivalent capacitance model is utilized to simplify the calculation [20], as shown in (24). Table II gives the device's equivalent junction capacitances, which are used for the calculation during the voltage variation process

$$C_{j,\text{eq}} = \frac{1}{V_{\text{dc}}} \int_0^{V_{\text{dc}}} C_j(v_{ds}) dv_{ds} \quad \text{with } j = gs,\ gd,\ ds,\ d \tag{24}$$

where $C_{gs,\text{eq}}$, $C_{gd,\text{eq}}$, $C_{ds,\text{eq}}$, $C_{d,\text{eq}}$ represent the MOSFET gate-source, gate-drain, drain-source capacitance, and diode capacitance, respectively.

2) *Diode Conduction Voltage*: As shown in Fig. 11, (20) and (25), a conducting diode can be modeled as a temperature-dependent voltage source V_T and a resistor R_T in series. By fitting the diode forward characteristics, the coefficients can be extracted as given in Table III

$$\begin{cases} V_T(T_j) = \alpha_1 + \beta_1 \cdot T_j \\ R_T(T_j) = \alpha_2 + \beta_2 \cdot T_j \end{cases}. \tag{25}$$

3) *Diode Thermal Impedance*: The diode junction-case thermal impedance curve in the datasheet is fitted to a five-order partial fraction model as shown in (26), of which the thermal resistance and capacitance are given in Table IV

$$\begin{cases} Z_{\text{th}}(t) = \sum_{i=1}^{n=5} R_{\text{th},i}(1 - e^{-t/\tau_i}) \\ \tau_i = R_{\text{th},i} \cdot C_{\text{th},i} \end{cases}. \tag{26}$$

IV. Experimental Validation

A. Testbench

Fig. 12 shows the experimental test bench. The bus capacitance is 4800 μF. The load inductance is 520 μH. The inductances of the air-core split inductor with multiple taps vary

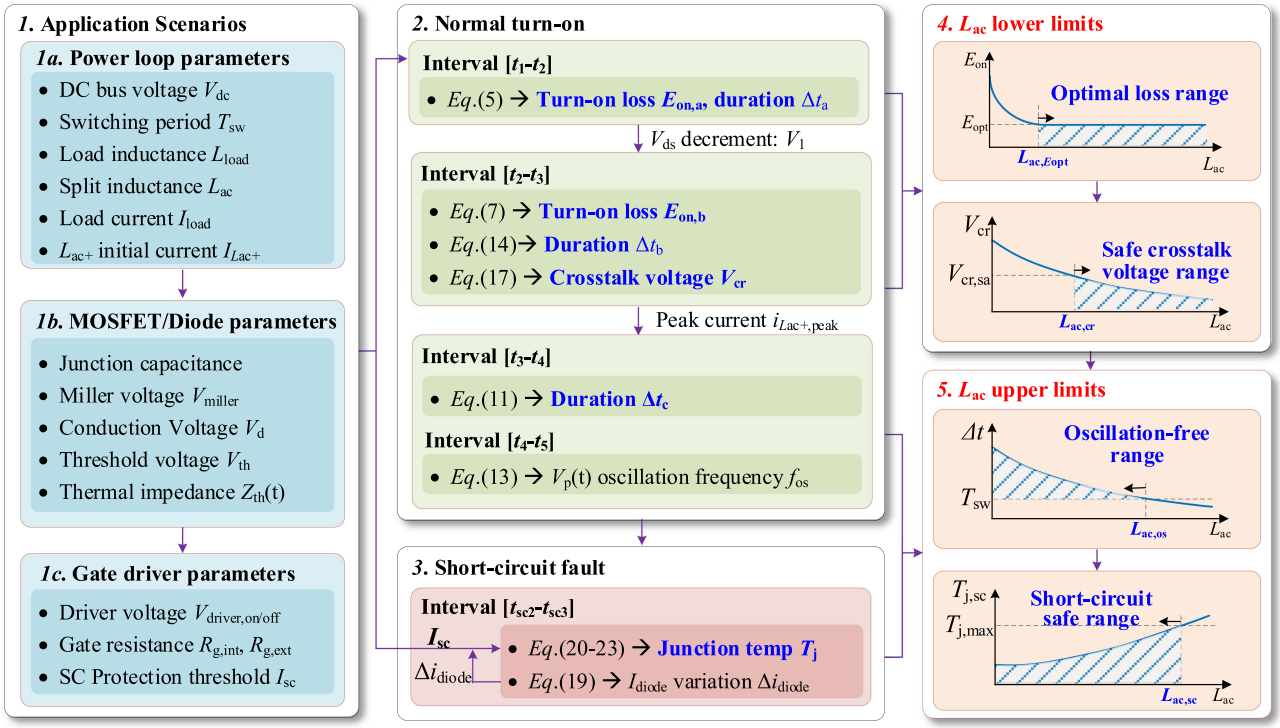


Fig. 13. Design guideline of optimal split inductance range considering constraints of normal and fault conditions.

from 1 to 20 μH. The parasitic capacitance of the air-core split inductor is neglected. As for the split inductance from tens of nH to hundreds of nH, it is achieved by twisted copper wires. The parasitic inductance of the wire connecting the air-core split inductor and the split-output power module is also considered and measured as around 600 nH. Regarding the measurement equipment, a differential voltage probe (SI-9010A) is adopted to measure the switching voltage. The current probe (CWT UM/6/B/1/80) is employed for current detection.

B. Suppression of Crosstalk Voltage and Turn-On Loss

Double pulse tests are conducted with various split inductances. The turn-ON and turn-OFF gate resistance is 15 and 39 Ω respectively to avoid the gate voltage ringing. Experimental waveforms with split inductance $L_{\rm ac} = 0$ μH and $L_{\rm ac} = 20$ μH are shown as examples in Fig. 14.

The experimental waveforms intuitively illustrate the suppression effect of the split inductance on the crosstalk voltage. It can be seen that the crosstalk voltage has risen to nearly 3.52V with $L_{\rm ac} = 0$ μH, which far exceeds the device threshold voltage of 1.8 V. With $L_{\rm ac} = 20$ μH, the crosstalk voltage is reduced to only 1.6 V.

The theoretical crosstalk voltage $V_{gs,\rm mea}$ in the time domain is calculated by the inverse Laplace transform of (17) and compared with the experimental results as shown in Fig. 15. The calculated and experimental results are generally consistent, which verifies the accuracy of the established model. Given that the crosstalk voltage decreases with the split inductance, the lower limit of the split inductance should prevent the device from falsely turning ON, as shown in

$$V_{cr}(L_{\rm ac}) < V_{\rm th} - V_{\rm drive,off} \tag{27}$$

where $V_{\rm th}$ is the threshold voltage of the device and $V_{\rm drive,off}$ is the turn-OFF gate voltage.

The turn-ON loss is also reduced by the split inductor since the turn-ON current overshoot is decreased, as shown in Fig. 14. It can be seen that the turn-ON current overshoot is only 4 A with $L_{\rm ac} = 20$ μH, while the turn-ON current overshoot is 22 A without the split inductor.

To verify the accuracy of the theoretical model (8) for the turn-ON loss, the calculation results are compared with the experimental results, as shown in Fig. 16. The vertical bias between the experimental and theoretical results is because the theoretical results only consider the turn-ON loss during the voltage variation phase. Nevertheless, the turn-ON loss variation trends of the experiments and theoretical calculations are generally consistent. Fig. 16 shows that the turn-ON loss decreases with the split inductance. Besides, it is worth noting that there is a split inductance turning point ($L_{\rm ac,Eopt}$), above which the turn-ON loss remains unchanged. The existence of the split inductance turning point can be explained as the $i_{\rm ac+}$ remains constant during the voltage variation phase of the active device when the split inductance is high enough. The split inductance turning points can also be extracted with the proposed model. It can be seen that the turn-ON gate resistance is an influencing factor of the split inductance turning point, as shown in Fig. 16. The split inductance turning point increases with the gate resistance. Therefore, the $L_{\rm ac}$ should be selected to exceed the split inductance turning point at least to achieve the lowest switching loss

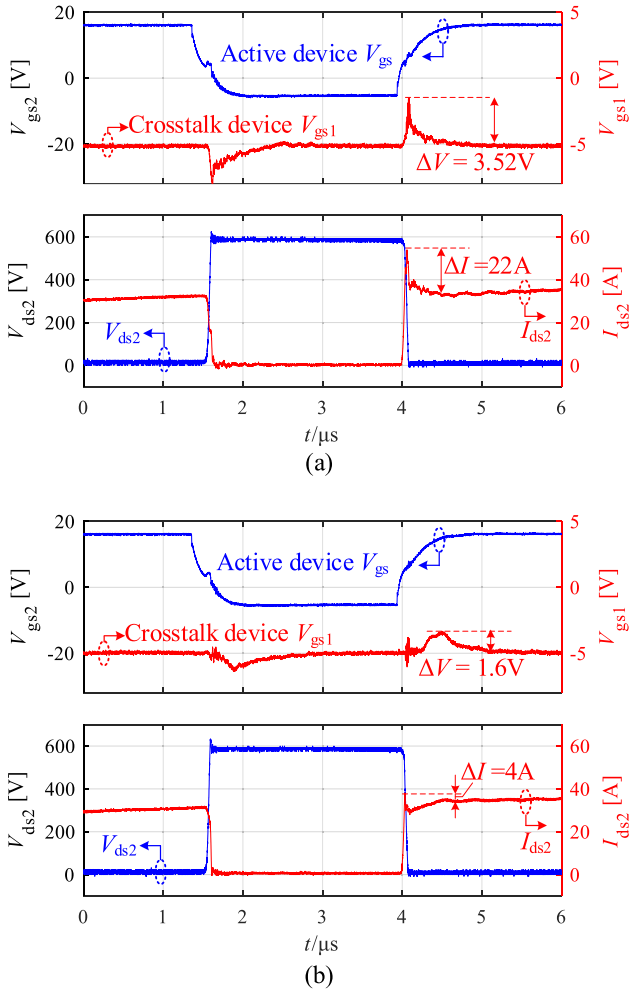


Fig. 14. Double pulse tests waveforms of split-output power module. (a) $L_{\rm ac}$ = 0 μH. (b) $L_{\rm ac}$ = 20 μH.

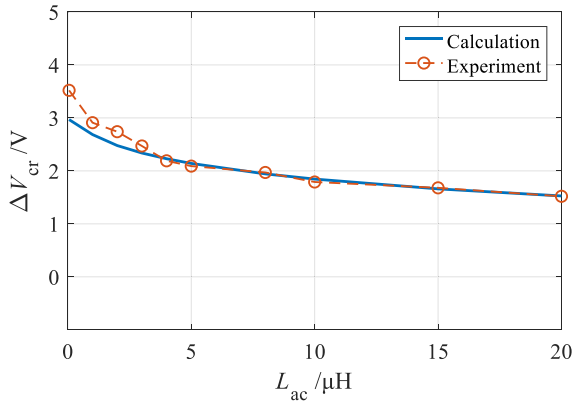


Fig. 15. Comparison of crosstalk voltage between calculated and experimental results with various split inductances and $L_{\rm load}$ = 520 μH.

as shown in

$$E_{\rm on}(L_{\rm ac}) \le E_{\rm opt} \tag{28}$$

where $E_{\rm on}$ and $E_{\rm opt}$ represent the $L_{\rm ac}$-dependent turn-ON loss and optimal turn-ON loss, respectively.

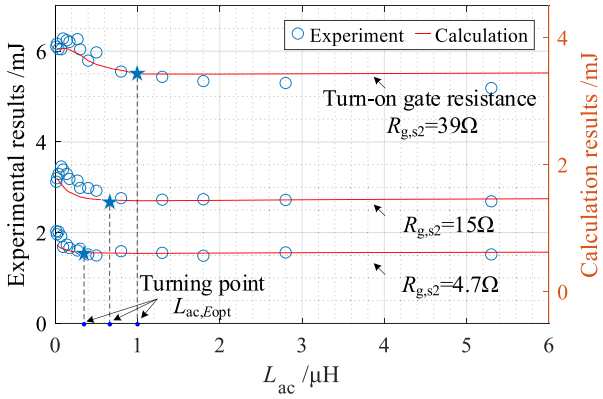


Fig. 16. Turn-ON loss variation with split inductance and turn-ON gate resistance.

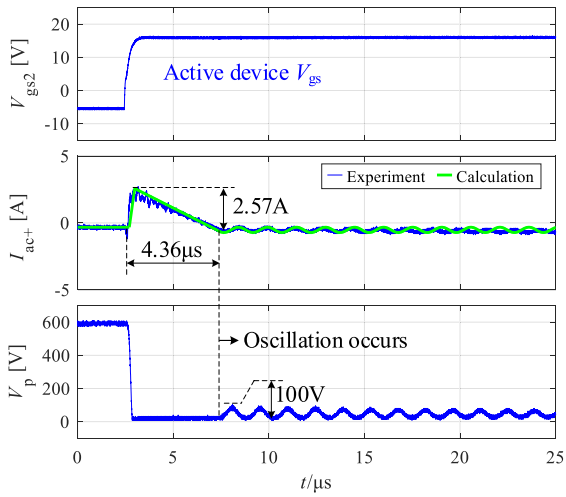


Fig. 17. Oscillation phenomenon of split-output power module with $L_{\rm ac+}$ = 20 μH and $L_{\rm load}$ = 520 μH.

C. Oscillation Analysis and Avoidance

As the above analysis, the current through $L_{\rm ac+}$ decreasing to zero triggers the undesirable oscillation on the node P voltage when the active device S_2 turns ON. The closer the split inductance and load inductance, the more obvious the oscillation phenomenon. The experimental waveforms with split inductance $L_{\rm ac}$ = 20 μH and load inductance $L_{\rm load}$ = 520 μH are shown as an example in Fig. 17. It can be seen that the current i_{Lac+} through $L_{\rm ac+}$ first increases and then decreases to zero, then the oscillation occurs and the voltage oscillation amplitude rises to around 100 V. The duration Δt_{Lac+} of the i_{Lac+} and oscillation frequency can be calculated by (12) and (13), respectively. The calculated results of i_{Lac+} are generally consistent with the experimental results as shown in Fig. 17. It can be concluded that the calculation model is accurate in calculating the duration Δt_{Lac+} and oscillation frequency $f_{\rm os}$. In addition, the experiments with $L_{\rm ac+}$ = 8 μH, 10 μH, and 15 μH are also conducted. The comparison of the duration Δt_{Lac+} between the calculation and experimental results is given in Table V. The calculation results agree with the experimental results generally, which verifies the accuracy of the proposed

TABLE V
COMPARISON BETWEEN CALCULATION AND EXPERIMENTS RESULTS FOR $\Delta t_{1\mathrm{AC}+}$ AND F_{os} WITH 520 μH LOAD INDUCTANCE

	L_{ac} [μH]	8	10	15	20
Δt_{Lac+} [μs]	Calculation	6.474	5.972	5.115	4.567
	Experiment	6.436	5.704	4.876	4.360
	Error	0.59%	4.69%	4.91%	4.75%
f_{os} [MHz]	Calculation	0.995	0.891	0.758	0.658
	Experiment	0.950	0.870	0.780	0.692
	Error	4.78%	2.43%	2.84%	4.94%

model for i_{Lac+} calculation. The duration decreases with the increasing split inductance. It can be explained that the higher the split inductance, the higher the voltage divided by the split inductor when connected in series with the load inductor, then the faster the changing rate of the current across the split inductor. Besides, the oscillation loop is also verified by comparing the calculated results of the oscillation frequency with the experimental results, as given in Table V. It can be deduced that the oscillation frequency decreases with the increasing split inductance.

Therefore, to avoid undesirable oscillation, a proper split inductance should satisfy that the duration Δt_{Lac+} of the current through L_{ac+} is longer than the switching period T_{sw}, as shown in

$$\Delta t_{Lac+}(L_{ac}) \geq T_{sw}. \tag{29}$$

D. Effects of Split Inductance on Short-Circuit Thermal Stress

As shown in Fig. 18, the short-circuit experiments are conducted with $L_{ac} = 10\ \mu$H and 20 μH. The current and voltage of the diode are monitored. The active device S_2 is shut down by the gate driver once the current reaches four times the nominal current to avoid failure. It can be seen that the larger the split inductance, the longer the freewheeling process lasts.

During the short-circuit freewheeling phase, the diode time-varying heat power can be calculated by (21) and compared with experimental results, as shown in Fig. 19. In addition, the experimental and calculated junction temperature curves are obtained by convolving the thermal impedance network with experimental and calculated power loss, respectively. The calculated and experimental results of the power loss and junction temperature are generally consistent, which proves the accuracy of the proposed thermal-electrical model.

It can be seen that the junction temperature first increases and then decreases with freewheeling time. The magnitude of the junction temperature increment increases with the split inductance and is 37 °C and 50 °C with $L_{ac} = 10\ \mu$H and $L_{ac} = 20\ \mu$H, respectively. Besides, the peak junction temperature occurs approximately at the midpoint of the heating power. Therefore, given that the maximum allowed junction temperature of the diode is limited, thus, the maximum split inductance needs to

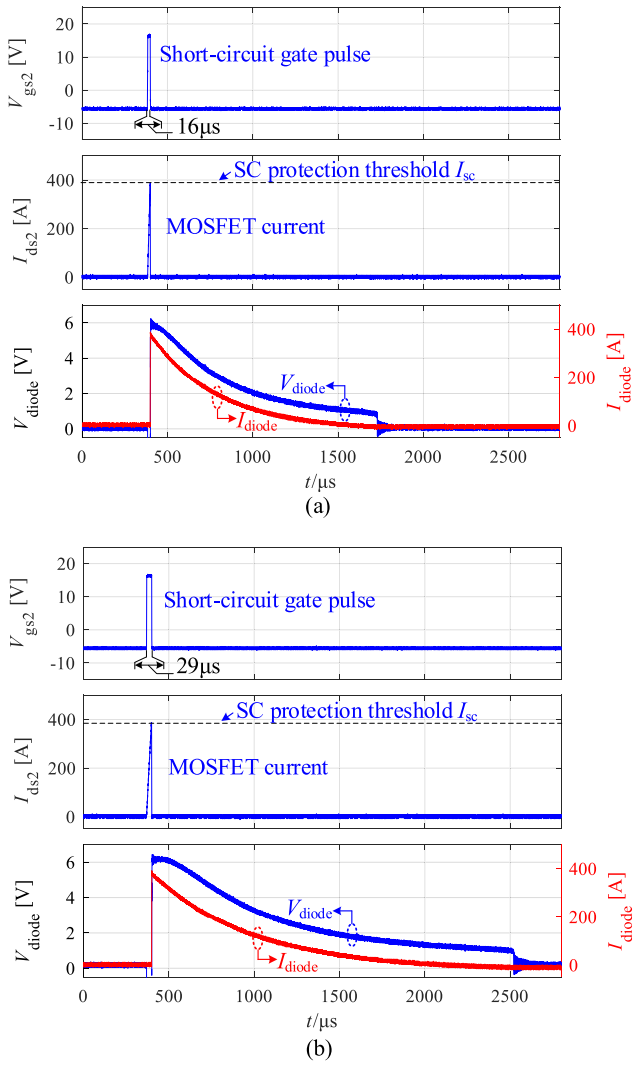


Fig. 18. Experimental short-circuit waveforms. (a) $L_{ac} = 10\ \mu$H. (b) $L_{ac} = 20\ \mu$H.

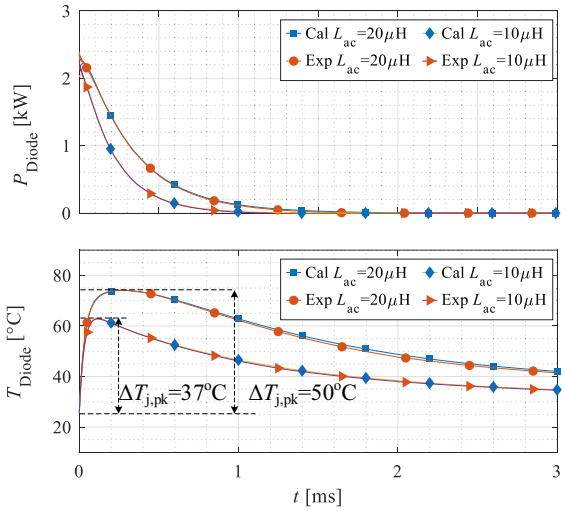


Fig. 19. Comparison of diode power loss and junction temperature with various split inductances and $I_{sc} = 400$ A.

TABLE VI
OPERATION CONDITIONS

Parameter	Value
Bus voltage V_{DC}	900 V
Load inductance	300 μH
Switching frequency f_{sw}	150 kHz
On/off gate resistance	15 Ω/39 Ω
Gate driver on/off voltage	+18 V/-3 V
Short-circuit protection current	600 A
Ambient temperature	75 °C
Maximum junction temperature	175 °C

meet

$$\Delta T_{j,pk}(L_{\mathrm{ac}}) \leq T_{j,\max} - T_a \tag{30}$$

where $\Delta T_{j,pk}$ is the magnitude of the junction temperature increment, $T_{j,\max}$ is the maximum allowed junction temperature, and T_a is the ambient temperature.

E. Example Analysis

As the above analysis and comparison, the accuracy of the proposed models considering the normal operation and short-circuit fault conditions are verified. Then, the flowchart summarized in Fig. 13 can be utilized to determine the upper and lower limits of the split inductance. A design example under the operation conditions given in Table VI is demonstrated. The devices under test including SiC MOSFET and diode remain unchanged, thus the device parameters derived in Section III can be utilized.

a) *Turn-On Loss Optimization:* With the bus voltage, load inductance, and gate driver parameters, the relationship between the turn-ON loss and split inductance can be calculated by (5)–(8). The split inductance turning point $L_{\mathrm{ac,Eopt}}$ achieving the lowest turn-ON loss can be derived as 0.9 μH, which is one of the lower limits of the split inductance.

b) *Crosstalk Voltage Optimization:* When the SiC MOSFET under test operates at an ambient temperature of 75 °C, the threshold voltage V_{th} can be as low as around 1 V. Given that the gate driver OFF voltage is −3 V, the maximum crosstalk voltage should not exceed 4 V. Then the relationship between the crosstalk voltage and split inductance can be calculated by (17). The crosstalk voltage is 3.97 V when the split inductance exceeds 0.25 μH. Thus, the other lower limit of the split inductance is 0.25 μH, which avoids the false turn-ON of the device.

c) *Oscillation-Free Optimization:* The switching period can be calculated as 6.67 μs according to Table VI**.** To avoid undesirable oscillation, the duration $\Delta t_{L\mathrm{ac}+}$ of the current through $L_{\mathrm{ac}+}$ should be longer than the switching period. The relationship between the duration $\Delta t_{L\mathrm{ac}+}$ and split inductance can be calculated by (12). The duration $\Delta t_{L\mathrm{ac}+}$ is calculated as 6.70 μs when the split inductance is 2.2 μH, which is regarded as one of the upper limits of the split inductance.

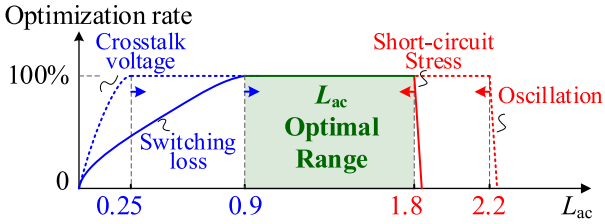


Fig. 20. Optimal split inductance range corresponding to various optimization objects.

d) *Short-Circuit Thermal Stress Optimization:* When the short-circuit SiC MOSFET is shut down, the short-circuit current freewheels through the diode and split inductors. The initial short-circuit freewheeling current through the diode is 600 A, as given in Table VI. The relationship between the diode maximum junction temperature and split inductance can be obtained by (23). The diode junction temperature reaches the maximum allowable junction temperature of 175 °C when the split inductance is 1.8 μH. Thus, the other upper limit of the split inductance is 1.8 μH, which avoids the excessive short-circuit thermal stress on the diode.

As a result, the optimal split inductance ranges corresponding to various optimization objects are calculated respectively, as shown in Fig. 20. The goal of achieving the minimum switching loss and safe crosstalk voltage determines the lower limit of the split inductance, while the goal of avoiding undesirable oscillation and excessive junction temperature defines the upper limit of the split inductance. Therefore, the optimal split inductance range is [0.9 μH–1.8 μH] for the predefined operation conditions.

V. CONCLUSION

The split-output structure possesses the potential superiorities in switching loss reduction, crosstalk voltage suppression, and zero dead time over the general half-bridge structure. The split inductance is the key to achieving the potential advantages of the split-output structure. Therefore, this article analyzes the characteristics of the split-output power module under both the normal operation and short-circuit fault by establishing *s*-domain models in stages. The accuracy of the models is verified by experiments. The influence mechanisms of the split inductance on the operation characteristics of the split-output power module are revealed based on the proposed models. The switching loss and crosstalk voltage decrease with the split inductance. The lowest switching loss is obtained once the split inductance exceeds the turning point. The split inductance turning point increases with the gate resistance. Besides, the negative effects of the improper split inductance are first uncovered and analyzed. It is observed that the undesirable oscillation and excessive short-circuit thermal stress are introduced by a high split inductance. Therefore, the calculation method of the split inductance upper limit is also demonstrated. As a result, a flowchart is presented to calculate the optimal split inductance range, relying only on the application conditions and device datasheet parameters.

The optimal split inductance range under the specific operation conditions is also demonstrated as an analysis case.

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