Model-Predictive Dual-Control Loop With Improved Current-Limiting Capability for Grid-Forming Inverter Under Grid Faults

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***Abstract*—Current-limiting capability is crucial for fault ride-through of grid-forming (GFM) inverters. Most current-limiting schemes for GFM inverters are implemented within classical linear controllers, which cannot guarantee optimal performance in case of emergencies like faults. Additionally, the inherent cascaded structure limits the bandwidth. The advanced model-predictive control (MPC) has been developed for power converters thanks to nonlinear objectives and constraints handling ability. One of the well-known MPCs, i.e., the finite-control-set MPC (FCS-MPC) has been employed to prevent overcurrent, which roughly includes a nonlinear penalization for current magnitude violation in the cost function. In this case, the cost function of FCS-MPC will go to infinity during faults at the expense of the voltage and current reference tracking ability, and thus, the power quality gets worse. Besides, the weighting factor design is usually a nontrivial task for MPC. To maintain the high bandwidth benefit of MPC and improve the power quality during faults, a model-predictive dual-control loop (MP-DCL) is proposed in this article. The proposed method involves the outer-voltage MPC loop to generate the optimal current reference. With the current-limiting factor applied, such a constrained reference will be tracked through the proposed inner-current MPC loop. The proposed MP-DCL expresses simple design benefits and ensures the GFM system recovers from fault to normal conditions smoothly with low overshoots and without oscillation. Experimental results verify the effectiveness of the proposed strategy through numerous comparisons with state-of-the-art solutions.**

***Index Terms*—Current-limiting, grid-forming inverters, model-predictive dual-control loop, power quality, resilient grid.**

I. Introduction

GRID-FORMING (GFM) inverters are gradually favored by industry and academia since they can not only operate stably under weak grids [1] but also in grid-connected and islanded modes [2]. However, unlike traditional synchronous generators, which can tolerate several times of overcurrent under faults, GFM inverters can only withstand 1.2–1.5 per unit (p.u.) of overcurrent due to the low thermal inertia of semiconductor switches [3]. Moreover, with a high penetration of power electronic devices and critical loads in the modern power system, inverters are required to remain connected to the power system and ride through faults [4]. Therefore, fault ride-through (FRT) strategies with superior current-limiting capabilities are vital for GFM inverters.

The majority of existing current-limiting schemes for GFM inverters are categorized into indirect current-limiting methods and direct current-limiting methods [3], [4], [5], [6], [7], [8], [9], [10], [11]. Indirect current-limiting strategies usually prevent overcurrent via modifying voltage references [3], [4]; thus, the dynamic response of indirect current-limiting methods is usually slow, inducing transient overcurrent. Additionally, the impedance design is complex and inflexible due to the high dependency on system parameters and fault types [4], [11]. Despite the virtual resistor implemented in terminal voltages can realize fast current limiting, the impedance design still requires complex tuning [10]. On the other hand, direct current-limiting schemes straightly modify current references in the current-control loop, ensuring a simple and fast current-limiting capability under faults. They mainly comprise the instantaneous limiter [7], [11], [12], the magnitude limiter [3], [6], [7], and the priority-based limiter [5], [7], [9], [10], as introduced in [8]. However, windup issues often occur in direct current-limiting strategies with classical linear controllers during faults, impeding inverters' recovery from fault to normal conditions. Therefore, additional antiwindup schemes such as the tracking integration antiwindup scheme must be applied and well designed in direct current-limiting schemes with linear controllers [12], which further complicates the system design.

Moreover, both indirect and direct current-limiting schemes for GFM inverters are implemented within the classical linear controller framework [3], [4], [5], [6], [7], [8], [9], [10], [11], which cannot guarantee optimal performance in case of emergencies like faults since classical linear controllers are usually tuned based on an operation point. In addition, a cascaded structure (outer-voltage loop and inner-current loop) with linear controllers, such as proportional-integral (PI)/proportional-resonant (PR) controllers, is usually adopted to realize the voltage and current reference tracking [13], where two groups of PI/PR controller parameters should be tuned. Moreover, to decouple the outer-voltage loop and the inner-current loop, the bandwidth

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of the outer-voltage loop is designed to be significantly lower than the bandwidth of the inner-current loop, which not only increases the tuning effort but also degrades the fault recovery for GFM inverters [14].

Recently, model predictive control (MPC) has been widely implemented for GFM inverters due to its superior advantages: fast dynamic response, intuitive concept, multiobjective optimization, nonlinear objectives, and constraints handling ability [15], [16], [17]. They are mainly categorized into two types according to the ways of generating control inputs: one is the direct utilization of finite switching states to minimize the cost function and sending the selected switching states to inverters, i.e., finite-control-set MPC (FCS-MPC); the other is to deduce the optimal voltage vector (OVV) that minimizes the cost function and synthesize the derived OVV by modulators. Currently, MPC-based current-limiting strategies for GFM inverters under faults or voltage sags are mainly implemented through FCS-MPC [15], [18], [19], [20], [21], [22], and the typical manner is to include the current magnitude violation penalization into the cost function, which turns into infinity to penalize the cost function under overcurrent conditions [15], [19], [22]. Similarly, the supplemented nonlinear term is changed into the magnitude of fault currents [20]. However, this penalization for current magnitude violation sacrifices the voltage and current reference tracking, resulting in significant voltage and current distortions. The overcurrent mitigation strategy in [23] does not consider grid faults, and it also adopts the nonlinear term in the cost function, which will also cause severe power quality issues during grid faults. In addition, the FCS-MPC also preserves a drawback that the high sampling frequency requirement is hindered by the computational capability of general digital controllers [14]. Furthermore, a variable switching frequency from FCS-MPC will increase switching losses and spread harmonic spectra [24], and the nontrivial weighting factor makes it difficult to achieve optimal performance, where both voltages and currents should be regulated [15].

The cascaded linear controller-based current-limiting strategies are complex in parameter design, and the low bandwidth of the outer-voltage loop impedes the fault recovery performance; the FCS-MPC-based current-limiting strategies result in harmonic distortion during faults. To fill these gaps, in this article, a model-predictive dual-control loop (MP-DCL) with improved current-limiting capability is proposed to improve the fault recovery performance and ensure the power quality during faults for GFM inverters. The proposed scheme separates the simultaneous voltage control and current control in one cost function into two individual MPC loops. The outer-voltage MPC loop realizes the voltage reference tracking and generates the unconstrained current reference in a deadbeat manner. The generated current reference from the outer-voltage MPC loop may exceed the maximum FRT current threshold during faults; thus, the current-limiting factor is adopted to proportionally scale down the current reference to the current threshold, which not only ensures a sinusoidal current reference but also fully utilizes the overcurrent capability of GFM inverters [3], [8]. Consequently, the current reference tracking is implemented in the inner-current MPC loop, where the OVV is derived by calculating the minimal analytical solution of the cost function and synthesized by a sinusoidal pulsewidth modulation (SPWM) block. In summary, the contributions of this article can be summarized as follows.

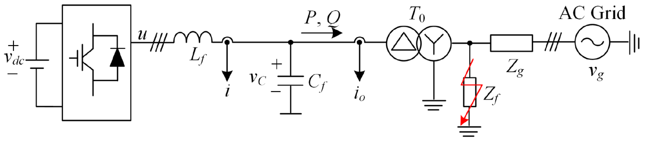


Fig. 1. Single-line diagram of a grid-connected GFM inverter.

1) Compared with the state-of-the-art cascaded linear controller-based current-limiting strategies for GFM inverters, the control bandwidths have been enhanced, especially for the outer-voltage control loop. As a result, around the fault clearance, the voltage recovers faster, the active power recovers to normal values without oscillation, and the reactive power recovers to normal values with lower overshoots. Moreover, antiwindup issues can be avoided in the proposed MP-DCL without the adoption of classical linear controllers.
2) Compared with the state-of-the-art FCS-MPC-based current-limiting strategies, the nontrivial weighing factor design can be avoided and active and reactive power overshoots around fault clearance are lower. In addition, the power quality during faults can be guaranteed since the current-limiting scheme only proportionally scales down the magnitude of the current reference, and the inner-current MPC loop ensures the current tracks such constrained reference. At the same time, the capacitor voltage during faults can track the voltage reference to the maximum extent, which is better than the aggressive manner by simply ignoring the power control property as employed in FCS-MPC. The proposed MP-DCL, thus, obtains better power quality. Moreover, the proposed strategy also maintains the constant switching frequency benefit.

II. SYSTEM MODELING AND FCS-MPC-BASED CURRENT-LIMITING SCHEME

A. System Modeling

Fig. 1 shows the single-line diagram of a grid-connected GFM inverter, where L_f and C_f denote the inductance and capacitance of the LC filter, T_0 is a delta-wye transformer, Z_g denotes the grid equivalent impedance, and Z_f denotes the fault impedance. Similarly, v_{dc} denotes the dc-link voltage, u denotes the inverter terminal voltage, i denotes the inverter-side current, v_C denotes the capacitor voltage, i_o denotes the output current, P denotes the output active power, and Q denotes the output reactive power.

According to Fig. 1, the continuous-time state-space model is shown as

$$\frac{d\mathbf{x}}{dt} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix}}_{\mathbf{A}} \mathbf{x} + \underbrace{\begin{bmatrix} \frac{1}{L_f} \\ 0 \end{bmatrix}}_{\mathbf{B}} \mathbf{u} + \underbrace{\begin{bmatrix} 0 \\ -\frac{1}{C_f} \end{bmatrix}}_{\mathbf{B}_g} \mathbf{i}_o \qquad (1)$$

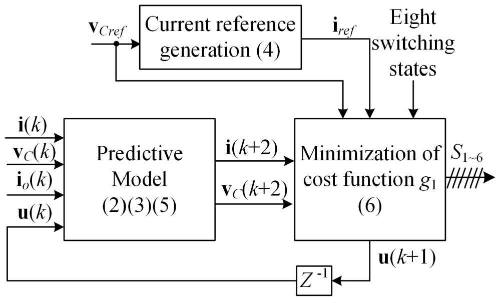


Fig. 2. Inner-loop diagram of FCS-MPC-based current-limiting scheme [15].

where $\mathbf{x} = [\mathbf{i}\ \mathbf{v}_C]^T, \mathbf{i} = i_\alpha + ji_\beta, \mathbf{v}_C = v_{C\alpha} + jv_{C\beta}, \mathbf{u} = u_\alpha + ju_\beta$, and $\mathbf{i}_o = i_{o\alpha} + ji_{o\beta}$. The signals in the $\alpha\beta$-frame are transferred from the *abc*-frame through *Clarke* transformation. According to the zero-order-holder principle, (1) can be discretized to deduce the predictive equation, which is

$$\mathbf{x}(k+1) = \mathbf{A}_d\mathbf{x}(k) + \mathbf{B}_d\mathbf{u}(k) + \mathbf{B}_{gd}\mathbf{i}_o(k) \tag{2}$$

where k is the current time instant. Assuming the sampling period is T_{s1}, the discrete matrix $\mathbf{A}_d$, $\mathbf{B}_d$, and $\mathbf{B}_{gd}$ can be calculated as

$$\mathbf{A}_d = e^{\mathbf{A}T_{s1}} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}, \mathbf{B}_d = \int_0^{T_{s1}} e^{\mathbf{A}\tau}\mathbf{B}_d d\tau = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix}$$
$$\mathbf{B}_{gd} = \int_0^{T_{s1}} e^{\mathbf{A}\tau}\mathbf{B}_{gd} d\tau = \begin{bmatrix} b_{g1} \\ b_{g2} \end{bmatrix}. \tag{3}$$

B. FCS-MPC-Based Current-Limiting Scheme

The FCS-MPC-based current-limiting scheme from [15], [19] is introduced in this section. The inner-loop diagram of the FCS-MPC-based current-limiting scheme is shown in Fig. 2, where voltage reference $\mathbf{v}_{Cref} = v_{C\alpha ref} + jv_{C\beta ref}$ comes from the outer-droop control loop, which will be specifically introduced in the following section. To improve voltage control accuracy, both capacitor voltage and inductor current tracking objectives are integrated into the cost function. The current references can be deduced from

$$\begin{cases} i_{\alpha ref} = i_{o\alpha} - \omega_{ref}C_f v_{C\beta ref} \\ i_{\beta ref} = i_{o\beta} + \omega_{ref}C_f v_{C\alpha ref} \end{cases} \tag{4}$$

where ω_{ref} denotes the angular frequency reference from the outer-droop control loop. To compensate for the time delay, a two-step forward prediction is employed, and the corresponding equation to calculate the inductor current and capacitor voltage at $k+2$ instant is written as

$$\mathbf{x}(k+2) = \mathbf{A}_d\mathbf{x}(k+1) + \mathbf{B}_d\mathbf{u}(k+1) + \mathbf{B}_{gd}\mathbf{i}_o(k+1) \tag{5}$$

where $\mathbf{x}(k+1)$ can be derived from (2), and $\mathbf{i}_o(k+1)$ is substituted with $\mathbf{i}_o(k)$ due to the slow dynamics of the output current. Eight switching states in FCS-MPC are utilized to minimize the cost function to determine the optimal switching states in each sampling period. The switching states and corresponding voltage vectors are listed in Table I.

TABLE I
SWITCHING STATES AND VOLTAGE VECTORS

Index n	Switching state S_{abc}	Voltage vector $\mathbf{u}$
0	000	0
1	100	$2V_{dc}/3$
2	110	$V_{dc}/3 + j\sqrt{3}V_{dc}/3$
3	010	$-V_{dc}/3 + j\sqrt{3}V_{dc}/3$
4	011	$-2V_{dc}/3$
5	001	$-V_{dc}/3 - j\sqrt{3}V_{dc}/3$
6	101	$V_{dc}/3 - j\sqrt{3}V_{dc}/3$
7	111	0

In addition to regulating voltages and currents, a nonlinear term is also included in the cost function to prevent overcurrent [15]. The final cost function g_1 is written as

$$g_1 = (v_{C\alpha ref} - v_{C\alpha}(k+2))^2 + (v_{C\beta ref} - v_{C\beta}(k+2))^2$$
$$+\gamma\left[(i_{\alpha ref} - i_\alpha(k+2))^2 + (i_{\beta ref} - i_\beta(k+2))^2\right] + I_{lim} \tag{6}$$

where γ is a weighting factor, which can be determined by trial and error [17]. Eight switching states for $\mathbf{u}(k+1)$ will be optimized to minimize the cost function g_1, and the corresponding optimal switching signals will be directly sent to inverters. Moreover, I_{lim} is the nonlinear term to prevent overcurrent, which is expressed as

$$I_{lim} = \begin{cases} \infty, & \text{if } \|\mathbf{i}(k+2)\| > I_{th} \\ 0, & \text{if } \|\mathbf{i}(k+2)\| \leq I_{th} \end{cases}. \tag{7}$$

As shown in (6), during normal conditions, I_{lim} is zero without affecting the voltage and current reference tracking. However, during faulty conditions, I_{lim} will go to infinity due to the current magnitude violation, which penalizes the whole cost function. In this case, both the voltage and current reference tracking cannot be accomplished, and thus, the power quality will be impaired severely.

III. PROPOSED MODEL-PREDICTIVE DUAL-CONTROL LOOP WITH IMPROVED CURRENT-LIMITING CAPABILITY

The block diagram of the proposed MP-DCL with improved current-limiting capability is shown in Fig. 3, where the outer-droop control loop, outer-voltage MPC loop, current-limiting loop, inner-current MPC loop, predictive loop, and modulation loop are illustrated.

A. Outer-Droop Control Loop

A typical droop control from [3], [4] is adopted, which is shown as the outer-droop control loop in Fig. 3, where P and Q denote average active and reactive powers, which can be deduced as

$$\begin{cases} P = 1.5(v_{C\alpha}i_{o\alpha} + v_{C\beta}i_{o\beta})s/(s+\omega_c) \\ Q = 1.5(v_{C\beta}i_{o\alpha} - v_{C\alpha}i_{o\beta})s/(s+\omega_c) \end{cases} \tag{8}$$

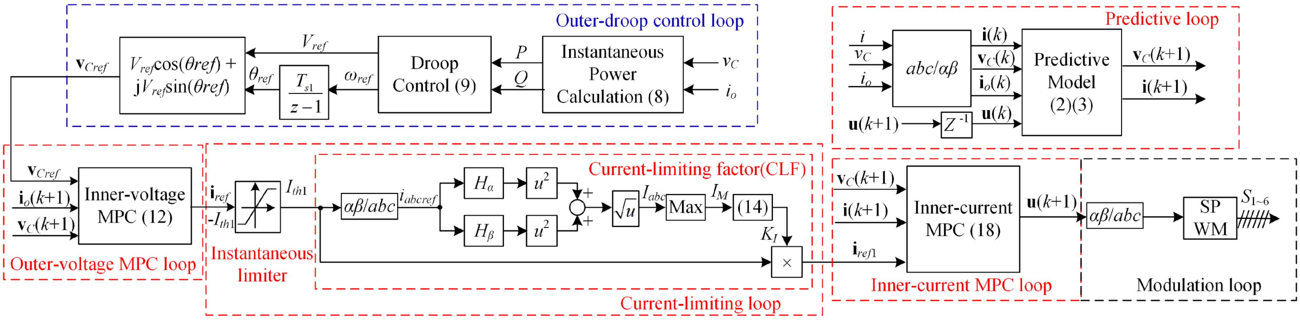


Fig. 3. Block diagram of the proposed MP-DCL with improved current-limiting capability.

where ω_c denotes the bandwidth of the low-pass filter. The droop control equation is written as

$$\begin{cases}\omega_{ref}-\omega_0=m\left(P_{set}-P\right)+k_{oq}v_{Cq}\\ V_{ref}-V_0=n\left(Q_{set}-Q\right)\end{cases}\tag{9}$$

where P_{set} and Q_{set} denote setting active and reactive power values, respectively. Additionally, ω_0 denotes the nominal angular frequency, V_0 denotes the nominal voltage magnitude, m and n denote active power-frequency droop gain and reactive power-voltage droop gain, respectively, ω_{ref} denotes the angular frequency reference, θ_{ref} denotes the reference angle, and V_{ref} denotes the voltage magnitude reference. The voltage references can be deduced as $v_{C\alpha ref}=V_{ref}\cos(\theta_{ref})$ and $v_{C\beta ref}=V_{ref}\sin(\theta_{ref})$. $k_{oq}v_{Cq}$ denotes the term of the transient stability enhancement control (TSEC) to improve the system's transient stability during faults. v_{Cq} is the q-axis capacitor voltage, and k_{oq} is a gain. The TSEC has been well proposed and analyzed in [25], and it has also been adopted and verified in [3], [4]. Therefore, the TSEC will not be explained again in this article.

B. Outer-Voltage MPC Loop for Unconstrained Current Reference Generation

The objective of the outer-voltage MPC loop is to implement the voltage reference tracking and generate the current reference for the inner-current MPC loop in a deadbeat manner, which is shown as the outer-voltage MPC loop in Fig. 3. Employing the forward Euler discretization method to the second raw of (1), the discrete model is obtained as

$$\mathbf{i}\left(k\right)=C_f/T_{s1}\left(\mathbf{v}_C\left(k+1\right)-\mathbf{v}_C\left(k\right)\right)+\mathbf{i}_o\left(k\right)\tag{10}$$

and considering a two-step forward prediction for the delay compensation [16], (10) can be further deduced as

$$\mathbf{i}\left(k+1\right)=C_f/T_{s1}\left(\mathbf{v}_C\left(k+2\right)-\mathbf{v}_C\left(k+1\right)\right)+\mathbf{i}_o\left(k+1\right)\tag{11}$$

where $\mathbf{v}_C(k+1)$ can be calculated from (2), and $\mathbf{i}_o(k+1)$ is substituted with $\mathbf{i}_o(k)$ due to the slow dynamics of the output current. To realize the voltage reference tracking, $\mathbf{v}_C(k+2)$ can be replaced by $\mathbf{v}_{Cref}=v_{C\alpha ref}+jv_{C\beta ref}$ from the outer-droop control loop. Consequently, $\mathbf{i}(k+1)$ is transferred to the inner-current MPC loop as the unconstrained inner-current reference, which can be constrained by the following direct current-limiting strategies, and the final equation to calculate the current reference can be written as

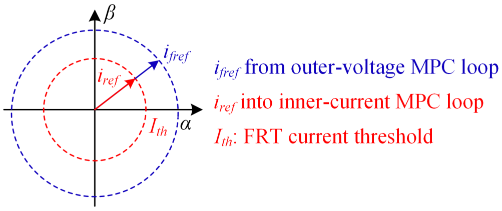


Fig. 4. Vector illustration of the effect of the current-limiting factor on the current reference from the outer-voltage MPC loop during faults.

$$\mathbf{i}_{ref}=C_f/T_{s1}\left(\mathbf{v}_{Cref}-\mathbf{v}_C\left(k+1\right)\right)+\mathbf{i}_o\left(k+1\right).\tag{12}$$

C. Inner-Current MPC Loop With Improved Current-Limiting Capability

As shown by the current-limiting loop in Fig. 3, the current reference from the outer-voltage MPC loop goes through an instantaneous limiter and current-limiting factor (CLF) before it is transferred to the inner-current MPC loop. The instantaneous current limiter can directly limit the current reference between $-I_{th1}$ and I_{th1} against transient overcurrent before activation of the CLF; thus, I_{th1} is set a little higher than the current threshold I_{th} of the CLF. The current reference i_{fref} from the outer-voltage MPC loop may exceed the FRT current threshold I_{th} during faults, as shown in Fig. 4. The CLF is, thus, adopted to proportionally scale down the magnitude of the current reference i_{fref} to the current reference i_{ref} [3], [7]. As shown in Fig. 4, the constrained current reference i_{ref} is the largest current reference, which can be generated by the outer-voltage MPC loop and simultaneously satisfy the current FRT requirement. In this case, the capacitor voltage during faults can track the voltage reference to the maximum extent. The diagram of CLF is specifically illustrated in the current-limiting loop of Fig. 3, where the current reference $i_{\alpha\beta ref}$ is transferred into reference i_{abcref}. The second-order generalized integrator (SOGI) is adopted to delay a signal by one-quarter period; thus, magnitudes I_{abc} of i_{abcref} can be calculated, as shown by the current-limiting loop in Fig. 3, where the transfer functions of H_α and H_β are shown as

$$H_\alpha=\frac{k\omega_0 s}{s^2+k\omega_0 s+\omega_0^2},H_\beta=\frac{k\omega_0^2}{s^2+k\omega_0 s+\omega_0^2}\tag{13}$$

where k is the SOGI proportional gain. Since the maximum magnitude I_M of i_{abcref} has been obtained, the CLF gain K_I can be deduced from

$$K_I = \begin{cases} 1, & I_M \le I_{th} \\ I_{th}/I_M, & I_M > I_{th} \end{cases} \tag{14}$$

where I_{th} is the current-limiting threshold, which is set as 1.5 p.u. of the base current in this article [3]. Moreover, K_I is a proportional gain that ensures the sinusoidal property of the current reference, and the constrained current reference $\mathbf{i}_{ref1}$ can be tracked by the inner-current MPC loop; hence, the power quality during faults with the proposed scheme can be ensured.

To compensate for the inherent computational delay, a two-step forward prediction method is also adopted [16]. To implement current reference tracking in the inner-current MPC loop, the cost function that only considers the current reference tracking is written as

$$g_i = \left(i_{\alpha ref1} - i_\alpha\left(k+2\right)\right)^2 + \left(i_{\beta ref1} - i_\beta\left(k+2\right)\right)^2 \tag{15}$$

where the predicted inductor current and capacitor voltage at the $k+2$ instant can be deduced from

$$\begin{aligned} \mathbf{i}\left(k+2\right) &= a_{11}\mathbf{i}\left(k+1\right) + a_{12}\mathbf{v}_C\left(k+1\right) \\ &\quad + b_1\mathbf{u}\left(k+1\right) + b_{g1}\mathbf{i}_o\left(k+1\right) \\ \mathbf{v}_C\left(k+2\right) &= a_{21}\mathbf{i}\left(k+1\right) + a_{22}\mathbf{v}_C\left(k+1\right) \\ &\quad + b_2\mathbf{u}\left(k+1\right) + b_{g2}\mathbf{i}_o\left(k+1\right). \end{aligned} \tag{16}$$

To find the (OVV $\mathbf{u}(k+1)$ that minimizes the cost function g_i, a simple approach is to solve the following equation:

$$\begin{cases} \partial g_i/\partial u_\alpha\left(k+1\right) = 0 \\ \partial g_i/\partial u_\beta\left(k+1\right) = 0 \end{cases}. \tag{17}$$

Substituting (15) and (16) into (17), the OVV $\mathbf{u}(k+1)$ can be deduced as

$$\begin{aligned} \mathbf{u}\left(k+1\right) &= \frac{1}{b_1}\mathbf{i}_{ref} - \frac{a_{11}}{b_1}\mathbf{i}\left(k+1\right) \\ &\quad - \frac{a_{12}}{b_1}\mathbf{v}_C\left(k+1\right) - \frac{b_{g1}}{b_1}\mathbf{i}_o\left(k+1\right) \end{aligned} \tag{18}$$

where $\mathbf{i}_o(k+1)$ is substituted with $\mathbf{i}_o(k)$, and $\mathbf{u}(k)$ is obtained from the last period $\mathbf{u}(k+1)$. Furthermore, the second-order partial derivative of the cost function g_i is calculated as

$$\frac{\partial^2 g_i}{\partial u_\alpha(k+1)^2} = \frac{\partial^2 g_i}{\partial u_\beta(k+1)^2} = 2b_1^2 > 0 \tag{19}$$

where $2b_1^2$ in (19) is always positive; thus, the obtained OVV in (18) can minimize the cost function g_i. Consequently, the OVV $\mathbf{u}(k+1)$ is modulated by a SPWM block to generate PWM pulses for GFM inverters, and a constant switching frequency can be maintained. In addition, thanks to the dual-loop structure, the nontrivial weighting factor design can be avoided for the proposed scheme. Additionally, no parameter needs to be tuned in the proposed scheme, which is simpler than the cascaded linear controllers, where both voltage and current PR/PI controller parameters should be tuned. Moreover, the fast dynamic response is another merit of the proposed approach, especially for the outer-voltage MPC loop, which will be explained in detail in Section III-E.

TABLE II
SYSTEM AND CONTROLLER PARAMETERS OF THE PROPOSED SCHEME

Symbol	Description	Value
S_n	Rated power	500 VA
V_{dc}	Dc voltage	200 V
V_g	Grid voltage (LL, rms)	104 V
L_f	Filter inductance	3 mH
C_f	Filter capacitance	30 μF
X_T	Inductance of transformer T_0	0.042 pu
L_g	Equivalent grid inductance	5 mH
R_g	Equivalent grid resistance	1 Ω
Z_f	Fault impedance	3.9 Ω
m	P-f droop gain	0.01 p.u.
n	Q-V droop gain	0.1 p.u.
P_{set}	Setting active power value	1 p.u.
Q_{set}	Setting reactive power value	0 p.u.
ω_0	Nominal angular frequency	314 rad/s
V_0	Nominal voltage magnitude	84.85 V
k_{oq}	Proportional gain of TSEC	0.4
ω_c	Cut off angular frequency	2π20 rad/s
I_{th}	Current-limiting threshold	1.5 p.u.
I_{th1}	Instantaneous current-limiting threshold	1.6 p.u.
T_{s1}	Sampling period of proposed MPC	100 μs

D. Stability and Robustness Analysis Against Mismatched Parameters

Accurate system parameters are crucial for MPC algorithms. To check the system stability and robustness against mismatched parameters with the proposed strategy, the closed-loop system modeling should be first established. Substituting (18) into (2), the closed-loop system modeling of the inner-current MPC loop is deduced as

$$\mathbf{i}\left(k+1\right) = \phi_1\mathbf{i}\left(k\right) + \phi_2\mathbf{i}_{ref} + \mathbf{D}_i \tag{20}$$

where $\phi_1 = a_{11}/(a_{11}+1)$, $\phi_2 = 1/(a_{11}+1)$, and $\mathbf{D}_i = a_{12}/(a_{11}+1)(\mathbf{v}_C(k) - \mathbf{v}_C(k+1))$. Substituting (12) and (18) into (2), the closed-loop system modeling of the outer-voltage MPC loop is obtained as

$$\mathbf{v}_C\left(k+1\right) = \varphi_1\mathbf{v}_C\left(k\right) + \varphi_2\mathbf{v}_{Cref} + \mathbf{D}_v \tag{21}$$

where $\varphi_1 = a_{22}b_1T_{s1}/(a_{12}b_2T_{s1} + b_1T_{s1} + b_2C_f)$, $\varphi_2 = b_2C_f/(a_{12}b_2T_{s1} + b_1T_{s1} + b_2C_f)$, and $\mathbf{D}_v = (b_2 + b_{g2}b_1 - b_{g1}b_2)T_{s1}/(a_{12}b_2T_{s1} + b_1T_{s1} + b_2C_f) + [a_{21}b_1\mathbf{i}(k) - a_{11}b_2\mathbf{i}(k+1)]T_{s1}/(a_{12}b_2T_{s1} + b_1T_{s1} + b_2C_f)$.

If the inner-current MPC loop and outer-voltage MPC loop are both stable, the eigenvalues of (20) and (21) should lie within the unit circle on the z-plane, which is equivalent to

$$\left|\lambda_i = \phi_1\right| < 1, \left|\lambda_v = \varphi_1\right| < 1. \tag{22}$$

The system and controller parameters of the proposed scheme are listed in Table II, which illustrates that the eigenvalues λ_i of the inner-current MPC loop and eigenvalues λ_v of the outer-voltage MPC loop can be calculated from (20) and (21), respectively. Fig. 5 shows the root loci of the inner-current MPC loop and outer-voltage MPC loop with ±30% mismatched inductance, where λ_i and λ_v are far from the boundary of the

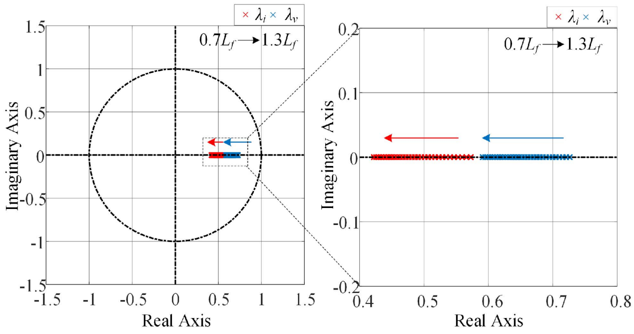


Fig. 5. Root loci of the proposed inner-current MPC loop and outer-voltage MPC loop with ±30% mismatched inductance.

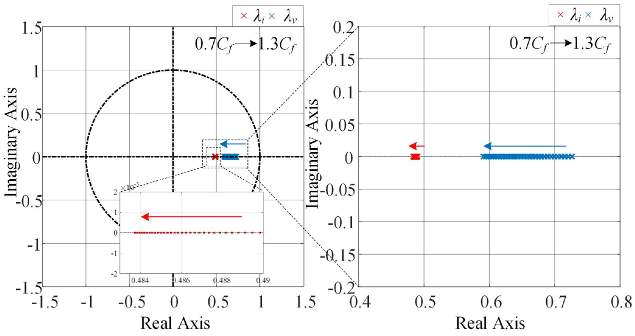


Fig. 6. Root loci of the proposed inner-current MPC loop and outer-voltage MPC loop with ±30% mismatched capacitance.

unit circle; hence, the inner-current MPC loop and outer-voltage MPC loop have good stability and robustness ability against mismatched inductances. When the inductance increases from $0.7L_f$ to $1.3L_f$, poles λ_i and λ_v will move toward the origin; thus, both the stability and dynamic response of the inner-current MPC loop and outer-voltage MPC loop are enhanced. Additionally, compared with poles λ_v, the poles λ_i are closer to the origin, meaning higher stability and dynamics for the inner-current MPC loop.

As shown in Fig. 6, increasing the capacitance, or reducing the capacitance has slight effects on the stability of the inner-current MPC loop, where all poles λ_i are closed to the origin. Therefore, the inner-current MPC loop also has a high robustness ability against mismatched capacitances. When the capacitance increases from $0.7C_f$ to $1.3C_f$, the poles λ_v move toward the origin; thus, both the stability and dynamic response are improved. Additionally, even when the capacitance reduces to $0.7C_f$, the poles λ_v are still far from the boundary of the unit circle. Therefore, the outer-voltage MPC loop has good stability and robustness ability against mismatched capacitances.

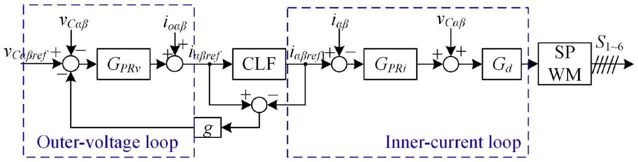


Fig. 7. Outer-voltage loop and inner-current loop diagrams of the state-of-the-art cascaded PR-based current-limiting scheme [3], [7].

E. Contribution Compared to the State-of-the-Art Solutions

The proposed MP-DCL has improved the control bandwidth, especially for the outer-voltage loop. To verify this contribution, the state-of-the-art cascaded PR-based current-limiting scheme is adopted as a comparison case in this section. The same outer-droop control loop in Section III-A is also employed and omitted here. The outer-voltage loop and inner-current loop diagrams with PR controllers are shown in Fig. 7 [3]. The CLF is also employed to ride through faults [3], [7], which has been introduced in Section III-C. For the PR controller parameters tuning, they can be referred to [13], which are both omitted due to page limitation. Consequently, the closed-loop transfer functions from the current reference to the current and from the voltage reference to the voltage with the PR controller can be deduced from Fig. 7 and written as

$$\begin{cases} G_{cli\_\mathrm{PR}} = \frac{i_{\alpha\beta}}{i_{\alpha\beta ref}} = \frac{G_d G_{\mathrm{PR}i}}{Z_{Lf} + G_d G_{\mathrm{PR}i}} \\ G_{clv\_\mathrm{PR}} = \frac{v_{C\alpha\beta}}{v_{C\alpha\beta ref}} = \frac{G_d G_{\mathrm{PR}i} G_{\mathrm{PR}v}}{1 + Z_{Lf} Y_{Cf} + G_d G_{\mathrm{PR}i} G_{\mathrm{PR}v} + Y_{Cf} G_d G_{\mathrm{PR}i}} \end{cases} \tag{23}$$

where filter inductor impedance is $Z_{Lf} = sL_f$, and filter capacitor admittance is $Y_{Cf} = sC_f$. $G_{\mathrm{PR}i}$ and $G_{\mathrm{PR}v}$ denote the inner-current controller and outer-voltage controller, respectively, while $G_d = e^{-1.5T s1}$ denotes the time delay [13].

The closed-loop transfer functions from the current reference to the current and from the voltage reference to the voltage with the proposed MP-DCL can be deduced from (20) and (21), written as

$$\begin{cases} G_{cli\_\mathrm{MPC}} = \frac{\mathbf{i}}{\mathbf{i}_{ref}} = \frac{1}{z(a_{11}+1) - a_{11}} \\ G_{clv\_\mathrm{MPC}} = \frac{\mathbf{v}_C}{\mathbf{v}_{Cref}} = \frac{b_2 C_f}{z(a_{12} b_2 T_{s1} + b_1 T_{s1} + b_2 C_f) - a_{22} b_1 T_{s1}}. \end{cases} \tag{24}$$

The closed-loop transfer functions G_{cli_PR} and G_{clv_PR} in the *s*-domain can be discretized into *z*-domain with the Tustin method, then bode diagrams of G_{cli_PR}, G_{clv_PR}, G_{cli_MPC}, and G_{clv_MPC} are depicted in Fig. 8 for comparison, where the bandwidths of the proposed inner-current MPC loop and the state-of-the-art inner-current PR are both close to 1200 Hz; thus, the dynamic response of the inner-current loop with the two schemes is similar. However, the bandwidth of the proposed outer-voltage MPC loop is around 700 Hz, which is significantly higher than the 170 Hz of the state-of-the-art outer-voltage PR. Therefore, the proposed MP-DCL has a higher dynamic response than the state-of-the-art cascaded PR controllers for the outer-voltage loop, which can enhance the voltage recovery dynamics after fault clearance.

Another contribution of the proposed strategy is that the power quality during faults can be ensured, which cannot be achieved by the FCS-MPC-based current-limiting strategy and has been introduced in Section II-B. To verify the above two contributions of the proposed scheme, the voltage and current reference tracking around the fault occurrence and clearance with the state-of-the-art cascaded PR-based and FCS-MPC-based

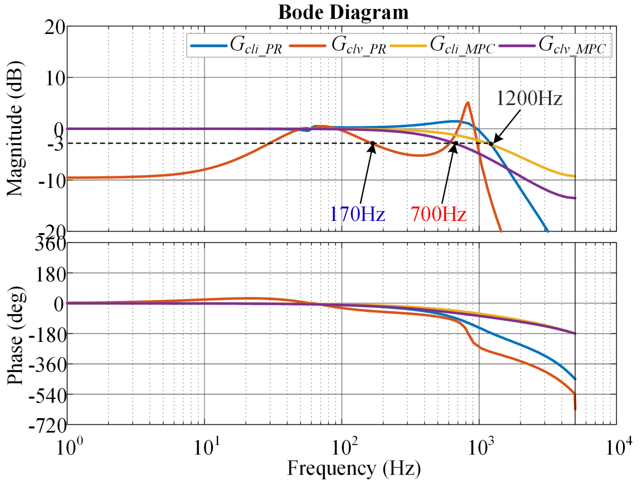


Fig. 8. Bode diagrams of closed-loop transfer functions of G_{cli_PR}, G_{clv_PR}, G_{cli_MPC}, and G_{clv_MPC}.

TABLE III
CONTROLLER PARAMETERS OF STATE-OF-THE-ART PR AND FCS-MPC

Symbol	Description	Value
ω_i	Bandwidth of the resonant part	πrad/s
K_{pv}/K_{rv}	PR gain of voltage controller	0.1/80
K_{pi}/K_{ri}	PR gain of current controller	10/500
g	Anti-windup gain	1.5
T_{s1}	Sampling period of dual PR	100 μs
γ	Weighting factor of FCS-MPC	0.7
T_{s2}	Sampling period of FCS-MPC	40 μs

current-limiting schemes, and the proposed MP-DCL are first developed in MATLAB/Simulink. The controller parameters of the cascaded PR and FCS-MPC are listed in Table III. Taking a line-to-line fault as an example, which is activated at $t = 3$ s and deactivated 2 s later. More detailed verification is developed by experiments in the following section.

Fig. 9 shows the voltage and current reference tracking around the fault occurrence with the state-of-the-art cascaded PR-based current-limiting scheme, the state-of-the-art FCS-MPC-based current-limiting scheme, and the proposed MP-DCL with improved current-limiting capability. As shown in Fig. 9(a) and (c), the current reference tracking takes around 2 ms with both the state-of-the-art cascaded PR-based current-limiting scheme and the proposed MP-DCL since the bandwidth of the inner-current loop for the two methods is similar, as shown in Fig. 8. In addition, the voltage reference tracking of both methods cannot be simultaneously implemented due to the adoption of the direct CLF). As shown in Fig. 9(b), during faults, the voltage and current reference tracking is damaged with the state-of-the-art FCS-MPC-based current-limiting scheme, and voltages and currents get distorted in each period. This phenomenon is caused by the aggressive penalization for the current magnitude violation in the cost function, which is at the expense of the voltage and current reference tracking and has been analyzed in Section II-B.

Fig. 10 shows the voltage and current reference tracking around the fault clearance with the three schemes. As shown in Fig. 10(b), the state-of-the-art FCS-MPC-based current-limiting strategy can accomplish the fast voltage and current reference tracking around the fault clearance because both voltage and current regulation objectives are included in one cost function with a high bandwidth. Comparing Fig. 10(c) to (a), the voltage reference tracking around the fault clearance with the proposed scheme only takes around 3 ms, significantly lower than the 30 ms with the state-of-the-art cascaded PR-based current-limiting method, which verifies the bandwidth improvement for the outer-voltage loop with the proposed strategy. Additionally, the current reference tracking around the fault clearance takes 1ms, which is lower than the 3 ms with the PR-based method since the slow voltage recovery with the PR-based method may affect its current reference tracking.

In summary, compared to the state-of-the-art cascaded PR-based current-limiting scheme, the voltage recovery dynamics have been significantly enhanced with the proposed MP-DCL with current-limiting capability thanks to the improved bandwidth of the outer-voltage loop. Additionally, compared to the state-of-the-art FCS-MPC-based current-limiting scheme, which sacrifices both voltage and current reference tracking to prevent overcurrent, the power quality during faults can be ensured with the proposed scheme since the current reference tracking can be accomplished.

F. Simplicity Analysis Compared to State-of-the-Art Solutions

In terms of the parameter design, the proposed MPDCL certainly expresses simpler design benefits than the PR-based strategy and FCS-MPC-based strategy. For the cascaded PR-based current-limiting strategy, at least two groups of PR parameters (e.g., two proportional gains and two resonant gains) need to be carefully designed [3], [7]. Additionally, these parameters are designed based on the constant operating point. If the operating point varies, new PR parameters should be redesigned to achieve optimal performance. Moreover, the antiwindup strategy must be designed for the PR-based strategy [12].

For the FCS-MPC-based current-limiting strategy, the weighting factor design is significantly nontrivial [15]. The most commonly utilized method is the trial-and-error approach, which relies on numerous time-consuming simulations [26]. In addition, some artificial intelligence-based methods are also adopted to design the weighting factor, e.g., the neural network [27]. However, these methods are all complex and take a long time. Moreover, whether the weighting factor designed during normal conditions is still effective during grid faults has not been investigated. Therefore, compared with the PR-based strategy and FCS-MPC-based strategy, the proposed MPDCL reveals a simpler parameter design and can be implemented with lower efforts.

IV. EXPERIMENTAL VERIFICATION

To verify the advantages of the proposed MP-DCL with improved current-limiting capability over the state-of-the-art cascaded PR-based current-limiting scheme [3] and the state-of-the-art FCS-MPC-based current-limiting scheme [15], [19], an experimental platform with the same topology as Fig. 1 is established and depicted in Fig. 11. All system and controller

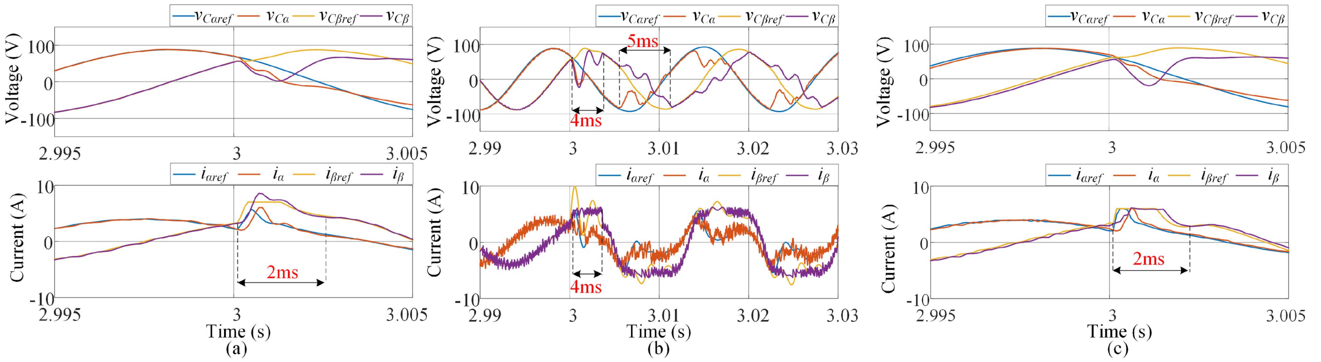


Fig. 9. Voltage and current reference tracking around the fault occurrence. (a) State-of-the-art cascaded PR-based current-limiting scheme. (b) State-of-the-art FCS-MPC-based current-limiting scheme. (c) Proposed MP-DCL with improved current-limiting capability.

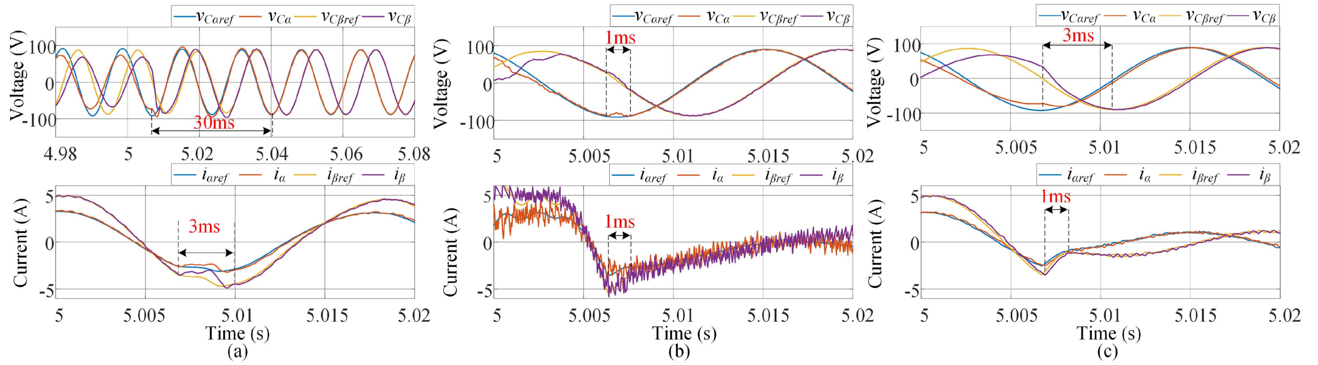


Fig. 10. Voltage and current reference tracking around the fault clearance. (a) State-of-the-art cascaded PR-based current-limiting scheme. (b) State-of-the-art FCS-MPC-based current-limiting scheme. (c) Proposed MP-DCL with improved current-limiting capability.

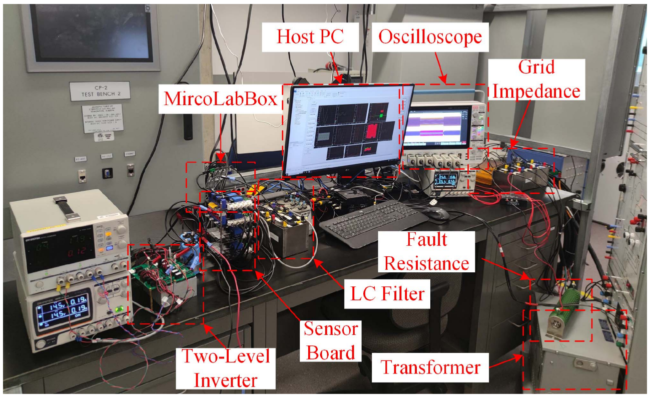


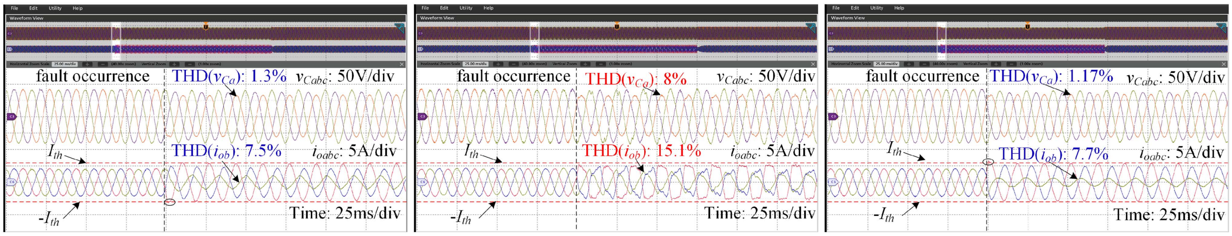
Fig. 11. Experimental setup of the grid-connected GFM inverter.

parameters listed in Tables II and III have been employed in experiments. The ac grid is simulated by a MX30 power supply, and the dc source is provided by a TC.GSS bidirectional power supply. Moreover, the dSPACE MicroLabBox DS1202 is adopted as the digital controller. The line-to-line voltages v_{Cab} and v_{Cbc} are collected by the voltage sensor LV20-P. The inverter-side currents i_a and i_b and the inverter output currents i_{oa} and i_{ob} are all collected by the current sensor LA55-P. The sampling rates of the PR-based strategy and the proposed MPDCL are both 10 kHz, and the sampling rate of the FCS-MPC-based strategy is 25 kHz. The sampling rate of the oscilloscope is 20 MHz. Experiments of single-line-to-ground (SLG) fault and line-to-line (LL) fault have been developed to verify the effectiveness of the proposed scheme.

A. FRT Performance Comparison for Voltage and Current

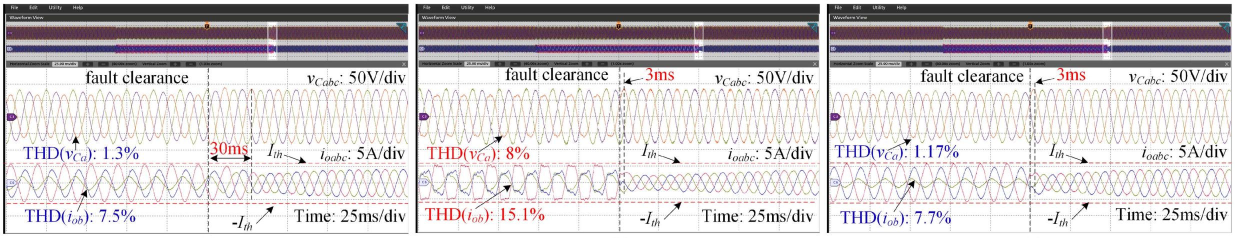
Figs. 12–15 show the experimental waveforms of the voltages and currents with the state-of-the-art cascaded PR-based current-limiting scheme, the state-of-the-art FCS-MPC-based current-limiting scheme, and the proposed MP-DCL with improved current-limiting capability around an SLG fault and an LL fault occurrence and clearance, respectively. These three strategies can all mitigate overcurrent during grid faults, where all maximum currents are lower than the current threshold I_{th}.

However, the three strategies' FRT performance regarding voltage recovery time (VRT) after fault clearance and power quality during grid faults significantly differ. As shown in Figs. 13(a) and 15(a), the VRT after fault clearance with the PR-based current-limiting strategy are both around 30 ms, which is significantly higher than 3 ms with the FCS-MPC-based current-limiting strategy in Figs. 13(b) and 15(b) and the proposed strategy in Figs. 13(c) and 15(c). The low bandwidth



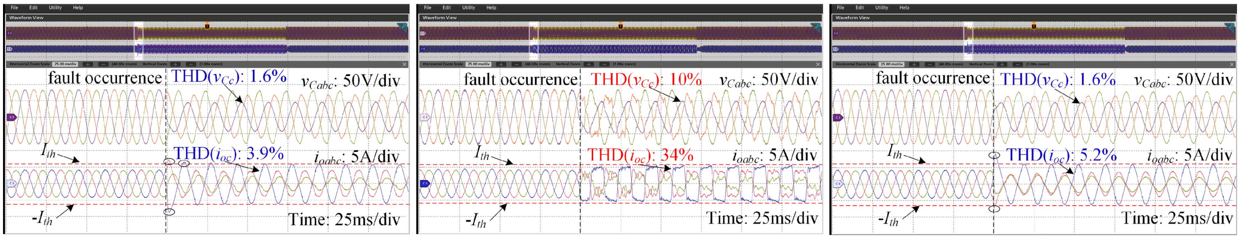
(a) (b) (c)

Fig. 12. Experimental waveforms of voltages and currents around an SLG fault occurrence. (a) State-of-the-art cascaded PR-based current-limiting strategy. (b) State-of-the-art FCS-MPC-based current-limiting strategy. (c) Proposed MP-DCL with improved current-limiting capability.



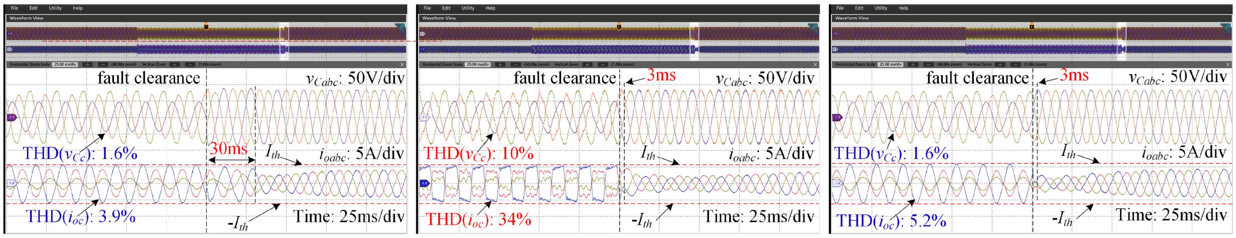
(a) (b) (c)

Fig. 13. Experimental waveforms of voltages and currents around an SLG fault clearance. (a) State-of-the-art cascaded PR-based current-limiting strategy. (b) State-of-the-art FCS-MPC-based current-limiting strategy. (c) Proposed MP-DCL with improved current-limiting capability.



(a) (b) (c)

Fig. 14. Experimental waveforms of voltages and currents around an LL fault occurrence. (a) State-of-the-art cascaded PR-based current-limiting strategy. (b) State-of-the-art FCS-MPC-based current-limiting strategy. (c) Proposed MP-DCL with improved current-limiting capability.



(a) (b) (c)

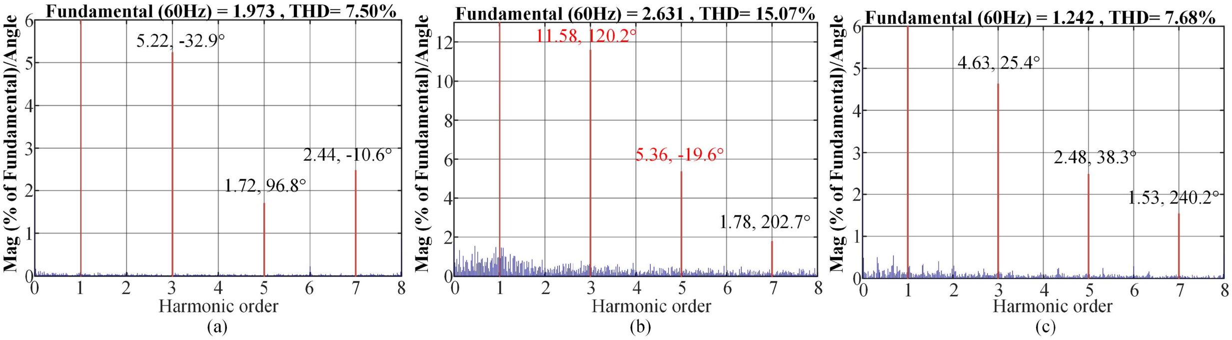
Fig. 15. Experimental waveforms of voltages and currents around an LL fault clearance. (a) State-of-the-art cascaded PR-based current-limiting strategy. (b) State-of-the-art FCS-MPC-based current-limiting strategy. (c) Proposed MP-DCL with improved current-limiting capability.

of the voltage control loop for the cascaded PR-based strategy causes such a long dynamic response, which has been analyzed in Section III-E. Additionally, although the bandwidth of the voltage control loop with the FCS-MPC is higher than the one with the proposed strategy, as shown in Figs. 13(b) and 15(b), the severe power quality of voltages and currents with the FCS-MPC impedes the fault recovery process. On the contrary, as shown in Figs. 13(c) and 15(c), both voltages and currents recover from a good power quality with the proposed strategy; hence, the VRT after fault clearance with the proposed strategy is similar to the FCS-MPC. Consequently, for convenient comparison, the VRT with the three strategies is summarized in Table IV, which can verify that the proposed strategy can significantly improve the fault recovery dynamic response in reducing the VRT.

Severe power quality will be caused by the FCS-MPC. As shown in Figs. 12(b)–15(b), obvious voltage and current distortions with the FCS-MPC can be observed during grid faults. Due to the adoption of a nonlinear term in the cost function

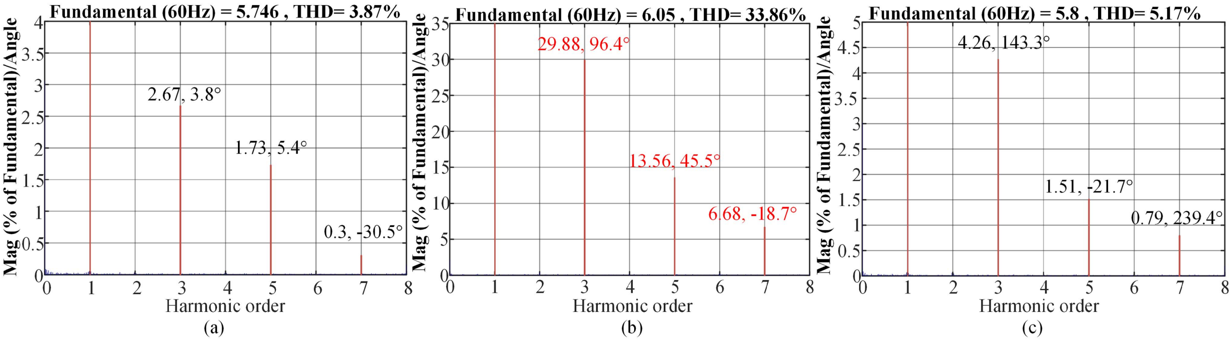
TABLE IV
VOLTAGE RECOVERY TIME AND POWER QUALITY COMPARISON FOR THREE SCHEMES

Fault	Schemes	VRT	THD(v)	THD(i)	Mag (% of fundamental) third harmonic order	Mag (% of fundamental) fifth harmonic order	Mag (% of fundamental) seventh harmonic order
SLG	PR	**30 ms**	1.3%	7.5%	5.22	1.72	2.44
SLG	FCS-MPC	3 ms	**8%**	**15.1%**	**11.58**	**5.36**	**1.78**
SLG	MP-DCL	3 ms	1.17%	7.7%	4.63	2.48	1.53
LL	PR	**30 ms**	1.6%	3.9%	2.67	1.73	0.3
LL	FCS-MPC	3 ms	**10%**	**34%**	**29.88**	**13.56**	**6.68**
LL	MP-DCL	3 ms	1.6%	5.2%	4.26	1.51	0.79



(a) (b) (c)

Fig. 16. Experimental FFT spectrum of currents during an SLG fault. (a) State-of-the-art cascaded PR-based current-limiting strategy. (b) State-of-the-art FCS-MPC-based current-limiting strategy. (c) Proposed MP-DCL with improved current-limiting capability.



(a) (b) (c)

Fig. 17. Experimental FFT spectrum of currents during an LL fault. (a) State-of-the-art cascaded PR-based current-limiting strategy. (b) State-of-the-art FCS-MPC-based current-limiting strategy. (c) Proposed MP-DCL with improved current-limiting capability.

to prevent overcurrent during faults, the voltage and current reference tracking cannot be simultaneously accomplished for the FCS-MPC, which causes such severe power quality issues during faults. On the contrary, as shown in Figs. 12(a)–15(a) and 12(c)–15(c), sinusoidal waveforms of voltages and currents during grid faults with the PR-based strategy and the proposed strategy can be observed since these two strategies both realize the current reference tracking during grid faults.

To further compare the power quality among the three strategies, the experimental FFT spectrum of currents i_{ob} and i_{oc} during SLG faults and LL faults are shown in Figs. 16 and 17, respectively. Moreover, the total harmonic distortions (THDs) of voltages and currents and the magnitude percentage of the fundamental current in third harmonic order, fifth harmonic order, and seventh harmonic order are summarized in Table IV. It is clear that the THDs of voltages and currents with the FCS-MPC are the highest among the three strategies during SLG and LL faults. Moreover, high THDs of currents with the FCS-MPC are caused by significant odd harmonics, as shown in Figs. 16(b) and 17(b). On the contrary, the THDs of voltages and currents for the PR-based strategy and the proposed strategy are similar during SLG and LL faults. As listed in Table IV, the highest voltage THD is 1.6% and the highest current THD is 7.7% for the PR-based strategy and the proposed strategy, which are both significantly lower than the highest voltage THD of 10% and the highest current THD of 34% with the FCS-MPC. Therefore, the experimental results of THDs and FFT spectrum can verify that the PR-based strategy and the proposed strategy can both ensure superior power quality during grid faults.

In summary, the PR-based strategy causes the longest VRT and the FCS-MPC causes the worst power quality during grid faults. On the contrary, the proposed strategy not only presents

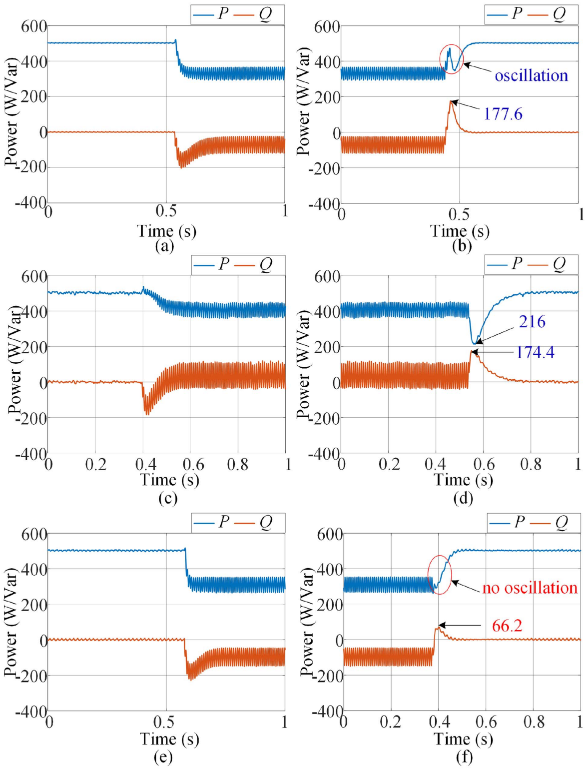


Fig. 18. Experimental active and reactive powers under an SLG fault. (a) With the state-of-the-art cascaded PR-based current-limiting scheme around the fault occurrence. (b) With the state-of-the-art cascaded PR-based current-limiting scheme around the fault clearance. (c) With the state-of-the-art FCS-MPC-based current-limiting scheme around the fault occurrence. (d) With the state-of-the-art FCS-MPC-based current-limiting scheme around the fault clearance. (e) With the proposed MP-DCL with improved current-limiting capability around the fault occurrence. (f) With the proposed MP-DCL with improved current-limiting capability around the fault clearance.

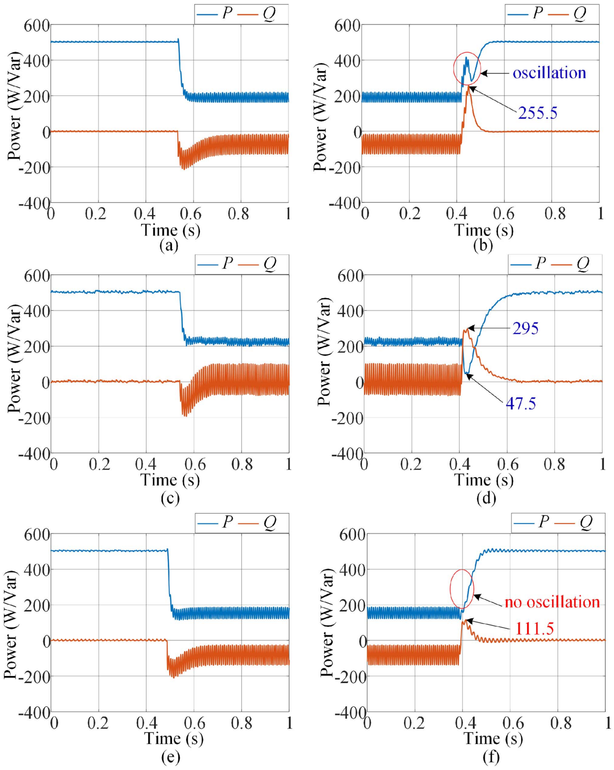


Fig. 19. Experimental active and reactive powers under an LL fault. (a) With the state-of-the-art cascaded PR-based current-limiting scheme around the fault occurrence. (b) With the state-of-the-art cascaded PR-based current-limiting scheme around the fault clearance. (c) With the state-of-the-art FCS-MPC-based current-limiting scheme around the fault occurrence. (d) With the state-of-the-art FCS-MPC-based current-limiting scheme around the fault clearance. (e) With the proposed MP-DCL with improved current-limiting capability around the fault occurrence. (f) With the proposed MP-DCL with improved current-limiting capability around the fault clearance.

the lowest VRT as the FCS-MPC but also ensures superior power quality as the PR-based strategy. Therefore, regarding both the VRT after fault clearance and power quality during grid faults, the proposed strategy performs the best among the three strategies.

B. FRT Performance Comparison for Power

Figs. 18 and 19 show the experimental active and reactive powers with the state-of-the-art cascaded PR-based current-limiting scheme, the state-of-the-art FCS-MPC-based current-limiting scheme, and the proposed MP-DCL with improved current-limiting capability under an SLG and LL fault, respectively. For a convenient comparison, the time duration is written as 0 s to 1 s for all figures. As shown in Fig. 18(a), (c), and (e) and Fig. 19(a), (c), and (e), the tendency of powers around the fault occurrence is similar for all three strategies; therefore, will not be further discussed.

As shown in Figs. 18(b) and 19(b), there is an active power oscillation with the state-of-the-art cascaded PR-based current-limiting scheme around the fault clearance, and the reactive power overshoot is 177.6 Var under the SLG fault and 255.5 Var under the LL fault, respectively. The active power oscillation and high reactive power overshoot may be induced by the slow voltage recovery and high currents after the fault, which have been observed in Figs. 13(a) and 15(a). As shown in Fig. 18(d) and Fig. 18(d), there is no active power oscillation with the state-of-the-art FCS-MPC-based current-limiting strategy around the fault clearance. However, there is an additional active power overshoot, which is 216 W under the SLG fault and 47.5 W under the LL fault. Additionally, the reactive power overshoot around the SLG fault clearance is 174.4 Var with the FCS-MPC, similar to the 177.6 Var with the cascaded PR, and the reactive power overshoot around the LL fault with the FCS-MPC is 295 Var, which is higher than the 255.5 Var with the cascaded PR. This may be caused by the distortion of voltages and currents with the FCS-MPC during the fault, the inconstant switching frequency, and large currents around the fault clearance, as shown in Figs. 13(b) and 15(b).

On the contrary, as shown in Figs. 18(f) and 19(f), after the fault clearance, the active power with the proposed MP-DCL rises smoothly to the normal value without any oscillation. Moreover, the reactive power overshoots with the proposed MP-DCL around the SLG and LL faults clearance are 66.2 Var and 111.5 Var, which are significantly lower than the other state-of-the-art methods. This advantage is attributed to the fast voltage recovery, good power quality during faults, and small currents

TABLE V
OVERSHOOT AND OSCILLATION COMPARISON AMONG THREE SCHEMES

Fault	Schemes	Overshoot(P)	Overshoot(Q)	Oscillation (P)
SLG	PR	×	177.6 Var	√
SLG	FCS-MPC	216 W	174.4 Var	×
SLG	MP-DCL	×	**66.2 Var**	×
LL	PR	×	255.5 Var	√
LL	FCS-MPC	47.5 W	295 Var	×
LL	MP-DCL	×	**111.5 Var**	×

TABLE VI
PERFORMANCE UNDER MISMATCHED PARAMETERS

Parameter	+30%L_f	−30%L_f	+30%C_f	−30%C_f
Overshoot(P)	×	×	×	56 W
Overshoot(Q)	126 Var	92 Var	120 Var	146.4 Var
Oscillation (P)	×	×	×	×
VRT	3 ms	3 ms	3 ms	3 ms
THD(v)	1.55%	1.68%	1.52%	1.66%
THD(i)	4.5%	6.43%	4.87%	5.1%

after the fault clearance with the proposed strategy, as shown in Figs. 13(c) and 15(c). The active power overshoot, reactive power overshoot, and active power oscillation around the SLG and LL fault clearance with the three schemes are summarized in Table V, where "×" denotes no existence, and "√" denotes existence. As shown in Table V, the proposed MP-DCL is the only strategy that does not cause active power overshoots and oscillations around the fault clearance. Moreover, the reactive power shoot around the fault clearance is the lowest with the proposed MP-DCL compared to the other two schemes. Therefore, the fault recovery for powers with the proposed MP-DCL performs significantly better than the state-of-the-art cascaded PR-based and FCS-MPC-based current-limiting schemes.

C. Robustness Test of the Proposed Scheme

To verify the robustness of the proposed MP-DCL with improved current-limiting capability against mismatched parameters, the voltages, currents, active powers, and reactive powers with the proposed scheme around the LL fault occurrence and clearance under +30% mismatched inductance, −30% mismatched inductance, +30% mismatched capacitance, and −30% mismatched capacitance are shown in Figs. 20–23. The performance under the SLG fault is similar to the LL fault; thus, the results under a severe fault (LL fault) are provided here. As shown in Figs. 20(a)–23(a), the overcurrent can be quickly mitigated by the proposed scheme with only two small overcurrent peaks. In addition, the steady-state THDs of voltages and currents under different mismatched parameters are all summarized in Table VI, which are all small and close to the values under normal parameters listed in Table V; thus, the proposed strategy has a good robustness in mitigating overcurrent and ensuring the power quality against mismatched parameters. As shown in Figs. 20(b)–23(b), the voltage recovery time around the fault clearance with the proposed strategy takes around 3 ms under different mismatched parameters; hence, the proposed strategy has a good robustness for the fast voltage recovery around the fault clearance against mismatched parameters.

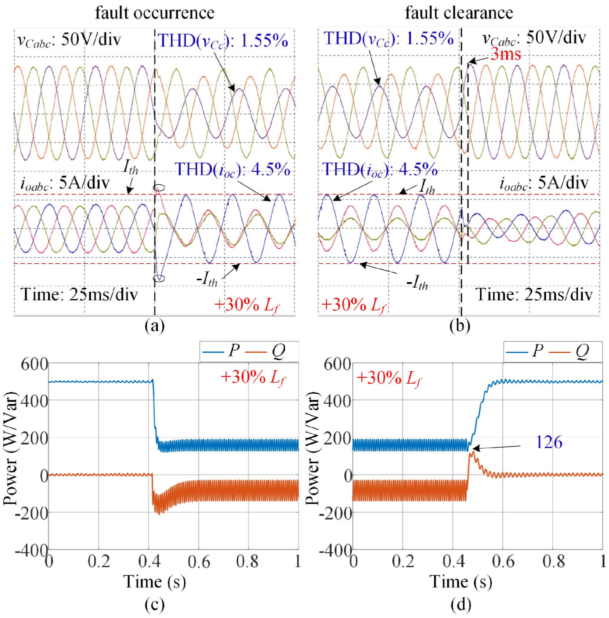


Fig. 20. Experimental results of voltages, currents, powers for +30% mismatched inductance with the proposed scheme under an LL fault. (a) Voltages and currents around the fault occurrence. (b) Voltages and currents around the fault clearance. (c) Powers around the fault clearance. (d) Powers around the fault clearance.

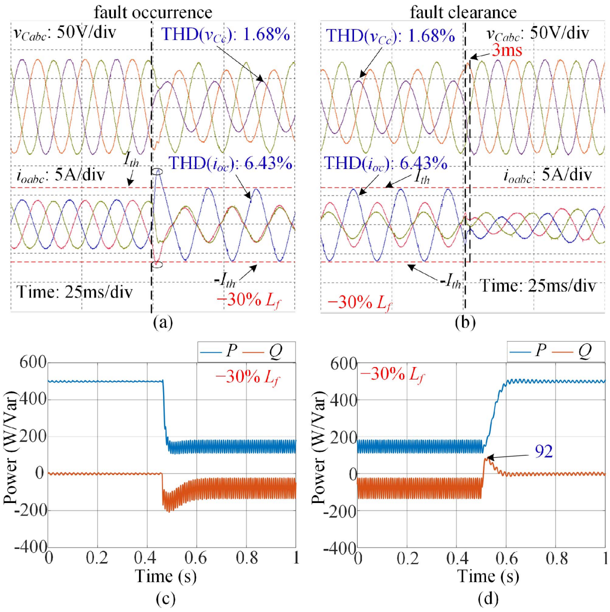
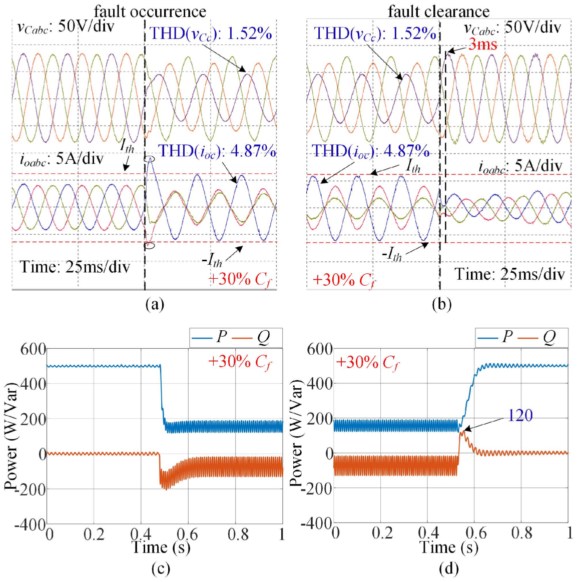


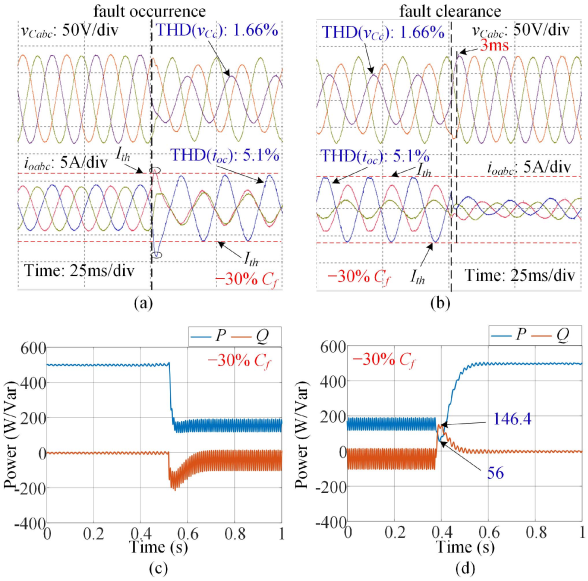
Fig. 21. Experimental results of voltages, currents, powers for −30% mismatched inductance with the proposed scheme under an LL fault. (a) Voltages and currents around the fault occurrence. (b) Voltages and currents around the fault clearance. (c) Powers around the fault clearance. (d) Powers around the fault clearance.

The active power oscillation around the fault clearance with the proposed scheme can be avoided under various mismatched parameters, which can be observed in Figs. 20(d)–23(d). The active power overshoot around the fault clearance with the proposed scheme can be eliminated under +30% mismatched



(a) (b) (c) (d)

Fig. 22. Experimental results of voltages, currents, powers for +30% mismatched capacitance with the proposed scheme under an LL fault. (a) Voltages and currents around the fault occurrence. (b) Voltages and currents around the fault clearance. (c) Powers around the fault clearance. (d) Powers around the fault clearance.



(a) (b) (c) (d)

Fig. 23. Experimental results of voltages, currents, powers for −30% mismatched capacitance with the proposed scheme under an LL fault. (a) Voltages and currents around the fault occurrence. (b) Voltages and currents around the fault clearance. (c) Powers around the fault clearance. (d) Powers around the fault clearance.

inductance, −30% mismatched inductance, and +30% mismatched capacitance. An active power overshoot of 56 W with the proposed scheme under −30% mismatched capacitance exists, but fortunately, this small value will not affect system safety. The reactive power overshoots around the fault clearance with the proposed scheme under different mismatched parameters are shown in Figs. 20(d)–23(d) and summarized in Table VI. These values are all close to 111.5 Var with accurate parameters and lower than the values with the state-of-the-art cascaded PR-based and FCS-MPC-based current-limiting strategies. Therefore, the proposed strategy has a good robustness for the power recovery around the fault clearance against mismatched parameters. It is noticed that the power recovery performance under −30% mismatched capacitance is slightly worse than the other three mismatched parameters, which is consistent with the robustness analysis in Fig. 6, where all poles under −30% mismatched capacitance are much closer to the boundary of the unit circle. Consequently, the GFM inverter performance that embraces the active power overshoot, active power oscillation, reactive power overshoot, voltage recovery time around the fault clearance, and steady-state voltage and current THDs during faults with the proposed MP-DCL with improved current-limiting capability under different mismatched parameters are all summarized in Table VI for a convenient comparison.

In summary, the performance of the proposed scheme is similar across different mismatched parameters and better than the state-of-the-art cascaded PR-based and FCS-MPC-based current-limiting strategies. Therefore, the proposed MP-DCL with improved current-limiting capability has good robustness against mismatched parameters in FRT performance for GFM inverters under grid faults.

D. Computational Burden Comparison Among the Three Strategies

The execution times of the PR, FCS-MPC, and the proposed strategy are measured by dSPACE Profiler 4.0. The execution time of the PR is 14.6 μs, which only occupies 14.6% of the sampling period for the PR controller. The execution times of the FCS-MPC and the proposed strategy are 18.92 μs and 19.68 μs, respectively, which are similar to each other. However, the sampling period of the FCS-MPC is 40 μs; thus, the execution time of the FCS-MPC occupies 47.3% of the sampling period. On the contrary, the sampling period of the proposed strategy is 100 μs; hence, the proposed strategy occupies 19.68% of the sampling period.

In summary, the computation burden of the PR is 14.6%, the lowest due to its linear control strategy. The computation burden of the proposed strategy is 19.68%, slightly higher than the PR, which is reasonable due to the matrix calculation of the proposed strategy. However, the computation burden of the proposed strategy is significantly lower than 47.3% of the FCS-MPC due to the shortest sampling period for the FCS-MPC.

E. Summary and Comparison Based on Experimental Results

The advantages and disadvantages of each technique based on the experimental tests are summarized and compared in Table VII to verify the superior performance of the proposed strategy. As shown in Table VII, the PR-based strategy can guarantee good power quality during grid faults, fast current limiting, and the lowest computational burden, and there is no active power overshoot after fault clearance. However, voltage recovery after fault clearance with the PR-based strategy is the slowest. Additionally, high reactive power overshoots and active

TABLE VII
Advantages and Disadvantages of Each Technique Based on the Experimental Tests

Strategy	Advantages	Disadvantages
PR-based strategy	Good power quality during faults Fast current limiting during faults Lowest computational burden No active power overshoot after fault clearance	Slowest voltage recovery after fault clearance High reactive power overshoot after fault clearance Active power oscillation after fault clearance
FCS-MPC-based strategy	Fast voltage recovery after fault clearance Fast current limiting during faults No active power oscillation after fault clearance	Terrible power quality during faults High active power overshoots after fault clearance High reactive power overshoots after fault clearance Highest computational burden
Proposed strategy	Fast current limiting during faults Good power quality during faults Low computational burden Fast voltage recovery after fault clearance No active power oscillation after fault clearance No active power overshoot after fault clearance Lowest reactive power overshoot after fault clearance High robustness against mismatched parameters	

power oscillations are produced after fault clearance with the PR-based strategy. The current limiting and voltage recovery after fault clearance with the FCS-MPC-based strategy are fast, and no active power oscillation after fault clearance is induced. However, terrible power quality during faults will be caused by the FCS-MPC-based strategy, and high active and reactive power overshoots after fault clearance are brought. Besides, the computational burden of the FCS-MPC is the highest.

Compared with the PR-based strategy and the FCS-MPC-based strategy, the proposed strategy can ensure fast current limiting during faults, good power quality during faults, low computational burden, fast voltage recovery after fault clearance, and the lowest reactive power overshoot after fault clearance. Moreover, there are no active power overshoots and oscillations after fault clearance with the proposed strategy. The high robustness against mismatched parameters for the proposed strategy is also tested by experimental results. Therefore, the proposed strategy reveals a superior FRT performance to the PR-based strategy and the FCS-MPC-based strategy.

V. Conclusion

This article proposes a model-predictive dual-control loop with improved current-limiting capability to address overcurrent issues for GFM inverters. The nontrivial weighting factor selection in general MPC strategies can be avoided in the proposed strategy. The power quality during faults can be guaranteed since the direct current-limiting scheme can be applied to proportionally scale down the current reference generated from the outer-voltage MPC loop in case of overcurrent, and such constrained current reference tracking can be implemented through the inner-current MPC loop. The optimal voltage vector can be derived in a continuous form by calculating the analytical solution of the cost function and synthesized by an SPWM block; thus, a constant switching frequency can be ensured. Ultimately, the voltage can recover rapidly from faults to normal conditions with the proposed strategy thanks to the high bandwidth of the outer-voltage MPC loop. Additionally, the active power can recover from the faulty value to the normal value smoothly without oscillation, and the reactive power can recover from the faulty value to the normal value with low overshoots.

References

[1] Y. Li, Y. Gu, and T. Green, "Revisiting grid-forming and grid-following inverters: A duality theory," *IEEE Trans. Power Syst.*, vol. 37, no. 6, pp. 4541–4554, Nov. 2022, doi: 10.1109/TPWRS.2022.3151851.

[2] Y. W. Li, F. Nejabatkhah, and H. Tian, *Smart Hybrid AC/DC Microgrids: Power Management, Energy Management, and Power Quality Control*. Hoboken, NJ, USA: Wiley, 2023.

[3] H. Zhang, R. Liu, C. Xue, and Y. Li, "Active power enhancement control strategy of grid-forming inverters under asymmetrical grid faults," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1447–1459, Jan. 2024, doi: 10.1109/TPEL.2023.3322042.

[4] Z. Li, K. W. Chan, J. Hu, and S. W. Or, "An adaptive fault ride-through scheme for grid-forming inverters under asymmetrical grid faults," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12912–12923, Dec. 2022, doi: 10.1109/TIE.2021.3135641.

[5] T. Qoria, F. Gruson, F. Colas, X. Kestelyn, and X. Guillaud, "Current limiting algorithms and transient stability analysis of grid-forming VSCs," *Electric Power Syst. Res.*, vol. 189, Dec. 2020, Art. no. 106726, doi: 10.1016/j.epsr.2020.106726.

[6] S. F. Zarei, H. Mokhtari, M. A. Ghasemi, and F. Blaabjerg, "Reinforcing fault ride through capability of grid forming voltage source converters using an enhanced voltage control scheme," *IEEE Trans. Power Del.*, vol. 34, no. 5, pp. 1827–1842, Oct. 2019, doi: 10.1109/TPWRD.2018.2844082.

[7] I. Sadeghkhani, M. E. H. Golshan, J. M. Guerrero, and A. Mehrizi-Sani, "A current limiting strategy to improve fault ride-through of inverter interfaced autonomous microgrids," *IEEE Trans. Smart Grid*, vol. 8, no. 5, pp. 2138–2148, Sep. 2017, doi: 10.1109/TSG.2016.2517201.

[8] B. Fan, T. Liu, F. Zhao, H. Wu, and X. Wang, "A review of current-limiting control of grid-forming inverters under symmetrical disturbances," *IEEE Open J. Power Electron.*, vol. 3, pp. 955–969, 2022, doi: 10.1109/OJPEL.2022.3227507.

[9] B. Fan and X. Wang, "Fault recovery analysis of grid-forming inverters with priority-based current limiters," *IEEE Trans. Power Syst.*, vol. 38, no. 6, pp. 5102–5112, Nov. 2023, doi: 10.1109/TPWRS.2022.3221209.

[10] S. P. Me, S. Zabihi, F. Blaabjerg, and B. Bahrani, "Adaptive virtual resistance for postfault oscillation damping in grid-forming inverters," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3813–3824, Apr. 2022, doi: 10.1109/TPEL.2021.3118677.

[11] A. D. Paquette and D. M. Divan, "Virtual impedance current limiting for inverters in microgrids with synchronous generators," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1630–1638, Mar./Apr. 2015, doi: 10.1109/TIA.2014.2345877.

[12] N. Bottrell and T. C. Green, "Comparison of current-limiting strategies during fault ride-through of inverters to prevent latch-up and wind-up," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3786–3797, Jul. 2014, doi: 10.1109/TPEL.2013.2279162.

[13] Y. Liao, X. Wang, and F. Blaabjerg, "Passivity-based analysis and design of linear voltage controllers for voltage-source converters," *IEEE Open J. Ind. Electron. Soc.*, vol. 1, pp. 114–126, 2020, doi: 10.1109/OJIES.2020.3001406.

[14] C. Alfaro, R. Guzman, L. G. d. Vicuña, J. Miret, and M. Castilla, "Dual-loop continuous control set model-predictive control for a three-phase unity power factor rectifier," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1447–1460, Feb. 2022, doi: 10.1109/TPEL.2021.3107221.

[15] C. Zheng, T. Dragičević, and F. Blaabjerg, "Model predictive control-based virtual inertia emulator for an islanded alternating current microgrid," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7167–7177, Aug. 2021, doi: 10.1109/TIE.2020.3007105.

[16] C. Xue, J. Wang, R. Liu, H. Zhang, Y. Li, and Y. Li, "Generalized predictive control for LC-filtered voltage-source inverters with enhanced predictive horizon," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13798–13810, Nov. 2023, doi: 10.1109/TPEL.2023.3304302.

[17] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: Advances and trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 935–947, Feb. 2017, doi: 10.1109/TIE.2016.2625238.

[18] M. Pouresmaeil, A. Sepehr, B. A. Khan, J. Adabi, and E. Pouresmaeil, "Model predictive-based control technique for fault ride-through capability of VSG-based grid-forming converter," in *Proc. 24th Eur. Conf. Power Electron. Appl.*, Sep. 2022, pp. 1–7.

[19] R. Aboelsaud, A. Ibrahim, I. V. Aleksandrov, and Z. M. Ali, "Model predictive control algorithm for fault ride-through of stand-alone microgrid inverter," *Int. J. Elect. Power Energy Syst.*, vol. 135, 2022, Art. no. 107485, doi: 10.1016/j.ijepes.2021.107485.

[20] H. A. Young, V. A. Marin, C. Pesce, and J. Rodriguez, "Simple finite-control-set model predictive control of grid-forming inverters with LCL filters," *IEEE Access*, vol. 8, pp. 81246–81256, 2020, doi: 10.1109/ACCESS.2020.2991396.

[21] J. Jongudomkarn, J. Liu, and T. Ise, "Virtual synchronous generator control with reliable fault ride-through ability: A solution based on finite-set model predictive control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 3811–3824, Dec. 2020, doi: 10.1109/JESTPE.2019.2942943.

[22] A. J. Babqi and A. H. Etemadi, "MPC-based microgrid control with supplementary fault current limitation and smooth transition mechanisms," *IET Gener., Transmiss. Distrib.*, vol. 11, no. 9, pp. 2164–2172, Apr. 2017, doi: 10.1049/iet-gtd.2016.1387.

[23] Z. Zhang et al., "An adaptive virtual synchronous generator based model predictive control with enhanced frequency support capability in micro-energy systems," in *Proc. IEEE Int. Conf. Predictive Control Elect. Drives Power Electron.*, Jun. 2023, pp. 1–6, doi: 10.1109/PRECEDE57319.2023.10174514.

[24] S. Vazquez et al., "Model predictive control for single-phase NPC converters based on optimal switching sequences," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7533–7541, Dec. 2016, doi: 10.1109/TIE.2016.2594227.

[25] L. Huang, H. Xin, Z. Wang, L. Zhang, K. Wu, and J. Hu, "Transient stability analysis and control design of droop-controlled voltage source converters considering current limitation," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 578–591, Jan. 2019, doi: 10.1109/TSG.2017.2749259.

[26] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive control of a three-phase neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2697–2705, Oct. 2007, doi: 10.1109/TIE.2007.899854.

[27] T. Dragičević and M. Novak, "Weighting factor design in model predictive control of power electronic converters: An artificial neural network approach," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8870–8880, Nov. 2019, doi: 10.1109/TIE.2018.2875660.

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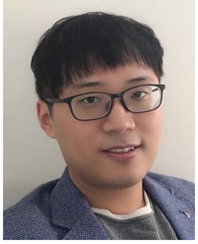

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