Low-Capacitance Operation and Its Hierarchical Control for STATCOM Based on T-Type Converter With MMDTC

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***Abstract*—For conventional operation, the submodules of a static synchronous compensator based on a T-type converter with modular multilevel dc-link require high capacitance to suppress capacitor voltage ripple. Being different from that, an intriguing discovery reveals the capacitor voltage ripple is in phase with arm voltage in capacitive reactive power mode and opposite in inductive reactive power mode. As a result, a low-capacitance operation is proposed by exploiting this intriguing discovery. To better accommodate the proposed low-capacitance operation, this article presents a hierarchical control strategy that integrates a single PI controller, a model predictive control with a single objective, and an enhanced algorithm for sorting capacitor voltages. Finally, simulation and experimental results validate the effectiveness of the proposed low-capacitance operation and its hierarchical control strategy.**

***Index Terms*—Low capacitance, model predictive control, multilevel converter, static synchronous compensator (STATCOM), T-type converter.**

I. Introduction

THE static synchronous compensator (STATCOM) is a power electronics-based shunt device utilized for rapid and dynamic compensation of reactive power [1], [2]. It finds extensive application in the power system for voltage and reactive power regulations [3], [4]. The significance of STATCOM has been growing due to the increased integration of renewable energy sources such as wind and photovoltaic power plants in recent years. Recent advancements in multilevel converters facilitate the development of medium-voltage high-power STATCOMs. Four fundamental multilevel topologies have been explored including cascaded H-bridge (CHB) converter [5], modular multilevel converter (MMC) [6], neutral point clamped (NPC) converter [7], and flying capacitor (FC) converter [8]. For STATCOM applications, NPC and FC converters exhibit suboptimal performance in terms of capacitor voltage balancing, especially when the number of voltage levels is high. Similarly, CHB and MMC face challenges due to a large number of semiconductor power devices needed to synthesize the desired multilevel voltage.

The STATCOMs based on hybrid multilevel topologies have attracted attention due to their features of integrating traditional designs and achieving higher output voltage levels with fewer power components [9], [10], [11]. Among these topologies, the T-type converter with modular multilevel dc-link (MMDTC) [12] combines features of different semiconductor devices, such as the high voltage capability, low conduction loss, and cost-effectiveness of thyristors, as well as the high-frequency characteristics and controllability offered by IGBTs. Moreover, it does not require multiple isolated power sources in the dc side of submodules in the reactive power compensation applications, making it a promising choice for medium-voltage high-power STATCOM.

Traditionally, high-capacitance electrolytic capacitors are utilized in MMDTC to mitigate voltage ripple. However, the electrolyte in these capacitors gradually volatilizes over time, resulting in a gradual decline in their electrical performance. The reliable operation of the entire system relies heavily on the reliability of SM capacitors, which has prompted researchers to explore film capacitors as a viable alternative. Existing literature [13], [14], [15], [16] have comprehensively compared film capacitors and electrolytic capacitors in converters, as shown in Table I, leading to the following conclusion: Film capacitors exhibit longer lifetimes, superior operating voltage capability, and stronger current capability compared to electrolytic counterparts. However, film capacitors have lower capacitance per volume ratio and higher cost implications. Direct replacement is impractical due to cost and volume considerations. Hence, it becomes imperative to explore new approaches for reducing capacitance in order to meet the demand for transitioning from electrolytic capacitors to film-based alternatives.

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TABLE I
ELECTROLYTIC VERSUS FILM CAPACITORS

Technical parameters	Electrolytic capacitor	Film capacitor
Capacitance per unit volume	High	Low
Cost per Joule	Low	High
Operating voltage	Low	High
Rms current rating	20 mA/μF	200–1000 mA/μF
Equivalent series resistance (ESR)	High	Low
Losses	High	Low
Operating lifetime	< 20 000 h	> 100 000 h

TABLE II
COMPARISON OF APPROACHES FOR REDUCING SM CAPACITANCE

Approaches	Methods	disadvantages
Suppressing voltage ripple	Circulating current injection [17-20]	Not suitable for MMDTC
	Both zero-sequence voltage and circulating current injection [21-22]	
	Negative-sequence current injection [23] and third-order harmonic injection [24]-[26]	
	Additional active power decoupling circuits [27-31]	Increased cost and volume
	Closed-loop voltage ripple controller [32]	Only for CHB drive
Taking advantage of voltage ripple	Through an increased number of series-connected submodules in each arm [33]	Increased number of power devices
	Skillfully utilizing the phase relationship between capacitor voltage and grid voltage [34-37]	Not suitable for MMDTC

In summary, previous research efforts have primarily focused on two approaches to mitigate the SM capacitance for multilevel converters: suppressing the voltage ripple across capacitors and effectively taking advantage of the inherent capacitor voltage ripple, as summarized in Table II. Since the MMDTC is different from existing conventional multilevel converters, the existing voltage-ripple suppression methods are not applicable. In detail, the existing methods suppressed capacitor voltage ripple by injecting circulating current [17], [18], [19], [20] and zero-sequence voltage [21], [22] in MMC. However, neither the circulating current injection nor the zero-sequence voltage injection methods are suitable for MMDTC due to the absence of a circulating current path and mutual cancellation of zero-sequence voltages within upper- and lower-arm modulation waves. Yang et al. [23] proposed similar methods to suppress voltage ripple of CHB converters by injecting negative-sequence current and third-order voltage [24], [25], [26]. However, they cause increased current stress and power losses of power devices. And the injected third-order voltage does not have any impact on MMDTC, since it would mutually cancel out within the upper and lower arm modulation waves. In addition, the additional active power decoupling circuits were employed to suppress capacitor voltage ripple, such as stacked switched-capacitor topologies [27], [28], buck-type active power filter decoupling circuit [29], [30], and three-terminal middle-cell between the upper arm, lower arm [31]. However, these methods result in significant hardware cost escalation. Ni et al. [32] introduced a novel closed-loop voltage ripple controller for regenerative CHB drive; however, it is not suitable for STATCOM application.

To take advantage of the inherent capacitor voltage ripple, the SM capacitance can be significantly reduced if a larger voltage ripple can be accepted. Song et al. [33] proposed a low-capacitance MMC operating with large capacitor voltage ripples through an increased number of series-connected submodules in each arm. However, this method leads to an increase in power devices. In [34] and [35], the capacitance in full bridge converter was reduced by tolerating a strongly fluctuating voltage at twice the line frequency using special control techniques. A low-capacitance CHB-STATCOM was suggested for operation with large capacitor voltage ripples [36]. Nevertheless, these methods cannot be directly applied to MMDTC topology due to its fundamentally different working principle from that of MMC and CHB.

To date, there is a scarcity of research literature addressing the reduction of SM capacitance value in MMDTC. Therefore, this article aims to minimize the required SM capacitance value in MMDTC-STATCOM. The unique contribution of this article lies in the theoretical analysis of SM capacitor voltage and arm voltage fluctuation laws, leading to a novel finding for the first time: during capacitive reactive power mode, the capacitor voltage ripple is found to be in phase with the arm voltage, while it is opposite during inductive reactive power mode. Based on this intriguing discovery, a low-capacitance operation strategy is proposed in this article. Subsequently, to better align with the proposed low-capacitance operation, a hierarchical control strategy is proposed in this article, which incorporates a single PI controller, a single objective optimization of model predictive control (MPC), and an enhanced algorithm for sorting capacitor voltages in a hierarchical manner.

II. OPERATIONAL PRINCIPLE OF MMDTC-STATCOM

The MMDTC-based STATCOM, as illustrated in Fig. 1, consists of two IGBT-based arms with a T-type structure. The upper and lower arms are cascaded by HBSMs, and then connects at the dc side of the T-type structure. Each phase of the T-type structure comprises three high-voltage switches (T_{ku}, T_{kn}, T_{kl}; k = a, b, c) designed to withstand line-to-line voltage [12].

For the convenience of analysis, the basic operational principles are briefly summarized in this section. The phase voltage of the converter is defined as

$$\begin{cases} u_{\mathbf{ao}} = V_{\mathrm{o}} \sin(\omega t + \pi/6) \\ u_{\mathbf{bo}} = V_{\mathrm{o}} \sin(\omega t - \pi/2) \\ u_{\mathbf{co}} = V_{\mathrm{o}} \sin(\omega t + 5\pi/6) \end{cases} \tag{1}$$

V_{o} refers to the phase voltage amplitude and $\omega = 2\pi f$.

The line-to-line voltages of the converter can be derived from (1) as follows:

$$\begin{cases} u_{\mathbf{ab}} = \sqrt{3} V_{\mathrm{o}} \sin(\omega t + \pi/3) \\ u_{\mathbf{bc}} = \sqrt{3} V_{\mathrm{o}} \sin(\omega t - \pi/3) \\ u_{\mathbf{ca}} = -\sqrt{3} V_{\mathrm{o}} \sin(\omega t) \end{cases}. \tag{2}$$

The switching sequences $\{S_a, S_b, S_c\}$ of the T-type structure are listed in Fig. 2, where $S_k = 1, 0, -1$ (k = a, b, c) denote the conduction states of the upper-, middle-, and lower-switches of

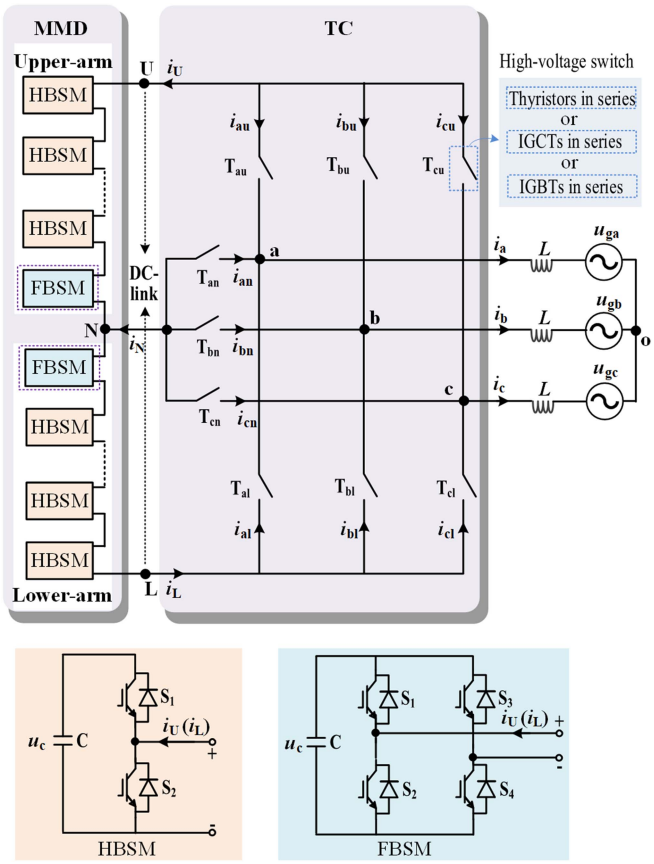


Fig. 1. Configuration of MMDTC-based STATCOM.

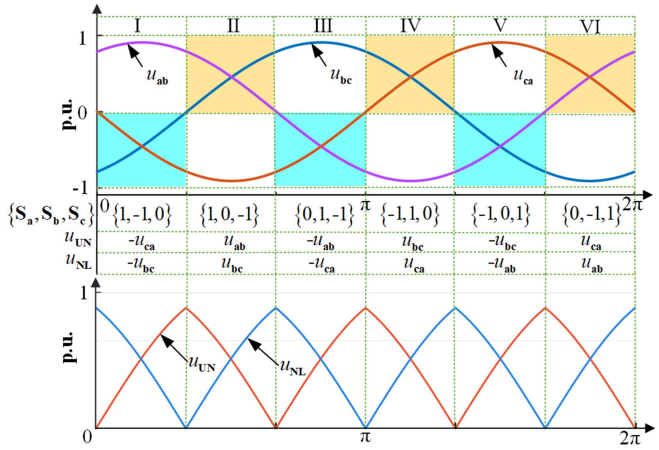


Fig. 2. Switching sequences of T-structure and arm voltages along with line-to-line voltages.

phase-*k*, respectively. The corresponding output voltages of the upper arm and lower arm, along with the line-to-line voltages, can be summarized, as shown in Fig. 2. Their time-variant expression can be deduced accordingly

$$u_{\mathrm{UN}} = \begin{cases} \sqrt{3}V_{\mathrm{o}} \sin\theta, \ \theta \in \left[0, \frac{\pi}{3}\right) \\ \sqrt{3}V_{\mathrm{o}} \sin\left(\theta + \frac{\pi}{3}\right), \theta \in \left[\frac{\pi}{3}, \frac{2\pi}{3}\right] \end{cases} \tag{3a}$$

$$u_{\mathrm{NL}} = \begin{cases} -\sqrt{3}V_{\mathrm{o}} \sin\left(\theta - \frac{\pi}{3}\right), \theta \in [0, \frac{\pi}{3}) \\ \sqrt{3}V_{\mathrm{o}} \sin\left(\theta - \frac{\pi}{3}\right), \theta \in \left[\frac{\pi}{3}, \frac{2\pi}{3}\right] \end{cases} \tag{3b}$$

where $\theta = \omega t - \mathrm{floor}(\omega t/(\frac{2\pi}{3}))$, floor (α) refers to rounding the elements of α down to the nearest integers. According to (3), the peak value of arm voltage $V_{\mathrm{arm\_peak}} = 1.5\ V_{\mathrm{o}}$ can be obtained when $\theta = \pi/3$.

By employing the Fourier series expansion formula [38] and disregarding its high-frequency components, the Formula (3) of arm voltages can be reformulated as follows:

$$u_{\mathrm{UN}}(t) \approx \mathrm{a}_0 - \mathrm{a}_3 \cos(3\omega t) \tag{4a}$$

$$u_{\mathrm{NL}}(t) \approx \mathrm{a}_0 + \mathrm{a}_3 \cos(3\omega t) \tag{4b}$$

where $\mathrm{a}_0 = \frac{3\sqrt{3}V_{\mathrm{o}}}{2\pi}$ and $\mathrm{a}_3 = \frac{9\sqrt{3}V_{\mathrm{o}}}{8\pi}$.

According to (4), the arm voltages mainly contain third-order harmonics.

III. Capacitance Reduction of MMDTC-STATCOM

Since the capacitor voltage ripple is related to the charging and discharging behaviors, to derive the capacitor voltage ripple, the capacitor currents are determined by the arm current and switching states of SMs. Then, the peak–peak ripple is derived from the capacitor current, which determines the capacitance.

When the MMDTC compensates for capacitive reactive power, the arm currents are expressed as

$$i_{\mathrm{U}} = -I_{\mathrm{o}} \sin\left(\theta - \frac{\pi}{3}\right), \theta \in \left[0, \frac{2\pi}{3}\right] \tag{5a}$$

$$i_{\mathrm{L}} = \begin{cases} I_{\mathrm{o}} \sin(\theta - \pi), \theta \in [0, \frac{\pi}{3}) \\ I_{\mathrm{o}} \sin\left(\theta + \frac{\pi}{3}\right), \theta \in \left[\frac{\pi}{3}, \frac{2\pi}{3}\right] \end{cases} \tag{5b}$$

where I_{o} represents the amplitude of phase current.

Assuming the SM system is lossless and in accordance with the principle of power conservation, the following expression can be derived:

$$C u_{\mathrm{c\_up}} \frac{du_{\mathrm{c\_up}}}{dt} = \frac{u_{\mathrm{UN}}}{N} i_{\mathrm{U}}. \tag{6}$$

And then combining (3a) and (5a), the time-variant SM capacitor voltage $u_{\mathrm{c\_up}}$ can be derived

$$u_{\mathrm{c\_up}}(t) = \begin{cases} \sqrt{U_{\mathrm{c\_peak}}^2 + \frac{\sqrt{3}V_{\mathrm{o}}I_{\mathrm{o}}}{2N\omega C}\left\{[\sin(2\theta - \pi/3) - \theta] - \left(\frac{\sqrt{3}}{2} - \frac{\pi}{3}\right)\right\}} \ \theta \in [0, \frac{\pi}{3}) \\ \sqrt{U_{\mathrm{c\_peak}}^2 + \frac{\sqrt{3}V_{\mathrm{o}}I_{\mathrm{o}}}{2N\omega C}\left\{[\sin(2\theta) + \theta] - \left(\frac{\sqrt{3}}{2} + \frac{\pi}{3}\right)\right\}} \ \theta \in \left[\frac{\pi}{3}, \frac{2\pi}{3}\right] \end{cases} \tag{7a}$$

where $U_{\mathrm{c\_peak}}$ refers to the peak value of SM capacitor voltage, C is capacitance value, and N is the number of SMs per arm.

In a similar way, the SM capacitor voltage within the lower arm can be derived

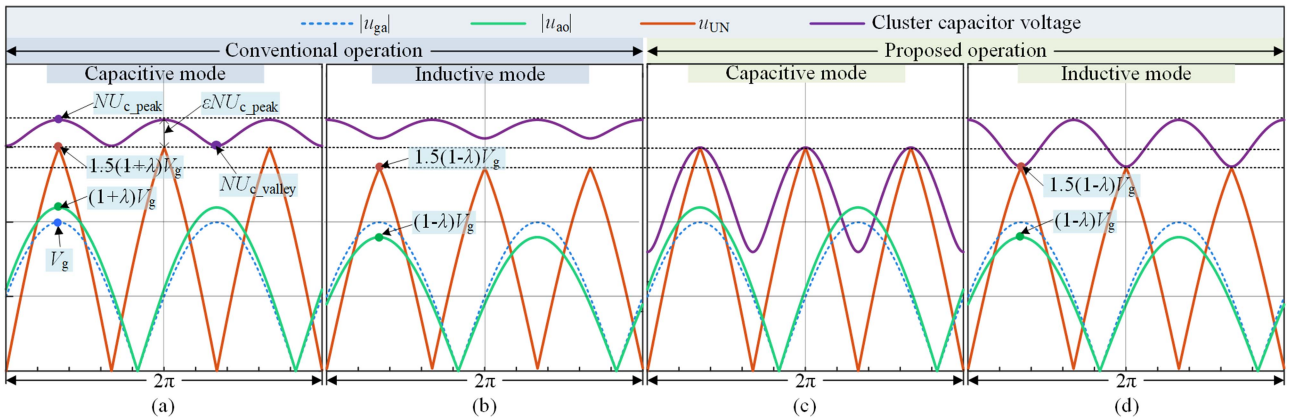


Fig. 3. Schematic diagrams of MMDTC-STATCOM operation. (a) and (b) in conventional operation. (c) and (d) in proposed low-capacitance operation.

$$u_{c\_low}(t) = \begin{cases} \sqrt{U_{c\_peak}^2 - \frac{\sqrt{3}V_oI_o}{2N\omega C}\left\{[\sin(2\theta - \pi/3) - \theta] + \frac{\sqrt{3}}{2}\right\}} \theta \in [0,\ \frac{\pi}{3}) \\ \sqrt{U_{c\_peak}^2 - \frac{\sqrt{3}V_oI_o}{2N\omega C}\left\{[\sin(2\theta) + \theta] + \left(\frac{\sqrt{3}}{2} - \frac{2\pi}{3}\right)\right\}} \theta \in \left[\frac{\pi}{3},\ \frac{2\pi}{3}\right] \end{cases}. \tag{7b}$$

The peak–peak ripple is determined by the peak and valley values of SM capacitor voltage. In order to quantitatively analyze the capacitance value below, the valley value of SM capacitor voltage is calculated as $\theta = 0$ in (7a), namely,

$$U_{c\_valley} = \sqrt{U_{c\_peak}^2 - \frac{\sqrt{3}V_oI_o}{2N\omega C}\left(\sqrt{3} - \frac{\pi}{3}\right)}. \tag{8}$$

A. Conventional Operation Without Considering Phase Relationship Between Capacitor Voltage and Arm Voltage

Under conventional operating conditions, the phase of capacitor voltage is typically disregarded, with emphasis solely on diminishing the ripple amplitude on capacitor voltage, which will be analyzed as follows.

To avoid overmodulation, it is necessary to ensure that the instantaneous value of the cluster capacitor voltage is always greater than the arm voltage. To achieve this, commonly set the valley value of the cluster capacitor voltage always higher than the maximum value of arm voltage. The operating mode of STATCOM is generally divided into capacitive and inductive ones. In the capacitive mode, the converter output voltage exceeds the grid voltage, whereas in the inductive mode, it falls below the grid voltage, i.e.,

$$V_o = \begin{cases} (1+\lambda)V_g, & \text{when in capacitive mode} \\ (1-\lambda)V_g, & \text{when in inductive mode} \end{cases} \tag{9}$$

where V_g refers to the amplitude of grid phase voltage, and $\lambda = \omega LI_o/V_g$ refers to the ratio of voltage drop across filtering inductor.

Then, the corresponding peak value of the arm voltage can be obtained

$$V_{arm\_peak} = \begin{cases} 1.5(1+\lambda)V_g, & \text{when in capacitive mode} \\ 1.5(1-\lambda)V_g, & \text{when in inductive mode} \end{cases}. \tag{10}$$

Fig. 3(a) and (b) shows the schematic diagram for the conventional operation. To avoid overmodulation both in capacitive and inductive modes, the valley value of cluster capacitor voltage must exceed the larger one between both values specified in (10), namely,

$$NU_{c\_valley} \geq 1.5(1+\lambda)V_g. \tag{11}$$

Assuming that the capacitor voltage ripple ratio $\varepsilon = \Delta U_{c\_peak}/U_{c\_peak}$, the following equation can be obtained:

$$NU_{c\_peak} = NU_{c\_valley} + \varepsilon NU_{c\_peak}. \tag{12}$$

Consider the critical case of (11): i.e., $NU_{c\_valley} = 1.5(1+\lambda)V_g$, and then according to (8), (11), and (12), the required capacitance C_0 can be expressed as

$$C_0 = \left(3 - \frac{\pi}{\sqrt{3}}\right)\frac{2NI_o(1-\varepsilon)^2}{9\omega V_g(1+\lambda)(2\varepsilon - \varepsilon^2)} \tag{13}$$

According to (13), once the filtering inductor voltage drop ratio λ is given, capacitance C_0 is inversely proportional to capacitor voltage ripple ratio ε, while once ε is given, and C_0 is inversely proportional to λ. Therefore, in order to reduce the required capacitance C_0, it becomes necessary to increase filtering inductor voltage drop ratio λ or capacitor voltage ripple ratio ε. However, the increased λ results in a larger filtering inductor, while the increase in ε would result in higher voltage stress on SM, both of which cause an increased cost of the converter.

B. Proposed Low-Capacitance Operation Utilizing Phase Relationship Between Capacitor Voltage and Arm Voltage

Based on the above analysis, when reducing capacitance, the voltage ripple is increased. In fact, overmodulation can be avoided as long as the instantaneous value of cluster capacitor

voltage surpasses that of arm voltage. Since there is a larger triple-frequency ripple on arm voltage according to (4), this would also allow a larger ripple on capacitor voltage in theory.

When employing Fourier expansion to capacitor voltages expressed in (7a) and (7b), they are reformulated as

$$u_{\mathrm{c\_up}}(t) \approx \mathrm{b}_0 - \mathrm{b}_3 \cos(3\omega t) \tag{14a}$$

$$u_{\mathrm{c\_low}}(t) \approx \mathrm{b}_0 + \mathrm{b}_3 \cos(3\omega t) \tag{14b}$$

where b_0 and b_3 are expressed as (15), shown at the bottom of this page.

According to (4) and (14), the third-order harmonic of arm voltage is in phase with capacitor voltage ripple. This interesting finding suggests that a larger ripple on capacitor voltage can be existing without adversely affecting arm voltage modulation. Taking advantage of this finding, the peak cluster capacitor voltage only needs to be higher than the peak arm voltage, as depicted in Fig. 3(c). In other words, the capacitor voltage ripple can be increased by leveraging the consistent phase relationship between capacitor voltage and arm voltage. Therefore, in the capacitive mode, a larger peak–peak ripple leads to lower capacitance.

However, in the inductive mode, the third-order harmonic of capacitor voltage is reversely in phase with that of arm voltage, as expressed in

$$u_{\mathrm{c\_up}}(t) \approx \mathrm{b}_0 + \mathrm{b}_3 \cos(3\omega t) \tag{16a}$$

$$u_{\mathrm{c\_low}}(t) \approx \mathrm{b}_0 - \mathrm{b}_3 \cos(3\omega t). \tag{16b}$$

This observation indicates that in order to avoid overmodulation, the valley value of cluster capacitor voltage must exceed the peak value of arm voltage, as shown in Fig. 3(d), i.e.,

$$NU_{\mathrm{c\_valley}} \geq 1.5(1-\lambda)V_g. \tag{17}$$

Assuming the peak value of cluster capacitor voltage remains the same as that in conventional operating mode, as shown in Fig. 3, the required capacitance C_1 for the proposed operation can be deduced based on (8), (13), and (17)

$$C_1 = (3 - \frac{\pi}{\sqrt{3}}) \frac{2NI_{\mathrm{o}}(1-\lambda)(1-\varepsilon)^2}{9\omega V_{\mathbf{g}} \left[(1+\lambda)^2 - (1-\lambda)^2(1-\varepsilon)^2\right]} \tag{18}$$

where ε represents the capacitor voltage ripple ratio under the conventional operation as tagged in Fig. 3(a).

Furthermore, the capacitance difference between the proposed operation and the conventional one can be expressed as

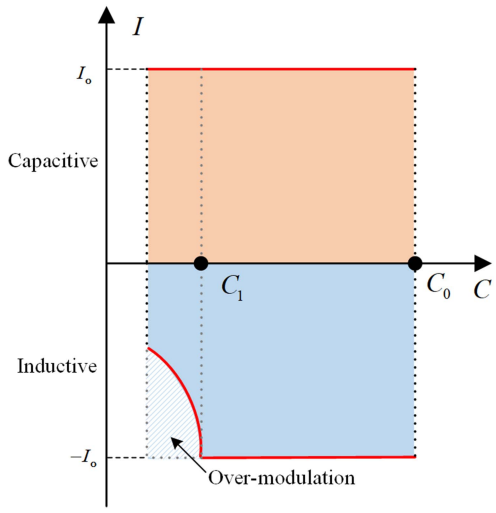


Fig. 4. Diagram illustrating the correlation between the maximum output current and the SM capacitance value.

$$C_0 - C_1 = \frac{4(\frac{\pi}{\sqrt{3}} - 3)NI_{\mathrm{o}}\lambda(1-\varepsilon)^2\left[(1-\lambda)(2-\varepsilon)\varepsilon - 2\right]}{9\omega V_{\mathbf{g}}\left[(1+\lambda)(2\varepsilon-\varepsilon^2)\right]\left[(1+\lambda)^2 - (1-\lambda)^2(1-\varepsilon)^2\right]}. \tag{19}$$

According to (19), $C_0 - C_1 > 0$ when $0 < \lambda < 1$ and $0 < \varepsilon < 1$, which indicates the proposed operation can achieve a reduction in capacitance compared to the conventional operation.

Phase alignment between the arm voltage and capacitor voltage ripple is the key feature utilized in the low-capacitance operation. By utilizing such phase alignment, MMDTC-STATCOM can operate with constant peak capacitor voltage independent of the ripple magnitude. However, this favorable phase alignment only exists in the capacitive mode. If the capacitance value is very low, the STATCOM's operation capability in the inductive mode maybe limited, which can be explained from Fig. 4. In Fig. 4, positive current values represents capacitive operating region, while negative values represents inductive operating region. I_{o} represents the rated reactive current. C_1 represents the critical value necessary for ensuring that the converter can output symmetric inductive and capacitive reactive current. In

$$\mathrm{b}_0 = \frac{4\sqrt{3}V_{\mathrm{o}}I_{\mathrm{o}}}{15\pi N\omega C\sqrt{U^2{}_{\mathrm{c\_peak}} + \left(\frac{\pi}{3} - \sqrt{3}\right)\frac{\sqrt{3}V_{\mathrm{o}}I_{\mathrm{o}}}{4N\omega C}} - \sqrt{U^4{}_{\mathrm{c\_peak}} + \left(\frac{\pi}{3} - \sqrt{3}\right)\frac{\sqrt{3}V_{\mathrm{o}}I_{\mathrm{o}}U^2{}_{\mathrm{c\_peak}}}{2N\omega C} + \left[\frac{3}{16}\left(\frac{\pi}{3} - \sqrt{3}\right)^2 - \frac{32}{225\pi^2}\right]\frac{V_{\mathrm{o}}{}^2I_{\mathrm{o}}{}^2}{N^2\omega^2C^2}}} \tag{15a}$$

$$\mathrm{b}_3 = \sqrt{U^2{}_{\mathrm{c\_peak}} + \left(\frac{\pi}{3} - \sqrt{3}\right)\frac{\sqrt{3}V_{\mathrm{o}}I_{\mathrm{o}}}{4N\omega C} - \sqrt{U^4{}_{\mathrm{c\_peak}} + \left(\frac{\pi}{3} - \sqrt{3}\right)\frac{\sqrt{3}V_{\mathrm{o}}I_{\mathrm{o}}U^2{}_{\mathrm{c\_peak}}}{2N\omega C} + \left[\frac{3}{16}\left(\frac{\pi}{3} - \sqrt{3}\right)^2 - \frac{32}{225\pi^2}\right]\frac{V_{\mathrm{o}}{}^2I_{\mathrm{o}}{}^2}{N^2\omega^2C^2}}}. \tag{15b}$$

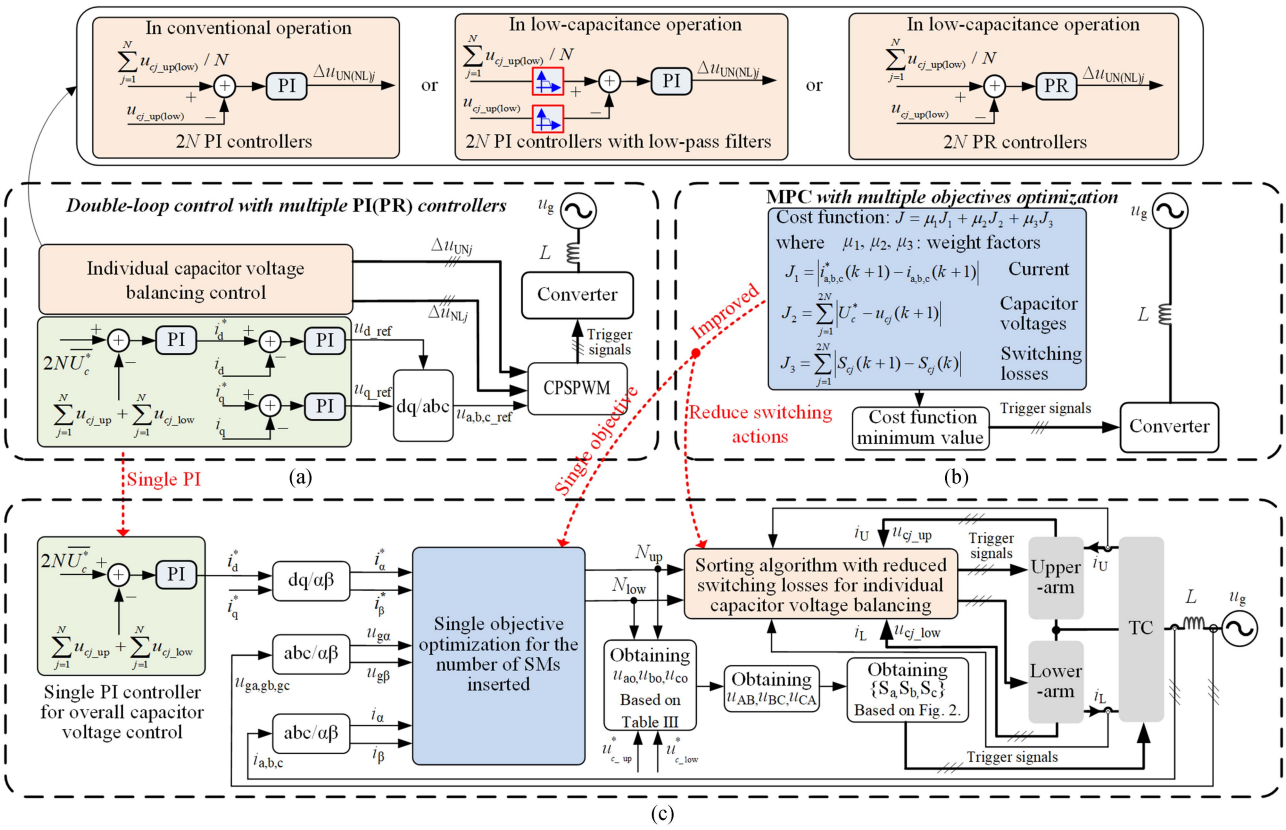


Fig. 5. Control Strategies comparison of (a) conventional double-loop control with multiple PI(PR) controllers, (b) conventional model predictive control with multiple objectives optimization, and (c) proposed hierarchical control.

other words, when $C_1 < C < C_0$, the symmetrical inductive and capacitive operating capability can be achievable. However, when $C < C_1$, the operational range of the converter is limited in inductive mode. That's to say, the reduction of output current is necessary to mitigate overmodulation, as it effectively diminishes the ripple value of capacitor voltage.

IV. Proposed Hierarchical Control for MMDTC-STATCOM

In the conventional operation of MMDTC-STATCOM mentioned in [12], multiple PI controllers are used to achieve multiple control objectives including the overall capacitor voltage-balancing, output currents and individual capacitor voltage-balancing, as shown in Fig. 5(a).

However, the reduced capacitance poses two challenges in the control design of MMDTC-STATCOM: 1) the need to consider a high-magnitude low-frequency ripple on the capacitor voltages, and 2) the requirement for a faster controller to regulate the voltages of capacitors during transients in order to prevent voltage overshoot. Consequently, tracking a sinusoidal reference becomes challenging for the PI controllers. To address this issue while still utilizing the multiple PI controllers for individual capacitor voltage control, it becomes necessary to incorporate a low-pass filter to extract the dc component from the capacitor voltage [see Fig. 5(a)]. Nevertheless, incorporating such a filter leads to reduced control bandwidth and inferior dynamics which can result in transient voltage overshoots. Alternatively, employing the PR controllers instead of PI controllers enable effective balance control of SM capacitor voltages [see Fig. 5(a)]. However, the conventional PR(PI) controller exhibits slow response due to significant delays, rendering it incapable of meeting the demands for swift adjustments in STATCOM. Simultaneously, the interdependence between multiple control objectives and controllers poses challenges in coordinating their dynamic characteristics, further complicating controller design [39], [40].

MPC, in contrast to conventional linear control, offers several advantages such as fast dynamic response, multiobjective control capability, straightforward implementation, and efficient handling of nonlinearities and constraints. However, conventional MPC involves evaluating all possible switching states of MMDTC to identify the optimal one that minimizes a cost function encompassing multiple control objectives like output current, SM capacitor voltages, and switching losses, as shown in Fig. 5(b). This is achieved by assigning weight factors reflecting their relative importance in overall system performance. Nevertheless, designing appropriate weight factors for multiobjective optimization poses challenges and may lead to potential conflicts arising from conflicting objectives [41], [42].

The limitations of the aforementioned control strategies are addressed by proposing a hierarchical control strategy, as shown

in Fig. 5(c). In this approach, the SM capacitor voltage-balancing control is excluded from the cost function and regulated individually using an improved sorting algorithm. The MPC scheme is designed to only predict the optimal output current through a single cost function and a single PI controller can effectively maintain balance in the total capacitor voltage.

A. Single PI Controller for Overall Capacitor Voltage Control

The overall control of capacitor voltage is implemented to regulate the total voltage across the capacitors. Despite larger ripples on the SM capacitor voltages, there is an opposite phase between the upper- and lower-arm voltage according to (14) and (16). As a result, the summation of capacitor voltages in both arms remains constant. Consequently, a single PI controller can be effectively employed to balance the total capacitor voltage.

B. Single Objective Optimization for the Number of SMs Inserted

In the conventional MPC, the trigger signal combinations of all power devices are done directly by solving the cost function for all possible sequences and one that provides a minimized cost will be selected. Being different from that, in the proposed hierarchical control, only the output current is evaluated and the corresponding optimal number of SMs inserted is obtained, which can reduce computation complexity.

The flow chart of single objective optimization for the number of SMs inserted is shown in Fig. 6. The number of SMs inserted references $N_{\mathrm{up}}(k)$ and $N_{\mathrm{low}}(k)$ are the basic components of the control set. Therefore, the evaluated control set can be expressed as

$$X(k) = [N_{\mathrm{up}}(k), N_{\mathrm{low}}(k)]\,. \tag{20}$$

And then the output voltage references of the upper and lower arm can be expressed as

$$[u_{\mathrm{UN}}(k), u_{\mathrm{NL}}(k)] = [N_{\mathrm{up}}(k), N_{\mathrm{low}}(k)] \begin{bmatrix} u_{\mathrm{c\_up}}(k) \\ u_{\mathrm{c\_low}}(k) \end{bmatrix}. \tag{21}$$

Furthermore, the phase voltage references $u_{\mathrm{ao}}(k)$, $u_{\mathrm{bo}}(k)$, $u_{\mathrm{co}}(k)$ of MMDTC can be deduced based on Table III.

The system model of MMDTC-STATCOM can be expressed as

$$L\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{a}} \\ i_{\mathrm{b}} \\ i_{\mathrm{c}} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{ga}} \\ u_{\mathrm{gb}} \\ u_{\mathrm{gc}} \end{bmatrix} - \begin{bmatrix} u_{\mathrm{ao}} \\ u_{\mathrm{bo}} \\ u_{\mathrm{co}} \end{bmatrix}. \tag{22}$$

By Clark transformation, the system model of the MMDTC can be further transferred into α-β coordinate as follows [28]:

$$L\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\alpha} \\ i_{\beta} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{g}\alpha} \\ u_{\mathrm{g}\beta} \end{bmatrix} - \begin{bmatrix} u_{\alpha} \\ u_{\beta} \end{bmatrix} \tag{23}$$

where i_α and i_β are the output current components in α- and β-axes; $u_{\mathrm{g}\alpha}$ and $u_{\mathrm{g}\beta}$ are the ac grid voltage components in α- and β-axes; u_α and u_β are the output voltage components in α- and β-axes.

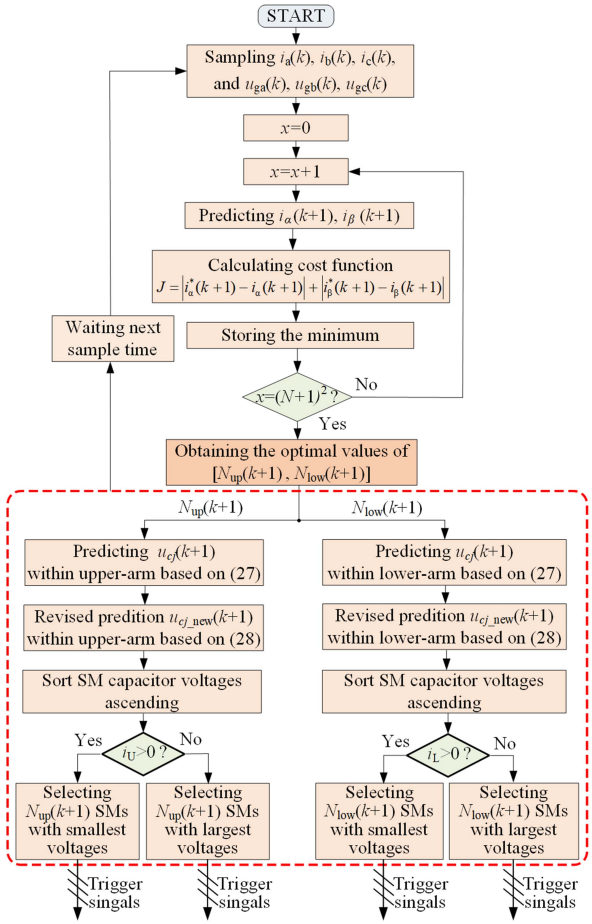


Fig. 6. Flow chart of the number of SMs inserted predictive control and individual capacitive voltage balancing control.

TABLE III
RELATIONSHIP BETWEEN PHASE VOLTAGES AND ARM VOLTAGES

Sector	$u_{\mathrm{ao}}(k)$	$u_{\mathrm{bo}}(k)$	$u_{\mathrm{co}}(k)$
I	$\frac{2u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$	$\frac{-u_{\mathrm{UN}}(k)-2u_{\mathrm{NL}}(k)}{3}$	$\frac{-u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$
II	$\frac{2u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$	$\frac{-u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$	$\frac{-u_{\mathrm{UN}}(k)-2u_{\mathrm{NL}}(k)}{3}$
III	$\frac{-u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$	$\frac{2u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$	$\frac{-u_{\mathrm{UN}}(k)-2u_{\mathrm{NL}}(k)}{3}$
IV	$\frac{-u_{\mathrm{UN}}(k)-2u_{\mathrm{NL}}(k)}{3}$	$\frac{2u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$	$\frac{-u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$
V	$\frac{-u_{\mathrm{UN}}(k)-2u_{\mathrm{NL}}(k)}{3}$	$\frac{-u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$	$\frac{2u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$
VI	$\frac{-u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$	$\frac{-u_{\mathrm{UN}}(k)-2u_{\mathrm{NL}}(k)}{3}$	$\frac{2u_{\mathrm{UN}}(k)+u_{\mathrm{NL}}(k)}{3}$

Equation (23) can be further discretized using the forward Euler approximation. The final discrete system model of the MMDTC-STATCOM can be expressed as follows:

$$\begin{cases} i_\alpha(k+1) = \frac{T_{\mathrm{S}}}{L}(u_{\mathrm{g}\alpha}(k) - u_\alpha(k)) + i_\alpha(k) \\ i_\beta(k+1) = \frac{T_{\mathrm{S}}}{L}(u_{\mathrm{g}\beta}(k) - u_\beta(k)) + i_\beta(k) \end{cases} \tag{24}$$

where T_s is the sampling period; $i_\alpha(k+1)$ and $i_\beta(k+1)$ are the predicted output currents at k+1 time instant; $u_{g\alpha}(k)$ and $u_{g\beta}(k)$ are the measured grid voltages at k time instant; $u_\alpha(k)$ and $u_\beta(k)$ are the output voltage references at k time instant; $i_\alpha(k)$and$i_\beta(k)$ are the measured output current at k time instant.

According to (20)–(24), it can be concluded that the output current in the k+1 time instant is determined by the output current and the number of SMs inserted references in the current k time constant.

With the determined search range (0∼N) of the number of SMs in the upper and lower arm, the evaluated control sets can be expressed as

$$\begin{aligned} &\text{for } i = 0:1:N \\ &\quad \text{for } j = 0:1:N \\ &\qquad [N_{\text{up}}(k+1), N_{\text{low}}(k+1)] = [i, j]\,. \end{aligned} \tag{25}$$

By incorporating the adaptive search range and evaluating control sets, the output current can be accurately predicted based on the discrete converter model presented in (24). The final cost function only contains the control target of output current in both α- and β-axes as follows:

$$J = \left| i_\alpha^*(k+1) - i_\alpha(k+1) \right| + \left| i_\beta^*(k+1) - i_\beta(k+1) \right| \tag{26}$$

where $i_\alpha^*(k+1)$ and $i_\beta^*(k+1)$ are the output current reference k+1 time instant. After calculating all the cost functions, the control set with the minimum cost function will be selected as the optimal control set for the next time instant. Ultimately, the optimal number of SMs inserted in the upper and lower arm can be obtained.

C. Sorting Algorithm With Reduced Switching Losses for Individual Capacitor Voltage Balancing

The sorting algorithm is commonly employed to balance individual capacitor voltages for multilevel converter. Usually, it is performed by directly organizing the capacitor voltages in ascending or descending order. When the capacitance of the capacitor decreases, there is a significant increase in the rate of change of its voltage. More frequent sorting and adjustment of capacitor voltages are required using the conventional sorting algorithm. This high-frequency switching action not only adds complexity to the system but also introduces additional switching losses. To address this issue, an improved sorting algorithm with a keeping factor is proposed.

Fig. 6 shows the flow chart used for selecting the number of SMs in the upper and lower arm. Once an SM is inserted, its capacitor voltage can be predicted for the next sampling period as follows:

$$u_{cj}(k+1) = u_{cj}(k) + \frac{T_s}{C} i_{\text{arm}}(k) S_j(k) \tag{27}$$

where u_{cj} represents the capacitor voltage of jth SM and i_{arm} is the measured arm's current. S_j represents the switching function of jth SM. When the SM is put in, $S_j = 1$, otherwise, $S_j = 0$.

The revised prediction of SM capacitor voltage at k+1 time is defined as

$$\begin{aligned} u_{cj\_new}(k+1) = u_{cj}(k+1) \\ + \text{sign}(i_{\text{arm}}(k)) * (1 - S_j(k)) * \delta \end{aligned} \tag{28}$$

where sign($i_{\text{arm}}(k)$) is a sign function; $\delta \geq 0$is keeping factor.

Once δ is taken into account, the SMs inserted in the current sampling period is still preferentially selected to be put into in the next sampling period. A larger value of δ leads to fewer switching actions between SMs, which in turn leads to lower switching losses. However, The SMs capacitor voltage balancing effect may be affected. Therefore, the value of δ should be considered in a compromise.

D. Fault-Tolerant Schemes for Low-Capacitance Operation

It is highly desirable for MMDTC to maintain uninterrupted normal operation even in the event of SM failures. To achieve this, fault-tolerant operation of MMDTC with a certain amount of redundant SMs is generally necessary. Fault-tolerant methods can be categorized into cold reserve mode and hot reserve mode. In the cold reserve mode, redundant SMs are typically bypassed and only activated when a fault occurs. While this reserve mode results in long charging times for the cold reserved SMs, distorted transient performance, and low SM utilization ratio. The hot reserve mode is preferable as it treats redundant SMs similarly to normal ones, resulting in higher SM utilization ratio and superior transient performance. Thence, the following two fault-tolerant schemes are introduced under the hot reserve mode.

Scheme 1: Once a SM fault occurs in the arm, bypass this failed SM and one healthy SMs in the other arm to achieve the symmetrical operation among both arms.

Scheme 2: Once a SM fault occurs in the arm, only bypass this failed SM. Doing so, the MMDTC needs to operate asymmetrically among both arms.

The proposed control strategy of Fig. 5(c) still can be employed under the aforementioned fault-tolerant schemes. But it is important to note that the capacitor voltage reference value of the remaining SMs need to be adjusted accordingly based on (7), and the search range in both arms in MPC should be adjusted accordingly based on (25), due to changes in the number of SMs.

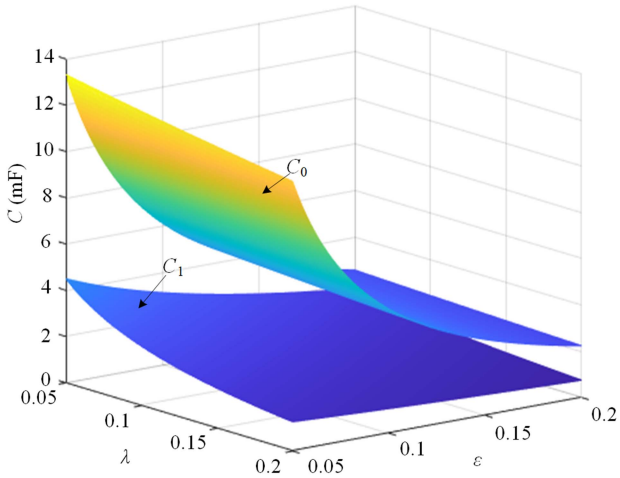
V. Simulation Results

The proposed low-capacitance operation of MMDTC-STATCOM is evaluated based on the circuit parameters presented in Table IV. Under the case of $Q_{\text{rated}} = 10$ MVar, Fig. 7 shows the comparison results of the required capacitance for the proposed and the conventional operation based on (13) and (18). It is noted again that ε only refers to the capacitor voltage ripple ratio for the conventional operation. It can be seen that the required capacitance of the proposed operation is always lower than that of the conventional operation regardless of capacitor voltage ripple ratio ε and filtering inductor voltage drop ratio λ, as shown in Fig. 7(a).

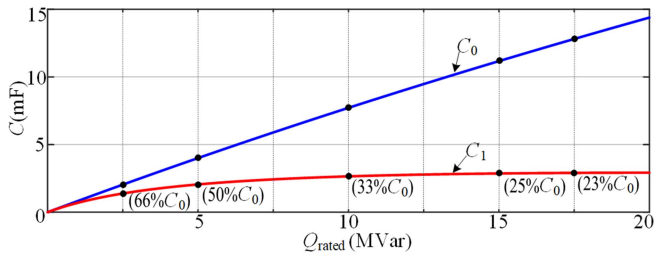
In (13), (18), and (19), the output current I_o and voltage drop ratio λ of filtering inductor can be expressed by the rated reactive

TABLE IV
MAIN PARAMETERS OF SIMULATION

Case	Variable	Symbol	Value
	Rated reactive power	Q_{rated}	0~20 MVar
	Rated line-to-line voltage	V_{line}	10 kV
	Rated grid phase voltage	V_g	$\sqrt{2}V_{\text{line}}/\sqrt{3}$
	Ac filtering inductor	L	2.5 mH
	Voltage ripple ratio	ε	0.08
	Number of SMs per arm	N	18
	Keeping factor	δ	20
When Q_{rated}=10 MVar	Rated amplitude of phase current	I_o	817A
	Voltage drop ratio	λ	0.078
	SM capacitance (conventional operation)	C_0	7.9 mF
	SM capacitance (proposed operation)	C_1	2.6 mF



(a)



(b)

Fig. 7. Comparison of the required capacitance for the conventional operation and the proposed low-capacitance operation. (a) Three-dimensional representation of the variation in capacitance with respect to ε and λ. (b) Reduction in capacitance corresponding to the rated reactive power.

power Q_{rated} as follows:

$$\begin{cases} I_o = \frac{2Q_{\text{rated}}}{3V_g} \\ \lambda = \frac{2\omega L Q_{\text{rated}}}{3V_g^2}. \end{cases} \tag{29}$$

The relationship between the reduction in capacitance and the rated reactive power can be determined by substituting (29) into (19). Once the grid voltage V_g, SM voltage ripple ratio ε, filter inductance L, and the number of SMs per arm are given, the amount of capacitance reduction can be calculated

TABLE V
TECHNICAL PARAMETERS LIST OF ELECTROLYTIC AND FILM CAPACITOR

Technical parameters	ALF80(1)122FP500 (Electrolytic capacitor)	C44UOGT7110M52K (Film capacitor)
Capacitance per unit volume	1.2 mF/166.91 cm³	1.1 mF/1647.82 cm³
Cost per	$19.84	$132.44
Normal voltage	500 V	900 V
Rms current rating	12.44 A	81 A
Operating lifetime	9000 h	200 000 h

Note: Technical parameters are obtained from *https://www.kemet.com* and *https://www.digikey.cn*

TABLE VI
COMPARISON RESULTS OF SM CAPACITOR UNDER CONVENTIONAL AND LOW-CAPACITANCE OPERATION CONDITIONS

	Conventional operation		Low-capacitance operation
Capacitor type	ALF80(1)122FP500 (Electrolytic)	C44UOGT7110M52K (Film)	C44UOGT7110M52K (Film)
Capacitance required	7.9 mF	7.9 mF	2.6 mF
Connection type	Two in series followed by fourteen in parallel	Eight in parallel	Three in parallel
Total Number of capacitors	28	8	3
Total volume	4673.50 cm³	13182.56 cm³	4943.46 cm³
Total cost	$555.52	$1059.52	$397.32

based on (19). Taking the parameters listed in Table IV, as an illustrative example, Fig. 7(b) demonstrates the reduction in capacitance corresponding to the rated reactive power. As seen, the greater the reactive power, the more pronounced the reduction in capacitance value.

When $Q_{\text{rated}} = 10$ MVar, $\lambda = 0.078$ is calculated in Table IV. Assuming $\varepsilon = 0.08$, for the conventional operation, the required capacitance is 7.9 mF and the peak value of SM capacitor voltage should always keep 800 V. While the required capacitance is only 2.6 mF for the proposed low-capacitance operation and the corresponding peak value of SM capacitor voltage is 735 V/800 V in capacitive mode and inductive mode, respectively.

For a more intuitive comparison, an illustrative example is provided below. Taking KEMET company's product as a representative case study, the selected electrolytic and film capacitor parameters are presented in Table V. The comparative results between conventional operation and low-capacitance operation can be found in Table VI. Given that the maximum operating voltage for electrolytic capacitors typically does not exceed 500 V, they need to be connected in series configuration. As indicated by Table VI, under conventional operation conditions, if film capacitors were to directly replace electrolytic ones, there would be a threefold increase in total capacitor volume along with a twofold increase in total capacitor cost incurred. However, under low-capacitance operation condition, the film capacitors exhibit a comparable total volume to that of the electrolytic capacitors under the conventional operation, while achieving a significant reduction of approximately 28% in overall cost.

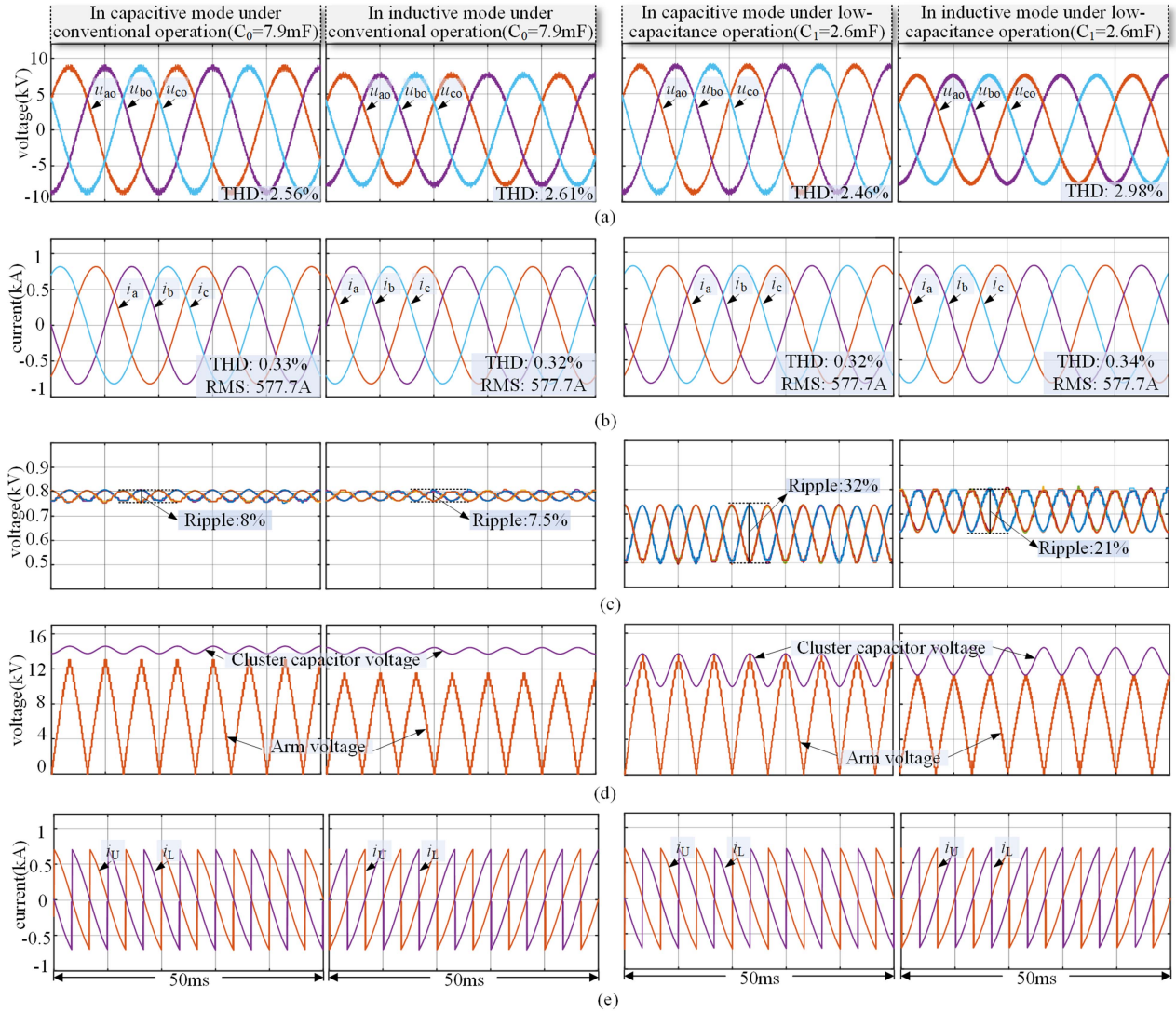


Fig. 8. Simulation results of (a) output phase voltages, (b) output currents, (c) SM capacitor voltages, (d) cluster capacitor voltages and arm voltages, and (e) arm currents in the conventional and proposed low-capacitance operation, respectively.

A. Comparison Between Proposed Low-Capacitance Operation and Conventional Operation

Fig. 8 presents the simulation waveforms including output voltages, output currents, SM capacitor voltage ripples, arm currents for the conventional operation and the low-capacitance operation, respectively. In comparison, regardless of whether operating in capacitive or inductive mode, the proposed low-capacitance operation demonstrates a larger voltage ripple across SM capacitors compared to conventional operation. However, there is minimal impact on the total harmonic distortion (THD) values of output voltages and output currents, as well as arm currents. Fig. 8(d) demonstrates the cluster capacitor voltage and arm voltage, clearly indicating an identical phase in capacitive mode and an opposite phase in inductive mode. These findings provide validation for the capacitor voltage analysis presented in Section III.

B. Comparison Between Proposed Hierarchical Control and Conventional Controls

To verify the steady-state and transient performances of the proposed hierarchical control in low-capacitance operation, a comparative study compared with the double-loop control with multiple PR controllers and MPC with multiple objectives optimization, has been conducted.

1) Steady-State Analysis: The steady-state behavior using the three control methods are investigated in capacitive and inductive modes, as shown in Figs. 9 and 10 (the first 100 ms of the image). In comparison, the output currents are almost the same under the three control methods. However, the SM capacitor voltage-balancing behavior achieved through the MPC is comparatively inferior to the other two control methods. The reason is that the multiobjective optimization pursues a global optimum rather than optimizing each individual control objective separately.

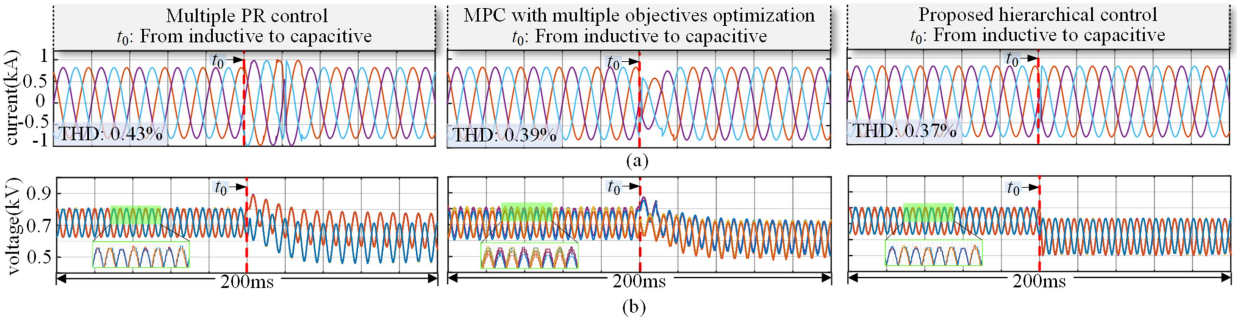


Fig. 9. Steady-state (the first 100 ms of the image) and transient comparison of (a) output currents and (b) SM capacitor voltages using the double-loop control with multiple PR controllers, MPC with multiple objectives optimization, and the propose hierarchical control when changing the reactive current reference from inductive to capacitive.

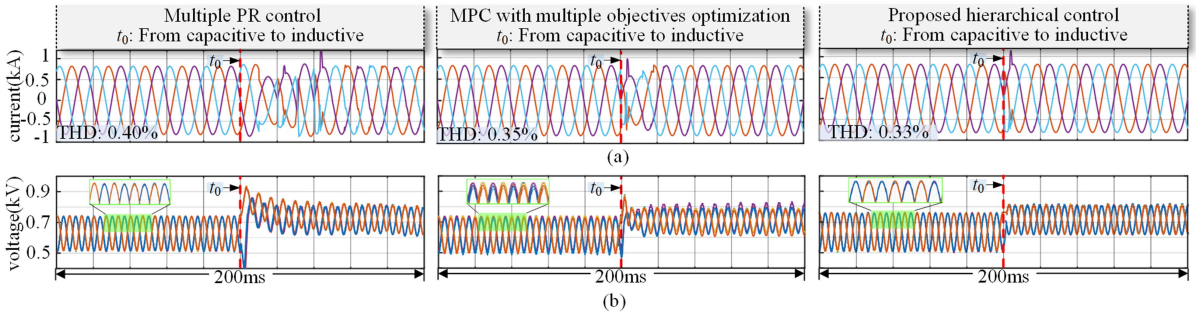


Fig. 10. Steady-state (the first 100 ms of the image) and transient comparison of (a) output currents and (b) SM capacitor voltages using the double-loop control with multiple PR controllers, MPC with multiple objectives optimization, and the propose hierarchical control when changing the reactive current reference from capacitive to inductive.

2) Transient Analysis: To analyze the transient behavior of MMDTC-STATCOM, a step change is applied to the reactive current reference at t_0. As seen from Figs. 9 and 10, the proposed control method demonstrates the smallest overshoot in capacitor voltage and output current during transient conditions, when compared to the other two control methods. This observation suggests that the proposed control method effectively mitigates voltage and current overshoot. Furthermore, the proposed control method exhibits the shortest time required for both capacitor voltage and output current to reach steady-state again, indicating its superior dynamic response.

C. Verification of Fault-Tolerant Schemes

The simulations are conducted to evaluate the fault-tolerant schemes abovementioned when one SM fault occurs. Using Scheme 1, Fig. 11 presents the simulation results of MMDTC, including output currents, phase voltages, SM capacitor voltages, and arm currents. As shown in Fig. 11, the first SM in the upper-arm failed and was bypassed along with the 19th SM in the lower-arm simultaneously. The remaining SMs' capacitor voltage peak values slightly increased but remained well balanced. Furthermore, fault-tolerant operation has minimal impact on output current and voltage waveforms as well as arm currents. Under Scheme 2, the corresponding simulation results are depicted in Fig. 12. It can be observed that following the failure of the first SM in the upper arm, only this faulty SM is bypassed, resulting in an asymmetric operation of MMDTC between both arms. The peak voltage of the lower-arm capacitor remains unaffected after the fault occurrence, while a slight increase in the peak voltage of the upper-arm capacitor. As seen, the output voltages, output currents, and arm currents remain unaffected. Regardless of Scheme 1 or 2, MMDTC exhibits a rapid dynamic response, thereby indicating excellent performance of the proposed control method even in the presence of SM faults.

D. Impact of Keeping Factors δ on SM Switching Frequency

To investigate the impact of different keeping factors δ on the SM switching frequency, a sudden change in keeping factor from 10 to 100 is introduced at time t_0. The resulting changes in output current, SM capacitor voltages, and PWM signals of HBSM1 and HBSM19 within the upper and lower arms are depicted in Fig. 13. It is evident that an increase in keeping factor leads to a decrease in SM switching frequency [see Fig. 13(c)] while leaving the output current unaffected [see Fig. 13(a)]. However, there is a slight degradation observed in the balance of SM capacitor voltages [see Fig. 13(b)].

VI. Experimental Results

The MMDTC-STATCOM has been constructed in a reduced-scale prototype, as depicted in Fig. 14, with its corresponding

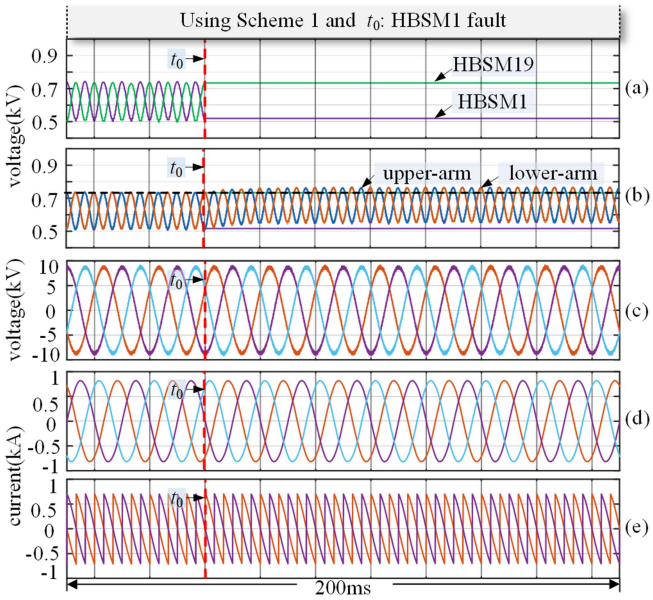


Fig. 11. Fault-tolerant operation waveforms using Scheme 1. (a) Capacitor voltages of HBSM1 and HBSM19. (b) All SM capacitor voltages. (c) Output phase voltages. (d) Output currents. (e) Arm currents.

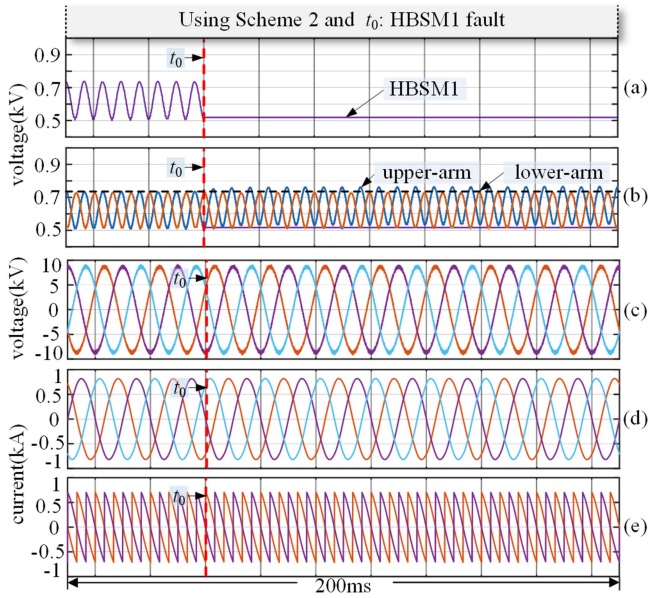


Fig. 12. Fault-tolerant operation waveforms using Scheme 2. (a) Capacitor voltage of HBSM1. (b) All SM capacitor voltages. (c) Output phase voltages. (d) Output currents. (e) Arm currents.

parameters provided in Table VII. The whole control program has been implemented by a Typhoon HIL 402 platform.

A. *Comparison Between Proposed Low-Capacitance Operation and Conventional Operation*

Fig. 15 presents the experimental waveforms including output voltages, output currents, SM capacitor voltages, arm voltages,

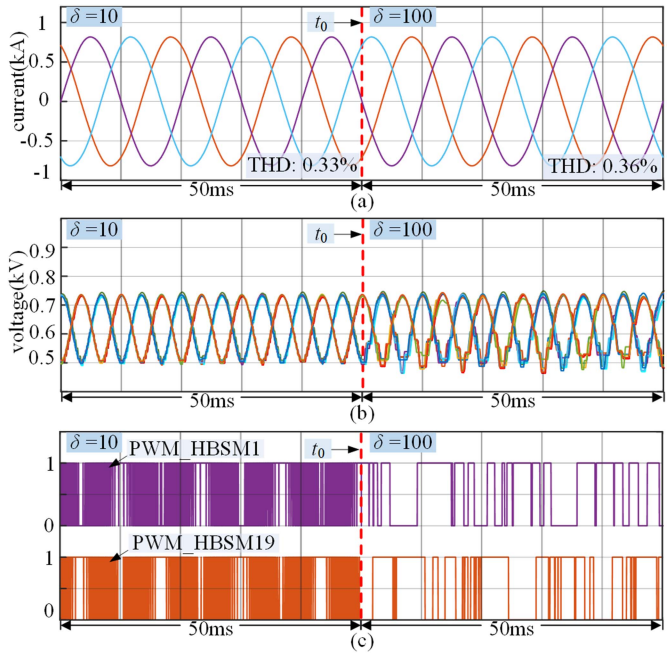


Fig. 13. Simulation results of (a) output currents, (b) SM capacitor voltages, (c) PWM signals of HBSM1 and HBSM19 in the upper arm and lower arm, respectively, when different keeping factors are given.

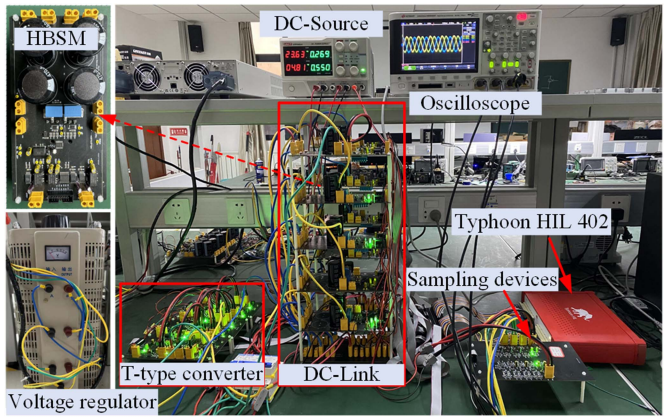


Fig. 14. Photograph of MMDTC-STATCOM prototype.

TABLE VII
MAIN EXPERIMENTAL PARAMETERS

Variable	Symbol	Value
Grid phase voltage	V_g	$110\sqrt{2}$ V
Rated amplitude of phase current	I_o	5 A
Fundamental frequency	f	50 Hz
SM capacitance (conventional operation)	C_0	470 μF
SM capacitance (proposed operation)	C_1	200 μF
Ac filtering inductor	L	10 mH
Number of SMs per arm	N	5
Peak voltage of SM capacitor	U_{c_peak}	55 V
Keeping factor	δ	3

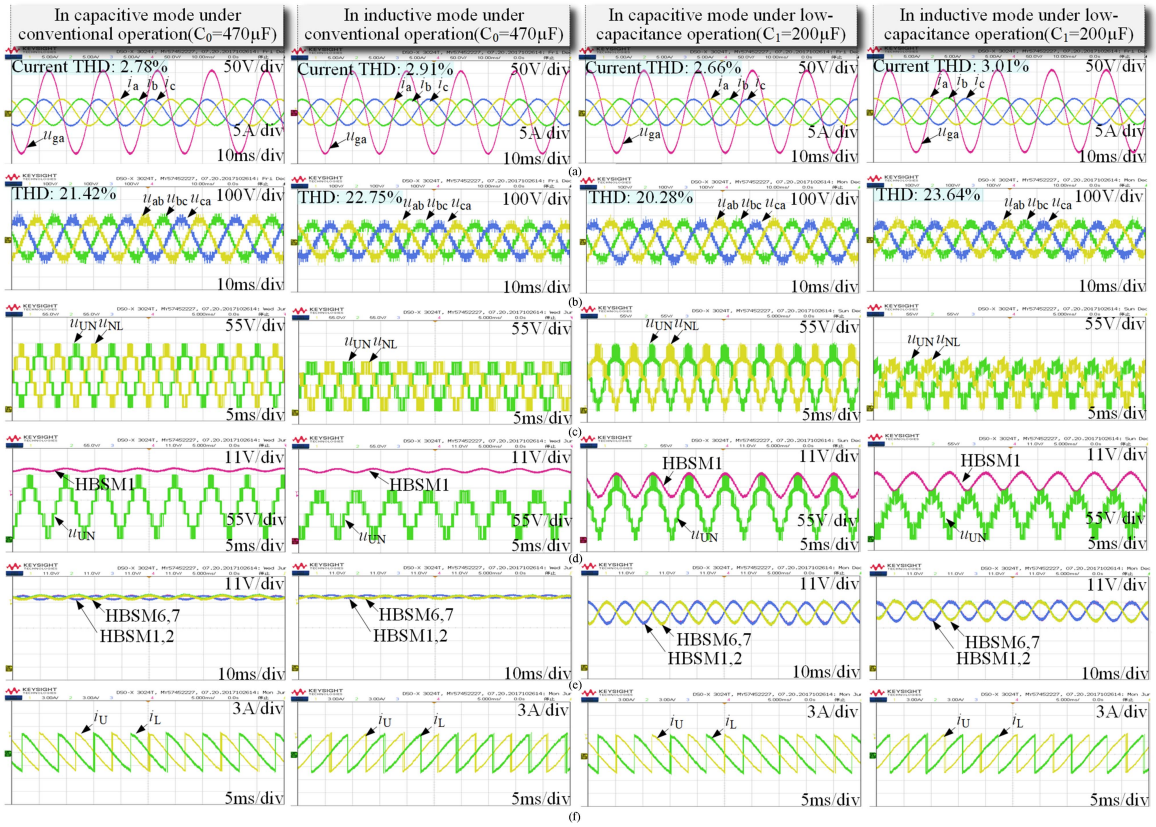


Fig. 15. Experimental results of (a) grid voltage of phase-a and output currents, (b) output line-to-line voltages, (c) output voltages of upper and lower arm, (d) HBSM1 capacitor voltage and output voltage of upper arm, (e) capacitor voltages of HBSM1 ∼ 2 within upper arm, and HBSM6 ∼ 7 within lower arm, and (f) arm currents using the conventional and proposed operation, respectively.

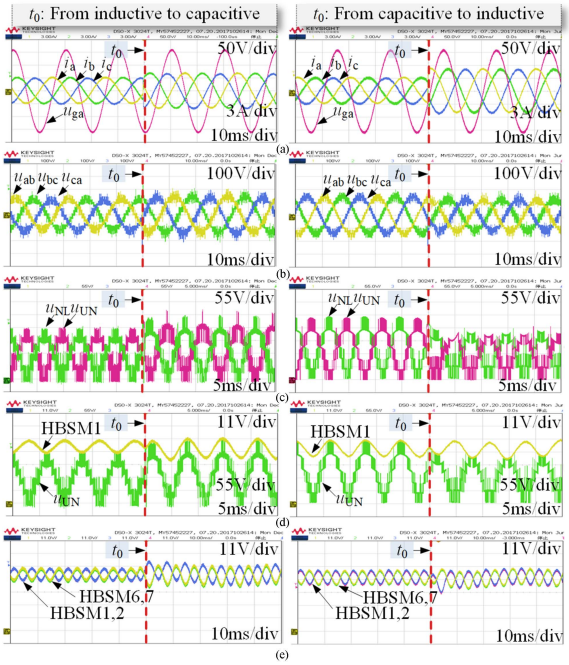


Fig. 16. Experimental results of (a) grid voltage and output currents, (b) output line-to-line voltages, (c) arm voltages, (d) HBSM1 capacitor voltage and upper arm voltage, and (e) capacitor voltages of HBSM1∼2 within upper arm, and HBSM6∼7 within lower arm when changing the reactive current reference from inductive to capacitive and vice versa.

and arm currents for the conventional operation and the low-capacitance operation, respectively. It can be observed that the output current exhibits low THD regardless of that in capacitive mode and inductive mode. The capacitor voltage ripple in capacitive mode is shown to be in phase with the arm voltage, as illustrated in Fig. 15(d). Conversely, the inductive mode exhibits an opposite phase relationship between the capacitor voltage ripple and the arm voltage. Additionally, Fig. 15(e) exhibits well-balanced yet larger ripple SM capacitor voltages, compared to that in conventional operation.

B. Dynamic Response Verification

The proposed hierarchical control strategy is further assessed by abruptly transitioning the reactive current reference from an inductive to a capacitive state, and vice versa. The corresponding experimental results are presented in Fig. 16. The output current can rapidly track its reference value and achieve balanced SM capacitor voltages in both scenarios, thereby indicating the superior dynamic response performance of the proposed control strategy.

VII. Conclusion

This article introduces a new operating approach for MMDTC-STATCOM, which effectively reduces capacitance by leveraging the phase relationship between capacitor voltage and

arm voltage. A qualitative and quantitative analysis is conducted to compare this mode with the conventional operation. To better accommodate the proposed low-capacitance operation, a hierarchical control strategy is presented to overcome the limitations associated with multiple PI (PR) controllers and multiobjective optimization of MPC. This hierarchical control enhances the clarity of respective control objectives and improves control effectiveness, thereby demonstrating superior performance in terms of steady-state and dynamic response through simulation and experimental results.

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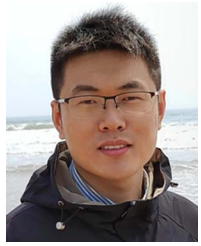

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