Load-Independent Junction Temperature Estimation via Combined TSEPs Modeling for SiC MOSFETs

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***Abstract*—Junction temperature estimation with high precision is crucial to the reliability and safe operating of silicon-carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs). Approaches using temperature-sensitive electrical parameters (TSEPs) are widely employed in the monitoring, offering the benefits of noninvasiveness and fast thermal response. This article proposes a load-independent junction temperature model incorporating three TSEPs, the peak drain voltage ($V_{\mathrm{DS,pk}}$), the peak drain current ($I_{\mathrm{D,pk}}$), and the turn-ON delay time ($t_{\mathrm{d,on}}$). This model eliminates the impact of both load voltage and current, thus improving the estimating accuracy and anti-interference ability compared with other approaches relying on single or fewer TSEPs. Initially, four typical TSEPs and their dependencies on junction temperature and load conditions are established theoretically. Then, the proposed modeling method via combined TSEPs is introduced. Its effectiveness and advantage are experimentally validated with double-pulse tests. Under various loading conditions, the conventional single TSEP method exhibits a mean absolute percentage error of up to 22.56%, whereas the proposed method effectively reduces it to 6.31%.**

***Index Terms*—Condition monitoring, junction temperature, silicon carbide (SiC) MOSFETs, temperature-sensitive electrical parameters (TSEPs).**

I. Introduction

SILICON carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) play a crucial role in advancing aerospace, electric vehicles, and power conversion systems due to their superior performance in high frequency, temperature, and voltage conditions. However, the use of SiC MOSFETs in harsher operating conditions presents challenges to their reliable operation. Overtemperature leads to over 50% of power equipment failures, whereas prolonged and repetitive fluctuation in junction temperature is a primary factor contributing to the fatigue of devices and packaging. This highlights the need for accurate junction temperature (T_{j}) monitoring to ensure the reliability of power devices and converters during lifespan [1]. Accurately measuring the junction temperature is also essential for determining the junction-to-case thermal resistance of power device packages [2].

Methods for the T_{j} measurement can be categorized into four groups: physical measurement, optical measurement, thermal network modeling, and temperature-sensitive electrical parameters (TSEPs). Direct contact methods involve thermocouples or thermistors. In industry, semiconductor device manufacturers integrate NTC thermistors into device packaging to monitor the temperature [3]. However, to achieve tight thermal coupling, thermistors need to be mounted in close proximity to the chip, which exposes thermistors to the risk of high-voltage breakdown; in addition, thermistors can only reflect the temperature at its position, rather than the chip temperature, and their response speed is too slow to reflect the transient temperature variations [4]. Others use chip-integrated temperature sensors to measure the chip temperature [5], which increases the complexity of the chip design and manufacturing process. Moreover, the integration of additional sensors requires additional space on the chip, which reduces the area of the active region and affects the performance and efficiency of the device. Optical methods, through SiC MOSFET diode electroluminescence, provide real-time measurements but damage the device and need a fluorescent coating, limiting the implementation [6]. Thermal network modeling simulates SiC MOSFET heat conduction, offering detailed temperature distribution within the device. However, its accuracy heavily relies on the precision of the model and input parameters [7].

Unlike the methods above, the TSEP method uses an indirect approach, deducing T_{j} by assessing electrical parameters measured externally. Furthermore, the TSEP method allows for instant and nonintrusive temperature monitoring. Previously studied TSEPs include: body diode forward voltage (V_{SD}) [8], turn-ON delay time ($t_{\mathrm{d,on}}$) [9], turn-OFF delay time ($t_{\mathrm{d,off}}$)

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[10], peak drain current ($I_{\mathrm{D,pk}}$) [11], drain current change rate ($dI_{\mathrm{D,on}}/dt$) [12], drain voltage rise time (t_{vr}) [13], drain voltage change rate (dV_{DS}/dt) [14], drain voltage overshoot ($V_{\mathrm{DS,pk}}$) [15], gate current ($I_{\mathrm{G,pk}}$) [16], threshold voltage (V_{th}) [17], conduction voltage drop ($V_{\mathrm{DS,on}}$) [18], and source parasitic inductance voltage drop (V_{ss}) [19]. Online T_{j} measurement typically refers to measuring the junction temperature of power devices when devices are operating normally in the power circuit. Common online TSEPs include: $t_{\mathrm{d,on}}, t_{\mathrm{d,off}}, I_{\mathrm{D,pk}}, dI_{\mathrm{D,on}}/dt, t_{\mathrm{vr}}, dV_{\mathrm{DS}}/dt, V_{\mathrm{DS,pk}}, I_{\mathrm{G,pk}}, V_{\mathrm{DS,on}}, V_{\mathrm{ss}}$, etc. Offline T_{j} measurement refers to measuring the junction temperature of power devices when they are not operating in the power circuit and are usually tested offsite. Common offline TSEPs include: V_{th}, V_{SD}, and internal gate resistance ($R_{\mathrm{G,int}}$). Offline TSEPs, such as V_{SD}, are challenging to be measured during the onsite operation of converters and devices. Therefore, they are rarely used in online junction temperature monitoring systems. However, an estimation model relying on a single TSEP presents limitations in sensitivity, accuracy, and stability under diverse load conditions [20]. In some studies, using multiple TSEPs in modeling is a way to tackle the above issues, for example, the turn-OFF loss and delay time are combined in [21]. Additionally, neural networks have been employed to combine four TSEPs for accuracy and precision enhancement; however, it is hard to implement online [22]. Researchers used regression to combine TSEPs, but load variations variably influence these combined TSEPs [23]. Furthermore, it should be noted that the electrical properties, such as V_{th} and $I_{\mathrm{D,sat}}$, of SiC MOSFETs may exhibit different sensitivity to T_{j} compared to insulated-gate bipolar transistors (IGBTs). This disparity could make some TSEP methods proposed for IGBTs invalidated in SiC MOSFETs application.

To tackle the challenges described above, this study utilizes multiple linear regression (MLR) to establish the relationships among multiple TSEPs, T_{j}, and load conditions, and matrix operations are used to create the load-independent T_{j} estimation model. The estimating accuracy and anti-interference ability can be improved by the proposed modeling method.

The rest of this article is organized as follows. Section II analyzes the temperature and load dependence of TSEPs. Section III describes the proposed modeling method for accurate T_{j} estimation, which decouples the impact of load current and voltage. Experimental results shown in Section IV demonstrate the effectiveness of the model combining $V_{\mathrm{DS,pk}}$, $I_{\mathrm{D,pk}}$, and $t_{\mathrm{d,on}}$, offering outstanding measurement precision compared to other models. Finally, Section V concludes this article.

II. Junction Temperature and Load Conditions Dependence of TSEPs

Fig. 1 shows the physical diagram, equivalent circuit diagram, and chip cross section of the SiC MOSFET. Fig. 1(c) shows the internal parameters of the device, including R_{JFET}, R_{CH}, and C_{GD}, which exert a significant influence on the trend of TSEPs with temperature.

Fig. 2 shows the switching waveform of a typical SiC MOSFET. Given the difficulty in accurately measuring initial values of gate–source voltage (V_{GS}) and drain current (I_{D}), this article defines $t_{\mathrm{d,on}}$ as the interval between the 10% turn-ON transient of V_{GS} (V_{GS1}) and 10% of I_{D} [10]. This interval corresponds to the duration t_0–t_1 shown in Fig. 2. $t_{\mathrm{d,on}}$ can be mathematically expressed using the following equation:

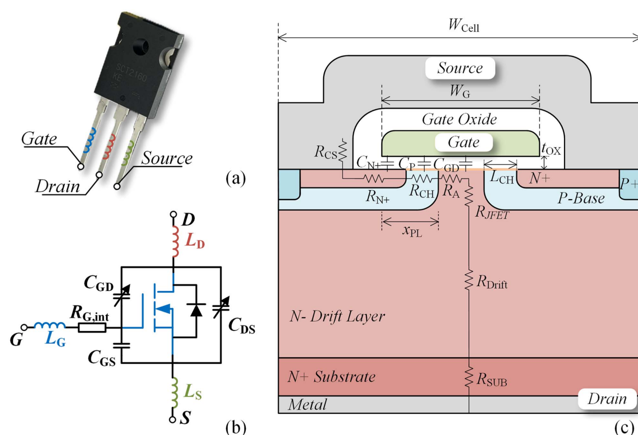

Fig. 1. Schematics of discrete SiC MOSFET. (a) Physical outline. (b) Equivalent circuit. (c) Cross section of the chip structure.

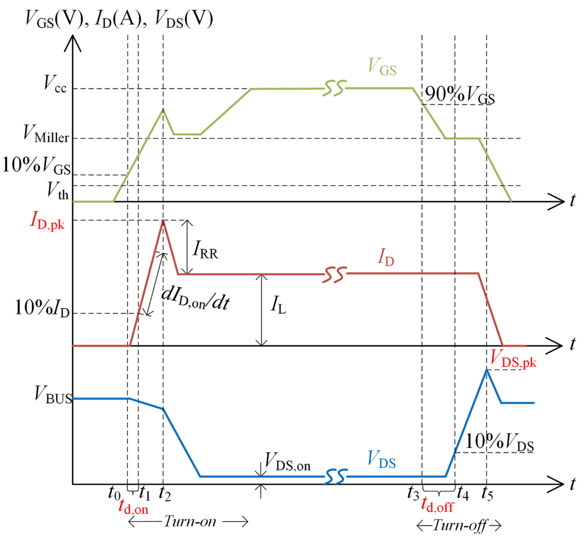

Fig. 2. Typical switching waveforms of SiC MOSFET and definition of parameters.

A. Temperature and Load Dependence of $T_{d,on}$

$$t_{\mathrm{d,on}} = (R_{\mathrm{G,ext}} + R_{\mathrm{G,int}})(C_{\mathrm{GS}} + C_{\mathrm{GD}}(V_{\mathrm{DS}}))\ln\left(\frac{V_{\mathrm{GS1}} - V_{\mathrm{CC}}}{V_{\mathrm{GS2}} - V_{\mathrm{CC}}}\right). \quad (1)$$

where V_{CC} is the drive positive voltage, $R_{\mathrm{G,ext}}$ is the external gate resistor, and V_{GS2} is the matching V_{GS} when I_{D} reaches $10\% I_{\mathrm{D}}$. Temperature minimally impacts $R_{\mathrm{G,ext}}$ while increasing temperatures elevate gate internal resistance ($R_{\mathrm{G,int}}$). The increase in temperature results in an increase in lattice vibration, which in turn causes an increase in the scattering of electrons

as they pass through the material, thereby increasing $R_{\mathrm{G,int}}$. For SiC MOSFETs, $R_{\mathrm{G,int}}$ is found to be positively correlated with T_{j}. Currently, the gate–drain capacitance (C_{GD}) is low but increases with temperature [24], despite the drain voltage nearing V_{BUS}. Temperature does not significantly affect V_{GS1}. Additionally, V_{th} and the rate of drain current change most significantly affect V_{GS2}'s temperature dependence.

Furthermore, V_{BUS} also moderately influences $t_{\mathrm{d,on}}$ [25]. As V_{BUS} increases, $t_{\mathrm{d,on}}$ decreases due to a reduction in C_{GD}.

$$I_{\mathrm{D}}(t) = \mu C_{\mathrm{ox}} \frac{W}{2L}[V_{\mathrm{GS}}(t) - V_{\mathrm{th}}]^2 \quad (2)$$

$$\frac{dI_{\mathrm{D,on}}}{dt} = \mu C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{th}})\frac{V_{\mathrm{CC}}}{R_{\mathrm{G}}} \times e^{-\frac{t}{R_{\mathrm{G}}C_{\mathrm{iss}}}}. \quad (3)$$

where μ is the electron mobility, C_{ox} is the oxide capacitance, and $C_{\mathrm{iss}} = C_{\mathrm{GS}}+C_{\mathrm{DS}}$.

In (2) and (3), the relationship between I_{D} and the rate of change of drain current $dI_{\mathrm{D,on}}/dt$ is described. As the temperature increases, the lattice vibration increases, leading to an increase in electron scattering, which in turn decreases μ. The increase in T_{j} also leads to a narrowing of the bandgap, which increases the intrinsic carrier concentration of the semiconductor, making the channel more susceptible to inversion [12], a decrease in V_{th}, and an increase in $dI_{\mathrm{D,on}}/dt$, with a more rapid rise in the drain current, resulting in a decrease in $t_{\mathrm{d,on}}$.

Practically, I_{L} significantly impacts the $t_{\mathrm{d,on}}$ of SiC MOSFETs. Activating these devices requires injecting charge into the gate to form a conducting channel. With increasing I_{L}, the need for more charge to maintain the channel extends the time needed for the gate drive circuit to deliver the required charge q. Consequently, this results in a slight increase in $t_{\mathrm{d,on}}$, highlighting I_{L}'s direct impact on the operational dynamics of SiC MOSFETs.

B. Temperature and Load Dependence of $T_{d,off}$

This study defines $t_{\mathrm{d,off}}$ as the interval between the turn-OFF transient of V_{GS} decreasing to 90% and V_{DS} increasing to 10%, as illustrated in Fig. 2 (t_3–t_4). This relationship is expressed by

$$t_{\mathrm{d,off}} = (R_{\mathrm{G,ext}} + R_{\mathrm{G,int}})(C_{\mathrm{GS}} + C_{\mathrm{GD}}(V_{\mathrm{DS,on}})) \ln\left(\frac{V_{\mathrm{CC}}}{V_{\mathrm{Miller}}}\right) \quad (4)$$

where V_{Miller} represents the miller plateau voltage during the device's turn-OFF transient. Given SiC MOSFETs' small C_{GD}, the miller plateau typically manifests as a miller ramp. This is expressed by

$$V_{\mathrm{Miller}} = V_{\mathrm{th}} + \sqrt{\frac{I_{\mathrm{L}}L_{\mathrm{CH}}}{\mu C_{\mathrm{ox}}W_{\mathrm{CH}}}}. \quad (5)$$

Channel length (L_{CH}), width (W_{CH}), and I_{L} are crucial in influencing semiconductor device dynamics. The behavior of V_{Miller}, mainly determined by V_{th} [12], is a vital aspect of these dynamics. Specifically, V_{Miller} has a negative temperature coefficient; thus, a higher junction temperature increases $R_{\mathrm{G,int}}$ and C_{GD}, reducing V_{Miller}. This directly results in a prolonged $t_{\mathrm{d,off}}$.

Additionally, $t_{\mathrm{d,off}}$ is responsive to changes in I_{L}. An increase in I_{L} leads to a higher V_{Miller}, inversely affecting $t_{\mathrm{d,off}}$ and resulting in its reduction. Fluctuations in V_{BUS} significantly impact $t_{\mathrm{d,off}}$, with an increase in V_{BUS} extending $t_{\mathrm{d,off}}$ [26].

C. Temperature and Load Dependence of $I_{D,pk}$

In a half-bridge setup, activating the lower SiC MOSFET induces a reverse recovery current via the body diode of the upper MOSFET. This current, added to the lower MOSFET's drain current, results in a significant peak at turn-ON. Fig. 2 shows this phenomenon, marked by the I_{D} value at t_2. Building on this, Zhang et al. [11] analyzed variations in the lower MOSFET's drain voltage, linking them to C_{DS} and the resulting parasitic capacitor current I_{CDS}. This analysis provides a detailed understanding of $I_{\mathrm{D,pk}}$, leading to its expression as shown in the following equation:

$$\begin{aligned} I_{\mathrm{D,pk}} &= I_{\mathrm{L}} + I_{\mathrm{CDS}} + I_{\mathrm{RR}} \\ &= I_{\mathrm{L}} + R_{\mathrm{ON}}C_{\mathrm{DS}}\frac{dI_{\mathrm{D,on}}}{dt} + \sqrt{2Q_{\mathrm{rr}}\frac{dI_{\mathrm{RR}}}{dt}} \end{aligned} \quad (6)$$

where I_{RR} is the reverse recovery current, R_{ON} is the ON-resistance, Q_{rr} is the reverse recovery charge, and dI_{RR}/dt indicates the change rate of I_{RR}. As the device's temperature rises, I_{RR} continuously increases. Concurrently, R_{ON} escalates [27], and $dI_{\mathrm{D,on}}/dt$ increases, together elevating $I_{\mathrm{D,pk}}$.

Additionally, load variations markedly affect $I_{\mathrm{D,pk}}$. The preceding equation shows $I_{\mathrm{D,pk}}$ linearly increases with I_{L}, a pattern also reflected in I_{CDS}. Moreover, a rise in V_{BUS} strengthens the MOSFET's electric field, directly increasing the drain current due to the proportional relationship between the channel's electric field and the drain current [28].

D. Temperature and Load Dependence of $V_{DS,pk}$

During turn-OFF, the device undergoes voltage spikes, mainly due to the swift decrease in I_{D} and the high rate of change ($dI_{\mathrm{D,off}}/dt$) interacting with the circuit's parasitic inductance. Furthermore, dV_{DS}/dt interacting with the circuit's parasitic capacitance intensifies these voltage spikes' amplitude. This phenomenon, including the spike in V_{DS} at t_5, is quantitatively illustrated in the following equation and shown in Fig. 2:

$$V_{\mathrm{DS,pk}} = V_{\mathrm{BUS}} + L_{\mathrm{loop}}\left|\frac{dI_{\mathrm{D,off}}}{dt}\right|. \quad (7)$$

L_{loop} denotes the parasitic inductance existing in the power loop, whereas $dI_{\mathrm{D,off}}/dt$ represents the rate of change of the drain current during turn-OFF. In the half-bridge circuit, L_{loop} consists of the equivalent series inductance (ESL) of the bus capacitor (L_{cap}), the stray inductance of the dc bus (L_{DC}), the drain inductance (L_{D}), and the source inductance (L_{S}) of the device package [20]. During the turn-OFF transient, I_{D} drops rapidly, causing a voltage spike across L_{loop} ($L_{\mathrm{loop}} \cdot dI_{\mathrm{D}}/dt$). This inductive voltage spike, combined with the bus voltage, results in $V_{\mathrm{DS,pk}}$.

Notably, $dI_{\mathrm{D,off}}/dt$ diminishes as the temperature rises [29], thereby endowing $|dI_{\mathrm{D,off}}/dt|$ with a negative temperature coefficient. Consequently, an increase in the device's T_{j} invariably results in a decreased $V_{\mathrm{DS,pk}}$.

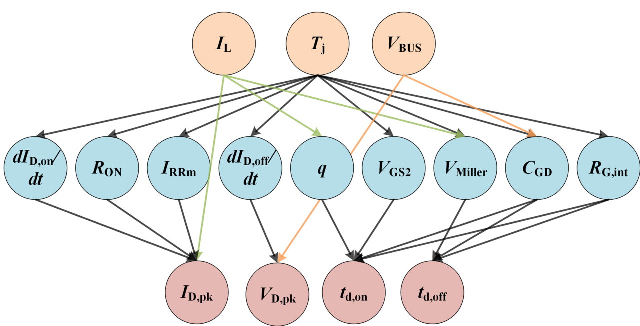

Fig. 3. Dependencies of typical TSEPs, T_j, and load conditions.

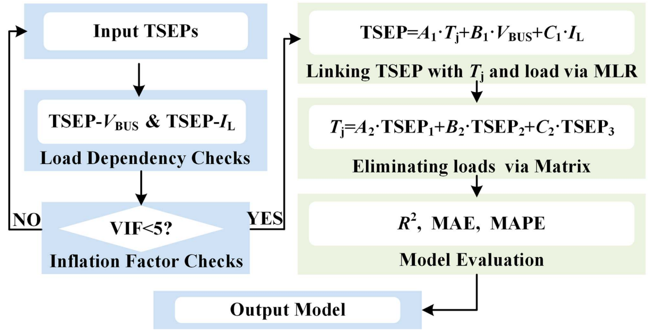

Fig. 4. Flowchart of proposed load-independent T_j modeling method.

The equation reveals that $V_{\mathrm{DS,pk}}$ is directly proportional to V_{BUS}. Additionally, during turn-OFF, an increased I_{L} requires the device under test (DUT) to interrupt a larger current in a shorter timeframe. This scenario precipitates a heightened rate of current change, meaning $|dI_{\mathrm{D,off}}/dt|$ experiences an increase. Fig. 3 shows the complex dependencies among certain TSEPs, junction temperature, and load conditions.

III. Proposed Junction Temperature Estimation Method

Traditional TSEP methods rely on a single parameter for estimation, showing limited capability of anti-interference. To develop an accurate and reliable junction temperature model, this study utilizes MLR to create a linear equation that connects multiple independent variables to a dependent variable, establishing the relationship among TSEPs, T_{j}, and load conditions. Furthermore, the matrix operations are used to eliminate the impact of load conditions to create the load-independent model. Fig. 4 shows a flowchart of the proposed modeling method.

After experimentally investigating the temperature-dependent switching characteristics of SiC MOSFETs, proper TSEPs need to be selected for modeling. First, in the load dependency checks section, the relationship between TSEPs and load voltage and current is analyzed using mathematical models (1), (4), (6), and (7), with the results verified through double-pulse experiments. Subsequently, the variance inflation factor (VIF) is calculated for different combinations of TSEPs to evaluate potential multicollinearity as shown in the following equation:

$$\mathrm{VIF}_i = \frac{1}{1 - R_i^2} \tag{8}$$

where R_i^2 denotes the coefficient of determination derived from regressing the i variable against the others. In particular, multicollinearity is characterized by the significant interdependence among predictors within a regression model. When multicollinearity is present in a model, even small changes in the data can result in significant fluctuations in the parameter estimates [30]. A higher VIF value indicates a significant influence of the independent variables on each other, flagging a potential collinearity problem within the model. Therefore, VIF checks can be employed to ascertain whether the TSEPs exert influence upon one another. A VIF value between 1 and 5 is considered acceptable, whereas a VIF above 5 indicates a significant collinearity problem [31]. This issue can lead to interactions among the independent variables, potentially compromising the accuracy of T_{j} measurements due to the interplay among some TSEPs. Hence, it is imperative to check VIF when selecting TSEPs for combination in modeling.

Due to the different units across TSEPs, normalization of independent variables is crucial to standardize data scales, improving the model's ability to understand feature interrelations and increasing the accuracy of prediction. After normalization, MLR is used to delineate the relationship among TSEPs, load voltage and current, and T_{j}, as shown in the following equation:

$$TSEP = a \cdot T_{\mathrm{j}} + b \cdot I_L + c \cdot V_{\mathrm{BUS}} + d. \tag{9}$$

Taking the TSEPs combination of $V_{\mathrm{DS,pk}}$-$I_{\mathrm{D,pk}}$-$t_{\mathrm{d,on}}$ as an example, matrix operations are used to mitigate load influences, as detailed in the following equations:

$$\begin{bmatrix} V_{\mathrm{DS,pk}} \\ I_{\mathrm{D,pk}} \\ t_{\mathrm{d,on}} \end{bmatrix} = \begin{bmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{bmatrix} \begin{bmatrix} T_{\mathrm{j}} \\ I_{\mathrm{L}} \\ V_{\mathrm{BUS}} \end{bmatrix} + \begin{bmatrix} \beta_1 \\ \beta_2 \\ \beta_3 \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} T_{\mathrm{j}} \\ I_{\mathrm{L}} \\ V_{\mathrm{BUS}} \end{bmatrix} = \begin{bmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{bmatrix}^{-1} \begin{bmatrix} V_{\mathrm{DS,pk}} \\ I_{\mathrm{D,pk}} \\ t_{\mathrm{d,on}} \end{bmatrix} - \begin{bmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{bmatrix}^{-1} \begin{bmatrix} \beta_1 \\ \beta_2 \\ \beta_3 \end{bmatrix} \tag{11}$$

$$T_{\mathrm{j}} = \alpha \cdot V_{\mathrm{DS,pk}} + \beta \cdot I_{\mathrm{D,pk}} + \gamma \cdot t_{\mathrm{d,on}} + \epsilon. \tag{12}$$

Therefore, (12) derives a combined T_{j} estimation model, created using MLR and matrix operations, that is independent of load conditions of I_{L} and V_{BUS} variations. By combining three specific TSEPs into the model, the estimation accuracy can be improved compared with methods using a single TSEP, meanwhile, the load impact can be eliminated to enhance the capability of anti-interference. Detailed validation and evaluation of this model are presented in the next section.

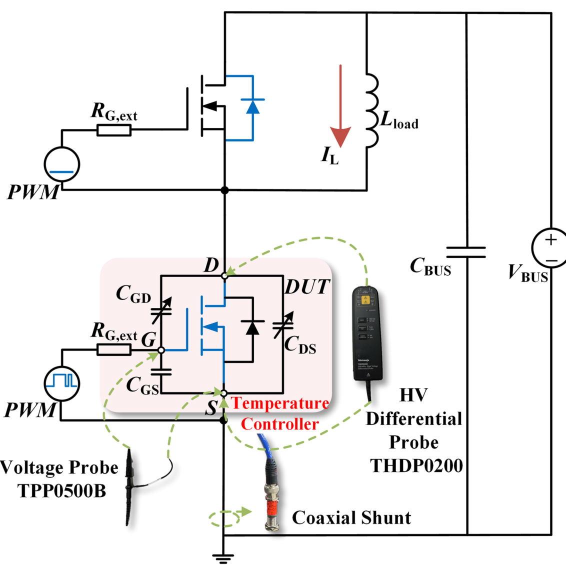

Fig. 5. Circuit diagram of the double-pulse test.

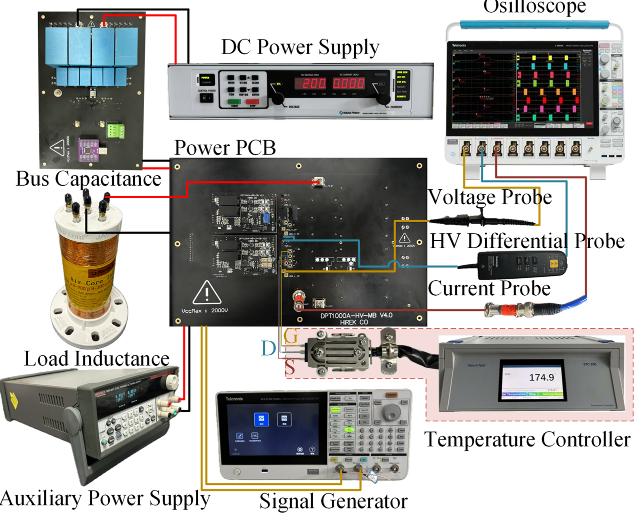

Fig. 6. Double-pulse test platform.

IV. Experimental Setup for Verification

A. Experimental Setup

To evaluate the dynamic behaviors of SiC MOSFETs under various junction temperatures and load conditions, experiments were carried out on a double-pulse test platform. The circuit of the test platform and instruments are shown in Figs. 5 and 6.

The 1200 V/22 A SiC MOSFET SCT2160KE manufactured by Rohm was used as the DUT. To characterize the DUT over various temperatures, a heating fixture was utilized to heat the DUT. Heating for at least 10 min is necessary to ensure the device reaches thermal equilibrium [16]. During tests, T_j was set to 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, 150 °C, and 175 °C, respectively. Alongside T_j, this study also examined how load voltage and current conditions influence the characteristics of SiC MOSFETs and their TSEPs. To evaluate the impact of V_{BUS},

TABLE I
Key Specifications of the DUT and Test Conditions

Parameter	Value
SiC MOSFET	SCT2160KE
DUT voltage rating	1200 V
DUT current rating	22 A
DUT ON-resistance R_{ON}	160 mΩ
DUT internal gate resistance $R_{G,int}$	13.7 Ω
Gate resistance $R_{G,ext}$	2.2 Ω
Gate driving voltage V_{CC}/V_{EE}	+18 V / 0 V
Tested bus voltage range V_{BUS}	200–800 V
Tested load current range I_L	5–20 A
Tested junction temperature T_j	25–175°C
DC-link capacitance	190 μF
Load inductance	200 μH

TABLE II
Information of Experimental Instrument

Instrument	Part number	Measurement
HV differential probe	Tektronix THDP0200	V_{DS}
Voltage probe	TektronixTPP0500B	V_{GS}
Current probe	SSDN-414-01	I_D
Osilloscope	TekTronix MSO58B	-
DC power supply	MAGNA-XR2000-1	-
Auxiliary power supply	KEITHLEY-2220-30	-
Temperature Controller	ETC-200	-
Thermocouple	TM-902C	T_j
Signal generator	Tektronix AFG31000	-

I_L was kept at 10 A, whereas V_{BUS} gradually increased from 200 to 800 V in 200 V increments. To evaluate the impact of I_L, V_{BUS} remained at 600 V, whereas I_L increased from 5 to 20 A in 5 A increments.

Table I summarizes key specifications of the DUT and test conditions. In terms of measurement, V_{GS} was measured by a single-ended probe, V_{DS} was measured by a high-voltage differential probe, and I_D was measured by a coaxial shunt resistor. Table II lists instruments applied on the double-pulse test platform. The dc power supply provides the load voltage, the auxiliary power supply powers the driver board, and the signal generator sends pulsewidth modulation (PWM) signals to the gate driver. A temperature controller with a heating fixture is used to heat the DUT with a K-type thermocouple attached to the thermal pad of the DUT to measure the actual temperature as a reference.

B. Analysis of Experimental Results

Figs. 7–9 show the SiC MOSFETs' switching waveforms under various temperature and load conditions. Specifically, Figs. 7(a), 8(a), and 9(a) illustrate the DUT's turn-ON waveforms at V_{BUS} /I_L conditions of 200 V/10 A, 600 V/10 A, and 600 V/20 A, respectively, whereas Figs. 7(b), 8(b), and 9(b) present the turn-OFF waveforms. For all tests, T_j varies between 25 °C and 175 °C with 25 °C steps. It can be seen that for all load conditions, an increase in temperature leads to a slight decrement in $t_{d,on}$, and a rise in the slope of I_D and $I_{D,pk}$ during the turn-ON

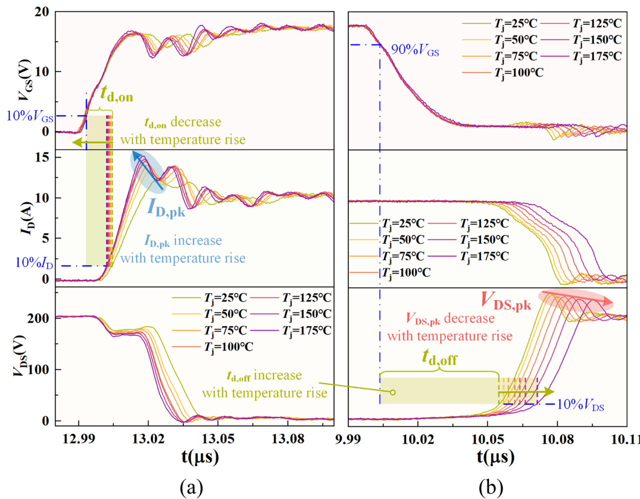

Fig. 7. Experimental waveforms of SiC MOSFET under $V_{\mathrm{BUS}} = 200$ V, $I_{\mathrm{L}} = 10$ A at temperatures ranging from 25 °C to 175 °C. (a) Turn-ON waveform. (b) Turn-OFF waveform.

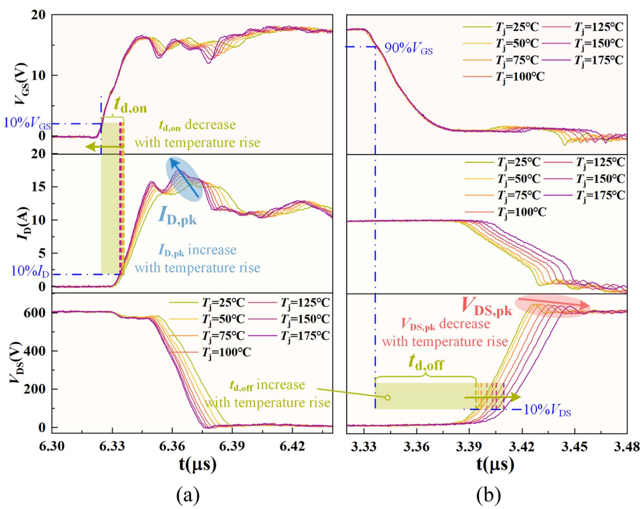

Fig. 8. Experimental waveforms of SiC MOSFET under $V_{\mathrm{BUS}} = 600$ V, $I_{\mathrm{L}} = 10$ A at temperatures ranging from 25 °C to 175 °C. (a) Turn-ON waveform. (b) Turn-OFF waveform.

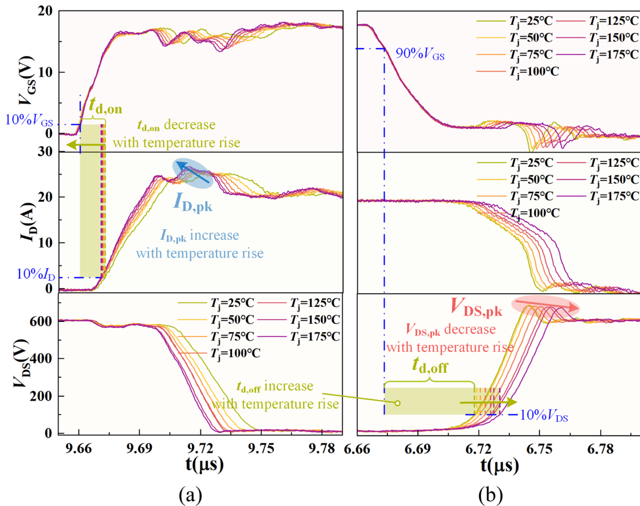

Fig. 9. Experimental waveforms of SiC MOSFET under $V_{\mathrm{BUS}} = 600$ V, $I_{\mathrm{L}} = 20$ A at temperatures ranging from 25 °C to 175 °C. (a) Turn-ON waveform. (b) Turn-OFF waveform.

transition. For the turn-OFF transition, a significant delay in $t_{\mathrm{d,off}}$ and decrease in the slope of V_{DS} and $V_{\mathrm{DS,pk}}$ can be observed.

Moreover, results in Figs. 7 and 8 present that with the elevation in V_{BUS} from 200 to 600 V, a substantial rise in $V_{\mathrm{DS,pk}}$ is obvious, and both $t_{\mathrm{d,on}}$ and $t_{\mathrm{d,off}}$ have minor reduction due to the change of C_{iss} introduced by the increasing V_{BUS} applied on the DUT. Comparing Figs. 8 and 9, it can be seen that increasing I_{L} to 20 A ascends V_{Miller}, leading to a shorter $t_{\mathrm{d,off}}$. Conversely, $V_{\mathrm{DS,pk}}$ and $I_{\mathrm{D,pk}}$ all exhibit a significant rise with a higher I_{L}. The impact of load voltage and current conditions on TSEPs coincides with the theoretical analysis presented in Section II.

Based on tested waveforms, parameter features under various temperature and load conditions are extracted and concluded in Fig. 10. Specifically, from Fig. 10(a) and (b), it can be seen that $I_{\mathrm{D,pk}}$ is positively correlated with T_{j} and load current and voltage, and from Fig. 10(b), it can be seen that the linearity of $I_{\mathrm{D,pk}}$ with T_{j} is poor when $V_{\mathrm{BUS}} = 200$ V. In Fig. 10(c), it can be observed that an increase in I_{L} results in an increase in $t_{\mathrm{d,on}}$. Similarly, in Fig. 10(d), increments in T_{j} and V_{BUS} both lead to a decrease in $t_{\mathrm{d,on}}$. In Fig. 10(e), the amplitude of the change in $V_{\mathrm{DS,pk}}$ is approximately 10 V even when T_{j} is increased from 25 °C to 175 °C at different I_{L}. In Fig. 10(f), $V_{\mathrm{DS,pk}}$ increases significantly with an increase in V_{BUS}. Despite the relatively small amplitude of the change in $V_{\mathrm{DS,pk}}$ with T_{j} in comparison to the amplitude of $V_{\mathrm{DS,pk}}$ itself, it is still possible to observe that $V_{\mathrm{DS,pk}}$ tends to decrease slowly with increasing temperature. In Fig. 10(g), $t_{\mathrm{d,off}}$ decreases with increasing I_{L}, which is caused by the positive correlation between V_{Miller} and I_{L}. In Fig. 10(h), the increase in V_{BUS} causes a small increase in $t_{\mathrm{d,off}}$. $t_{\mathrm{d,off}}$ increases linearly with increasing temperature. Concurrently, the absolute temperature sensitivities of the three TSEPs undergo a transformation when I_{L} is elevated from 5 to 20 A. The sensitivity of $I_{\mathrm{D,pk}}$ declines from 17.43 to 7.58 mA/°C. The absolute sensitivity of $t_{\mathrm{d,on}}$ increases from 7.93 to 12.81 ps/°C, and the absolute sensitivity of $V_{\mathrm{DS,pk}}$ increases from 70.51 to 75.22 mV/°C. The sensitivity of $t_{\mathrm{d,off}}$ declines from 130.13 to 101.33 ps/°C. Upon increasing V_{BUS} from 200 to 800 V, the sensitivity of $I_{\mathrm{D,pk}}$ decreased from 18.92 mA/°C to 11.31 mA/°C, and the absolute sensitivity of $t_{\mathrm{d,on}}$ increased from 9.53 to 12.72 ps/°C. The absolute sensitivity of $V_{\mathrm{DS,pk}}$ decreased from 84.54–79.72 mV/°C. The sensitivity of $t_{\mathrm{d,off}}$ increases from 96.10 to 106.67 ps/°C. Therefore, when measuring T_{j} of SiC MOSFETs by the TSEP method, it is necessary to eliminate the effects of V_{BUS} and I_{L} on parameters to ensure accurate T_{j} measurement.

Table III shows the VIF checking results of three different combinations of typical TSEPs, including $I_{\mathrm{D,pk}}$, $V_{\mathrm{DS,pk}}$, $t_{\mathrm{d,on}}$, and $t_{\mathrm{d,off}}$. The VIF1 to VIF3 represent the first to third parameter in the combination, respectively. Commonly, a VIF below 5 indicates no significant collinearity problems among parameters. However, in the combination ($I_{\mathrm{D,pk}}$-$t_{\mathrm{d,on}}$-$t_{\mathrm{d,off}}$), the VIFs

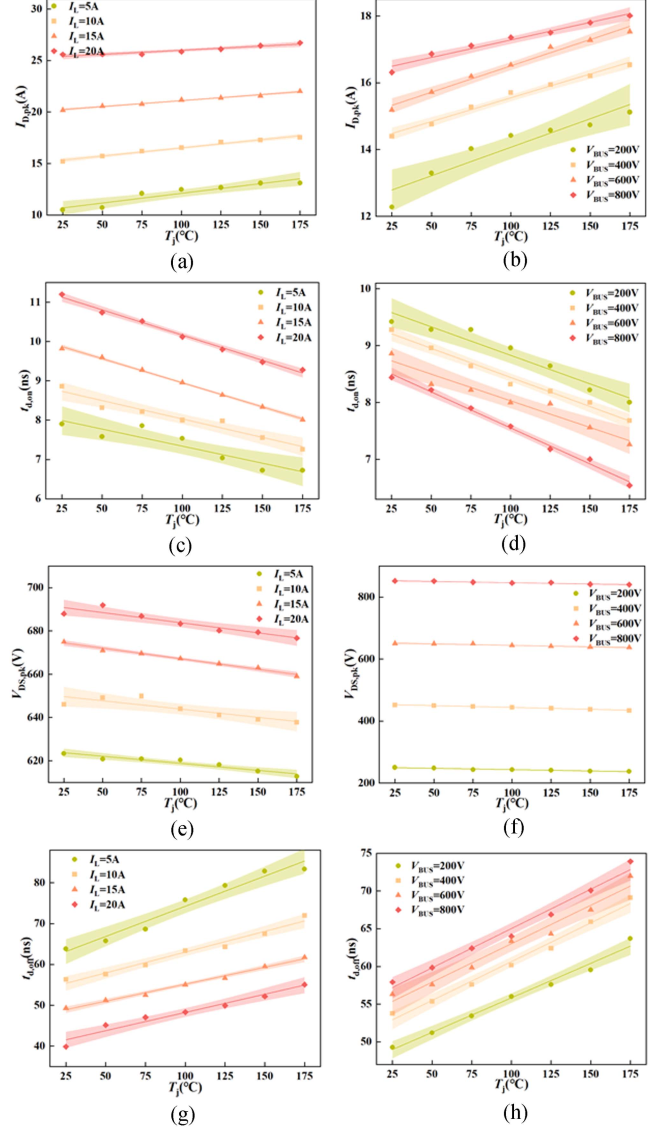

Fig. 10. Relationship of TSEPs with temperature and load conditions. (a) $I_{\mathrm{D,pk}}$-T_{j}-I_{L}. (b) $I_{\mathrm{D,pk}}$-T_{j}-V_{BUS}. (c) $t_{\mathrm{d,on}}$-T_{j}-I_{L}. (d) $t_{\mathrm{d,on}}$-T_{j}-V_{BUS}. (e) $V_{\mathrm{DS,pk}}$-T_{j}-I_{L}. (f) $V_{\mathrm{DS,pk}}$-T_{j}-V_{BUS}. (g) $t_{\mathrm{d,off}}$-T_{j}-I_{L}. (h) $t_{\mathrm{d,off}}$-T_{j}-V_{BUS}.

TABLE III
VARIANCE INFLATION FACTOR OF DIFFERENT TSEPS COMBINATIONS

Combined TSEPs	VIF1	VIF2	VIF3
$V_{\mathrm{DS,pk}}$-$I_{\mathrm{D,pk}}$-$t_{\mathrm{d,on}}$	2.41	1.63	2.07
$I_{\mathrm{D,pk}}$-$t_{\mathrm{d,on}}$-$t_{\mathrm{d,off}}$	1.51	7.86	7.49
$I_{\mathrm{D,pk}}$-$t_{\mathrm{d,off}}$	1.94	1.85	–

corresponding to $t_{\mathrm{d,on}}$ and $t_{\mathrm{d,off}}$ exceed 7, indicating potential interactions. This interaction necessitates careful consideration when selecting TSEPs combination to ensure the accuracy and fitting of the T_{j} estimation model.

After VIF checking, normalization is employed to unify the different scales of TSEPs, which facilitates the analysis of each variable's weight in the model. Following normalization, MLR is applied to model the relationship among TSEPs, load conditions, and T_{j}. The following equations can be derived for the $V_{\mathrm{DS,pk}}$-$I_{\mathrm{D,pk}}$-$t_{\mathrm{d,on}}$ combination:

$$I_{\mathrm{D,pk}} = 0.0009T_{\mathrm{j}} + 0.8705I_{\mathrm{L}} + 0.1852V_{\mathrm{BUS}} - 0.1330 \quad (13)$$

$$V_{\mathrm{DS,pk}} = -0.0001T_{\mathrm{j}} + 0.1049I_{\mathrm{L}} + 0.9794V_{\mathrm{BUS}} - 0.0122 \quad (14)$$

$$t_{\mathrm{d,on}} = -0.0023T_{\mathrm{j}} + 0.6258I_{\mathrm{L}} - 0.2707V_{\mathrm{BUS}} - 0.5284. \quad (15)$$

Then, the influence of V_{BUS} and I_{L} can be mitigated through matrix operations. Eventually, a T_{j} estimation model unaffected by V_{BUS} and I_{L} variations is derived as

$$T_{\mathrm{j}} = 253.63I_{\mathrm{D,pk}} - 139.03V_{\mathrm{DS,pk}} - 329.49t_{\mathrm{d,on}} + 206.14. \quad (16)$$

C. Junction Temperature Models Evaluation

The proposed T_{j} estimation modeling method based on multi-TSEPs is evaluated by comparing it with the conventional model based on a single TSEP. Additionally, the model incorporating two TSEPs, aimed at negating I_{L}'s influence, is compared with the proposed model. Each temperature model's robustness and interpretability are assessed by the coefficient of determination R^2, where a higher R^2 value indicates an enhanced ability to account for T_{j} variations. Considering the constant variations in load conditions in practical applications of devices, the mean absolute percentage error (MAPE) and mean absolute error (MAE) are calculated to quantify the prediction errors of models. These facilitate a comprehensive evaluation of model accuracy, allowing for direct comparison under standardized conditions.

Fig. 11 compares T_{j} predicted results of the traditional model, double TSEPs model, and proposed model under different load conditions varying between 200 and 800 V and 5 and 20 A. The traditional models, as shown in Fig. 11(a), exhibit significant discrepancies between predicted and actual T_{j}, with maximum error reaching nearly 65°C when the actual T_{j} is 25°C. In contrast, the proposed model shown in Fig. 11(d) illustrates good alignment between the predicted and actual T_{j}. The double TSEPs model is shown in Fig. 11(b). A comparison of the prediction results of the double TSEPs model with the effect of I_{L} eliminated to those of Fig. 11(a) reveals that the former is closer to the actual values, particularly under 25°C–75°C. This indicates that the load current affects the prediction results of the junction temperature model. Fig. 11(c) shows T_{j} prediction outcomes of the model combining three TSEPs via the proposed approach, but the VIF check failed (VIF>5, cf., Table III). Fig. 11(c) shows that, despite the elimination of load conditions, the prediction result of T_{j} model with multi-TSEPs remains unsatisfactory when VIF>5. Therefore, it is worth pointing out the importance of VIF checks when selecting TSEPs for modeling. Fig. 11(d) shows that when the VIF among the TSEPs combination remains below 5, the prediction error is notably improved, demonstrating the importance of managing covariance among TSEPs in modeling for accurate T_{j} estimation. All results shown above prove the substantial improvement in prediction accuracy and capability to eliminate load impacts.

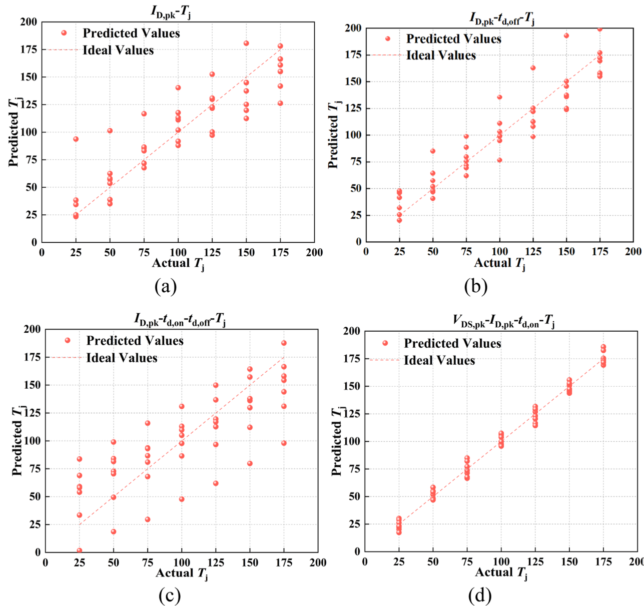

Fig. 11. Comparison of T_j predicted results of single TSEP model, double TSEPs model, and proposed model under $V_\mathrm{BUS} = 200$–800 V, $I_\mathrm{L} = 5$–20 A. (a) $I_\mathrm{D,pk}$-T_j. (b) $I_\mathrm{D,pk}$-$t_\mathrm{d,off}$-T_j. (c) $I_\mathrm{D,pk}$-$t_\mathrm{d,on}$-$t_\mathrm{d,off}$ -T_j. (d) $V_\mathrm{DS,pk}$-$I_\mathrm{D,pk}$-$t_\mathrm{d,on}$-T_j (proposed).

TABLE IV
JUNCTION TEMPERATURE MODEL EVALUATION RESULTS

Model	Fitting degree R^2	MAE (in°C)	MAPE
$V_\mathrm{DS,pk}$-$I_\mathrm{D,pk}$-$t_\mathrm{d,on}$-T_j (Proposed)	97.01%	4.49	6.31%
$I_\mathrm{D,pk}$ -$t_\mathrm{d,on}$-$t_\mathrm{d,off}$-T_j (VIF check failed)	64.06%	24.38	39.99%
$I_\mathrm{D,pk}$ -$t_\mathrm{d,off}$-T_j	89.87%	11.85	16.12%
$I_\mathrm{D,pk}$-T_j	81.80%	15.47	22.56%

Table IV provides a comparative analysis of T_j models developed by the proposed method and other methods. A model using a single TSEP of $I_\mathrm{D,pk}$ records a significant divergence of estimation results under fluctuating V_BUS and I_L conditions, showing only 81.8% fitting degree. The model's MAE and MAPE stand at 15.47°C and 22.56%, respectively, underlining the significant impact of load conditions on T_j predictions and highlighting its restricted capability to account for interference in real applications. The $I_\mathrm{D,pk}$-$t_\mathrm{d,off}$-T_j model with I_L's impact eliminated reduces the MAE by about 4°C and the MAPE by about 6% compared to the traditional single-TSEP model. This indicates that the removal of I_L may facilitate more accurate predictions of T_j model. Additionally, for the $I_\mathrm{D,pk}$-$t_\mathrm{d,on}$-$t_\mathrm{d,off}$-T_j model in the event of a failed VIF check, only 64.06% of R^2 is reached with MAE of 24.38°C and MAPE of 39.99%, although the impact of V_BUS and I_L can be removed in modeling. This result is expected and demonstrates the importance of VIF verification before selecting TESPs for combination.

Notably, the $V_\mathrm{DS,pk}$-$I_\mathrm{D,pk}$-$t_\mathrm{d,on}$-T_j model represents a significant advancement, with a 97.01% fit rate. This high fit rate indicates its competency in capturing the nuances of T_j variations, with an MAE of 4.49°C and a MAPE of 6.31% after adjusting for

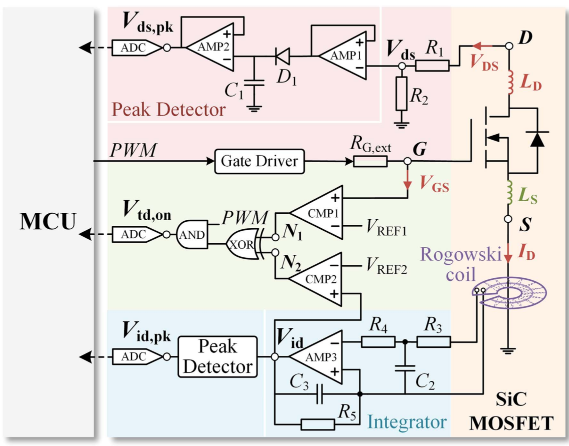

Fig. 12. Online detection circuit of the proposed method.

V_BUS and current effects. This model addresses the critical issue overlooked by conventional models—the pronounced impact of load variations on T_j predictions.

In conclusion, through rigorous comparison and analysis, the proposed model exhibits marked superiority in predicting T_j with high accuracy, particularly after accounting for variations in V_BUS and I_L. This achievement holds significant implications for the thermal management and reliability evaluation of SiC MOSFETs in future applications.

V. DISCUSSION ON ONLINE IMPLEMENTATION

In this section, a reference design regarding the implementation of the proposed method for online T_j measurement applications is given. The design incorporates detection circuits for multiple TSEPs ($V_\mathrm{DS,pk}$, $t_\mathrm{d,on}$, and $I_\mathrm{D,pk}$), as shown in Fig. 12, ensuring accurate and continuous T_j estimation for SiC MOSFETs.

In Fig. 12, the detection circuit can be divided into three parts. The first part is $V_\mathrm{DS,pk}$ measurement, where a resistive voltage divider (R_1, R_2) scales down V_DS proportionally to V_ds. A peak detector then captures the peak value of V_ds ($V_\mathrm{ds,pk}$), which consists of two operational amplifiers (AMP1, AMP2), a capacitor (C_1), and a diode (D_1) [16]. C_1 stores the maximum value of V_ds and D_1 sets the direction of the current. The second part is $I_\mathrm{D,pk}$ measurement. A Rogowski coil can be used to convert the current signal into a voltage signal (V_coil) and then integrate it into a voltage signal (V_id), which is proportional to I_D [32]. The peak value of V_id ($V_\mathrm{id,pk}$) is then captured by a peak detector, which can be used to calculate out $I_\mathrm{D,pk}$. The expressions for V_coil and V_id are given in the following equations [33]:

$$V_\mathrm{coil}(t) = K\frac{dI_\mathrm{D}(t)}{dt} \tag{17}$$

$$V_\mathrm{id} = \int V_\mathrm{coil}(t)\cdot dt = \int K\frac{dI_\mathrm{D}(t)}{dt}\cdot dt = K\cdot I_\mathrm{D} \tag{18}$$

where K is the proportionality constant.

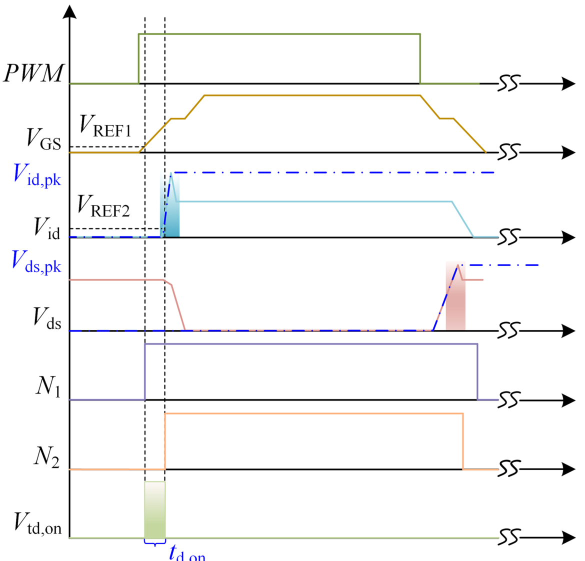

Fig. 13. Simplified waveforms of the TSEPs detection circuit.

The third part involves $t_{d,on}$ measurement. The V_{GS} signal is sent to comparator CMP1 to check the point of 10% of V_{GS}. Similarly, V_{id} is sent to comparator CMP2 to obtain 10% of V_{id}. Outputs of N_1 and N_2 are processed through an XOR gate and then an AND gate with a PWM signal to produce a voltage signal ($V_{td,on}$) with a pulsewidth equal to $t_{d,on}$. The AND gate is designed to prevent the false occurrence of a high level of $V_{td,on}$ during the turn-OFF transient of the SiC MOSFET.

Fig. 13 shows the simplified waveforms of the detection circuits for TSEPs. During the device turn-ON transient, N_1 switches to a high level after V_{GS} reaches V_{REF1}, and N_2 switches to a high level when V_{id} rises to V_{REF2}. N_1 and N_2 are processed through the XOR gate and AND gate with PWM to produce $V_{td,on}$. V_{id} continues to rise to its maximum value, and the peak detector captures the maximum value of V_{id} to obtain $V_{id,pk}$. During the device turn-OFF transient, V_{DS} rises rapidly, causing V_{ds} to increase to its peak value, which the peak detector captures to obtain $V_{ds,pk}$.

The collected $V_{ds,pk}$, $V_{id,pk}$, and $V_{td,on}$ signals are sent to a high-precision analog-to-digital converter and converted into digital signals for a microcontroller unit (MCU) through digital isolators [18]. The MCU scales $V_{ds,pk}$ to $V_{DS,pk}$ and calculates the pulsewidth of $V_{td,on}$ to obtain $t_{d,on}$. During each switching cycle, the three TSEPs are sent to the MCU, and the $V_{DS,pk}$-$I_{D,pk}$-$t_{d,on}$-T_j model stored in the MCU returns the T_j information based on the measured $V_{DS,pk}$, $I_{D,pk}$, and $t_{d,on}$.

VI. Conclusion

This study introduces a modeling method of junction temperature estimation for SiC MOSFETs that combines multiple TSEPs, which significantly improves precision over traditional methods. Through theoretical analysis and experimental validation, this model effectively eliminates the load fluctuations and impacts, reaching a temperature measurement error under 4.49°C, a model fitting degree of 97.01%, and MAPE down to 6.31% under tested operating ranges. The proposed method applies not only to the upper and lower devices of half-bridge structures but also to discrete devices and modules at the same time. The proposed model's high accuracy under diverse load conditions benefits power device condition monitoring and its practical application in the field.

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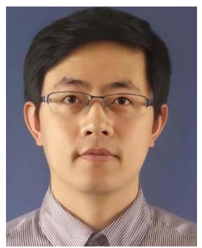

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