Impedance Reshaping Method Based on Compensating PLL Dynamic to Improve Active Power Transfer Capability of VSC Under Weak Grid

Xiaoling Xiong, *Member, IEEE*, and Bochen Luo, *Member, IEEE*

***Abstract*—The vector current control scheme based on the phase-locked loop (PLL) is widely used in grid-connected voltage-source converters (VSCs). However, the power transfer capability of the VSC will first be limited by dynamic power limitation (DPL) and then by static power limitation (SPL). The SPL is determined by the steady-state operation of the system, such as steady-state algebraic equations. Simultaneously, the DPL mainly relies on control strategy and controller parameters, which is also called the small-signal stability boundary and will not exceed SPL. In this article, the SPL and DPL of the VSC with different outer control loops are investigated, i.e., active power and reactive power (PQ) outer control loops, or active power and ac voltage (PV) outer control loops. It is found that extra reactive power injected into the grid is beneficial for improving the SPL and DPL of the VSC, especially under weak grid conditions. To maximize the SPL within the power constraint of VSC, the optimal design method for power references is presented. Meanwhile, a comparative analysis for the SPL of VSC with PQ or PV control loops is given, and the application scenario of both control strategies is clarified. Furthermore, aiming at the main factor restricting the DPL, i.e., PLL influence, an impedance reshaping method based on compensating PLL dynamics is proposed to increase the DPL of VSC, resulting in the DPL of the VSC almost extended to SPL. Finally, simulation and experimental tests are also carried out, and the results validate the effectiveness of the proposed methods.**

***Index Terms*—Impedance reshaping, power transfer capability, small-signal stability, weak grid, weak-grid-tied voltage-source converters (VSCs).**

I. Introduction

POWER electronic equipment has been widely promoted due to the increasing penetration of renewable energies and the rapid development of high voltage direct current transmission [1], [2], [3]. As the most commonly used interface equipment, voltage source converters (VSCs) have attracted extensive concerns all over the world. Generally, most of the VSCs still adopt the conventional grid-following control strategy, i.e., synchronizing with the grid through the phase-locked loop (PLL) and facilitating the current-vector control method [4], [5]. However, due to the high penetration of renewable energies and power electronic equipment, the grid becomes weak, giving the characteristic of a low short circuit ratio (SCR) at the point of common coupling (PCC) [6]. Under weak grid conditions, the power transfer capacity of VSCs will be limited, which is also one of the most significant challenges at present.

For VSCs, it has been reported that the power transfer capacity will be limited in two aspects, i.e., the static power limitation (SPL) [7] and the dynamic power limitation (DPL) [8]. The SPL is determined by the steady-state operation of the system, such as steady-state algebraic equations, which characterizes the maximum transferable power of the VSC under a specific circuit topology. However, if the VSC control system is involved, the DPL should be considered, which can be estimated based on the stability criteria using control theory. Thus, the DPL can also be regarded as the small-signal stability boundary when the VSC transfer power varies. The DPL of VSCs is generally lower than the SPL, especially when the controller parameters deteriorate, which may lead to an inadequate utilization of the VSC capacity.

Therefore, how to enlarge the VSC power transfer capacity as much as possible is a hot topic, which attracts many research efforts devoted to revealing the key factors that limit the SPL and DPL. In [9], the SPL of VSC under different operating conditions is analyzed, and it is found that the VSC can be operated under a lower SCR as the power factor (PF) reduces. However, the underlying mechanism of extending the SPL by reducing PF has not been revealed, and the influence of outer control loops on SPL remains to be studied. Huang et al. [8] further discussed the SPL of VSC with active power and ac voltage (PV) outer loops when SCR varies, but the SPL of adopting other outer control loops, such as active power and reactive power (PQ) loops, is not analyzed. Meanwhile, the influence of the VSC power constraint is not fully considered.

On the other hand, the DPL is mainly affected by the interactions of different control loops [10]. To study their influence on DPL more clearly, the VSC model sometimes needs to be simplified. Wu et al. [11] neglected the effects of outer loops and study the interactions of PLL and inner current loops. Meanwhile, Huang et al. [12] assumed the loop gain of the inner current loop is one and mainly focus on the interactions of PLL and outer control loops. However, no matter how the VSC model

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The authors are with the School of Electrical and Electronic Engineering, North China Electric Power University, Beijing 102206, China (e-mail: xiongxl1102@ncepu.edu.cn; luobochen2021@ncepu.edu.cn).

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is simplified, the research results indicate that the frequency coupling and negative resistance characteristic caused by PLL are among the key factors that lead to VSC instability issues and the reduction of DPL.

To solve the instability issues caused by PLL and extend the DPL of VSCs as much as possible, many different methods have been proposed to enhance or modify the conventional vector current control (VCC). The most direct method is to reduce the bandwidth of PLL, thus decreasing its influence [13]. However, a much lower PLL bandwidth will worsen the dynamic performance of the system and even be unable to reach the requirement of low voltage ride-through [14], [15]. Damping controllers [16], virtual impedance [17], or additional filters [18], [19] are often used to suppress the sub-/supersynchronous oscillations that occur in VSC systems with a high power rating. However, due to the relatively fixed parameters, their effectiveness can be easily influenced by system operating conditions or parameters. In [20] and [21], the VSC stability-enhanced method based on impedance reshaping in the *q*-*q* channel is proposed to resolve the instability issues caused by PLL and extend the small-signal stability boundary. However, the influence of *d*-*q* channel is not fully considered.

Moreover, some study efforts are devoted to using new control strategies for VSC to replace VCC that relied on conventional PLL. In [22] and [23], direct power control is proposed to address the oscillation risk in low frequency caused by PLL. However, strong frequency coupling will be introduced in high frequencies, resulting in high-frequency resonance issues. In [24], an observer-based current control is proposed, which can improve the stability of the system in a wide SCR range. However, due to the controller relying on calculating the state equation in real-time, the implementation of the method is complex. Zhang et al. [25] proposed an adaptive robust H_∞ control method for the grid-connected VSC, which can restrain the voltage distortion adaptively when SCR varies. However, the parameter design is based on the Lyapunov stability theorem, which increases the difficulty of practical application. Recently, grid-forming control strategies, such as power-synchronization control (PSC) [26] and virtual synchronous generator (VSG) [27] are developing rapidly due to their improved stability under weak girds. However, they still suffer from other stability issues, such as synchronous frequency resonance [28]. Meanwhile, lots of wind power converters and photovoltaic converters are still operating as grid-following converters, which synchronize with the power grid based on PLL. Thus, this type of converter is our main concern in this article. Other research attempts to modify the structure of the conventional PLL, thus reducing its influence. Yang et al. [29] proposed a symmetrical PLL, which can eliminate the frequency coupling phenomena and make the grid-connected VSC system become a single-input single-output (SISO) system. However, it still fundamentally does not remove the negative resistance introduced by the PLL. Therefore, the effect of this method on improving DPL is limited.

To cover the aforementioned insufficient studies for SPL and DPL of VSC adopting conventional VCC based on PLL, this article not only analyzes the SPL and DPL for VSC with two normal control strategies, i.e., PQ as well as PV control strategies but also presents design-oriented methods to improve the SPL and DPL, thus maximizing the VSC power transfer capability. The contributions of this article can be summarized as follows.

1) Based on the steady-state algebraic equations of the system, the SPL of VSC with PQ or PV control strategies is analyzed from multiple dimensions. It is found that extra reactive power generation is the fundamental reason for the improvement of SPL of VSC with PQ or PV outer loops.
2) To extend the SPL of VSC as much as possible within the power constraint, the optimal designed method for VSC power references with PQ or PV outer loops is presented. Meanwhile, a comparative analysis for the SPL of VSC with PQ or PV control loops is carried out, and the application scenario of different outer loops is clarified.
3) The DPL of the VSC with PQ or PV outer loops in different operation conditions is analyzed. Aiming at the key factor that limits DPL, i.e., PLL dynamics, an impedance reshaping method is proposed to reduce PLL influence. Thus, the DPL of the VSC can be almost extended to SPL.

The rest of this article is organized as follows. Section II gives the VSC grid-connected system configuration, and the SPL of VSC with PQ or PV control loops is analyzed. Meanwhile, the optimal values for power references are presented. In Section III, the DPL of VSC with PQ or PV control strategies is studied based on the small-signal impedance model. In Section IV, an impedance reshaping method based on compensating PLL dynamic is proposed, which can effectively improve the stability margin of the system and further extend the DPL almost to SPL. Section V shows the simulation and experimental results to verify the correctness of the theoretical analysis. Finally, Section VI concludes this article.

II. Static Power Limitation Analysis

A. VSC Grid-Connected System Configuration

The topology and control diagram of the grid-connected VSC is shown in Fig. 1(a), where $V_{\rm dc}$ is the dc side voltage. For the ac side, the VSC connects to the grid through an *LC* filter, where $L_{\rm f}$, $R_{\rm f}$, and $C_{\rm f}$ represent the filter inductance, resistance, and capacitance, respectively. $R_{\rm g}$ and $L_{\rm g}$ are the equivalent resistance and inductance of the grid. $\boldsymbol{v}_{\rm cabc}$ and $\boldsymbol{i}_{\rm abc}$ are the VSC output voltage vector and current vector, and $\boldsymbol{v}_{\rm abc}$ represents the PCC voltage. $\boldsymbol{i}_{\rm gabc}$ and $\boldsymbol{v}_{\rm gabc}$ are the grid current and voltage. The subscript "abc" means that they are in the three-phase stationary frame. Meanwhile, the above vectors can also be expressed in the synchronous rotating frame, i.e., $\boldsymbol{v}_{\rm cdq}$, $\boldsymbol{i}_{\rm dq}$, $\boldsymbol{v}_{\rm dq}$, $\boldsymbol{i}_{\rm gdq}$, $\boldsymbol{v}_{\rm gdq}$. For example, the PCC voltage vector in these two frames can be written as $\boldsymbol{v}_{\rm abc}=[v_{\rm a}\ v_{\rm b}\ v_{\rm c}]^{\rm T}$ and $\boldsymbol{v}_{\rm dq}=[v_{\rm d}\ v_{\rm q}]^{\rm T}$, respectively. The typical control strategy of the VSC is using a PLL to obtain the phase of PCC voltage $\theta_{\rm pll}$, thus realizing synchronization with the grid. To achieve different control goals, there are two usual options for the outer control loops, i.e., adopting PQ control loops or PV control loops. PQ control loops can flexibly adjust the PCC output power, i.e., *P* and *Q*, while the PV control loops can stabilize the PCC voltage amplitude $V_{\rm pcc}$ when the VSC output power varies. $\boldsymbol{i}_{\rm dqref}$ is the output of the outer control loops,

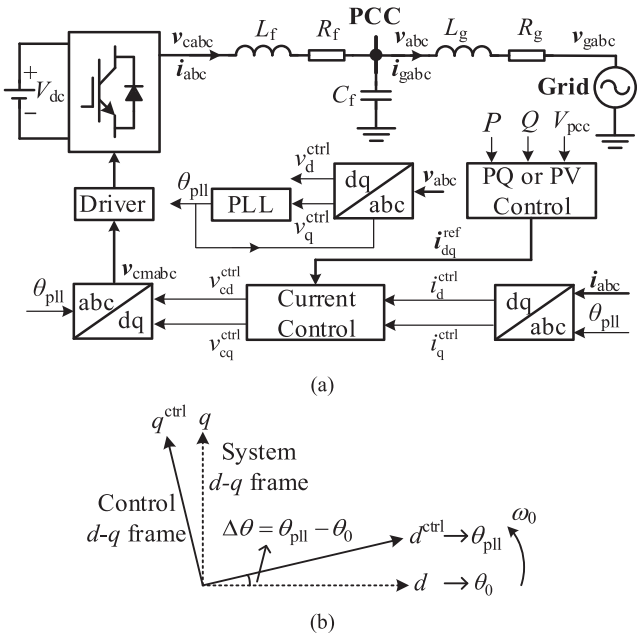

Fig. 1. Topology of grid-connected VSC and the relationship between different *d-q* frames. (a) Topology of grid-connected VSC. (b) Diagram of the system *d-q* frame and control *d-q* frame.

which is also the reference for the inner current loop. When the PCC voltage perturbations and PLL dynamics are considered, there will be two different *d-q* frames, i.e., the system and the control *d-q* frames [30]. Fig. 1(b) gives the relationship of these two *d-q* frames, where both frames are rotating at synchronous frequency ω_0, i.e., 100 π rad/s, and θ_0 is the PCC voltage phase angle in the system *d-q* frame. The dynamics of PLL will lead to a phase error $\Delta\theta$. To distinguish from the components in the system *d-q* frame, the superscript "ctrl" is used to denote the components in the control *d-q* frame.

B. SPL Analysis for VSC With the Outer PQ Control Loops

According to Fig. 1(a), the algebraic equations for steady-state operation in the *d-q* frame can be expressed as follows:

$$\begin{cases} P = 1.5\left(V_{d0}I_{d0} + V_{q0}I_{q0}\right) \\ Q = 1.5\left(V_{q0}I_{d0} - V_{d0}I_{q0}\right) \\ V_{d0} = V_{gd0} + R_gI_{d0} - \omega_0L_gI_{q0} \\ V_{q0} = V_{gq0} + R_gI_{q0} + \omega_0L_gI_{d0} \\ V_{gd0}^2 + V_{gq0}^2 = V_g^2. \end{cases} \tag{1}$$

Here, V_{cd0}, V_{cq0}, V_{d0}, V_{q0}, V_{gd0}, V_{gq0}, I_{d0}, and I_{q0}, denote the steady-state values. V_g is the amplitude of grid phase voltage. Considering the control effect of PLL and the outer PQ control loops, in the steady state, the following relationships should be satisfied:

$$\begin{cases} V_{q0} = 0 \\ P = P_{ref}; Q = Q_{ref} \end{cases} \tag{2}$$

where P_{ref} and Q_{ref} are the active and reactive power references, respectively. Combining (1) and (2), the complete steady-state algebraic equations of the system can be obtained, which considers both the constraints of the main circuit and the control effects. If the equations have no solutions, the grid-connected VSC can not work properly no matter how the controllers are enhanced.

$$\left(\frac{1}{1.5}\right)^2 X^2 - \left(\frac{2}{1.5}(R_gP + X_gQ) + {V_g}^2\right) X + (R_gP + X_gQ)^2 + (R_gQ - X_gP)^2 = 0. \tag{3}$$

To further reveal the requirement for the steady-state solutions, substituting (2) into (1) and eliminating the intermediate variables, the multivariate equations can be simplified as an equivalent quadratic equation in (3), where $X = (1.5V_{d0})^2$, and $X_g = \omega_0L_g$, representing the equivalent reactance of the grid. At the same time, VSCs usually are fed into the high-voltage transmission network. In other words, $R_g << X_g$, R_g is, thus, ignored in (3). If the solution for (3) exists, the following relationship should be satisfied:

$$\left(\frac{2}{1.5}X_gQ + {V_g}^2\right)^2 - 4\left(\frac{1}{1.5}\right)^2\left(P^2X_g^2 + Q^2X_g^2\right) \geq 0. \tag{4}$$

According to (4), the maximum value of P, i.e., the SPL of the VSC with outer PQ control loops, can be calculated as

$$\mathrm{SPL}_{\mathrm{PQ}} = \sqrt{\frac{3{V_g}^2}{2X_g}Q + \left(\frac{3{V_g}^2}{4X_g}\right)^2}. \tag{5}$$

Moreover, X_g can be depicted by SCR [8], which is the short-circuit ratio of the power grid, such as

$$X_g = \frac{V_g/I_N}{\mathrm{SCR}\sqrt{1 + (R_g/X_g)^2}} \approx \frac{V_g/I_N}{\mathrm{SCR}} \tag{6}$$

here I_N is the amplitude of the rated phase current. Substituting (6) into (5), the expression of $\mathrm{SPL}_{\mathrm{PQ}}$ can be further derived as

$$\mathrm{SPL}_{\mathrm{PQ}} = \sqrt{P_NQ\mathrm{SCR} + \left(\frac{1}{2}P_N\mathrm{SCR}\right)^2} \tag{7}$$

where $P_N = 1.5V_gI_N$, denoting the rated power of the VSC. Meanwhile, because $\mathrm{SPL}_{\mathrm{PQ}} \geq 0$, the following inequality also should be satisfied:

$$Q \geq -\frac{1}{4}P_N\mathrm{SCR}. \tag{8}$$

From (8), it can be found that the maximum reactive power that VSC can absorb from the grid is also limited by SCR. Besides, when the VSC operates at unity PF, i.e., $Q = 0$, (7) can be further derived as

$$\mathrm{SPL}^0_{\mathrm{PQ}} = \frac{1}{2}P_N\mathrm{SCR}. \tag{9}$$

To have a clear insight into the relationships, the three-dimensional (3-D) view of $\mathrm{SPL}_{\mathrm{PQ}}$ and ${\mathrm{SPL}^0}_{\mathrm{PQ}}$ can be drawn based on (7) and (9), as shown in Fig. 2(a). At the same time, the front view, right view, and vertical view are given in Fig. 2(b)–(d), respectively. In Fig. 2, the red solid line represents ${\mathrm{SPL}^0}_{\mathrm{PQ}}$, i.e., the VSC operating at unity PF. From Fig. 2(b), it can be seen that when VSC operates at unity PF, ${\mathrm{SPL}^0}_{\mathrm{PQ}}$(p.u.) is proportional to SCR with a sloop of 0.5, indicating that the minimum SCR required for VSC should be not less than 2 to

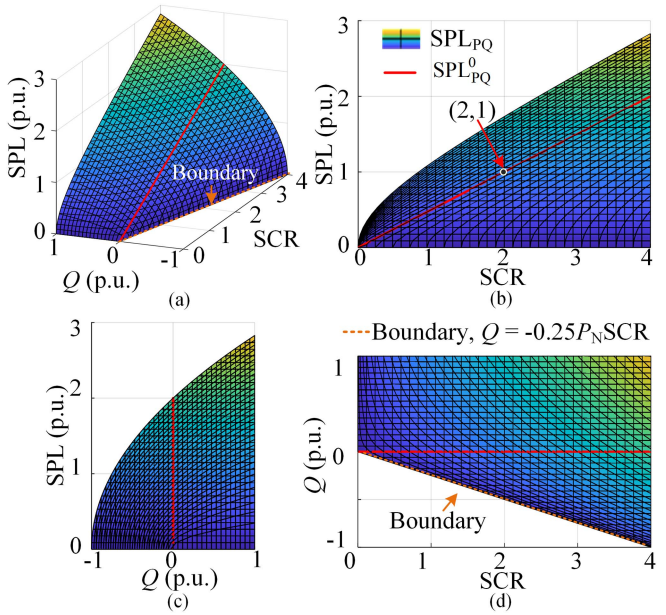

Fig. 2. Three-dimensional view of the SPL of the VSC with outer PQ loops when SCR and Q vary. (a) Three-dimensional view. (b) Front view. (c) Right view. (d) Vertical view.

transfer rated active power, which corresponds to the conclusion mentioned in [9]. Moreover, in ultraweak grid conditions, $\mathrm{SPL}^0{}_{\mathrm{PQ}}$ will be reduced further. For example, when SCR = 1, $\mathrm{SPL}^0{}_{\mathrm{PQ}}$(p.u.) is only 0.5 p.u., which may cause insufficient utilization of the VSC capacity. Fortunately, from Fig. 2(c), it can be seen that $\mathrm{SPL}_{\mathrm{PQ}}$ will be improved when Q increases, indicating that the SPL will be extended when extra reactive power is injected into the grid.

On the other hand, excessive reactive power will also occupy the VSC capacity, leading to overload issues or overcurrent damage. Therefore, the output power needs to be designed to maximize the VSC power transfer capacity under the power constraint. When the VSC power constraint is considered, the following relationship should be satisfied:

$$S = \sqrt{P^2 + Q^2} \le nP_{\mathrm{N}} \tag{10}$$

where S is the apparent power of the VSC, and n is a factor, denoting the limitation of different conditions. In this article, the maximum allowable capacity of the VSC is set as $1.1P_{\mathrm{N}}$, thus, n will be lower than 1.1.

When the SPL and power constraint mentioned in (7) and (10) are both considered, the optimal design for Q to extend VSC power transfer capacity can be deduced as

$$Q_{op} = \begin{cases} P_N\left(n - \frac{1}{2}\mathrm{SCR}\right), & 0 \le \mathrm{SCR} \le 2n \\ 0, & \mathrm{SCR} > 2n \end{cases}. \tag{11}$$

Based on the Q_{op} derived from (11), the optimal values of P can also be calculated, which can be written as

$$P_{\mathrm{op}} = \begin{cases} P_N\sqrt{n\mathrm{SCR} - \frac{1}{4}\mathrm{SCR}^2}, & 0 \le \mathrm{SCR} \le 2n \\ nP_N, & \mathrm{SCR} > 2n \end{cases}. \tag{12}$$

Fig. 3(a) further gives the 3-D view of P_{op}, and Q_{op} with the power constraint of P_{N} and $1.1P_{\mathrm{N}}$ when SCR varies. The

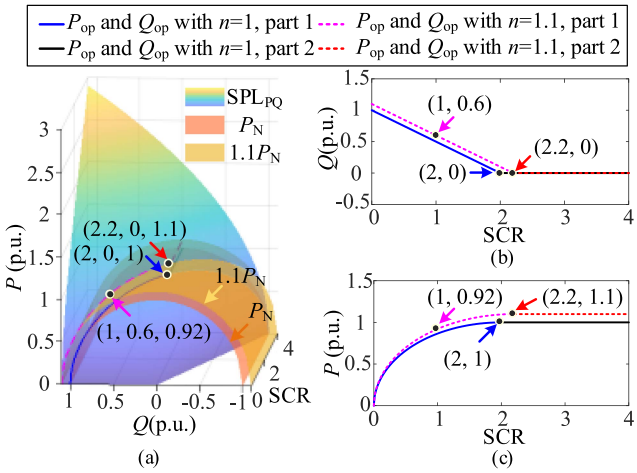

Fig. 3. Optimal values of P and Q to fully utilize VSC capacity when SCR varies. (a) Three-dimensional overall view. (b) Vertical view. (c) Right view.

cylindrical surfaces represent the power constraints of P_{N} and $1.1P_{\mathrm{N}}$, which intersect with $\mathrm{SPL}_{\mathrm{PQ}}$ at the blue solid line and pink dashed line, respectively, standing for the values of P_{op} and Q_{op} when SCR varies from 0 to $2n$. However, when SCR increases over $2n$, P_{op} reaches the maximum value nP_{N} and can not be further extended due to the VSC power constraint, as shown in the black solid line and red dashed line. At this time, the VSC can operate at rated active power even without extra reactive power injection. Fig. 3(b) and (c) further shows the vertical view and right view of P_{op} and Q_{op}, respectively. From here, the P_{op} and Q_{op} at different power constraints can be easily observed when SCR varies. For example, when the power constraint is $1.1P_{\mathrm{N}}$ and SCR decreases to 1, it can be seen that the optimal reactive power is 0.6 p.u., which can extend the SPL to almost 0.92 p.u. Except for the power constraint, the current limitation is also a key factor that should be considered when P_{op} and Q_{op} are adopted. Suppose the maximum allowable current of the VSC is 1.5 p.u. [31]. Substituting P_{op} and Q_{op} into (1), the maximum value of VSC output current can be calculated as 1.45 p.u. in the case of SCR = $2n$. Therefore, P_{op} and Q_{op} are still applicable when the current limitation of VSC is considered and will not lead to overcurrent issues.

C. SPL Analysis for VSC With the Outer PV Control Loops

The above analysis mainly focuses on the power transfer capacity of VSC with outer PQ control loops. When the PV control loops are adopted, the steady-state equations mentioned in (2) need to be modified as

$$\begin{cases} V_{\mathrm{q0}} = 0 \\ P = P_{ref}; V_{\mathrm{d0}} = V_{\mathrm{pcc}} = V_{\mathrm{ref}} \end{cases} \tag{13}$$

where V_{ref} is the reference value of PCC voltage amplitude. Similar to the SPL analysis for PQ control loops, substituting (13) into (1), and based on the quadratic equation about I_{q0}, the SPL of the VSC with PV outer loops can be calculated as

$$\mathrm{SPL}_{\mathrm{PV}} = \frac{3}{2}V_{\mathrm{pcc}}I_{\mathrm{N}}\mathrm{SCR}. \tag{14}$$

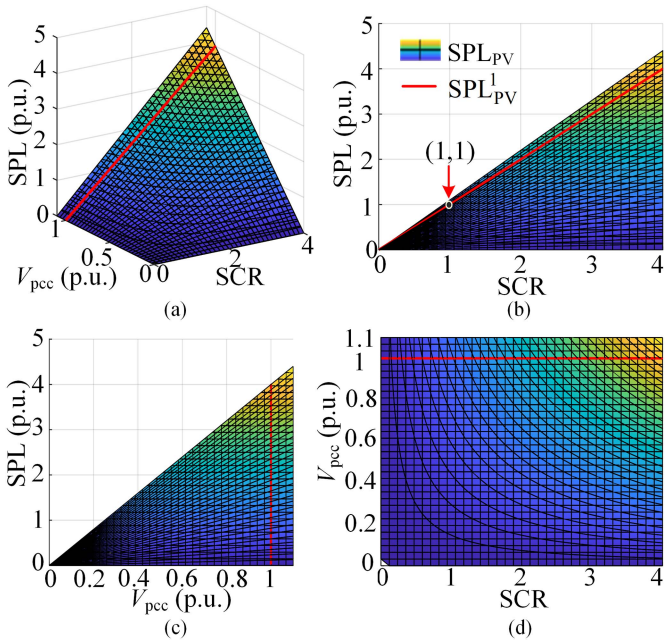

Fig. 4. Three-dimensional view of the SPL with PV outer loops when SCR and V_{pcc} vary. (a) Overall view. (b) Front view. (c) Right view. (d) Vertical view.

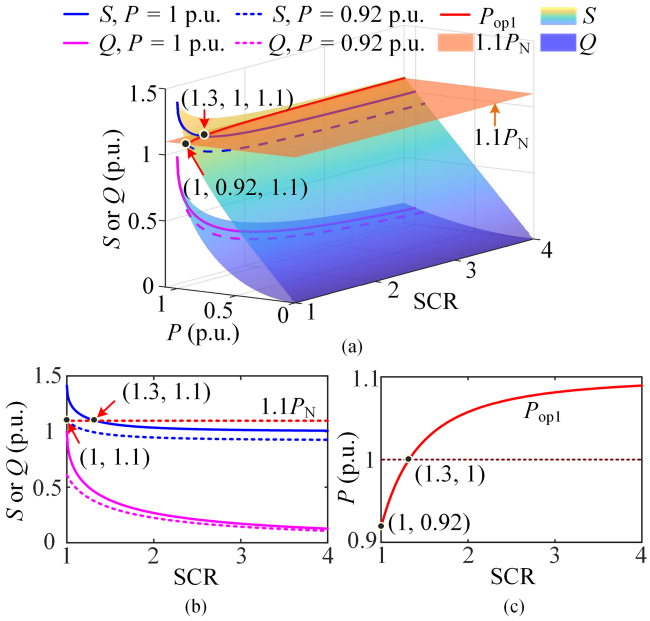

Fig. 5. VSC output powers when outer PV loops are adopted and SCR varies. (a) Three-dimensional overall view of Q and S with different P and SCR. (b) Front view of Q and S when P is 0.92 p.u. or 1 p.u. (c) Optimal values of P when SCR varies.

Moreover, if V_{pcc} is equal to the rated value V_g, (14) can be further simplified as

$$\mathrm{SPL}^1_{\mathrm{PV}} = P_{\mathrm{N}}\mathrm{SCR}. \tag{15}$$

According to (14) and (15), the 3-D view of $\mathrm{SPL}_{\mathrm{PV}}$ and $\mathrm{SPL}^1{}_{\mathrm{PV}}$ can be obtained, as shown in Fig. 4(a). The front view, right view, and vertical view are given in Fig. 4(b)–(d), respectively. From here, it can be seen that the SPL of VSC with PV loops will be extended when SCR and V_{pcc} increase. Furthermore, $\mathrm{SPL}^1{}_{\mathrm{PV}}$(p.u.) is proportional to the SCR with a scale factor of 1, indicating that the VSC with PV control loops can transfer rated active power when SCR = 1. Noting that the power constraint is not considered here.

However, as the output active power increases, the VSC will inevitably supply extra reactive power to support the PCC voltage if other compensation equipment is not adopted, which may cause overload issues. Therefore, the reactive power characteristic of the VSC with PV control loops should be analyzed, thus ensuring the apparent power of the VSC is always lower than the power constraint. The output reactive power of the VSC with PV control loops can be calculated as

$$Q = -\frac{3}{2}V_{pcc}I_{q0} \approx \frac{3}{2}\frac{V_{pcc}^2 - V_{pcc}\sqrt{V_g^2 - \left(\frac{V_g}{\mathrm{SCR}I_N}\frac{P}{1.5V_{pcc}}\right)^2}}{V_g/(\mathrm{SCR}I_N)}. \tag{16}$$

According to (16), when PV control loops are used, the 3-D view of S and Q can be obtained, as shown in Fig. 5(a), where V_{pcc} is set as 1 p.u.. The red surface represents the power constraint of $1.1P_N$. From Fig. 5(a), it can be seen that in some cases, S will exceed the power constraint, especially when SCR is low. For clarity, Fig. 5(a) further gives the curves of S and Q when P is taken as 0.92 p.u. and 1 p.u., respectively. Meanwhile, the front view of them is shown in Fig. 5(b). From here, it can be seen that when P is 1 p.u., S will exceed the power constraint if SCR < 1.3, resulting in overload issues. Therefore, the minimum SCR required for VSC to transfer rated active power is about 1.3 with PV control loops and a power constraint of $1.1P_N$. In other words, P needs to be properly reduced to ensure S will not exceed the power constraint with a lower SCR. For example, when P reduces to 0.92 p.u., the curve of S will move downward and intersect with $1.1P_N$ at SCR = 1. Therefore, 0.92 p.u. can be regarded as the optimal value of P when SCR is 1. Similarly, other optimal values of P when SCR varies can also be obtained, as presented on the red solid line, i.e., the intersection of $1.1P_N$ and S, which can be expressed as

$$P_{op1} = P_N\mathrm{SCR}\sqrt{1-\left(1-\frac{1}{2}\frac{n^2}{\mathrm{SCR}^2}\right)^2}, \quad \mathrm{SCR} \geq \frac{n}{2}. \tag{17}$$

Moreover, the vertical view of P_{op1} is given in Fig. 5(c). From Fig. 5(c), it can be seen that P_{op1} will gradually approach $1.1P_N$ when SCR increases. It should be mentioned that the design of P_{op1} assumes $V_{pcc} = 1$ p.u.. Thus, the per-unit value of S will be equivalent to the per-unit value of the VSC output current. Due to $S \leq 1.1\ P_N$, the output current will also be smaller than 1.1 p.u., which will not cause overcurrent issues.

D. Comparative Analysis of SPL for VSC With Outer PQ or PV Control Loops

To have an overall insight into the SPL with these two types of control strategies, Fig. 6 further gives the comparison plots of SPL with PQ or PV control loops. From Fig. 6, when the power constraint is ignored and the VSC works in normal conditions, such as using PQ loops with unit PF or PV loops with

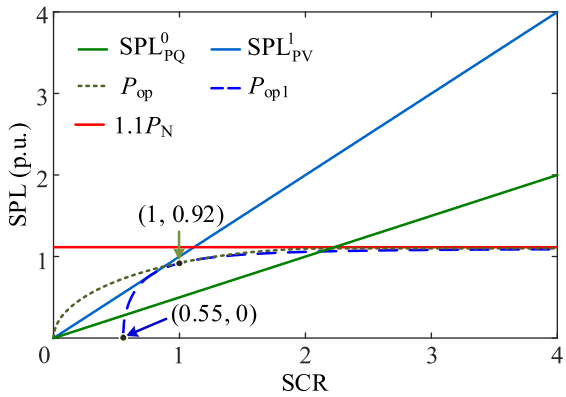

Fig. 6. Comparison plots of SPL for VSC with PQ or PV control loops with or without considering power constraints.

$V_{pcc} = 1$ p.u., it can be seen that SPL^1_{PV} is almost two times of SPL^0_{PQ}, indicating that the VSC with PV control loops processes a better power transfer potential compared to the VSC in unit PF. The fundamental reason is extra reactive power is injected to support the PCC voltage as the output active power increases when PV loops are adopted, as shown in Fig. 5(a). However, when the power constraint is considered, such as $1.1P_N$, the SPL of the VSC with PV control loops will greatly reduce and reach the optimal value P_{op1}. On the contrary, the SPL of VSC with PQ control loops will extend to P_{op} under ultraweak grid conditions, such as SCR < 1. Moreover, the VSC with PV control loops may not be able to work properly when SCR further decreases, such as SCR < 0.55, due to the constraint mentioned in (17). Fortunately, if SCR ≥ 1, there will be little difference between P_{op} and P_{op1}, meaning the SPL of VSC with PQ or PV loops are almost the same. Therefore, PV outer loops are more applicable for a low SCR grid than PQ loops due to better power transfer potential and voltage support capability. However, in ultraweak grids, PV or PQ outer loops will also be limited due to power constraint or PCC voltage constraint.

III. Dynamic Power Limitation Analysis

The abovementioned analysis shows that the SPL of VSC can be extended by combining the operating point design and control mode. However, the actual transferable power of VSC, i.e., the DPL, will be much lower than SPL due to the effect of the control system. To analyze the DPL of VSC, the small-signal relationships of the grid-connected VSC should be deduced, and the detailed process is omitted in this article for simplification. Considering the effect of different control loops, the impedance models of the VSC adopting PQ or PV control strategies are depicted in Fig. 7, where the detailed expression of the transfer functions or matrices is given in (18) shown at the bottom of the next page [12], [32], where V_{d0}, V_{q0}, I_{d0}, I_{q0}, V_{cd0}, and V_{cq0} denote the steady-state values. k_{pP}, k_{iP}, k_{pQ}, k_{iQ}, k_{pAC}, k_{iAC}, k_{pI}, k_{iI}, K_{pPLL}, and K_{iPLL} are the proportional gain and integral gain of the active power, reactive power, ac voltage, inner current, and PLL controllers. ω_{LPF} is the cut-off angular frequency of the low-pass filter in the outer loops. According to Fig. 7, the admittance of the VSC with PQ control loops

TABLE I
Parameters of VSC Used in Simulation and Experiment

Symbol	Parameter	Value
V_g	Grid phase voltage, peak value	1 p.u. (50 V)
P_N	Rated power	1 p.u. (1 kVA)
f_1	Fundamental frequency	1 p.u. (50 Hz)
V_{dc}	Dc-link voltage	1 p.u. (300 V)
L_f	Filter inductance	4 mH
R_f	Filter resistance	5 mΩ
C_f	Filter capacitance	3.5 μF
L_g	Grid inductance	12 mH
R_g	Grid resistance	37 mΩ
SCR	Short-circuit ratio	1
T_s	Switching period	0.1 ms
ω_i	Bandwidth of the current loop	1000 rad/s
ω_{pll}	Bandwidth of the PLL	100 rad/s
ω_p	Bandwidth of the active power loop	50 rad/s
ω_q	Bandwidth of reactive power loop	50 rad/s
ω_{ac}	Bandwidth of the AC voltage loop	50 rad/s
ω_{LPF}	Cut-off angular frequency of LPFs	50 rad/s

in the d-q frame can be deduced as (19). When the PV loops are adopted, the matrix $\boldsymbol{G}^v_Q$, $\boldsymbol{G}_{pq}$, and $\boldsymbol{G}^i_Q$ in (19) should be replaced by $\boldsymbol{G}_1$, $\boldsymbol{G}_{pv}$, and 0 accordingly. Moreover, $\boldsymbol{Y}_{dq}(s)$ can be further transformed into the stationary domain as [33]

$$\boldsymbol{Y}_{\alpha\beta}(s)=\frac{1}{2}\begin{bmatrix}1 & j\\ 1 & -j\end{bmatrix}\boldsymbol{Y}_{dq}(s-j\omega_0)\begin{bmatrix}1 & 1\\ -j & j\end{bmatrix}. \tag{20}$$

Based on (20), the DPL of the VSC can be assessed through the generalized Nyquist criterion (GNC), i.e., analyzing the eigen-loci, which can be calculated as

$$\det(\lambda\boldsymbol{I}-\boldsymbol{Y}_{\alpha\beta}\boldsymbol{Z}_g)=0 \tag{21}$$

where $\boldsymbol{Z}_g$ represents the grid impedance matrix [30].

Fig. 8 shows the eigen-loci of the system with SCR $= 1$ when the outer PQ control loops are adopted. The detailed parameters are shown in Table I, where the bandwidth of different control loops is calculated using their closed-loop transfer function. From Fig. 8(a), it can be seen that when $P = 0.4$ p.u. and $Q = 0$ p.u., i.e., the VSC operating at unity PF, the eigen-loci of the system will not encircle the critical point $(-1, j0)$, representing that the system is stable. However, when P further increases to 0.45 p.u., the $(-1, j0)$ point will be encircled, and the system has oscillation risk, indicating that the DPL of the VSC is about 0.45 p.u. under unit PF, which is less than the SPL in the case of $Q = 0$ p.u., as shown in Fig. 2, i.e., 0.5 p.u., meaning the DPL can not exceed the SPL. Fortunately, if extra reactive power is generated, the DPL of VSC will also be extended, as shown in Fig. 8(b). For example, when Q is improved to the optimal designed value Q_{op} for SCR $= 1$ mentioned in Fig. 3, i.e., 0.6 p.u.. It can be seen that the DPL will be extended to about 0.75 p.u., which is much greater than the DPL with $Q = 0$ p.u., i.e., 0.45 p.u., however, still smaller than the optimal value P_{op}, i.e., 0.92 p.u.. Therefore, extra reactive power injected into the grid can also improve the DPL of the VSC, but the DPL can not exceed the SPL.

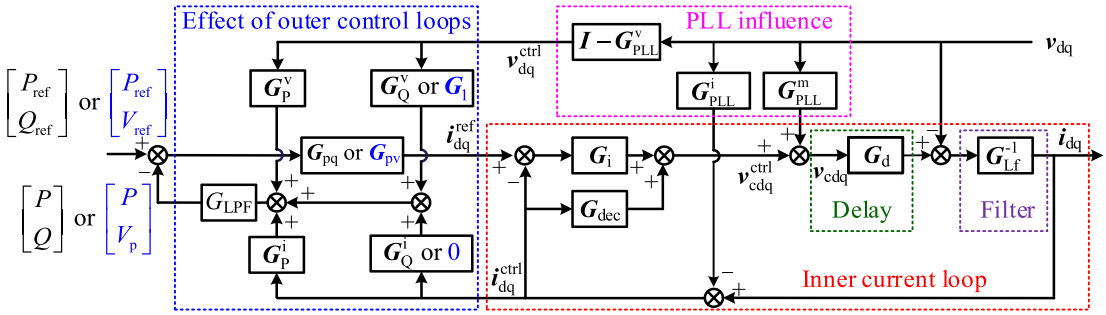

Fig. 7. Impedance model of the VSC adopting PQ or PV control strategies in *d-q* frame.

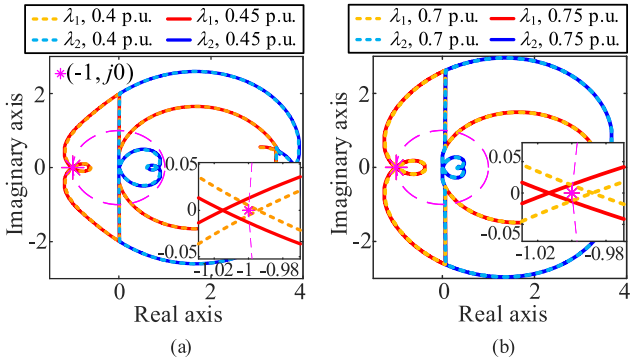

Fig. 8. Generalized Nyquist diagram of the grid-connected VSC with PQ control loops when SCR = 1. (a) $Q = 0$ p.u. and P increases from 0.4 p.u. to 0.45 p.u. (b) $Q = 0.6$ p.u. and P increases from 0.7 p.u. to 0.75 p.u.

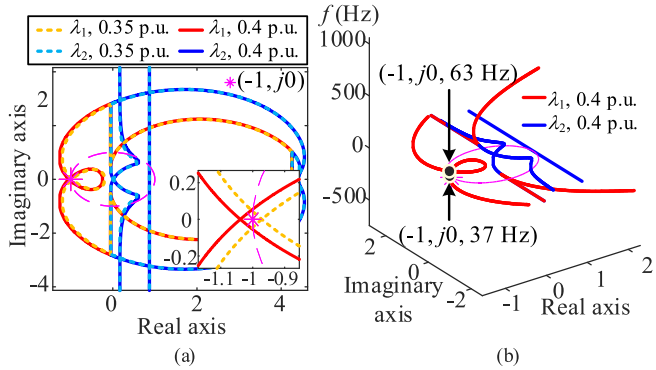

Fig. 9. Generalized nyquist diagram of the grid-connected VSC with PV control loops when SCR = 1. (a) P increases from 0.35 p.u. to 0.4 p.u. (b) Enlarged three-dimensional view for $P = 0.4$ p.u.

Fig. 9 further gives the generalized Nyquist diagram of the system with outer PV control loops. From Fig. 9(a), the DPL of the VSC with PV loops can be estimated at 0.4 p.u., which is still lower than the optimal designed value, i.e., $P_{\mathrm{op1}} = 0.92$ p.u., mentioned in Fig. 5. Meanwhile, through the enlarged 3-D view Nyquist diagram in Fig. 9(b), the oscillation will occur at 63 Hz and 37 Hz, which corresponds to the frequency coupling phenomena mentioned in [33]. The analysis shows that the DPL of VSC with PV control loops will also be lower than SPL, resulting from the effect of the control system.

IV. Impedance Reshaping Method

A. Proposal of Impedance Reshaping Method

The abovementioned analysis indicates that the DPL of the VSC will be much lower than SPL, because of the effect of different control loops. Meanwhile, it has been widely accepted

$$\boldsymbol{G}_{\mathrm{P}}^{\mathrm{v}}=\begin{bmatrix}1.5I_{\mathrm{d0}} & 1.5I_{\mathrm{q}}0\\ 0 & 0\end{bmatrix};\boldsymbol{G}_{\mathrm{P}}^{\mathrm{i}}=\begin{bmatrix}1.5V_{\mathrm{d0}} & 1.5V_{\mathrm{q}}0\\ 0 & 0\end{bmatrix};\boldsymbol{G}_{\mathrm{Q}}^{\mathrm{v}}=\begin{bmatrix}0 & 0\\ -1.5I_{\mathrm{q0}} & 1.5I_{\mathrm{d0}}\end{bmatrix};\boldsymbol{G}_{\mathrm{Q}}^{\mathrm{i}}=\begin{bmatrix}0 & 0\\ 1.5V_{\mathrm{q}}0 & -1.5V_{\mathrm{d0}}\end{bmatrix}$$

$$\boldsymbol{G}_{\mathrm{pq}}=\begin{bmatrix}k_{\mathrm{pP}}+k_{\mathrm{iP}}/s & 0\\ 0 & -(k_{\mathrm{pQ}}+k_{\mathrm{iQ}}/s)\end{bmatrix};\boldsymbol{G}_{1}=\begin{bmatrix}0 & 0\\ 1 & 0\end{bmatrix};\boldsymbol{G}_{\mathrm{pv}}=\begin{bmatrix}k_{\mathrm{pP}}+k_{\mathrm{iP}}/s & 0\\ 0 & -(k_{\mathrm{pAC}}+k_{\mathrm{iAC}}/s)\end{bmatrix};$$

$$G_{LPF}=\frac{\omega_{LPF}}{s+\omega_{LPF}}$$

$$\boldsymbol{G}_{i}=\begin{bmatrix}k_{\mathrm{pI}}+k_{\mathrm{iI}}/s & 0\\ 0 & k_{\mathrm{pI}}+k_{\mathrm{iI}}/s\end{bmatrix};\boldsymbol{G}_{dec}=\begin{bmatrix}0 & -\omega_1 L_{\mathrm{f}}\\ \omega_1 L_{\mathrm{f}} & 0\end{bmatrix};H_{pll}=\frac{K_{pPLL}s+K_{iPLL}}{s^2+K_{pPLL}V_{d0}s+K_{iPLL}V_{d0}}$$

$$\boldsymbol{G}_{PLL}^{v}=\begin{bmatrix}0 & -V_{q0}H_{pll}\\ 0 & V_{d0}H_{pll}\end{bmatrix};\boldsymbol{G}_{PLL}^{i}=\begin{bmatrix}0 & -I_{q0}H_{pll}\\ 0 & I_{d0}H_{pll}\end{bmatrix};\boldsymbol{G}_{PLL}^{m}=\begin{bmatrix}0 & -V_{cq0}H_{pll}\\ 0 & V_{cd0}H_{pll}\end{bmatrix};\boldsymbol{G}_{\mathrm{Lf}}=\begin{bmatrix}sL_{\mathrm{f}}+R_{\mathrm{f}} & -\omega_1 L_{\mathrm{f}}\\ \omega_1 L_{\mathrm{f}} & sL_{\mathrm{f}}+R_{\mathrm{f}}\end{bmatrix} \tag{18}$$

$$\begin{aligned}\boldsymbol{Y}_{dq}(s)=&\left(\boldsymbol{G}_{\mathrm{Lf}}-\boldsymbol{G}_{\mathrm{d}}\left(\boldsymbol{G}_{\mathrm{dec}}-\boldsymbol{G}_{\mathrm{i}}-\boldsymbol{G}_{\mathrm{i}}\boldsymbol{G}_{\mathrm{pq}}G_{LPF}(\boldsymbol{G}_{\mathrm{P}}^{\mathrm{i}}+\boldsymbol{G}_{\mathrm{Q}}^{\mathrm{i}})\right)\right)^{-1}\cdot\left(\boldsymbol{G}_{\mathrm{d}}\boldsymbol{G}_{\mathrm{i}}\boldsymbol{G}_{\mathrm{pq}}G_{LPF}(\boldsymbol{G}_{\mathrm{P}}^{\mathrm{v}}+\boldsymbol{G}_{\mathrm{Q}}^{\mathrm{v}})(\boldsymbol{I}-\boldsymbol{G}_{\mathrm{PLL}}^{\mathrm{v}})\right.\\&\left.+\boldsymbol{G}_{\mathrm{d}}\left(\boldsymbol{G}_{\mathrm{dec}}-\boldsymbol{G}_{\mathrm{i}}-\boldsymbol{G}_{\mathrm{i}}\boldsymbol{G}_{\mathrm{pq}}G_{LPF}(\boldsymbol{G}_{\mathrm{P}}^{\mathrm{i}}+\boldsymbol{G}_{\mathrm{Q}}^{\mathrm{i}})\right)\boldsymbol{G}_{\mathrm{PLL}}^{\mathrm{i}}+\boldsymbol{I}-\boldsymbol{G}_{\mathrm{d}}\boldsymbol{G}_{\mathrm{PLL}}^{\mathrm{m}}\right)\end{aligned} \tag{19}$$

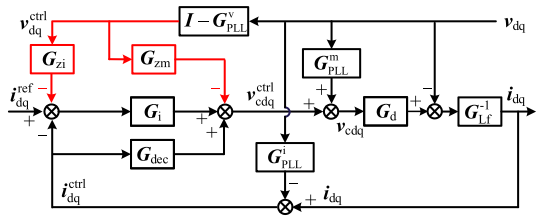

Fig. 10. Control diagram of the impedance reshaping method to improve the VSC power transfer capacity.

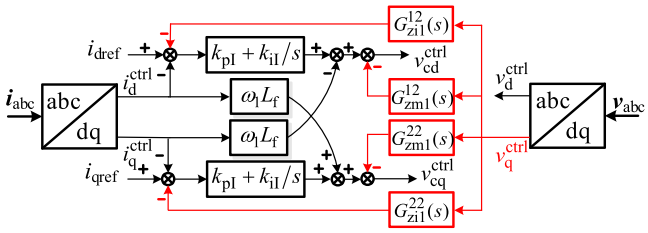

Fig. 11. Implementation diagram of the proposed method.

that the frequency coupling and negative resistance characteristics brought by PLL are among the key factors that limit DPL. According to the standard cascaded control tuning methodologies [11], the outer loops (no matter PQ, PV, or dc outer loops) are always designed much slower than the inner loop. Thus, the outputs of the outer control loops of VSC can be approximately regarded as constants [34]. Therefore, the PLL dynamics contained in the inner current loop should be mainly focused on here. For the VSC with a low power, $\boldsymbol{G}^{\mathrm{i}}{}_{\mathrm{PLL}}$ and $\boldsymbol{G}^{\mathrm{m}}{}_{\mathrm{PLL}}$ will both introduce an amount of PLL dynamics into the control system and jeopardize the DPL because the steady-state values in $\boldsymbol{G}^{\mathrm{i}}{}_{\mathrm{PLL}}$ and $\boldsymbol{G}^{\mathrm{m}}{}_{\mathrm{PLL}}$ are not significantly different. However, suppose the operating power rating is higher, the rated current of the VSC will be much greater than the rated voltage, resulting in the PLL dynamic in $\boldsymbol{G}^{\mathrm{i}}{}_{\mathrm{PLL}}$ dominated. Therefore, to ensure the proposed reshaping method can reduce the influence of PLL and extend the VSC power transfer capacity even if the operating point and power rating vary, two reshaping branches are introduced, respectively, to compensate for the PLL dynamics in $\boldsymbol{G}^{\mathrm{i}}{}_{\mathrm{PLL}}$ and $\boldsymbol{G}^{\mathrm{m}}{}_{\mathrm{PLL}}$. As shown in Fig. 10, the reshaping terms are plotted in red.

It can be seen that the reshaping method includes two blocks, i.e., $\boldsymbol{G}_{\mathrm{zi}}$ and $\boldsymbol{G}_{\mathrm{zm}}$. To eliminate the influence of $\boldsymbol{G}^{\mathrm{i}}{}_{\mathrm{PLL}}$ and $\boldsymbol{G}^{\mathrm{m}}{}_{\mathrm{PLL}}$, the following relationships need to be satisfied:

$$\begin{aligned}\boldsymbol{G}_{\mathrm{zi}} &= \boldsymbol{G}^{i}_{PLL}(\boldsymbol{I}-\boldsymbol{G}^{v}_{PLL})^{-1}\\ &= \begin{bmatrix}0 & -I_{q0}\cdot(K_{\mathrm{pPLL}}s+K_{\mathrm{iPLL}})/s^2\\ 0 & I_{d0}\cdot(K_{\mathrm{pPLL}}s+K_{\mathrm{iPLL}})/s^2\end{bmatrix}\\ \boldsymbol{G}_{\mathrm{zm}} &= \boldsymbol{G}^{m}_{PLL}(\boldsymbol{I}-\boldsymbol{G}^{v}_{PLL})^{-1}\\ &= \begin{bmatrix}0 & -V_{cq0}\cdot(K_{\mathrm{pPLL}}s+K_{\mathrm{iPLL}})/s^2\\ 0 & V_{cd0}\cdot(K_{\mathrm{pPLL}}s+K_{\mathrm{iPLL}})/s^2\end{bmatrix}\end{aligned} \tag{22}$$

where $\boldsymbol{I}$ represent a 2×2 identity matrix. According to (22), it can be seen that the elements of $\boldsymbol{G}_{\mathrm{zi}}$ and $\boldsymbol{G}_{\mathrm{zm}}$ only exist in the second column and are similar to second-order integral terms, which may amplify the dc components in $v^{\mathrm{ctrl}}{}_{\mathrm{q}}$, leading to the VSC output deviating from its expected values. Therefore, adding a second-order high pass filter (HPF) in the reshaping branches is necessary, thus removing the dc components in $v^{\mathrm{ctrl}}{}_{\mathrm{q}}$. Besides, to improve the adaptability of the proposed method, the steady-state values $\boldsymbol{I}_{\mathrm{dq0}}$ and $\boldsymbol{V}_{\mathrm{cdq0}}$ can be replaced by the current references and modulating signals, i.e., $\boldsymbol{i}_{\mathrm{dqref}}$ and $\boldsymbol{v}_{\mathrm{cmdq}}$. Finally, $\boldsymbol{G}_{\mathrm{zi}}$ and $\boldsymbol{G}_{\mathrm{zm}}$ can be modified as

$$\begin{aligned}\boldsymbol{G}_{\mathrm{zi1}} &= G_{\mathrm{HPF}}(s)\begin{bmatrix}0 & -i_{\mathrm{qref}}\cdot(K_{\mathrm{pPLL}}s+K_{\mathrm{iPLL}})/s^2\\ 0 & i_{\mathrm{dref}}\cdot(K_{\mathrm{pPLL}}s+K_{\mathrm{iPLL}})/s^2\end{bmatrix}\\ \boldsymbol{G}_{\mathrm{zm1}} &= G_{\mathrm{HPF}}(s)\begin{bmatrix}0 & -0.5V_{\mathrm{dc}}v_{cmq}\cdot(K_{\mathrm{pPLL}}s+K_{\mathrm{iPLL}})/s^2\\ 0 & 0.5V_{\mathrm{dc}}v_{cmd}\cdot(K_{\mathrm{pPLL}}s+K_{\mathrm{iPLL}})/s^2\end{bmatrix}.\end{aligned} \tag{23}$$

In (23), $G_{\mathrm{HPF}}(s)$ is the transfer function of the second-order HPF, which can be expressed as

$$G_{\mathrm{HPF}}(s) = \frac{A(\infty)s^2}{s^2+(\omega_{\mathrm{HPF}}/Q)\,s+\omega^2_{\mathrm{HPF}}}. \tag{24}$$

Overall, removing the dc component in $v^{\mathrm{ctrl}}{}_{\mathrm{q}}$ is effective by taking the HPF with a high (HPF). However, a much higher ω_{HPF} will also worsen the effect of the reshaping method for eliminating PLL dynamics. To ensure the HPF will not worsen the effect of the proposed method, the corner frequency ω_{HPF} should be taken as small as possible, which is set as·5 rad/s in this article. Accordingly, the quality factor Q and the gain coefficient $A(\infty)$ are taken as 1.

Fig. 11 further shows the implementation diagram of the proposed reshaping method, where $G^{12}{}_{\mathrm{zi1}}(s)$, $G^{22}{}_{\mathrm{zi1}}(s)$, $G^{12}{}_{\mathrm{zm1}}(s)$, and $G^{22}{}_{\mathrm{zm1}}(s)$ are the second column elements of $\boldsymbol{G}_{\mathrm{zi1}}$ and $\boldsymbol{G}_{\mathrm{zm1}}$, respectively.

B. Effects of the Reshaping Method

To verify the effectiveness of the proposed method and observe the stability margin more conveniently, Fig. 12 further gives the equivalent SISO impedance model of the grid-connected VSC with or without adopting the proposed reshaping method [35], which is the closed-loop equivalent model derived from the characteristic equation of the system. Since the grid impedance is R_{g}+jX_{g}, thus, the OFF-diagonal elements of $\boldsymbol{Z}_{\mathrm{g}}$ i.e., Z_{g12} and Z_{g21}, are zeros, and the positive-sequence one can be written as

$$\begin{cases}Z_{peq} = Z_{11} - Z_{12}\frac{Z_{21}}{Z_{22}+Z_{g22}}\\ Z_{pgeq} = Z_{g11}\end{cases} \tag{25}$$

where Z_{peq} and Z_{pgeq} are the positive-sequence equivalent SISO impedance of VSC and the grid. Z_{11}, Z_{12}, Z_{21}, and Z_{22} are the corresponding row and column elements of $(\boldsymbol{Y}_{\alpha\beta})^{-1}$.

From Fig. 12, it can be seen that if the VSC uses PQ outer loops and operates at unit PF with $P = 0.45$ p.u., the amplitude-frequency characteristic curves of Z_{peq} will intersect with Z_{pgeq} at 60 Hz, where the phase difference is 183°, which

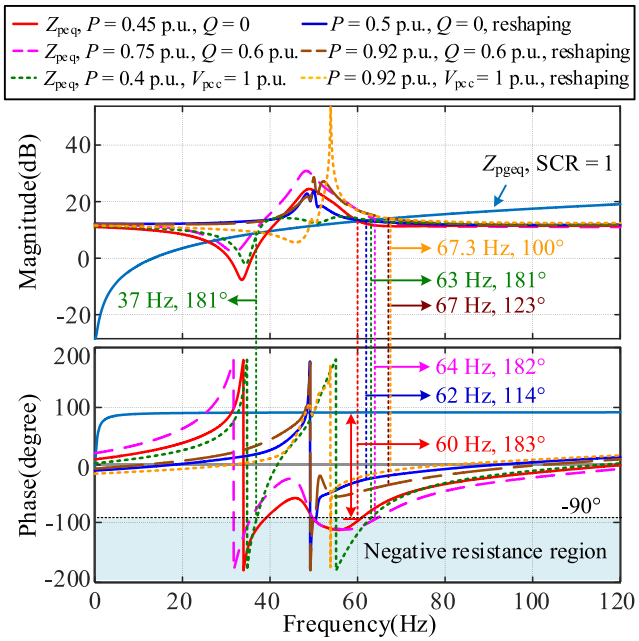

Fig. 12. Bode diagram of the equivalent SISO impedance model of the system with or without adopting the proposed reshaping method.

exceeds $-180° \sim 180°$, meaning the system has oscillation risk. Similarly, the system is also unstable when $P = 0.75$ p.u. and $Q = 0.6$ p.u., according to the phase difference at 64 Hz, i.e., 182°. The results are consistent with the DPL analysis using GNC in Fig. 8. Fortunately, when the proposed reshaping method is adopted, the negative resistance of Z_{peq} will be greatly reduced and the stability margin of the system will improve a lot. For example, when the reshaping method is applied and the output powers of VSC further extend to SPL, i.e., $P = 0.5$ p.u. with $Q = 0$ p.u. or $P = 0.92$ p.u. with $Q = 0.6$ p.u., the phase difference at intersection frequencies will reduce to 114° and 123°, respectively, which are far less than 180°, meaning the system is quite stable.

At the same time, the amplitude-frequency characteristic curves of Z_{peq} using PV loops will intersect with Z_{pgeq} at 37 Hz and 63 Hz when P is 0.4 p.u., where the phase differences are about 181°, indicating the oscillation will happen at 37 Hz and 63 Hz, which consistent with the DPL and oscillation frequencies mentioned in Fig. 9. Moreover, if the reshaping method is adopted and P further increases to 0.92 p.u., i.e., P_{op1} for SCR = 1 mentioned in Fig. 5, the negative resistance of Z_{peq} will be greatly reduced. At this time, Z_{peq} and Z_{pgeq} will intersect at 67.3 Hz, and the corresponding phase difference is 100°, indicating that the stability of the system also improves a lot, and the DPL is extended to SPL too. All of the results proved that the proposed reshaping method can reduce the influence of PLL and extend the DPL to SPL regardless of whether the PQ or PV outer loops are adopted.

C. Comparison of Different Stability Enhancement Method

To further highlight the advantage of the proposed reshaping method, a comparison with the existing VSC stability-enhanced method is presented in Table II, where four indicators are selected for comparison, i.e., the implementation complexity, robustness, parameter design criteria, and other stability issues.

1) *Implementation Complexity:* If the method contains higher order terms or iterative algorithms, it may increase the complexity of the controller and affect the calculating speed in engineering applications. This kind of method is classified as having high implementation complexity.
2) *Robustness:* If the method can work properly when system operating conditions and parameters vary, it can be classified as having good robustness.
3) *Parameter Design Criteria:* If the parameters can be quantitatively designed according to application scenarios, it can be classified as having detailed parameter design criteria.
4) *Other Stability Issues:* The method should improve the stability margin of the system and avoid causing other stability issues as much as possible.

Based on these four indexes, it can be seen that compared to the existing methods, the proposed method can greatly reduce the PLL influence contained in the inner current loop, thus improving the DPL of VSC a lot. Meanwhile, only two feedforward branches are added in the inner loop, which is easy to implement with detailed design criteria. Moreover, the steady-state values are replaced by the current references and modulating signals, which ensures the robustness of the method under different system operating conditions.

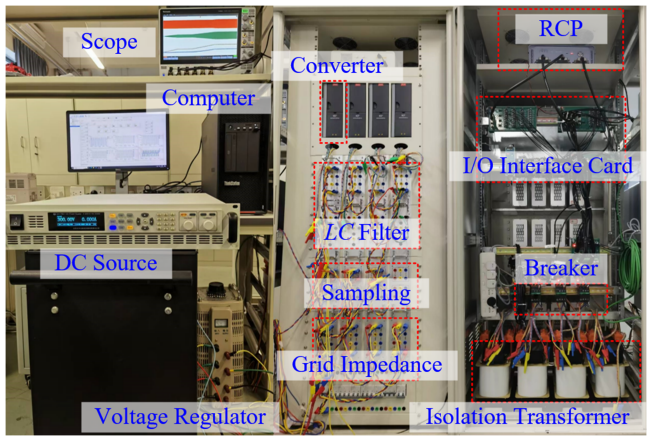

Fig. 13. Experimental platform of a grid-connected VSC with outer PQ or PV control loops.

V. Simulation and Experimental Verification

To verify the correctness of the theoretical analysis and the effectiveness of the proposed impedance reshaping method, a hardware experimental platform of a grid-connected VSC is built in the laboratory, as shown in Fig. 13. The system parameters are the same as the theoretical analysis, which are listed in Table I.

A. Steady-State Operation Validation

Fig. 14 shows the experimental waveforms of the PCC voltage, output current, and the active/reactive power of VSC with

TABLE II
COMPARISON OF ADVANTAGES AND DISADVANTAGES OF DIFFERENT VSC STABILITY-ENHANCED METHODS

Methods	Implementation complexity	Robustness	Parameter design criteria	Other stability issues
Damping controllers [16], virtual impedance [17], or filters [18], [19]	Low	Poor	Not fully discussed	Yes
Direct power control [22], [23]	Medium	Good	Yes	Yes
Observer-based controllers [24]	High	Good	Yes (but complex)	Not mentioned
Adaptive H_∞ control method [25]	High	Good	Yes (but complex)	Not mentioned
PSC [26], VSG [27]	Medium	Good	Yes	Yes
Symmetric PLL [29]	Low	Good	Yes	Yes
Proposed method in this article	Low	Good	Yes	Not found

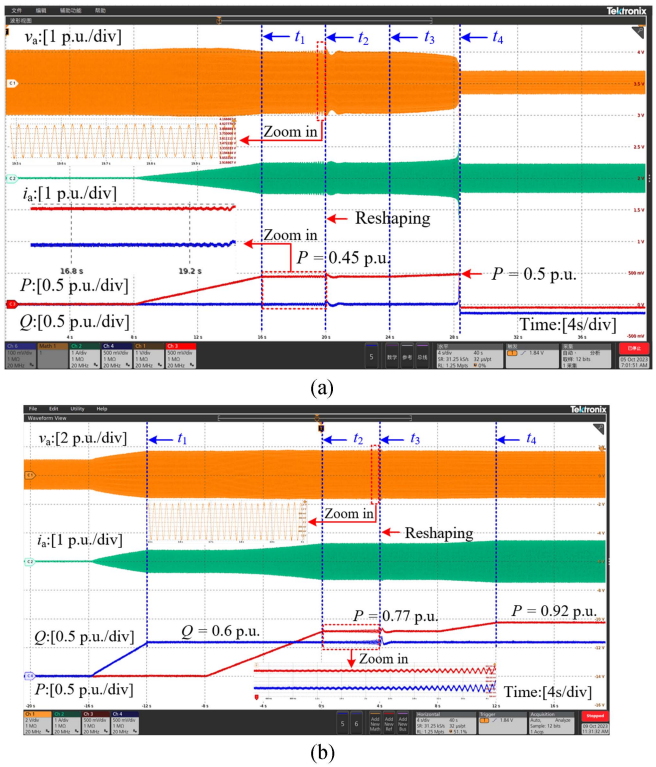

Fig. 14. Experimental waveforms of improving VSC power transfer capacity with PQ control loops by reactive power injection or proposed reshaping method. (a) $Q = 0$ p.u. (b) $Q = 0.6$ p.u.

outer PQ control loops, where the impedance reshaping method is not added at the beginning. In Fig. 14(a), the reactive power Q is kept at 0 p.u.. At $t = t_1$, P is increased to 0.45 p.u., it can be seen that the system loses its stability and starts to oscillate, which is consistent with the theoretical DPL analyzed in Fig. 8(a). Then, the proposed impedance reshaping method is introduced at $t = t_2$, the oscillation is, thus, suppressed, and the system returns to stable. Further increasing P at $t = t_3$, the system is still stable. However, when P is improved to a little more than the SPL, i.e., 0.5 p.u., at $t = t_4$, the system collapses, and the protection system is triggered. The experimental results prove that the proposed reshaping method can improve the stability margin of the system and extend the DPL of VSC almost to SPL. However, due to $Q = 0$ p.u., the SPL is limited at 0.5 p.u..

Fortunately, when extra reactive power is injected into the grid, the DPL can be improved. For example, the reactive power of VSC is increased to 0.6 p.u. at $t = t_1$, as shown in Fig. 14(b), and then the active power is increased gradually. From it, it can be seen that the DPL is improved to about 0.77 p.u., which is close to the theoretical value obtained in Fig. 8(b). Then, adopting the reshaping method at $t = t_3$, the oscillation is suppressed, and P can be further extended to 0.92 p.u., which is consistent with $P_{\rm op}$ obtained in Fig. 3. The experimental result validates that extra reactive power injected into the grid can improve the SPL as well as DPL of the VSC. Meanwhile, when the reshaping method is applied, the DPL can be almost extended to SPL.

Fig. 15(a) further shows the experimental results when outer PV loops are used, where the impedance reshaping method is adopted at $t = t_2$. From it, it can be observed that when the output active power of VSC increases to 0.37 p.u. at $t = t_1$, the system loses its stability and an oscillation occurs. Fast Fourier transformation (FFT) is performed for PCC voltage during $t_1 \sim t_2$, and the result is shown in Fig. 15(b). It can be seen that the oscillation frequencies are 61 Hz and 39 Hz, which almost agree with the theoretical analysis results in Fig. 9(b). Fortunately, when the proposed reshaping method is adopted at $t = t_2$, from Fig. 15(a), it can be seen that the oscillation is suppressed, and the system returns stable. Furthermore, increasing P to 0.92 p.u. at $t = t_3$, i.e., the $P_{\rm op1}$ obtained in Fig. 5, it can be found that the system still runs stably and the oscillation did not occur again. The experimental result verifies that the proposed impedance reshaping method can effectively improve the stability margin of the system and extend the power transfer capability of VSC to SPL when outer PV loops are adopted.

B. Transient Operation

It should be mentioned that when the VSC is connected to the grid, except for the above steady-state operating conditions, many transient scenarios, such as power step, voltage sag, frequency deviation, and SCR variation may also occur. Therefore, the effectiveness of the proposed method in transient scenarios also needs to be tested. Fig. 16 shows the experimental waveforms of adopting the proposed reshaping method to improve

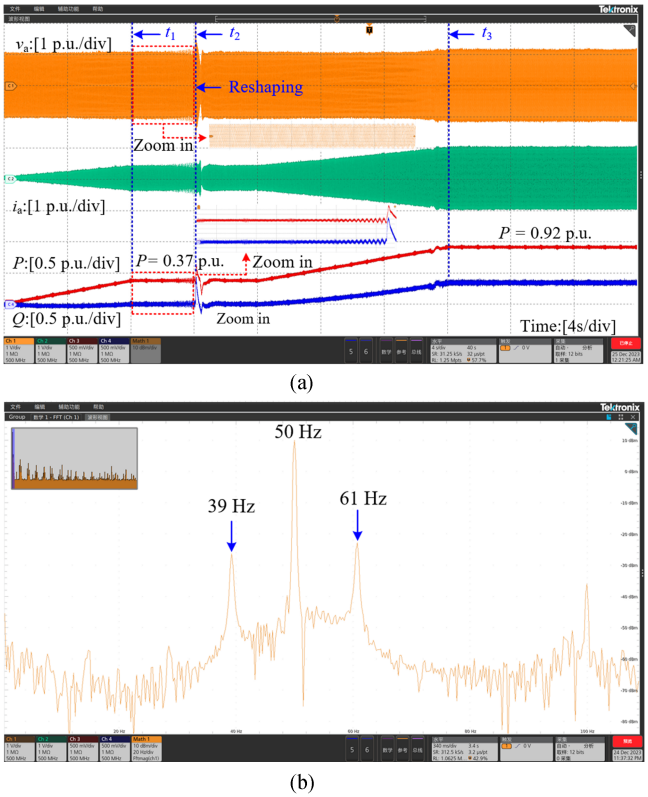

Fig. 15. Experimental waveforms of improving VSC power transfer capacity with PV control loops by proposed reshaping method and FFT analysis. (a) Experimental waveforms of the grid-connected VSC. (b) FFT analysis results of the PCC voltage waveform during $t_1 \sim t_2$.

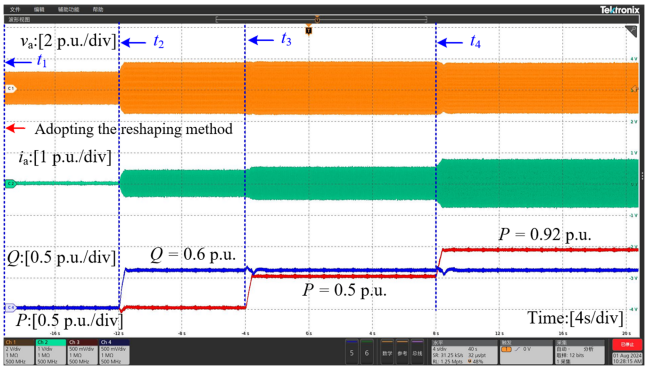

Fig. 16. Experimental waveforms of adopting the proposed reshaping method to improve the transfer power of VSC to SPL through power steps.

the transfer power of VSC to SPL through power steps, where the reshaping method is adopted first at $t = t_1$. Then, the reactive power Q steps up from 0 p.u. to 0.6 p.u. at t_2, and the active power P steps up to 0.5 p.u. and 0.92 p.u. at t_3 and t_4, respectively. It can be seen that similar to the result of extending DPL to SPL by slopes in Fig. 14(b), when the power step-up occurs, the VSC transfer power can be also improved to SPL stably. The experimental results validate the reshaping method can still improve the VSC power transfer capacity to SPL even if the power step happens.

Furthermore, the robustness of the proposed method against voltage sag, frequency deviation, and SCR variation is also tested

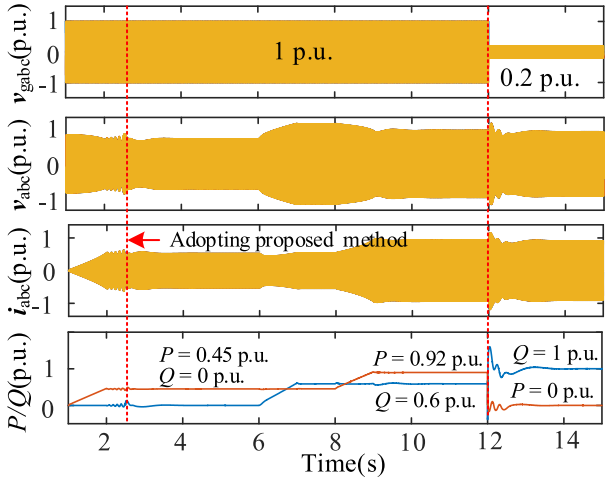

Fig. 17. Simulation waveforms of adopting the proposed reshaping method during an 80% voltage sag.

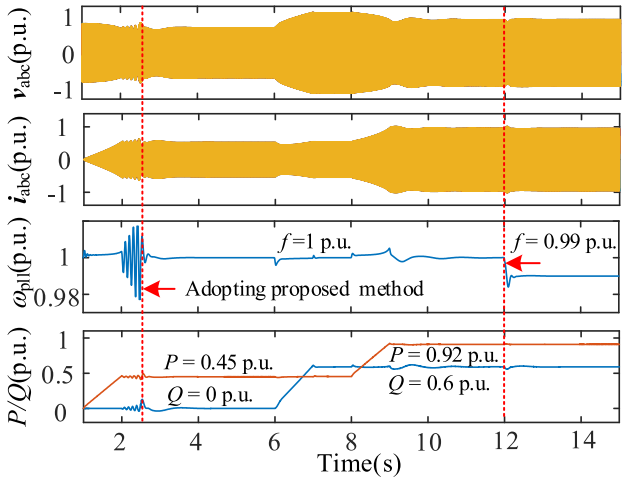

Fig. 18. Simulation waveforms of adopting the proposed reshaping method to improve DPL to SPL when the grid frequency varies.

by simulation results (These conditions are very difficult to change in our lab as the VSC is connected to the real power grid), as shown in Figs. 17–19. In Fig. 17, the reactive power Q is kept at 0 p.u. before $t = 6$ s, and the active power P is increased to 0.45 p.u. at $t = 2$ s. It can be seen the system loses its stability and starts to oscillate, which agrees with the DPL mentioned in Fig. 8(a). Then, increasing Q to 0.6 p.u., and P can be further improved to 0.92 p.u., i.e., the SPL. Finally, a voltage sag with an 80% sag happens at $t = 12$ s. According to the grid code [36], the active power P decreases to 0 p.u. and the reactive power Q jumps to 1 p.u. to support the PCC voltage. It can be seen that the system can still operate stably, which validates that the proposed reshaping method can still work properly during voltage sags.

The simulation results in Figs. 18 and 19 are the same as that in Fig. 17 before $t = 12$ s. At $t = 12$ s, the grid frequency changes to 0.99 p.u. and SCR jumps to 5 in Figs. 18 and 19, respectively. It can be seen that the system does not lose its stability, and the VSC can still operate at SPL stably even if the grid frequency or SCR varies. The simulation results verified

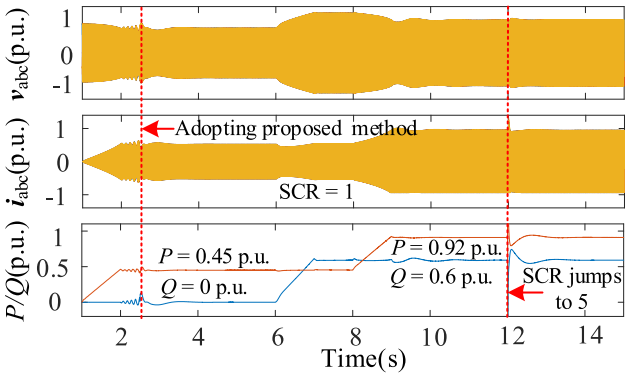

Fig. 19. Simulation waveforms of adopting the proposed reshaping method to improve DPL to SPL when the SCR varies.

that the proposed reshaping method can still improve the DPL to SPL during frequency deviation and SCR variation.

VI. Conclusion

In this article, the power transfer capacity of the VSCs with outer PQ or PV control strategies is analyzed in detail from two aspects, i.e., the SPL and DPL. Based on the steady-state algebraic equations of the system, the SPL of VSC with PQ or PV control loops is first analyzed from multiple dimensions, it is found that extra reactive power generation is beneficial to extend the SPL of VSC no matter using PQ or PV outer loops, especially under weak grid conditions. From the power system aspect, it means that the transfer power of the system will be improved when the voltages of key nodes are supported by the equipment itself or additional reactive power compensation devices. To extend the SPL as much as possible within the VSC power constraint, the optimal designed method for VSC power references is given, thus, the VSC capacity can be fully utilized in different grid conditions. Moreover, a comparative analysis for the SPL of VSC with PQ or PV control loops shows that when power constraint is considered, the SPL of VSC with PQ or PV loops is almost the same in the case of SCR $\geq$ 1. On the other hand, the DPL of the VSC with PQ or PV outer loops is also analyzed according to the impedance model of the system. An impedance reshaping method is proposed to reduce the PLL influence, thus, the DPL of the VSC can be almost extended to SPL. Finally, simulation and experimental results validate the correctness of the theoretical analysis and the effectiveness of the proposed reshaping method under different operating conditions.

References

[1] Y. Cheng et al., "Real-world subsynchronous oscillation events in power grids with high penetrations of inverter-based resources," *IEEE Trans. Power Syst.*, vol. 38, no. 1, pp. 316–330, Jan. 2023.

[2] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.

[3] Y. Song and F. Blaabjerg, "Overview of DFIG-based wind power system resonances under weak networks," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4370–4394, Jun. 2017.

[4] Y. Song and F. Blaabjerg, "Analysis of middle frequency resonance in DFIG system considering phase locked loop," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 343–356, Jan. 2018.

[5] H. Zhang, X. Wang, L. Harnefors, H. Gong, J.-P. Hasler, and H.-P. Nee, "SISO transfer functions for stability analysis of grid-connected voltage-source converters," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2931–2941, May/Jun. 2019.

[6] C. Zhang, X. Cai, M. Molinas, and A. Rygg, "On the impedance modeling and equivalence of AC/DC side stability analysis of a grid-tied Type IV wind turbine system," *IEEE Trans. Energy Convers.*, vol. 34, no. 2, pp. 1000–1009, Jun. 2019.

[7] J. A. Suul, S. D'Arco, P. Rodriguez, and M. Molinas, "Impedance-compensated grid synchronization for extending the stability range of weak grids with voltage source converters," *IET Gener., Transmiss. Distrib.*, vol. 10, no. 6, pp. 1315–1326, Apr. 2016.

[8] L. Huang, C. Wu, D. Zhou, and F. Blaabjerg, "A double-PLLs-based impedance reshaping method for extending stability range of grid-following inverter under weak grid," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4091–4104, Apr. 2022.

[9] D. Yang, X. Wang, F. Liu, K. Xin, Y. Liu, and F. Blaabjerg, "Adaptive reactive power control of PV power plants for improved power transfer capability under ultra-weak grid conditions," *IEEE Trans. Smart Grid*, vol. 10, no. 2, pp. 1269–1279, Mar. 2019.

[10] J. F. Morris, K. H. Ahmed, and A. Egea-Àlvarez, "Analysis of controller bandwidth interactions for vector-controlled VSC connected to very weak AC grids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 7343–7354, Dec. 2021.

[11] G. Wu et al., "Parameter design oriented analysis of the current control stability of the weak-grid-tied VSC," *IEEE Trans. Power Del.*, vol. 36, no. 3, pp. 1458–1470, Jun. 2021.

[12] L. Huang, C. Wu, D. Zhou, and F. Blaabjerg, "Comparison of DC-link voltage control schemes on grid-side and machine-side for type-4 wind generation system under weak grid," in *Proc. 47th Annu. Conf. IEEE Ind. Electron. Soc.*, Toronto, Canada, Oct. 2021, pp. 1–6.

[13] J. Z. Zhou, H. Ding, S. Fan, Y. Zhang, and A. M. Gole, "Impact of short-circuit ratio and phase-locked-loop parameters on the small-signal behavior of a VSC-HVDC converter," *IEEE Trans. Power Del.*, vol. 29, no. 5, pp. 2287–2296, Oct. 2014.

[14] H. Wu and X. Wang, "Design-oriented transient stability analysis of PLL-synchronized voltage-source converters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3573–3589, Apr. 2020.

[15] X. Wang, J. Yao, J. Pei, P. Sun, H. Zhang, and R. Liu, "Analysis and damping control of small-signal oscillations for VSC connected to weak AC grid during LVRT," *IEEE Trans. Energy Convers.*, vol. 34, no. 3, pp. 1667–1676, Sep. 2019.

[16] T. Zhou, Z. Chen, B. Ren, S. Bu, and P. Wang, "Damping torque analysis of VSC-HVDC supplementary damping controller for small-signal stability," *IEEE Access*, vol. 8, pp. 202696–202706, 2020.

[17] X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-impedance-based control for voltage-source and current-source converters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7019–7037, Dec. 2015.

[18] K. M. Alawasa, Y. A.-R. I. Mohamed, and W. Xu, "Active mitigation of subsynchronous interactions between PWM voltage-source converters and power networks," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 121–134, Jan. 2014.

[19] A. Akhavan, J. C. Vasquez, and J. M. Guerrero, "A robust method for controlling grid-connected inverters in weak grids," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 4, pp. 1333–1337, Apr. 2021.

[20] J. Fang, X. Li, H. Li, and Y. Tang, "Stability improvement for three-phase grid-connected converters through impedance reshaping in quadrature-axis," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8365–8375, Oct. 2018.

[21] M. Li et al., "The control strategy for the grid-connected inverter through impedance reshaping in q-axis and its stability analysis under a weak grid," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3229–3242, Jun. 2021.

[22] Y. Gui, X. Wang, and F. Blaabjerg, "Vector current control derived from direct power control for grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9224–9235, Sep. 2019.

[23] B. Hu, H. Nian, J. Yang, M. Li, and Y. Xu, "High-frequency resonance analysis and reshaping control strategy of DFIG system based on DPC," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7810–7819, Jul. 2021.

[24] F. M. M. Rahman, U. Riaz, J. Kukkola, M. Routimo, and M. Hinkkanen, "Observer-based current control for converters with an LCL filter: Robust design for weak grids," in *Proc. IEEE 9th Int. Symp. Sensorless Control Elect. Drives*, Helsinki, 2018, pp. 36–41.
[25] Z. Zhang, P. Wang, P. Jiang, F. Gao, L. Fu, and Z. Liu, "Robust control method of grid-connected inverters with enhanced current quality while connected to a weak power grid," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 7263–7274, Jun. 2022.
[26] L. Harnefors, M. Hinkkanen, U. Riaz, F. M. M. Rahman, and L. Zhang, "Robust analytic design of power-synchronization control," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 5810–5819, Aug. 2019.
[27] C. Li, Y. Yang, Y. Cao, A. Aleshina, J. Xu, and F. Blaabjerg, "Grid inertia and damping support enabled by proposed virtual inductance control for grid-forming virtual synchronous generator," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 294–303, Jan. 2023.
[28] D. Yang, X. Wang, and F. Blaabjerg, "Fast power control for VSCs to enhance the synchronization stability in ultra-weak grids," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, Portland, OR, USA, 2018, pp. 1–6.
[29] D. Yang, X. Wang, F. Liu, K. Xin, Y. Liu, and F. Blaabjerg, "Symmetrical PLL for SISO impedance modeling and enhanced stability in weak grids," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1473–1483, Feb. 2020.
[30] B. Hu, H. Nian, M. Li, Y. Liao, J. Yang, and H. Tong, "Impedance characteristic analysis and stability improvement method for DFIG system within PLL bandwidth based on different reference frames," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 532–543, Jan. 2023.
[31] L. Huang, C. Wu, D. Zhou, and F. Blaabjerg, "A power-angle-based adaptive overcurrent protection scheme for grid-forming inverter under large grid disturbances," *IEEE Trans. Ind. Electron.*, vol. 70, no. 6, pp. 5927–5936, Jun. 2023.
[32] C. Zhang, M. Molinas, A. Rygg, and X. Cai, "Impedance-based analysis of interconnected power electronics systems: Impedance network modeling and comparative studies of stability criteria," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2520–2533, Sep. 2020.
[33] X. Wang, L. Harnefors, and F. Blaabjerg, "Unified impedance model of grid-connected voltage-source converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1775–1787, Feb. 2018.
[34] Y. Li and Z. Du, "Stabilizing condition of grid-connected VSC as affected by phase locked loop (PLL)," *IEEE Trans. Power Del.*, vol. 37, no. 2, pp. 1336–1339, Apr. 2022.
[35] C. Zhang, X. Cai, A. Rygg, and M. Molinas, "Sequence domain SISO equivalent models of a grid-tied voltage source converter system for small-signal stability analysis," *IEEE Trans. Energy Convers.*, vol. 33, no. 2, pp. 741–749, Jun. 2018.
[36] J. Sarbazi, A. A. Najafabadi, S. H. Hosseinian, G. B. Gharehpetian, and A. Khorsandi, "Effects of photovoltaic power plants grid code requirements on transient stability," in *Proc. 12th Smart Grid Conf.*, Kerman, Iran, 2022, pp. 1–7.

Xiaoling Xiong (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2007, 2010, and 2015, respectively.

From Feb. 2011 to Jul. 2012, she was a Research Assistant with the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong. Since 2015, she has been with North China Electric Power University, Beijing, China, where she is currently an Associate Professor. Simultaneously, she was with Aalborg University, Aalborg, Denmark, where she was a Visiting Postdoctoral with the Department of Energy Technology from Dec. 2018 to Nov. 2020. Her current research interests include HVdc system, modeling, analysis, and design power electronic systems and study the nonlinear behaviors in power electronic circuits.

Bochen Luo (Member, IEEE) was born in Hunan, China. He received the B.S. degree from Changsha University of Science and Technology, Changsha, China, in 2021, and the M.S. degree in 2024 from North China Electric Power University, Beijing, China, where he is currently working toward the Ph.D. degree with the School of Electrical and Electronic Engineering, all in electrical engineering.

His research interests include modeling, analysis, and design of converter-based power systems.