High-Efficiency Wide-Range RF Power Generation Systems With Discrete Power Back-Off From Multiple Inverters

Haoquan Zhang, *Student Member, IEEE*, Alexander S. Jurkov, Vladimir Kozitsky, Ky Luu, Anas Al Bastami, Grace Cassidy, Aaron Radomski, and David J. Perreault, *Fellow, IEEE*

***Abstract*—Industrial radio frequency (rf) power applications, such as plasma generation for semiconductor processing, require the delivery of rf power over a wide dynamic power range and across variable load impedances. It is desirable for the rf power system to maintain high efficiency, continuous power control, and fast dynamic response over the operating power range. This article introduces a scalable switched-mode power amplifier (PA) architecture and control approach suitable for such applications. This approach, which we refer to as multi-inverter discrete backoff (MIDB), losslessly combines the outputs of switched-mode PAs, and modulates the number of active PAs to provide discrete steps in rf output. It further employs discrete supply modulation and outphasing among groups of PAs for rapid, efficient, and continuous output power control over a very wide range. A system prototype is built with 4 GaN-based, zero-voltage switching Class-D PA units, 2-level discrete supply modulation, and calibrated Chireix outphasing. The system achieves and maintains high efficiency and continuous power control over the designed continuous-wave operating range of 5 W–1 kW, and dynamically over 5 W–5 kW, with micro-second level transient performance. The proposed system demonstrates reduced power losses compared with existing linear-amplifier based solutions.**

***Index Terms*—Chireix, GaN HEMTs, outphasing, plasma generation, radio frequency (rf), RF inverters, switched-mode power amplifiers (PAs), zero-voltage switching (ZVS) class-D.**

I. Introduction

SWITCHED-MODE radio-frequency (rf) power amplifiers (PAs), also known as rf inverters, are important in many industrial applications, e.g., plasma generation for semiconductor processing equipment. In plasma generation applications, the PAs typically operate into variable load impedances at high frequency (e.g., tens of MHz) and power levels (e.g., several kilo-watts of peak power), and often with wide overall power ranges and high peak-to-average power ratios [2], [3], [4], [5], [6], [7].

Received 5 March 2024; revised 29 July 2024; accepted 5 September 2024. Date of publication 10 September 2024; date of current version 12 December 2024. This work was supported by MKS Instruments Inc. An earlier version of this paper was presented in part at the 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL) [DOI: 10.1109/COMPEL49091.2020.9265702]. Recommended for publication by Associate Editor D. Dujic. *(Corresponding author: David J. Perreault.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3457535.

Digital Object Identifier 10.1109/TPEL.2024.3457535

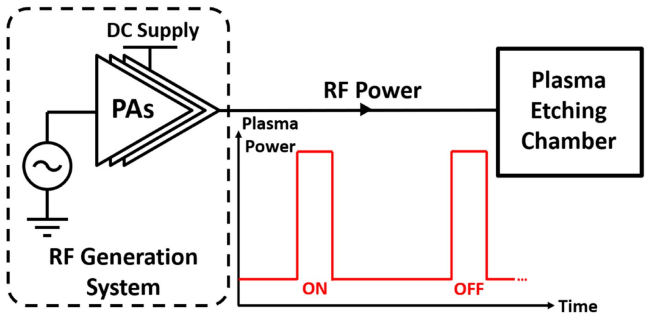


Fig. 1. High-level block diagram of industrial rf generation for semiconductor processing, and an example periodic RF power profile over time. The RF generation system requirements include high peak power levels, very wide output power range, and fast dynamic response, in order to accommodate the short-duration, high-power pulses with sharp transitions.

A. Overview and Target Application Scenario

Fig. 1 shows a high-level block diagram and an example power profile for such applications. To meet the evolving needs for semiconductor processing, goals for rf power generation systems in these applications include 1) operation across a very wide output power range (e.g., 1000:1 or 30 dB); 2) very fast dynamic response to output power commands (e.g., μs scale); 3) high peak and average efficiency (to reduce cooling requirements and electricity costs), and 4) operation over a wide load impedance range (as determined by the plasma load). The wide load impedance range can be addressed through high-speed tunable impedance matching (e.g., [8], [9]), or other impedance compressing techniques [10], [11], [12]. However, existing techniques based on linear amplifiers have difficulties meeting the remaining goals, and efficiency is often sacrificed to meet the other performance metrics, yielding solutions with excessive power ratings, complex cooling solutions, and poor peak and average power efficiencies. This article focuses on a rf power generation system with switched-mode PAs, with a scalable architecture, to achieve both high performance and

good efficiency. The key innovative aspects of the proposed approach include a dynamic "ON/OFF" control of constituent inverters to extend high-efficiency power range, together with an architecture that leverages discrete supply modulation and outphasing to achieve the target operating spec. The proposed approach also has value in a wide range of rf power applications with similar challenges, such as wireless power transfer, rf heating and welding, etc.

B. Prior Art

1) Outphasing: One important approach for efficient and fast power control used in the proposed architecture is outphasing, or phase-shift control [13], [14], [15], [16], [17]. In this technique, the outputs of two or more PAs (or blocks of power-combined PAs) are combined via a lossless network and phase-shifted such that output power is modulated through the variation in the vector sum of combined PA outputs, with individual PAs seeing effective load impedance variations. This approach has the advantage that it enables high-bandwidth output power modulation through rapid variations in phase-shift. However, outphasing alone has two key limitations in this context. First, because power backoff via outphasing addresses output-current-related losses in PAs, but not voltage-related losses, efficiency declines steeply at low power levels, reducing average efficiency in applications with high peak-to-average power ratios. This occurs because the constituent PAs in an outphasing system operate at reduced current under backed-off output power, but still at full voltage. Thus, loss components relating to output current (e.g., conduction losses) decrease with output power, but loss components relating to supply voltage (e.g., device output capacitor losses [18], [19], resonant losses to provide zero-voltage switching (ZVS) [20], [21], etc.) do not. Second, since outphasing relies on vector cancellation of the output voltage of PAs for power control, the achievable output power range can be limited by timing resolutions and/or mismatches between PAs, and cannot typically reach a large ratio such as 30 dB [22].

2) Supply Modulation: To further extend the output power range while maintaining efficiency, the proposed system also optionally leverages supply modulation (also known as drain modulation). In many supply-modulated systems, the PA's dc supply voltage is varied continuously (e.g., in [23], [24]), and is also sometimes called envelope tracking. However, in this application context, continuous supply modulation can incur significant cost, efficiency, and controller design overhead due to the hardware and control challenges in rapidly modulating supply voltages. On the other hand, discrete drain modulation (e.g., in [24], [25]), switches the supply voltage among a number of pregenerated dc sources, and hence has less efficiency overhead and control bandwidth challenges for system integration.

C. Proposed Approaches

To address the limitations of outphasing and supply modulation, this work proposes an additional way to control power, termed multi-inverter discrete backoff (MIDB). This technique losslessly combines the outputs of parallel-grouped (i.e., current-combined or voltage-combined) groups of switched-mode PAs, with outphasing among groups of PAs providing continuous and fast-response control of output power. In this approach, rather than outphasing between individual PAs, one outphases between two or more groups of PAs, with each group comprising several PAs with their outputs combined. The key idea of MIDB is that, by changing the number of active PAs within each PA group, we can achieve discrete steps in rf output voltage of the group, providing an extra degree of freedom in power control. This enables the degree of outphasing to be always kept within a reasonable range, yielding much higher average efficiency and wider backoff range than can be achieved with outphasing alone.

In terms of output power control, both discrete drain modulation and MIDB can provide discrete steps in rf voltage magnitudes to be used together with outphasing. However, an advantage of the MIDB-based architecture is that it is highly modular and mitigates the supply generation and modulation overhead from multilevel discrete drain modulation alone. In addition, MIDB offers greater flexibility in discrete rf voltage levels than can be achieved with only drain modulation, as the allowable supply voltage modulation range is often limited by device capacitance nonlinearity, where below a certain supply voltage level, changes in device capacitance can severely harm PA performance. In the proposed system, we advantageously combine the two approaches, achieving very wide power range capability as well as low hardware complexity.

In summary, the proposed rf PA architecture employs 1) outphasing, for fast-response, continuous output power control, 2) the MIDB technique, which discretely modulates output power through discrete output voltage modulation, achieved by turning PAs ON/OFF in a PA-group, and 3) discrete drain modulation to further expand the high-efficiency operating power range of the system. In doing so, the proposed architecture can maintain high efficiency, together with fast and continuous control across a very wide power range.

The proposed approach builds upon previous techniques but is substantially distinct in both its system architecture and its power control methodology. While discrete power modulation through PA ON/OFF switching has been explored in linear amplifiers for power control [26], [27], it has not been widely exploited for use with high-efficiency switched-mode PAs, and the application space is different (e.g., for mm-wave ICs). The use of variable numbers of paralleled PAs with outphasing for a similar application has been explored independently and in parallel with this work in [1], [17], [28]. However, while the approach of [28] has some of the features and merits of the MIDB technique described here, it operates using a somewhat restrictive "combinerless" structure [29], with different practical characteristics that impose significant load variations on its constituent amplifiers (including reverse power flow), resulting in limits on circuit topologies and operating range. Moreover, previous systems have not utilized PA ON/OFF switching together with discrete drain modulation to achieve high performance across wide operating conditions.

The rest of the article is organized as follows. Section II describes the structure of the proposed power generation system and output power control scheme, and Section III discusses the implementation details of key functional blocks of the system. Experimental setup and results are presented in Section IV.

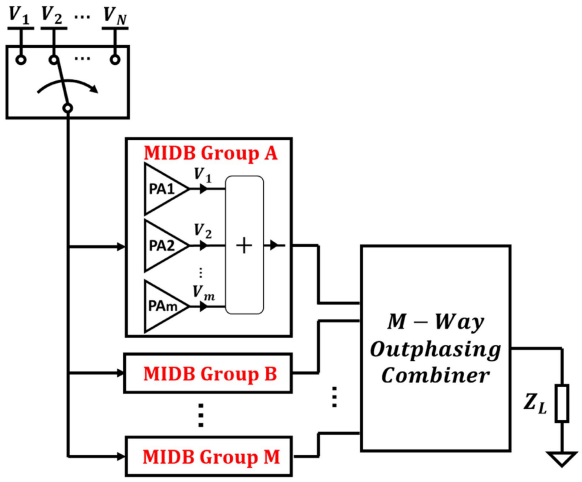


Fig. 2. Generalized block diagram of the proposed rf plasma power generation architecture: The M MIDB PA groups are powered from a DC supply selected from N levels. Each group comprises m ON/OFF controlled, in-phase PA units that are power-combined. The M rf outputs from the groups are outphased against one another via an M-way outphasing combiner. The output of the outphasing combiner is interfaced with the load Z_L (e.g., a plasma chamber load transformed through a TMN. The following Sections II-B–II-F discuss the design considerations and elaborate on the implementations of these functional blocks.

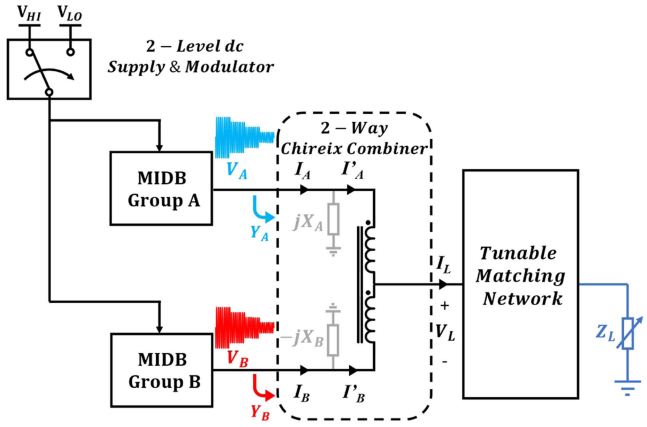


Fig. 3. More specific implementation of the rf generation system, with 2 DC sources powering 2 MIDB PA groups. The rf output voltage from the groups (V_A, V_B) are outphased and combined with a lossless combiner (illustrated here as a Chireix-type combiner with asymmetric shunt reactive compensation (jX_A & $-jX_B$) for more effective power range control. The output of the combiner (V_L) interfaces with the load (Z_L) through a TMN.

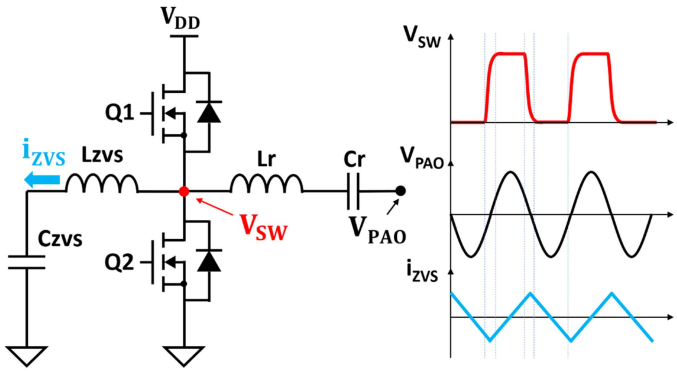


Fig. 4. ZVS Class-D inverter circuit as a PA unit in the proposed system, together with key operating waveforms. The two transistors each conduct an equal amount of time in a switching period, the series $L_r - C_r$ filter is tuned to resonance at the switching frequency, and the $L_{zvs} - C_{zvs}$ shunt leg provides additional inductive loading (i_{ZVS}) at the switching node to assist the transistors in achieving ZVS even as the load seen by the PA varies within a moderate range.

Finally, Section V concludes this article. Further, Appendix A outlines a system optimization procedure with a target power profile, and Appendix B discusses a method to measure PA load impedance under outphasing.

II. MIDB System Structure and Operation

This section begins with an overview and then discusses the structure of each functional block in the proposed rf power generation system. The major blocks include the MIDB-based PA architecture, the individual PA units, the associated power control technique, and the optional discrete supply modulator. A brief discussion on potential implementations of the impedance transformation subsystem is also given.

A. Overview

Fig. 2 illustrates a general high-level structure of the proposed power generation system including N-level discrete drain modulation, M PA groups each comprising m PAs with outputs combined via an m-way combining system, and the groups' power outputs are combined via an M-way outphasing combiner. Fig. 3 shows a more specific implementation with $N = 2$, $m = 2$ and $M = 2$, in other words, we use a two-level supply modulator to supply two groups of PAs, with the two groups outphased and power-combined via a two-way Chireix combiner. The rest of this section focuses on this example implementation and discusses its structure and operating principles in detail.

B. PA Unit

Each block labeled "PA" in Fig. 3 refers to an individual switched-mode rf PA, also known as an rf inverter. The characteristics of a suitable rf PA for the proposed system include 1) high efficiency at the required switching frequency range (e.g., 13.56 MHz), 2) capable of efficient ac grounding of its rf output for MIDB control (or other connections as required for turning "OFF" an individual PA), 3) capable of maintaining efficiency with moderate variations in load impedance (for outphasing and for easing requirements on impedance transformation), and 4) capable of fast dynamic response in output power, e.g., in the present context, to step changes in outphasing angle, ON/OFF status, and supply level.

Numerous candidate PA designs exist for this function, such as the ZVS class-D inverter [30], the single-switch class-E inverter (e.g., in [30] and [31]) and the class-Φ_2 inverter (e.g., in [32]). PA variants which are tolerant of load impedance variations (e.g., resistive load variation) are usually preferred. In particular, the ZVS Class-D inverter shown in Fig. 4 has low voltage stress on the devices and can maintain ZVS and hence high efficiency for a moderate range of load variation [20], [30] (e.g., during

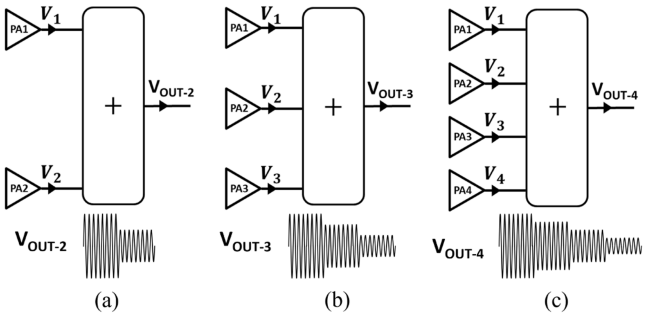


Fig. 5. Example MIDB group configurations, with 2, 3, and 4 PA units in each group. The PA output are combined in common-mode such that the output voltage is the average of all PA output voltages with uniform weight, and the output current is the sum of all PA output currents with equal magnitudes. Discrete output voltage modulation is thus achieved by turning PAs ON/OFF.

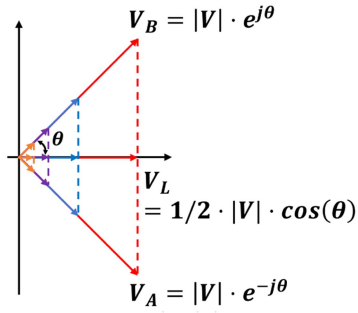


Fig. 6. Voltage vector graph of the power generation system. V_A and V_B represent the output voltages of the two MIDB PA groups. The load voltage V_L can be controlled through both the outphasing angle θ (i.e., the phase shift across the two MIDB groups), and the magnitude of the MIDB block output voltage $|V|$ (i.e., combined effects from drain modulation and PA ON/OFF control). With 2-level supply modulation and MIDB-2 configuration, 4 discrete steps in $|V|$ are available. Note that this graph shows the vector operation of uncompensated Chireix outphasing, and in practice some form of compensation (such as the asymmetric shunt reactances jX_A, $-jX_B$ from Fig. 3) is often introduced to improve the load impedance characteristics imposed on the PAs [30].

output power modulation through outphasing control), and is a promising candidate as the PA unit. With the ZVS-Class D PA unit, when the PA is "ON", both switches are actively switching and each conducts for approximately half of a switching period, and when the PA is "OFF", one switch is turned OFF while the other conducts constantly, effectively ac grounding the output port and lowering the output voltage amplitude of the MIDB group. Other unit selections are also possible as long as they possess the desired characteristics, and similar ON/OFF modulation strategy applies. In some PA types, such as class-E, class- Φ_2 etc., one may require an additional switch to disconnect the PA from the input power supply when the PA is in the "OFF" state, and the PA transistor itself may be held on to provide the desired ac ground.

C. MIDB-Based PA Architecture

The MIDB PA groups (shown in Fig. 3 as A and B) are constructed identically, and each consists of a group of power-combined rf PAs so that the amplitude of the rf output voltage from the blocks (V_A and V_B) can be modulated among discrete levels (by turning the PAs ON and OFF inside each group). Fig. 5 illustrates example configurations of such a PA group, with $m = 2$, 3, and 4, respectively, dubbed MIDB-m.

Within the same group, all constituent PAs are combined with common-mode power combiners, in which the output current of each PA is identical, and the group output voltage is a weighted sum (e.g., the average) of the individual PA outputs. For instance, in the case of Fig. 3, we have $I'_A = I'_B = I_L/2$, $V_L = (V_A + V_B)/2$). This can be implemented with, for example, an m-way interphase transformer, or cascaded two-way transmission-line-based power combiners [15], [16], [33], [34]. In addition, nonuniform weights can be assigned to each PAs when voltage or current-combining, e.g., binary weighted, in order to gain more flexibility in the available number of discrete levels, although this may lead to asymmetrically distributed losses and reduced system modularity and scalability. Further, a uniform number of active PAs may be preferred across MIDB groups for high-performance power combining.

Therefore, by turning all PAs ON, peak output voltage and power is achieved, which can be reduced in discrete steps by turning OFF, i.e. ac grounding, the outputs of PAs simultaneously in groups A and B. This has the additional benefit of supplying rf current through paths with reduced resistance, since the switch resistances from PAs in the "OFF" state is much less than those from the actively switching PAs due to the dynamic $R_{\text{ds,on}}$ effect [35].

D. Output Power Control

In general, the very wide output power control range is achieved with the combined effects of 1) discrete steps in rf output voltage (through MIDB on/off control, optionally along with discrete drain modulation) and 2) fine, continuous tuning of rf output voltage (via outphasing among the MIDB groups).

Fig. 6 illustrates the system output power control scheme as a vector graph. The magnitude of the load voltage ($|V_L|$) directly correlates to the output power ($P_{\text{out}} \propto |V_L|^2$), and can be modulated through the combined effects of outphasing and MIDB modulation. Outphasing provides continuous control as the phase shift can be continuously varied. However, the range over which the PAs can remain efficient through outphasing alone is limited. On the other hand, large, discrete power steps, by switching to a different supply rail or MIDB ON/OFF configuration, enable rescaling of the output power for a given outphasing angle. By combining the discrete power steps with outphasing adjustment, a very wide continuous power range can be achieved at high efficiency.

An example situation is helpful to illustrate how the control mechanism functions and maintains high system efficiency over a wide power back-off range. Suppose the system operates at peak power, with the highest supply rail, and all MIDB PAs active. We can gain some power range by leveraging outphasing, however, at a certain point the PAs will become less efficient when the outphasing angle θ approaches extreme ends (e.g. due to disproportionate reactive loading on the PAs [30]). Therefore, if we discretely modulate the output voltage, by either grounding a PA in each MIDB block or by switching to the lower supply rail,

we can achieve the same output power but with an outphasing angle more conducive to desired loading range of the PAs. Further examples of the control system in action can be found in [36].

E. Power Supply and Modulator

To further extend the achievable output power range, and reduce the voltage-related losses (e.g., transistor C_{oss}-related losses and ZVS resonance losses) of the PAs, which become dominant at low power levels, the proposed system also leverages discrete supply modulation. However, with increasing number of discrete drain voltage levels, the multilevel voltage generation and modulation requirements become higher, and may begin to negatively impact the system in terms of complexity, cost, and overall efficiency [37], [38]. It is therefore important to select an appropriate number of discrete voltage levels in order to achieve high overall efficiency, power range, and fast response speed, while keeping the cost and complexity low. It should also be noted that for many devices, the allowable supply voltage range that can be used is limited by the nonlinearity of semiconductor device capacitances. Often, below some supply voltage level, device capacitances increase radically, which can cause deteriorated inverter performance from mis-tuning and/or loss of ZVS.

In many implementations of the proposed system, two discrete drain voltage levels suffice, enabling the system to achieve wide power range and high efficiency with very limited supply generation and modulation overhead. In such designs, it may be preferable to select the lower supply voltage level at or just above the lowest voltage level before the semiconductor device capacitance nonlinearity substantially hurts PA performance.

F. Load Impedance Transformation

If direct interface with a variable load is required (e.g., as presented by a plasma chamber), the system may also include an impedance transformation stage that transforms and matches the variable rf load Z_L into a particular impedance (or a narrowed range of impedances) desired by the PA system. Depending on the specific application scenarios, one or more of the tunable matching techniques or load compression techniques in [8], [9], [10], [11], [12], and [39] may be desirable. Appendix C discusses further design considerations for this block.

III. MIDB System Implementation

This section discusses several key aspects of implementing the rf generation system. The prototype system is rated for 1 kW continuous operation, and dynamically cover an even wider power range of 30 dB (or 1000:1) from 5 W to 5 kW. Follwoing the optimization procedure detailed in Appendix A, a prototype power generation system design is obtained as shown in Fig. 7, with two-level discrete supply modulation, two PAs per MIDB group, and outphasing between the outputs of the two MIDB groups. The system also employs Chireix outphasing with shunt compensation and half-bridge ZVS Class-D PA units. We detail the design of the Class-D PA circuit, its associated supply modulators and performance enhancement techniques, then we discuss the power combining techniques and Chireix outphasing mechanism.

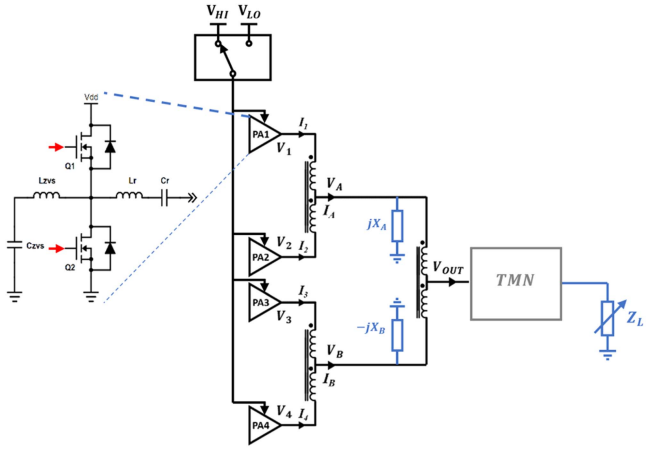


Fig. 7. Prototype rf power generation system with an MIDB-2 structure and 2-level discrete supply modulation.

A. PA Unit

The switched-mode PA units are the major building block of the system. Key PA design goals include maintaining high efficiency against a moderate amount of load impedance variations (as expected from outphasing); fast dynamic response (for startup, shutdown and supply voltage changes); and good efficiency at high frequency and high power.

1) Supply Modulator and Dynamic Enhancements: In the prototype system, the dc supply rail is modulated between two pregenerated voltage levels in order to cover a wide power range while maintaining high efficiency and fast dynamic response. Here, we discuss an implementation of the discrete supply modulator, working in conjunction with how the PA unit is designed to achieve good dynamic transient performance.

As shown in Fig. 8, the PA drain voltage (V_{Supply}) is selected from one of two pregenerated dc voltage levels (V_{HI} and V_{LOW}) through a pair of selector switches Q_{HI}, Q_{LO}. This configuration enables low steady-state modulator loss and simplifies gating control. A further improvement is made on the ZVS Class-D PA unit. After the PA supply rail V_{Supply} is toggled (e.g., from V_{LO} to V_{HI}), the average dc voltage at V_{SW} will vary accordingly (e.g., from $V_{\text{LO}}/2$ to $V_{\text{HI}}/2$). This leads to the need to rebalance the ZVS capacitor's dc-blocking voltage, potentially delaying settling during the supply voltage transition. To minimize the transient response duration and device stress during supply transitions, the ZVS capacitor is equally split and connected to ground and V_{Supply}, respectively. Compared to the single, ground-referenced C_{ZVS} design, this modification allows automatic rebalancing of dc-blocking voltages with supply voltage transients and reduces transient losses. Of course, to minimize losses associated with changing the ZVS capacitor bias values, the ZVS capacitor values should be made as small as practically

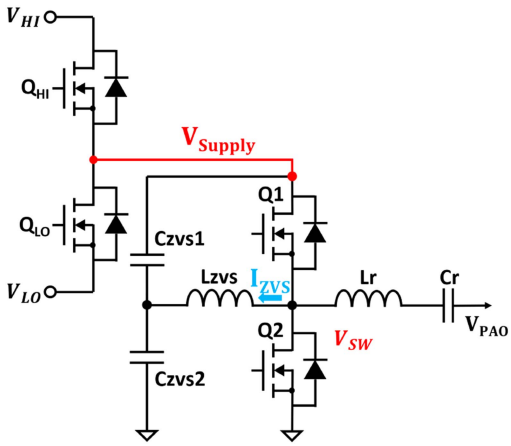


Fig. 8. Two-level supply modulator and a half-bridge ZVS Class-D PA unit designed for supply-voltage modulation. The ZVS capacitors are equally split and referenced to both ground and DC supply, reducing the operation transient during supply voltage transitions.

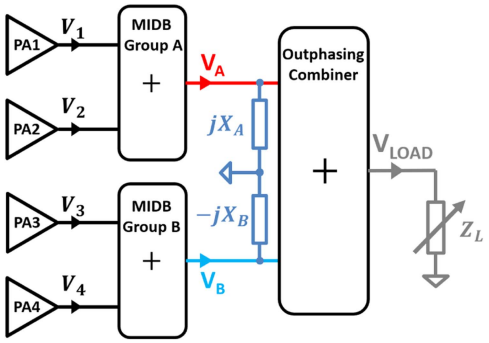


Fig. 9. Block diagram of the power combiner network, with three combiners merging power from 4 PA units. Two power combiners performs in-phase ON/OFF power combining in MIDB PA groups A and B, and another combiner enables Chireix-style outphasing with shunt reactive compensation (shown as jX_A and $-jX_B$).

allowed. In addition, some practical aspects on supply modulator design for voltage transition optimizations are discussed in [36].

It should be noted that the dc voltage on C_r also needs to rebalance during supply transitions. As this resonant capacitor is small, however, the duration for the rebalancing is acceptably short. Were faster response required, one could move from half-bridge PA units as in Fig. 8 to full-bridge PA units (with appropriate differential-to-single-ended conversion at the PA unit output). With a full-bridge design, the ZVS inductor can be connected differentially between the two half bridges, such that the ZVS capacitor can be eliminated, which also eliminates any transient losses associated with it.

B. Power Combining

As the rf generation system leverages MIDB ON–OFF control and also outphasing control between MIDB-combined groups, a high-performance combiner network is needed. The overall combiner network concept is presented in Fig. 9, with two MIDB combiners carrying out in-phase ON/OFF power combining, and another combiner between the phase-shifted outputs of MIDB PA groups, V_A and V_B.

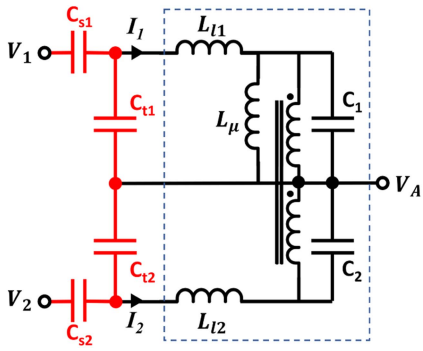


Fig. 10. Circuit showing the structure of the transmission-line-based power combiner for MIDB Group A from Fig. 9. $L_{l1,l2}$ are leakage inductances, L_μ is the magnetizing inductance, and $C_{1,2}$ are parasitic capacitances. The detailed model derivation can be found in [34].

In essence, the combiner network ensures that 1) the MIDB on/off control within a PA group is reflected at the output port of the group, as shown in Fig. 5, and 2) the phase-shifts introduced across MIDB groups can modulate the load voltage power, and the impedance variations seen by each constituent PAs are balanced, and will not become overly inductive or capacitive such that it leads to significant efficiency drops.

Fig. 10 shows a detailed structure of the combiner, where the circuit inside the dotted box models the combiner itself, and the four capacitors shown in red are added externally. This combiner acts closely to an ideal "interphase transformer" where the rf current from the PAs ($I_{1,2}$) are equal and the combiner output voltage (V_A) is a weighted sum of the two PA voltages ($V_{1,2}$). At the target operating frequency of around 13.56 MHz, the two series capacitors $C_{s1,2}$ serve to resonate out the combiner leakage inductances $L_{l1,2}$, and the two shunt capacitors $C_{t1,2}$ fine-tunes the parallel resonance with the combiner magnetizing inductances L_μ and parasitic capacitance $C_{1,2}$. The other combiners have similar structures. Further details regarding combiner design and modeling are extensively discussed in [33], [34], [36].

The measured PA load impedance levels versus a range of outphasing angle is shown in Fig. 11, these are measured using the technique described in Appendix B. It can be observed that over the outphasing operating range (approximately 30°–60°), the resistive portion of the two load impedances matches closely, while the reactive portion stay mostly inductive and close to zero, as expected from Chireix-style outphasing.

IV. Experimental Setup and Results

A hardware prototype system is built following the MIDB concepts in Section II and the implementation techniques in Section III. To validate the proposed concepts, this section outlines the test environment setup, and presents the experimental results both for continuous operation (termed continuous-wave or CW), and for the periodic dynamic pulsing operations typically seen in industrial plasma generation applications.

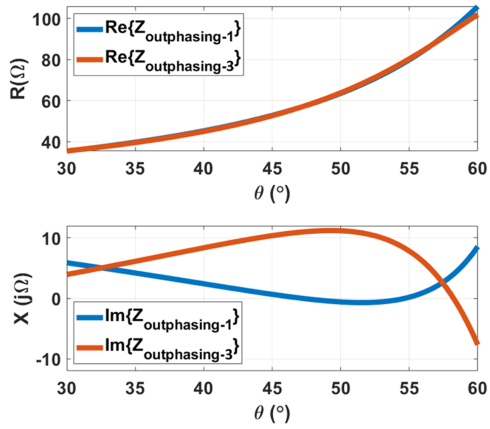


Fig. 11. Measured load resistances (R) and reactances (jX) seen by the PAs versus outphasing angle θ.

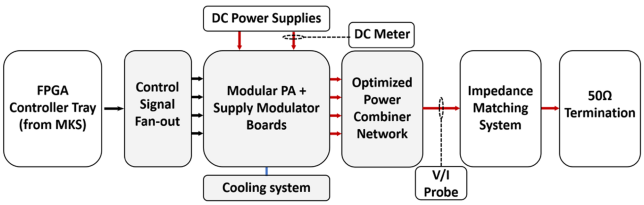


Fig. 12. Block diagram of test environment.

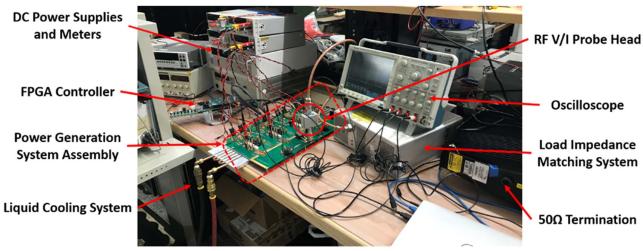


Fig. 13. Annotated photograph of the test environment.

A. Test Environment Setup

A block diagram of the experimental setup is given in Fig. 12 and a corresponding photo of the setup is shown in Fig. 13. The system-under-test is the prototype rf power generation system whose block diagram is presented in Fig. 7. A list of external supply and test equipment is given in Table I and the key prototype circuit components and parameters are listed in Table II.

The rf generation system uses an industrial FPGA controller tray, which takes in control commands sent by a laptop and generates logic control signals for the PAs and supply modulators. Two dc power supplies with different dc voltage levels ($V_{\mathrm{HI}} = 310\,V$, $V_{\mathrm{LO}} = 100\,\mathrm{V}$) are used to provide input power to the system-under-test. The prototype system includes 1) a controller interface board, which processes the logic control signals and distributes them to individual boards; 2) four sets of modular boards, each containing a ZVS Class-D PA unit and its local discrete supply modulator; and 3) a combiner network board, performing in-phase MIDB power combining and Chireix outphasing together with shunt impedance compensation. A liquid cooling system is used for the PA boards, consisting of a cold-plate on which the boards are mounted, and a circulation pump (Koolance ERM-3K3U). A close-up photo of the interface-PA-combiner board assembly is given in Fig. 14.

The system is designed for application scenarios in which a dynamically varying load impedance (e.g., from a plasma

TABLE I
EQUIPMENT IN EXPERIMENTAL SETUP

Description	Model
DC V/I Meter	Agilent 34401A
DC Power Supply (V_{HI})	Xantrex XDC 600-10
DC Power Supply (V_{LO})	HP 6010A
DC Power Supply (Control)	Keithley 2420
Controller	MKS Instruments Novina FPGA
RF V/I Probe	MKS Instruments #000-1106-117
Tunable Matching Network	MKS Instruments MW2513
50 Ω Termination	Bird 8890-300SC13
Oscilloscope	Tektronix MSO4104
Voltage Probe	LeCroy PPE 4 kV
Thermal Camera	FLIR E6

TABLE II
PROTOTYPE SYSTEM COMPONENTS AND PARAMETERS

Description	Model
Modulator Switch (Q_{HI}, Q_{LO})	Infineon Si IPT60R028G7
PA Switch (Q_1, Q_2)	Infineon GaN IGLD60R190D1
PA Resonant Inductance (L_r)	415 nH nominal*
PA Resonant Capacitance (C_r)	330 pF nominal, 1.5 kV C0G
PA ZVS Inductance (L_{ZVS})	520 nH nominal
HV Supply (V_{HI})	310 V
LV Supply (V_{LO})	100 V
MIDB A Compensation (jX_A)	158 nH
MIDB B Compensation ($-jX_B$)	747 pF
MIDB Combiner	RG316/25 on Fair-Rite 2861010002
Outphasing Combiner	HF141-12 on Fair-Rite 2861010002

*: System performance is not impacted with <5% part-to-part variations.

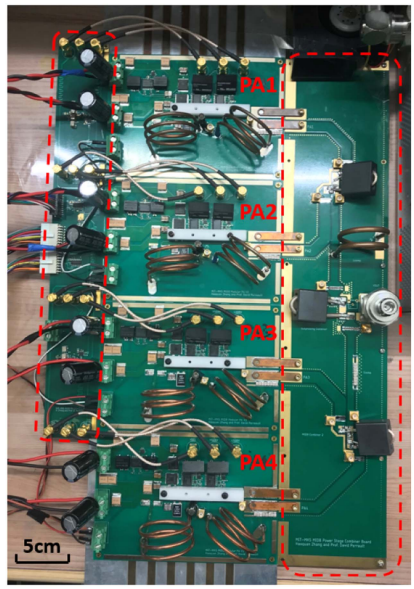


Fig. 14. Close-up photograph of the controller interface board (left), the modular PA boards (PA1-PA4, middle), and the combiner network board (right).

Fig. 15. Thermal image of the hotspot (PA3 Q2) when the system is operating at approximately 1.2 kW, slightly above the full rated power for continuous operation.

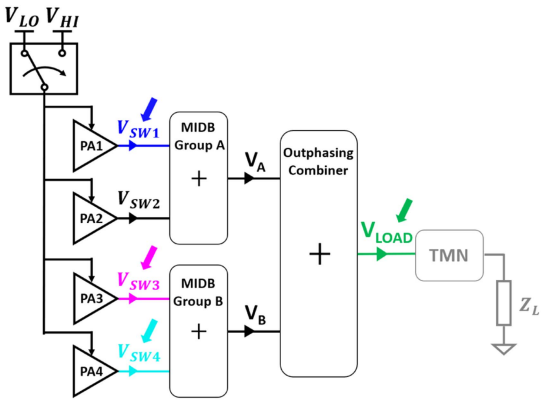


Fig. 16. Diagram of the prototype rf power generation system illustrating key nodes for oscilloscope voltage probing.

chamber) is transformed to a target load impedance via a tunable matching network (TMN). The rf generator system is designed to deliver power to a custom load impedance level (approximately 3.1 Ω), for which the rf generation system performance is optimized. For testing purposes, an impedance matching system is utilized to synthesize the desired 3.1 Ω load impedance Z_{Load} from a fixed 50 Ω load. In addition, in order to evaluate the system efficiency, dc voltage, and current meters are used to measure the total input power, and an rf V/I probe (MKS#000-1106-117) is placed at the output port to sense the rf output power.

B. CW Measurement Results

This section presents experimental results of the system for CW. The prototype is designed to allow CW operation at up to 1 kW. Here, we show system operation across the outphasing control range for three states: 1) V_{LO} dc supply, with one PA active per MIDB group; 2) V_{LO} dc supply, with both PAs active per MIDB group, and 3) V_{HI} dc supply, with one PA active per MIDB group.

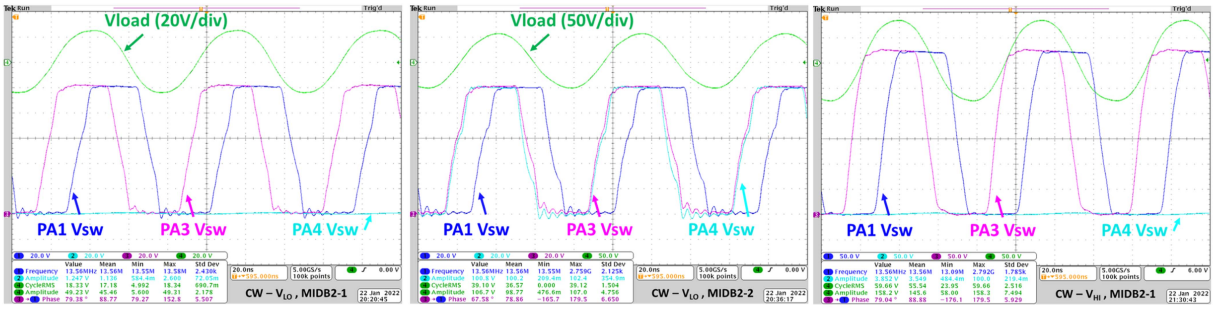
A thermal image showing the hotspot temperature from the PA when the system is continuously operating at about 1.2 kW is shown in Fig. 15. Fig. 16 shows the oscilloscope voltage probe locations, and Fig. 17 shows the waveforms when the system is operating under three different dc supply voltage and MIDB ON–OFF status combinations. The observations are discussed in detail here.

1) Case 1, V_{LO} dc supply, with one PA active per MIDB group of two PAs (dubbed MIDB2-1). Fig. 17(a) corresponds to this case, where V_{SW4} is mostly flat since it is ac-grounded (same for V_{SW2}), while PA1 and PA3 are ON (actively switching). With the outphasing control between the two MIDB PA groups, a phase-shift can be clearly seen between V_{SW1} and V_{SW3}. A sinusoidal ac voltage V_{load} at the target operating frequency of 13.56 MHz is produced across the 3.1 Ω load impedance synthesized from a 50 Ω termination via a TMN, and the system output power is approximately 100 W at the shown outphasing angle.
2) Case 2, V_{LO} dc supply, MIDB2-2. As shown in Fig. 17(b), all PAs are on and actively switching. The PAs within the same MIDB group (e.g., PA3, 4) are synchronized, while a phase-shift exists between MIDB groups. The V_{load} amplitude is larger compared to the first case, indicating higher rf power delivered to the load (approximately 450 W at the illustrated operating point).
3) Case 3, V_{HI} dc supply, MIDB2-1. Fig. 17(c) shows this case. The higher dc supply voltage leads to higher peak circulating current in the ZVS tank, as well as reduced effective output capacitances in the transistors, leading to cleaner ZVS and improved system efficiencies. Approximately 940 W load power is delivered at the shown outphasing angle. Note that the system is rated to operate continuously in this case, and only operates transiently at the maximum power state (V_{HI} dc supply, MIDB2-2).

The system was tested across a range of outphasing angles for each operating state. The measured system efficiency is calculated as the rf output power (P_{out}, sensed with the V/I probe at the output of the combiner network) divided by the total input power from the dc supplies (P_{in}, measured by the dc voltage and current meters). The efficiency is plotted versus P_{out} (with P_{out} shown on a log-scale axis) as the solid lines in Fig. 18. By properly selecting the control handles (i.e., the dc supply level, MIDB control, and outphasing angle), the prototype system can maintain CW operation and continuous power control over the power range of 5 W–1.23 kW, with >85% efficiency at 50 W and above. Further, the prototype system achieves a peak efficiency of 90.97% at 1.03 kW P_{out}. Compared with traditional linear PA based implementations (e.g., a commercial 5 kW, 13.56 MHz generator with 50% nominal efficiency [40]), the proposed system benefits from significantly reduced power losses and better potential for electricity cost reduction.

C. Dynamic Pulsing Measurement Results

The target application scenario requires high-power, short-duration rf power pulses from the generation system at up to 5 kW, and the generator is designed to provide this capability. In addition to CW operation (where the rf output power remains steady and constant), the prototype system is also tested with high-power pulsated output to verify that the system can have fast dynamic response and maintain good efficiency under this



(a) (b) (c)

Fig. 17. System CW operation waveforms under three DC supply level and MIDB ON/OFF control combinations, with 20 ns per horizontal division for all channels. (a) has 20 V/div for all channels, (b) has 20 V/div for $V_{SW1,3,4}$ and 50 V/div for V_{load}, and (c) has 50 V/div for all channels. (a) V_{LO} DC supply, MIDB 2-1. (b) V_{LO} DC supply, MIDB 2-2. (c) V_{HI} DC supply, MIDB 2-1.

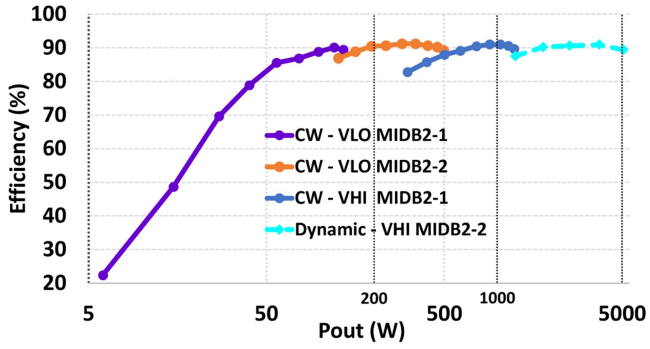


Fig. 18. Measured system efficiency (rf power at the output of combiner network board versus total DC input power) versus output power, with output power shown on a log scale. The dotted vertical lines mark power levels at 200 W, 1 kW, and 5 kW, respectively; these power levels correspond to optimization targets for the design.

condition. The prototype system is rated for 1 kW CW operation, and dynamically covers a 30 dB range from 5 W to 5 kW. The remaining control handle combination (V_{HI} and both PAs active) is leveraged to achieve the highest power levels, thus covering the entire target power range.

Fig. 19(a) shows a short, high power pulse, captured from a periodic train of pulsations. For this instance, the pulsing is achieved with all PAs active and toggling dc supply voltage levels between V_{LO} and V_{HI}, with 500 transitions per second and each high power pulse lasting for 20 μs. The rf output power pulsates between approximately 500 W at low power and 5.1 kW at high power. Fig. 19(b) and (c) zoom in on the transition edges of the power pulse. It can be observed that the load rf voltage settles down rapidly, within 1 μs after each step, which enables the narrow, tens of μs scale power pulses desired for industrial plasma generation applications.

The dynamic system efficiency (the dashed segment in Fig. 18) is calculated indirectly according to (1). The CW system efficiency at the lower power level (η_{LO} at P_{out-LO}) is measured and recorded, then, with periodic high-power pulses upon P_{out-LO}, the total dc input power P_{in-dc}, the power level of the pulse (P_{out-HI}), and the duty cycle of the power pulse D_{HI} are measured. The system efficiency during the high-power pulses can thus be calculated, as the time-averaged power of the pulse ($D_{HI} \times P_{out-HI}$) divided by the total input power minus the portion from the lower output power ($P_{in-dc} - (1 - D_{HI}) \times P_{out-LO}/\eta_{LO}$). High dynamic efficiencies above 87% are observed throughout the range of 1.2–5.1 kW.

$$\eta_{pulse} \approx \frac{D_{HI} \times P_{out-HI}}{P_{in-dc} - \frac{(1-D_{HI}) \times P_{out-LO}}{\eta_{LO}}} \quad (1)$$

Overall, the rf power generation system is demonstrated to maintain continuous power control over the target power range of 5–5 kW, with CW operation up to 1.2 kW, low power losses throughout the range, and fast dynamic response to realize narrow, high-power pulses with sharp transitions.

D. Load Impedance Variation Measurement Results

While the nominal load impedance is at 3.1 Ω, some techniques for tunable impedance matching do not yield perfectly tuned load impedances for the PAs. Thus, a compressed but nonperfectly matched range of load impedances may be seen by the power generation system [17]. Therefore, we demonstrate the system performance and sensitivities against a certain degree of load impedance variation. We focus on CW operation since the thermal stress on the devices is higher and the efficiency impact is more significant for this case as compared with the dynamic pulsing scenario.

The system efficiencies under various synthesized load impedances Z_L are plotted in Fig. 20. It can be observed that the system maintains good performances against a moderate range of load impedance variations. In addition, as expected with additional capacitive loading at the output, the system efficiency at peak power levels start to drop, due to the loss of ZVS at the edges of outphasing angle range.

V. Conclusion

This article introduces a new rf power generation system architecture suitable for industrial rf power applications, such as plasma generation for semiconductor processing equipment. The MIDB-based architecture and control technique offers clear benefits in terms of enhanced efficiencies over a very wide power range. In addition, this technique can seamlessly work together with other power control approaches such as supply

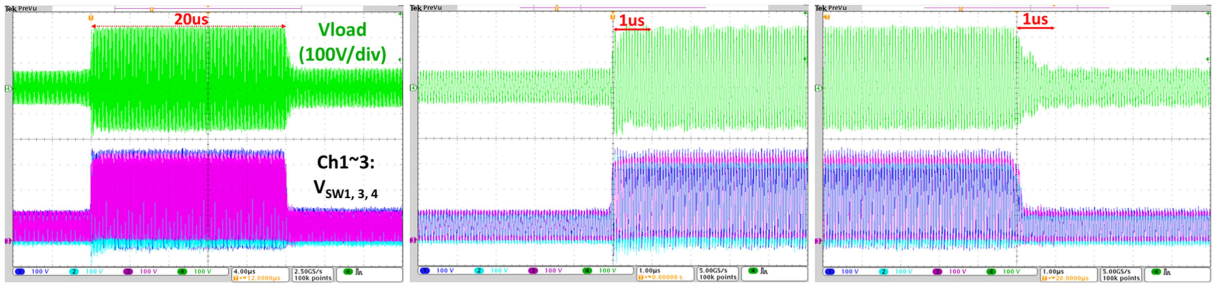


Fig. 19. System dynamic pulsing waveforms showing a short (20 μs), high power (5.1 kW) pulse, together with zoomed in transitions. The power pulse is enabled via a supply voltage transition from V_{LO} to V_{HI}. All channels shown are 100 V/div. (a) has 4 μs/div, and (b), (c) zoom in on the transitions with 1 μs/div. The output power settles within 1 μs after each transition. (a) A short, high power pulse. (b) Zoomed in low-to-high transition. (c) Zoomed in high-to-low transition.

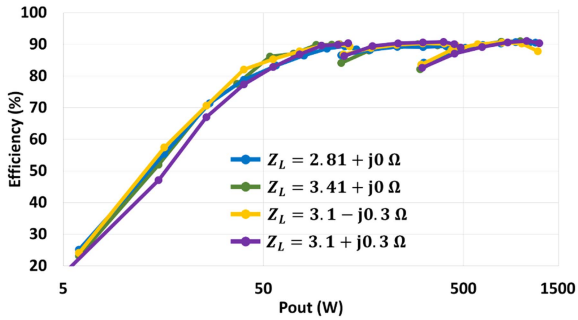


Fig. 20. Measured system efficiency under CW operation versus output power for load impedance variations from the nominal target.

modulation and outphasing, to provide fast dynamic response and continuous power control. Systems based on this technique also enjoy a modularized PA unit design, which can be easily expanded to meet specifications such as higher peak or average power levels.

A systematic optimization procedure is established for MIDB system design toward a given power profile. Further, a ZVS Class-D PA based prototype system, with two PAs per MIDB group and two dc supply levels is constructed and tested. This system achieves high efficiency and continuous power control over the designed CW operating range of 5 W–1 kW, and dynamically over 5 W–5 kW, with fast dynamic response and significantly reduced power loss compared to existing linear-amplifier based solutions. Further, the system is demonstrated to have good robustness against moderate load impedance variations from the nominal load impedance level.

It is anticipated that the proposed architecture and design approach has significant potential for advancing the performance of industrial rf plasma generation systems.

Acknowledgment

The authors would like to thanks MKS Instruments, Inc., for financial and technical support.

Appendix A
MIDB System Design and Loss Optimization

This appendix discusses the design process of MIDB-based PA systems, where the outcome include the selection of supply voltage levels, device areas, and some critical circuit components. We outline the process of power loss optimization toward a target power profile. The dominant sources of loss are identified, and an optimization procedure is described based on the example system implementation illustrated in Fig. 3, with MIDB-2 PA groups, and modular, GaN-FET based ZVS class-D PA units. For simplicity, we assume ideal power combiners and that a TMN perfectly matches the variable plasma load to some fixed real impedance.

A. PA Loss Analysis

As the majority of power losses in an rf power delivery system come from its PAs, this section performs a simplified loss analysis on a PA unit. The goal is to quantitatively guide parameter selections in system-level design, such as number of PA units per MIDB block, operating voltage, device area etc.

The dominant sources of losses in a GaN-based ZVS class-D PA include device output capacitance (C_{OSS}) losses $P_{C_{\text{OSS}}}$, device conduction losses P_{Cond}, and ZVS inductor and resonant inductor conduction losses $P_{L_{\text{ZVS}}}$ and P_{L_r} as given in (2).

$$P_{\text{loss}} \approx P_{C_{\text{OSS}}} + P_{\text{Cond}} + P_{L_{\text{ZVS}}} + P_{L_r}. \tag{2}$$

$P_{C_{\text{OSS}}}$ can be expressed as (3) where A is the area of the device, f is switching frequency, V is the supply voltage level $K_{C_{\text{OSS}}}$ is a loss proportionality constant, and α, β are switch-dependent constants [18].

$$P_{C_{\text{OSS}}} \approx K_{C_{\text{OSS}}} \cdot A \cdot f^{\alpha} \cdot V^{\beta}. \tag{3}$$

The current passing through the devices mainly consists of two parts, the output current to the load and the current from the L_{ZVS} shunt leg. Assuming square-wave voltage at the switching node and using first-harmonic approximation (FHA), P_{Cond} can be expressed by (4), where $K_{R_{\text{on}}}$ is a device-dependent constant that captures the device on-state resistance's inverse relationship with area, and R_L is the load (assumed to be real and fixed).

$$P_{\text{Cond}} \approx K_{R_{\text{on}}} \cdot A^{-1} \cdot V^2 \cdot \left(\frac{2}{\pi^2 R_L^2} + \frac{1}{192 f^2 L_{\text{ZVS}}^2} \right). \tag{4}$$

Assuming the ZVS tank only sees a square-wave voltage and the series resonant tank only sees a sinusoidal output current, $P_{L_{\text{ZVS}}}$ and P_{L_r} can be approximated by (5) and (6), respectively, where

Q_L denotes the inductors' quality factor at switching frequency

$$P_{L_{\text{ZVS}}} \approx \frac{\pi}{96 f L_{\text{ZVS}} Q_{L_{\text{ZVS}}}} \cdot V^2 \tag{5}$$

$$P_{L_r} \approx \frac{4 f L_r}{\pi R_L^2 Q_{L_r}} \cdot V^2. \tag{6}$$

If the PA is commanded to deliver a given output power P_{out}, with FHA the relationship between P_{out} and V can be established as (7), and the overall PA efficiency η_{PA} expressed in (8)

$$V \approx \sqrt{\frac{\pi^2 R_L P_{\text{out}}}{2}} \tag{7}$$

$$\eta_{\text{PA}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}}. \tag{8}$$

Finally, plugging (2–7) into (8), the PA efficiency at given P_{out}, η_{PA}, can be expressed as in (9), with device and topology-dependent constants abstracted out as $K_1 = K_{C_{\text{OSS}}} f^{\alpha}(\pi^2/8)$, $K_2 = K_{R_{\text{on}}}$, $K_3 = K_{R_{\text{on}}}\pi^2/(384 f^2 L_{\text{ZVS}}^2)$, $K_4 = \pi^3/(192 f L_{\text{ZVS}} Q_{L_{\text{ZVS}}})$, and $K_5 = 2\pi f L_r / Q_{L_r}$. We observe from (9) that at given P_{out}, η_{PA} is related to device area, load resistance, and supply voltage. Since the C_{OSS} loss Steinmetz parameter β is typically < 2 for most GaN devices [19], provided that we can freely design A and R_L and that additional losses from impedance transformation stages are small, the supply voltage should be set at a high dc voltage level where the devices can reliably operate at. In some cases, however, C_{OSS} loss and/or transformation-related losses may motivate using a lower-than-maximum supply voltage for a given device with fixed area and load conditions.

B. Optimization Procedure

With losses in individual PAs analytically expressed, this section addresses system-level behaviors in the MIDB setting, and outlines a general optimization procedure that, with operating frequency and desired output power profile as input, yields the efficiency-optimized MIDB configuration (number of PAs per group) and device area.

1) Outphasing Characteristics: We start with discussions on the load modulation effects seen by the PAs during outphasing and the corresponding Chireix compensation component design and outphasing angle range selection. Both the resistive and reactive loadings on the inverters of the system will change based on the outphasing design, which primarily impacts the system efficiency. The uncompensated load admittance curves seen by the two MIDB PA groups during outphasing is shown in Fig. A1. Each group sees a load admittance point on their corresponding curve as described in (10), and the output power of a block can be expressed by (11), where $V_{\text{MIDB-rms}}$ is the rms output voltage magnitude of a PA block. Varying θ from 0° to 90° results in the MIDB blocks seeing admittances tracing along the curves from $(2/R_L, 0)$ to (0,0), and adding shunt reactive compensation components (X_A, X_B) shifts the curves vertically based on the added reactances [13], [30]

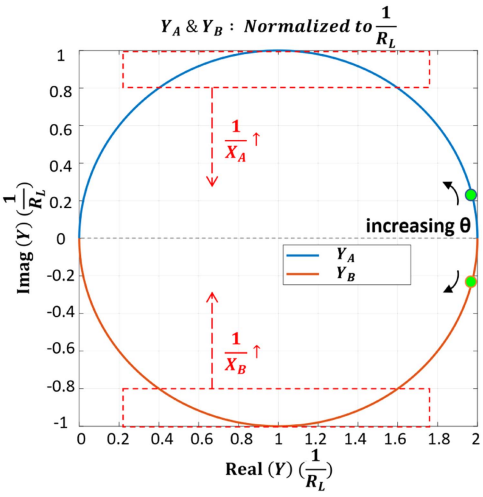


Fig. 21. Uncompensated load admittance curves seen by MIDB groups (Y_A and Y_B in Fig. 3) during outphasing, with axes normalized to $1/R_L$. Actual load admittances are determined by outphasing angle θ and compensation reactances X_A, X_B. The output power of MIDB groups is proportional to their real part of the load admittances. After compensation, the outphasing operating angle is controlled such that the load admittance seen by the PAs are mostly resistive and good system performance can be maintained.

$$Y_A = \frac{1}{R_L}(1 + e^{j2\theta}) - j\frac{1}{X_A} \tag{10a}$$

$$Y_B = \frac{1}{R_L}(1 + e^{-j2\theta}) + j\frac{1}{X_B} \tag{10b}$$

$$P_{\text{group}} = V_{\text{MIDB-rms}}^2 \cdot Re\{Y_{A\ or\ B}\}. \tag{11}$$

Generally, the closer the load admittance is to the real axis (dashed line in Fig. 21), the more efficiently the PA operates. However, with variations in θ, both load conductances and susceptances seen by the PAs change, affecting the system efficiency. This is one of the reasons outphasing alone has a limited power range where the system efficiency can be kept high. To mitigate this, one selects the Chireix compensation components to vertically shift the curves such that the admittances stay close to the real axis for as wide a power modulation range as possible within allowable reactive loading constraints [13], [30]. For example, we may select the compensation reactances such that the portion of admittance curves encircled by the dashed red box in Fig. 21 is close to the real axis.

2) Simulation-Based Optimization: Based on the modeled PA losses, this section discusses a simulation-based optimization procedure to holistically evaluate and design a fully specified loss-optimized MIDB system towards a targeted output power profile.

$$\eta_{\text{PA}} \approx \frac{1}{1 + K_1 \cdot A \cdot R_L \cdot \boldsymbol{V^{\beta-2}} + (K_2 \cdot R_L^{-1} + K_3 \cdot R_L) \cdot A^{-1} + K_4 \cdot R_L + K_5 \cdot R_L^{-1}}. \tag{9}$$

A key assumption in the optimization is the linear relationship between power losses and device area. That is, if an optimized system with total device area A_{tot} achieves peak efficiency at some output power P, then for the actual target output power $k \cdot P$, we can construct the new optimal system using k paralleled copies of the original system, with $k \cdot A_{\text{tot}}$ total device area and maintain the same peak efficiency. Here, k is a unit-less proportionality factor and may be fractional. This assumption allows us to start the simulation process with a random device area, using any available manufacturer–supplied device model from the same device family, and at the preidentified supply voltage level. At this stage, we can construct modular PA units using the device model, and simulate across multiple MIDB configurations (e.g., $m = 2$, 3, and 4), θ ranges, X_A, $-X_B$ shunt compensation reactances, and MIDB on/off operating conditions. The goal of this step is to identify the output power level where the system has highest efficiencies (or average efficiencies), then, based on the actual power profile, we find the scalar k such that the simulated power level corresponds to the actual power profile target.

The simulation-based optimization steps are thus as follows:

1) Step 1: Select PA topology and device family, determine loss components (e.g., for ZVS-Class D PA and Infineon GaN devices). Assume freedom in device area A, identify a suitable supply voltage level V.
2) Step 2: On a system level, determine MIDB configuration and outphasing angle range for output power levels of interest. With the power-area relationship assumption, simulations can be performed with any random device model available (e.g., area of A_r), and the ratios between power levels are more important than the actual power level for this step.
3) Step 3: Perform simulations at pre-determined V and selected device model accounting for dynamic $R_{ds,on}$ effects [35], swept over a range of: MIDB system configurations (m PA, ON–OFF), outphasing angle θ and compensation components X_A, X_B. Find the power levels of maximum (average) efficiency, and the ratio k to the actual desired power level.
4) Step 4: Identify a specific device (area closest to $k \cdot A_r$) and a suitable MIDB system configuration (m). Reoptimize supply levels and load impedance as needed.

Promising MIDB systems with performance optimized against the given load profile, along with the desired device area can thus be shortlisted. Note that in reality there are often limited options of the devices available, therefore, a further reoptimization of the supply voltage (and associated load impedance) based on the target power profile may be needed. In addition, since the exact device is identified, when discrete supply modulation is desired, additional sets of simulations can be conducted to identify suitable discrete voltage levels.

Appendix B
Outphasing Load Impedance Measurements

This appendix presents a technique to measure the PA load impedances under outphasing, e.g., by performing a two-port measurement at the switching-node of two PA units (from two MIDB PA groups with phase-shifts, e.g., at V_1 and V_3 from Fig. 9) using a network analyzer. Denoting the voltage and current at the switching nodes of the two measured PAs as $V_{1,3}$ and $I_{1,3}$, we can establish a general two-port network impedance matrix relationship as expressed as follows:

$$\begin{bmatrix} V_1 \\ V_3 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{13} \\ Z_{31} & Z_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_3 \end{bmatrix}. \tag{12}$$

Since we know that in an outphased system, V_1 leads V_3 by a certain angle (denoted here as twice the outphasing angle θ), and also for a balanced system, $|V_1| = |V_3|$. We can leverage this to express V_3 and I_3 in terms of V_1 and I_1, as given follows:

$$V_1 = V_3 \cdot e^{+j2\theta} \tag{13a}$$

$$I_1 = \frac{Z_{33}e^{j2\theta} - Z_{13}}{Z_{11} - Z_{31}e^{j2\theta}} \cdot I_3 = x \cdot I_3. \tag{13b}$$

Next, from (14), we can express the impedance seen by the two PAs, $Z_{\text{outphasing}-1}$ and $Z_{\text{outphasing}-3}$, as functions of the outphasing angle. Therefore, we can plot the outphasing impedance levels versus the outphasing angle control range

$$Z_{\text{outphasing}-1}(\theta) = \frac{V_1}{I_1} = Z_{11} + \frac{Z_{13}}{x} \tag{14a}$$

$$Z_{\text{outphasing}-3}(\theta) = \frac{V_3}{I_3} = Z_{33} + \frac{Z_{31}}{x}. \tag{14b}$$

Appendix C
TMN Considerations

Corresponding to the block labeled "Impedance Transformation" in Fig. 3, a common approach to realize the functional block is through a TMN, i.e., a two-port network of variable reactances connected between the PAs and the load. To ensure that PAs maintain a reasonably high efficiency and endure less thermal stresses, the TMNs need to achieve 1) an appropriate tuning range covering potential plasma load impedance ranges, and 2) adequate tuning precision matching the load impedance to the target impedance level or within a narrow scope, and also 3) fast tuning speed, reacting to the time-varying plasma load in-time. A TMN technique that potentially satisfies the above criteria leverages discrete capacitors, where several binary-valued rf capacitors are optionally connected to the system through switches, to provide a range of discrete matching reactances. Further, the dynamic frequency tuning technique (DFT, e.g., in [10]), can be leveraged to provide part of the reactances in a matching network. In the DFT technique, the frequency of the

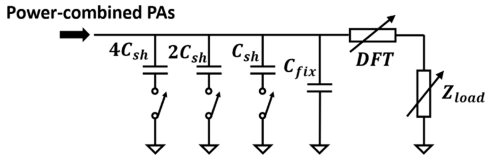


Fig. 22. Example implementation of the TMN with switched capacitors and dynamic frequency tuning.

power source (e.g., the PA switching frequency) is dynamically varied to a small extent and combined with passive components (e.g. a high-Q resonant tank) to provide a range of continuously tunable reactances. Fig. 22 shows an example TMN implemented with the discrete switched capacitors and DFT. Another TMN approach that would be highly effective in this application is based on phase-switched impedance modulation (PSIM), as described in [8], [9].

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