Flexible 1.5-GHz Probe Isolation Extension With High CMRR and Robust d*v*/d*t* Immunity Empowering Next-Generation WBG Measurement

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***Abstract*—Advancements in the next-generation wide-bandgap (WBG) power devices, distinguished by higher blocking voltage and faster switching speed, give rise to the advent of ultrahigh d*v*/d*t*. These three factors collectively impose demanding performance requirements on future high-performance measurement systems. This article conducts an in-depth exploration of the challenges encountered during the low- and high-side dynamic testing of the next-generation WBG device. Drawing from this examination, the performance requirements for future galvanically isolated testing systems are summarized, i.e., a broad dynamic range extending to medium voltage levels, a minimum measurement bandwidth of 500 MHz, a common-mode rejection ratio (CMRR) of at least 50 dB at 100 MHz, and a d*v*/d*t* immunity exceeding 100 V/ns. To effectively response these objectives, the concept of probe isolation extension (PIE) is introduced, with the aim of providing exceptional galvanic isolation while preserving the high electrical performance of traditional nonisolated testing systems to the greatest extent possible. Building upon the PIE concept, an optics-based physical implementation method, known as optical dock (OD), is presented. The operating principles of the OD are derived, and a detailed analysis is conducted to examine the factors that influence its high-frequency response. Additionally, parameter tuning methods are provided to maximize its bandwidth. These collective efforts have successfully resulted in the development of a high-performance PIE OD, which exhibits outstanding galvanic isolation capability, an ultrahigh bandwidth of 1.53 GHz, a high CMRR of 72 dB at 100 MHz, and robust d*v*/d*t* immunity of 1.3 kV/ns. Extensive comparative experiments with the state-of-the-art galvanically isolated probes/systems have demonstrated that by incorporating PIE OD to expand various different nonisolated probes/systems, precise characterization of all high-side dynamic electrical parameters, i.e., v_{gs}, v_{ds}, and i_d, for the MV SiC MOSFET can be achieved. This highlights the significant potential of the PIE OD for next-generation WBG and even ultra-WBG applications.**

***Index Terms*—Common-mode rejection ratio (CMRR), dv/dt immunity, galvanic isolation, medium voltage (MV), probe isolation extension (PIE), ultrahigh bandwidth, wide-bandgap (WBG) device.**

I. Introduction

THE advancement in next-generation wide-bandgap (WBG) semiconductor technologies, along with advanced packaging techniques, has yielded the development of power devices with higher breakdown voltage and faster switching speeds [1]. This enhanced blocking voltage allows for a substantial reduction in the number of cascaded conversion stages required at the same bus voltage, leading to reduced system complexity and higher reliability and density [2], [3]. Additionally, the faster switching speed contributes to lower switching losses, enabling higher switching frequencies, efficiency, as well as power density [4]. Together, these factors contribute to advancing the overall performance of power electronics systems. Nevertheless, along with these advancements come extremely brief switching times, as short as a few nanoseconds, and ultrahigh d*v*/d*t* exceeding 100 V/ns, cf. Fig. 1, posing significant challenges for the dynamic testing of the next-generation WBG power devices.

In traditional low-voltage dynamic testing, the main focus is on the lower side of the bridge. Since the reference potential remains relatively stable and is located at the lowest point of the circuit under test, nonisolated testing methods are commonly utilized. Furthermore, for the WBG power devices with the very low switching times, meeting the testing requirements involves optimizing nonisolated testing systems for their high-speed response, e.g., high-bandwidth single-ended voltage dividers [5], [6], and ultrafast current shunts [7], [8].

As the next-generation WBG power devices transition into the medium-voltage (MV) range, the issues stemming from common-mode (CM) grounding loops in low-side testing become more pronounced. These loops have the potential to introduce substantial errors in testing results, such as zero drift and false low-frequency oscillations [9], [10]. Hence, relying

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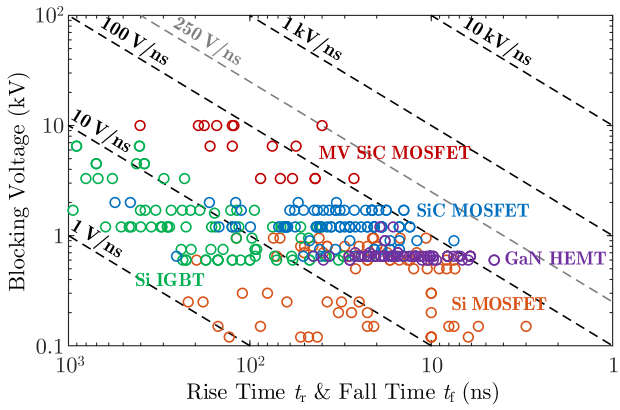

Fig. 1. Blocking voltage, switching time t_r and t_f, and corresponding switching voltage slew rate dv/dt of different types of power devices. Please note that dv/dt includes both turn-ON dv/dt_r and turn-OFF slew rate dv/dt_f.

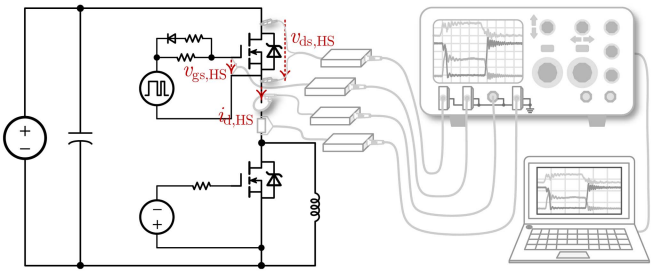

Fig. 2. Test principle and configuration of high-side double pulse test (DPT) for MV SiC MOSFETs.

solely on high-bandwidth, nonisolated testing approaches is insufficient for conducting the low-side dynamic testing of the next-generation WBG devices, and it is essential to incorporate the galvanic isolation capability [11].

When considering the high-side testing shown in Fig. 2, the situation becomes increasingly challenging. In this scenario, the reference potential of the testing system is positioned at the midpoint of the bridge, resulting in rapid fluctuations between the power ground and bus voltage during switching operations. This implies that the entire system is subjected to a significant direct current (dc) CM with respect to the bus voltage, and an ultrafast CM interference in the form of dv/dt. Achieving the accurate capture and reproduction of switching characteristics under such intense interference poses considerable challenges [12], [13]. What is worse, the next-generation WBG power devices exhibit both MV-level blocking voltages and ultrahigh dv/dt exceeding 100 V/ns [14], [15], which compels testing systems to prioritize crucial indicators like galvanic isolation, common-mode rejection ratio (CMRR), and dv/dt immunity.

Therefore, the next-generation WBG measurements require high-performance galvanically isolated testing methods with an eye on multiple dimensions, including measurement bandwidth, dynamic testing range, galvanic isolation capability, wideband CMRR, and dv/dt immunity.

Isolating the power supply of the oscilloscope shown in Fig. 2 to achieve galvanic isolation is a straightforward approach [9], [10]. However, it introduces concerns regarding the entire backend operating in a high-potential environment, posing safety risks. Moreover, the significant fluctuation of the reference potential can also greatly impact the measurement accuracy. The differential method is the most commonly used galvanic isolation technique [16], and the advanced concept of the transmission line voltage divider (TL-VD) enables the differential system with a high dynamic range and GHz-level bandwidth [11]. Nevertheless, its high-frequency CMRR is still limited by the operational amplifier (op-amp) in the backend. Integrating the differential topology with the nonelectrical isolation techniques can further improve the CMRR [12], [13]. However, nonelectrical isolation methods are currently not fully developed, thus, isolated differential approaches are mainly demonstrated as concepts, and their feasibility requires further exploration. Analog and digital isolation chips are also employed for the galvanically isolated dynamic testing [17]. However, their bandwidth is often limited to a few MHz due to the data transmission rate of the isolation chips. Furthermore, their galvanic isolation capability, relying on either capacitive [18] or magnetic isolation [19] techniques within the chips, falls far short of the testing range required for MV applications. By leveraging the inherent isolation of wireless data transmission, a wireless oscilloscope concept, WiScope14 [20], was proposed. Through further optimization, the WiScope23 [21] achieved a remarkable CMRR of up to 100 dB at 100 MHz. Nevertheless, their bandwidths are primarily restricted to 200 MHz, and the need for substantial data for high resolution and sampling rate poses limitation on real-time measurements, thus restricting their applications to some extent. Optically isolated probes, such as TIVP1 [18], have gained widespread attention recently due to their impressive overall performance. However, the high price of these commercial products deters potential users. Moreover, these probes/systems typically have a measurement dynamic range of around $\pm$2.5 kV, primarily designed for the low-voltage applications, thus struggling to meet the demanding MV testing requirements, which can reach up to 35 kV [23], [24].

Based on the analysis and discussion above, it is clear that there is currently no comprehensive solution that can satisfy all the demanding performance requirements of next-generation WBG measurements, including high measurement bandwidth, wide dynamic testing range, robust galvanic isolation capability, wideband high CMRR, and strong dv/dt immunity. The field of the next-generation WBG measurements still faces significant challenges that need to be explored and resolved urgently.

Driven by these challenges, the optical dock (OD) based on probe isolation extension (PIE) concept is proposed, aiming to further push the boundaries of high-performance galvanically isolated measurements, particularly tailored for next-generation WBG and even ultra-WBG applications. The rest of this article is organized as follows. In Section II, an in-depth examination of the electrical characteristics of next-generation WBG power devices is provided, highlighting the severe challenges faced in their dynamic testing, and summarizing the crucial performance requirements for future high-performance galvanically isolated testing systems. In Section III, the innovative concept of PIE OD is introduced, accompanied by a comprehensive theoretical derivation of design guidelines to maximize its bandwidth

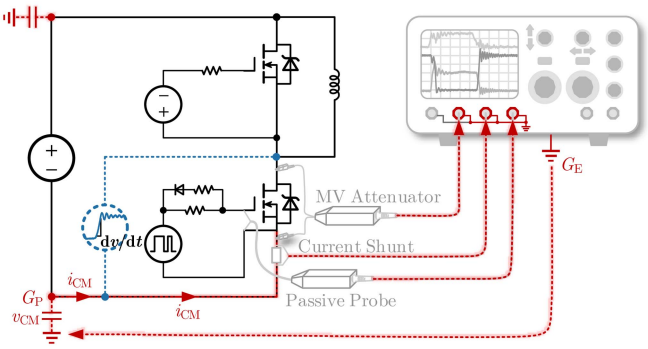

Fig. 3. Common-mode current path i_{CM} parasitized in low-side DPT system, containing only low-frequency CM source v_{CM}.

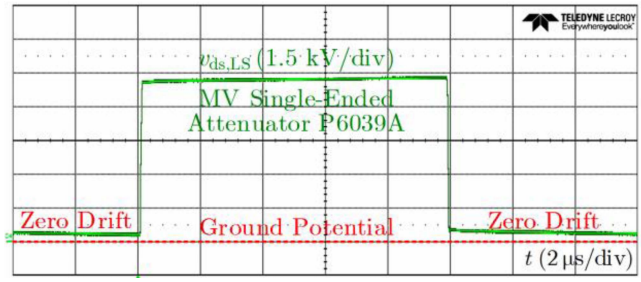

Fig. 4. Low-side drain-source voltage $v_{ds,LS}$ of 10-kV SiC MOSFETs at $V_{dc} = 7.0$ kV and no load current, measured with MV single-ended attenuator P6039A, exhibits a zero-drift voltage error of up to 400 V.

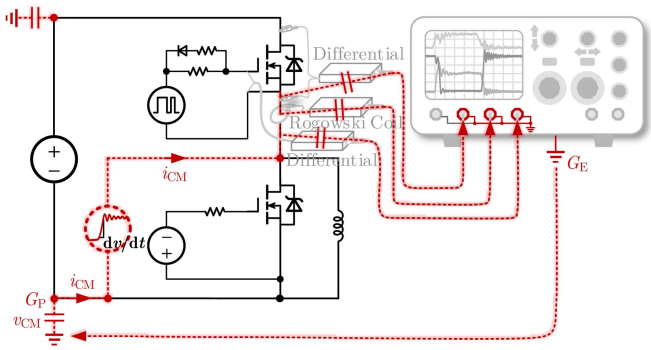

Fig. 5. Common-mode current path i_{CM} parasitized in high-side DPT system, containing both low-frequency CM source v_{CM} and high-frequency CM source dv/dt.

performance. Moving on to Section IV, the focus shifts to the frequency domain, encompassing the theoretical calculations, submodule optimization, and extensive comparisons with the state-of-the-art galvanically isolated testing probes/systems. In Section V, a comprehensive verification is conducted in the time domain, under the most demanding high-side testing conditions, to demonstrate the exceptional performance of the developed PIE OD. Finally, Section VI concludes this article.

II. Pursuits and Challenges Existing in Next-Generation WBG Measurements

A. Rigorous Challenges Encountered in Next-Generation WBG Measurements

1) Low-Side DPT and Low-Frequency CM Noise Source v_{CM}: In the low-side DPT, the ground of the isolated power supply G_P serves as the reference potential for testing probes/systems. However, to ensure operator safety, the oscilloscope is typically connected to the earth ground G_E. This connection introduces parasitic capacitance and potential differences between the G_P and G_E, leading to the emergence of a low-frequency CM noise interference source referred to as v_{CM}, as shown in Fig. 3.

Therefore, in the low-side DPT, when nonisolated probes/systems are employed, there is a lack of fundamental galvanic isolation between the circuit under test and the oscilloscope, resulting in the formation of a CM grounding loop throughout the entire testing system. This parasitic loop primarily arises from the CM leakage current i_{CM} of the isolated power supply, flowing through the ground layers of the nonisolated probes/systems and the oscilloscope, eventually being injected into the earth ground, before returning to the isolated power supply via the grounding connection and parasitic capacitance.

When the bus voltage V_{dc} and switching rate dv/dt are not excessively high, the issues arising from the CM grounding loop may not be very noticeable. Nevertheless, as the blocking voltage and dv/dt of the next-generation WBG devices continue to rise, significant measurement errors induced by v_{CM} can be observed.

A typical example is the low-side DPT with the MV SiC MOSFETs, where the low-side drain-source voltage $v_{ds,LS}$ is often characterized using a MV single-ended attenuator with an attenuation ratio of up to several thousand. Consequently, in the presence of v_{CM} interference, even a minor deviation of a few tens of millivolts, when amplified by a factor of several thousand, can lead to zero-drift errors reaching tens or even hundreds of volts in the final measurement results, as illustrated in Fig. 4. Note that, to eliminate the influence of the transistor's conduction voltage drop, the test performed here is under no-load conditions, meaning $I_d = 0$ A.

2) High-Side DPT and High-Frequency CM Noise Source dv/dt: In contrast to the low-side DPT, in the high-side DPT, the reference potential of the testing probes/systems is located at the bridge's midpoint, cf. Fig. 5. As the upper switch operates, the reference potential of the testing system will fluctuate between the isolated power supply ground G_P (instead of the earth ground G_E) and the bus voltage V_{dc}. Therefore, the CM interference sources in the high-side DPT will not only include the low-frequency noise source v_{CM} but also the high-frequency source dv/dt.

Among them, the effects of v_{CM} are similar to those in the low-side DPT, with a relatively broad time span and resulting in the potential ground level drift. On the other hand, dv/dt primarily affects the switching edges and their immediate vicinity within a small time span, leading to transient waveform spikes or dips.

A typical example involves the utilization of a Rogowski coil (RC) to measure the high-side drain current $i_{d,HS}$, cf. Fig. 5. The traditional RC, being a purely isolated current sensor, lacks an inherent CM rejection capability. Consequently, both the low- and high-frequency CM noise sources will concurrently impact the RC testing results through the parasitic capacitance between the circuit under test and the RC.

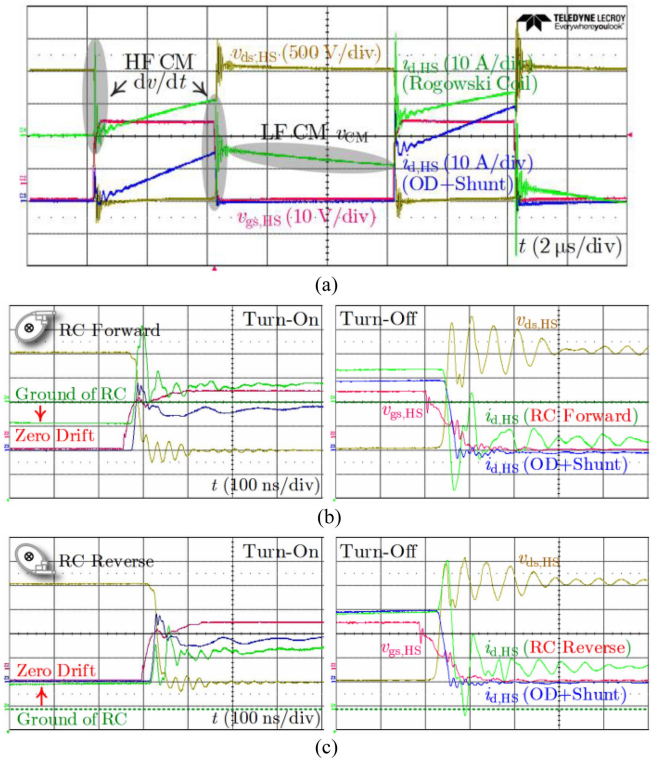

Fig. 6. High-side switching characteristics of 3.3-kV SiC MOSFET at V_{dc} = 2.0 kV. (a) Both low- and high-frequency CM sources, i.e., v_{CM} and dv/dt, coexist and have a significant impact on the measurements of high-side drain current $i_{d,HS}$ with a commercial Rogowski coil CP9006S. (b) Impact of high-frequency CM source dv/dt on the *RC* in forward connection. (c) Impact of high-frequency CM source dv/dt on the *RC* in reverse connection.

Fig. 6 depicts the typical high-side switching behaviors of a 3.3-kV SiC MOSFET. To provide a comprehensive display of the influence of the two CM sources on the testing outcomes of the commercial RC CP9006S, the results from the "OD + Shunt" configuration, which can effectively address both interferences concurrently, are also included as a reference benchmark.

From Fig. 6(a), it is evident that when measuring $i_{d,HS}$ using the RC, the measurement results exhibit both high-frequency distortions at the switching edges, indicating the impact of dv/dt, and a reference ground potential drift, indicating the impact of v_{CM}. Moreover, the zero-drift error accumulates over time due to the integration effect of the internal integrator in the RC, further exacerbating the issue.

Fig. 6(b) and (c) visually illustrates the significant influence of dv/dt through varying connections of the RC. *Initially*, due to the interference of dv/dt, the switching current waveforms recorded by the RC display noticeable overshoot or undershoot distortions. *Additionally*, regardless of whether the RC is connected in a forward or reverse orientation to the tested circuit, the direction of injection of high-frequency CM current on the RC remains consistent, while the recorded current directions are opposite. As a result, during the turn-ON (or turn-OFF) transitions, the distortions arising from the two connection directions of the RC exhibit opposite orientations, highlighting distinct differential characteristics.

To sum up, the next-generation WBG power devices provide increased breakdown voltage and decreased switching times, leading to exceptionally high dv/dt levels as well as a variety of intricate CM testing issues. These factors collectively set forth new while more rigorous performance demands for the next-generation WBG measurement probes/systems, encompassing aspects such as measurement bandwidth, galvanic isolation, wideband CMRR, and dv/dt immunity, among others.

B. Performance Requirements of Galvanically Isolated Probes/Systems for Next-Generation WBG Measurements

1) Rise Time t_r Oriented Bandwidth f_{BW} Requirements: The minimum required measurement bandwidth f_{BW} for accurately characterizing the switching transients of the power devices with a rise time of t_r can be calculated as [8]

$$\left\{ f_{BW} = 5\frac{0.35}{t_r} \right\} \Leftrightarrow \left\{ t_r = 5\frac{0.35}{f_{BW}} \right\}. \tag{1}$$

It can be concluded from (1) that, to precisely capture the switching dynamics of next-generation WBG devices, which can have switching time as short as a few nanoseconds, the measurement system's bandwidth should be at least 500 MHz.

2) dv/dt Immunity Oriented CMRR Requirements: To effectively mitigate the CM interference caused by dv/dt and ensure that the unwanted signal peak-to-peak amplitude at the output, under the influence of dv/dt, does not exceed $\Delta v_{\varepsilon,pp}$, the minimum required CMRR of the measurement system at different frequencies f can be calculated as [21]

$$\left\{ \mathrm{CMRR} = 20\lg\frac{\mathrm{d}v/\mathrm{d}t}{\pi f \cdot \Delta v_{\varepsilon,pp}} \right\} \Leftrightarrow \left\{ \frac{\mathrm{d}v}{\mathrm{d}t} = \pi f \cdot \Delta v_{\varepsilon,pp} 10^{\frac{\mathrm{CMRR}}{20}} \right\}. \tag{2}$$

Considering the most rigorous conditions encountered during power devices dynamic testing, i.e., the characterization of high-side gate-source voltage $v_{gs,HS}$, it is necessary to address several challenges. These challenges include a very narrow effective voltage measuring range typically spanning from −5 to +20 V, testing conducted under harsh conditions of high CM interference span with a V_{dc} reaching several or even tens of kV, and the presence of an ultrafast CM interference noise source with a dv/dt beyond 100 V/ns. To effectively distinguish and accurately restore $v_{gs,HS}$ under such demanding CM interference, the $\Delta v_{\varepsilon,pp}$ is limited to no more than 1 V, which helps to further determine the minimum required CMRR on the basis of (2).

By utilizing the relationships (1) and (2), a four-quadrant coordinate system can be constructed, as shown in Fig. 7, where the direction of the arrows represents the future development trends of the WBG devices switching characteristics and the corresponding testing probes/systems performance.

The axes of this coordinate system are defined jointly by

$$(f_{BW} = 500\,\mathrm{MHz}) \equiv (t_r = 3.5\,\mathrm{ns}) \tag{3}$$

$$(\mathrm{d}v/\mathrm{d}t = 100\,\mathrm{V/ns}) \equiv (\mathrm{CMRR@100MHz} = 50\,\mathrm{dB}). \tag{4}$$

Within this representation, the parameters f_{BW} and CMRR serve as crucial performance indicators for the galvanically isolated probes/systems, while t_r and dv/dt depict the typical switching characteristics of the power semiconductor devices.

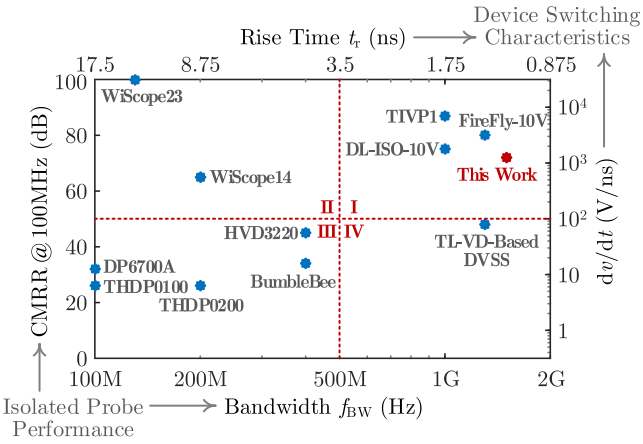

Fig. 7. Bandwidth performance f_{BW} of the state-of-the-art galvanically isolated probes/systems corresponds to the minimum rise time t_r of power devices that can be accurately characterized by them. CMRR performance at 100 MHz of the state-of-the-art galvanically isolated probes/systems corresponds to the maximum dv/dt of power devices that can be effectively immunized by them.

Based on Fig. 7, it is clear that high-performance differential voltage probes are positioned exclusively in quadrants III and IV. The CMRR@100 MHz, reaching 50 dB, represents a potential performance limit for the high-voltage differential measurements. Therefore, enhancing CMRR becomes a crucial aspect for further refining and optimizing high-performance differential measurement techniques. To surpass this constraint, measurement methods based on the nonelectrical isolation principles, situated in quadrants I and II, offer promising avenues for advancement.

By further integrating the evolving trends of next-generation WBG power devices depicted in Fig. 1, it becomes evident that the "Quadrant I" in Fig. 7 delineates the performance objectives for advanced measurement systems targeting dynamic testing of next-generation WBG power devices. More specifically, to effectively meet the dynamic testing requirements of the next-generation WBG devices, a high-performance testing system should exhibit the following performance metrics.

① To accurately characterize ultralow switching times within 5 ns, a high measurement bandwidth of at least 500 MHz is required.
② To effectively tackle the potential zero-drift issues resulting from the increasingly significant low-frequency CM source v_{CM}, which is exacerbated by higher blocking voltages reaching MV levels, the implementation of an appropriate galvanic isolation is imperative.
③ To effectively resist transient measurement issues induced by the high-frequency CM source dv/dt of up to 100 V/ns, a minimum CMRR of no less than 50 dB at 100 MHz is essential.

III. Concept Description, Operating Principle, and Design Considerations of Optical Dock

A. Concept Description of PIE

After undergoing extensive optimization and development, traditional nonisolated probes/systems such as passive probes,

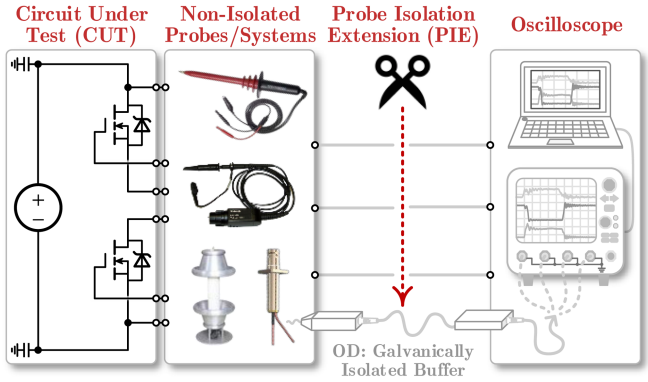

Fig. 8. PIE OD is compatible with various nonisolated probes/systems outputs, serving as a galvanically isolated buffer between nonisolated probes/systems and oscilloscope, effectively blocking potential low- and high-frequency CM current paths.

current shunts, and MV single-ended attenuators, cf. Fig. 8, have evolved into a diverse range of high-performing options. They have successfully fulfilled various power-level testing requirements, utilizing ground potential G_E as the reference. Nevertheless, these testing methods fall short when it comes to characterizing the next-generation WBG power devices, which exhibit higher blocking voltages and dv/dt, and consequently introduce the inextricable CM testing issues. Beyond these, further considering the pressing requirements for the dynamic characterization of the high-side power devices, traditional nonisolated measurement techniques relying on G_E as a reference prove clearly powerless in addressing these specific challenges.

In order to effectively tackle the aforementioned challenges, the concept of PIE is introduced. It acts as a high-performance galvanically isolated buffer, cf. Fig. 8, to disrupt the connection pathway between the output of the nonisolated probes/systems and the input of the oscilloscope, meanwhile blocking the potential CM current paths, as depicted in Figs. 3 and 5. To meet the performance demands of next-generation measurement systems discussed in Section II-B, the PIE should exhibit the following characteristics.

① *Flexibility:* PIE's input should possess compatibility with diverse output load requirements of nonisolated probes/systems, enabling a flexible isolated extension of suitable nonisolated methods for different testing scenarios.
② *Galvanic Isolation:* PIE should serve as a buffer between the front-end power stage and the back-end signal stage by employing nonelectric physical quantities, to maximize the interruption of potential CM current paths throughout the entire measurement system.
③ *High Bandwidth:* PIE's bandwidth should significantly exceed that of nonisolated probes/systems to ensure that the excellent electrical performance of various traditional nonisolated testing methods can still be fully utilized after integrating PIE.
④ *High CMRR and Robust dv/dt Immunity:* PIE should possess a wideband high CMRR to effectively suppress various CM issues resulting from ultrahigh dv/dt surpassing 100 V/ns, thereby accurately reproducing the measured signals.

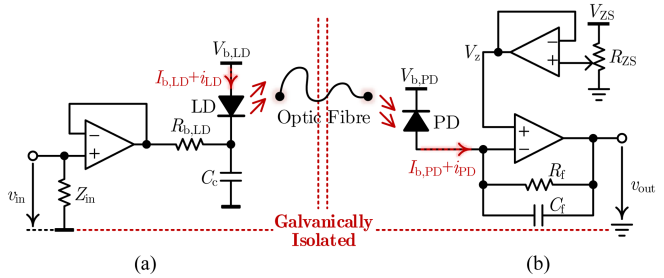

Fig. 9. Schematic overview of proposed optical dock. (a) Optical dock frontend (OD-FE). (b) Optical dock backend (OD-BE).

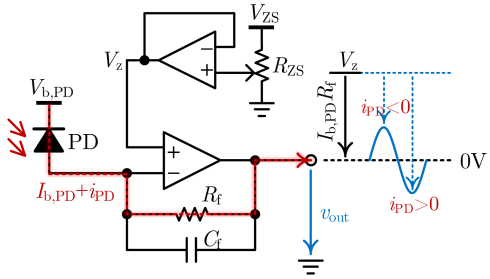

Fig. 10. DC operating point setting and zero setting principle of OD.

B. Operating Principle of Proposed Optical Dock

The configuration of the proposed PIE OD is depicted in Fig. 9, comprising three primary components: 1) optical dock frontend (OD-FE), 2) optic fiber, and 3) optical dock backend (OD-BE). The OD utilizes an optical pathway to separate the front-end power stage from the back-end signal stage. Essential components primarily involve a laser diode (LD) in the OD-FE and a photodiode (PD) in the OD-BE.

Note that, the main purpose of this section is to introduce the fundamental operating principles of the OD. This includes deriving the forward gain from the input $v_{\rm in}$ to the output $v_{\rm out}$ in the low and medium frequency range, without taking into account the role of $C_{\rm c}$ and $C_{\rm f}$ illustrated in Fig. 9. For a more comprehensive understanding of the high-frequency design considerations and parameter setting for the $C_{\rm c}$ and $C_{\rm f}$, please refer to Section III-C.

1) OD-FE, cf. Fig. 9(a): To cater to the output load requirements of different nonisolated probes/systems, the OD is equipped with a switchable input impedance $Z_{\rm in}$, which can be set between 50 Ω and 1 MΩ. Furthermore, to ensure optimal dynamic response performance of the LD, it is crucial to prevent it from switching between ON and OFF states during regular operation. These safeguards also against introducing nonlinear distortion that arise from LD toggling. Consequently, it becomes necessary to establish a dc operating point for the OD system, allowing the transmission signals along the entire chain to oscillate around the dc operating point, facilitating a linearized approximation.

Based on Fig. 9(a), the positive terminal of the LD is supplied with the bias voltage $V_{\rm b,LD}$. Subsequently the bias current $I_{\rm b,LD}$ is directed in the reverse direction through the bias resistor $R_{\rm b,LD}$ and injected into the op-amp. This current serves as the basis for establishing the LD's dc operating point. By following this current path, applying the Kirchhoff's voltage law, it can be obtained that

$$\begin{aligned} I_{\rm b,LD}+i_{\rm LD} &= \frac{V_{\rm b,LD}-V_{\rm op,LD}}{R_{\rm b,LD}}+\frac{-1}{R_{\rm b,LD}}v_{\rm in} \\ &= \frac{V_{\rm b,LD}-V_{\rm op,LD}}{R_{\rm b,LD}}+A_{\rm FE,LF}v_{\rm in} \end{aligned} \tag{5}$$

where $V_{\rm op,LD}$ represents the forward operating voltage of the LD. $R_{\rm b,LD}$ serves a dual purpose, acting as both the bias resistor that limits the value of $I_{\rm b,LD}$, and the low-frequency gain resistor that sets the basic gain $A_{\rm FE,LF}$ of the OD-FE. $v_{\rm in}$ and $i_{\rm LD}$ correspond to the input voltage signals and small-signal current oscillating around the dc operating point of the LD, respectively.

Once the LD bias current $I_{\rm b,LD}$ and the small-signal current $i_{\rm LD}$ traverse through the LD, the resulting optical power output from the LD can be calculated as

$$P_{\rm b,LD}+p_{\rm LD}=\alpha\left[(I_{\rm b,LD}-I_{\rm th,LD})+i_{\rm LD}\right] \tag{6}$$

where α denotes the slope efficiency, or differential efficiency, of the electrically pumped LD, which is measured in W/A. It characterizes the relationship between the LD's output optical power and the effective pump current above the threshold current, i.e., "$I_{\rm b,LD}-I_{\rm th,LD}$". The disparity between $I_{\rm b,LD}$ and $I_{\rm th,LD}$ plays a role in determining the fixed bias optical power $P_{\rm b,LD}$, which also establishes the dc operating point of the electro-optic-electro link. On the other side, the current $i_{\rm LD}$ corresponds to the signal optical power $p_{\rm LD}$ fluctuating around the $P_{\rm b,LD}$.

2) OD-BE, cf. Fig. 9(b): The optical power "$P_{\rm b,LD}+p_{\rm LD}$" emitted by the LD in the OD-FE is then transmitted through an optical fiber to reach the PD situated in the OD-BE. The PD receives this optical power, which subsequently leads to the generation of both a static bias current $I_{\rm b,PD}$ and a dynamic signal current $i_{\rm PD}$. These currents can be mathematically expressed as

$$I_{\rm b,PD}+i_{\rm PD}=\beta(P_{\rm b,LD}+p_{\rm LD}) \tag{7}$$

where β is the responsivity of the PD under a given bias voltage $V_{\rm b,PD}$, measured in A/W. It indicates the amount of conduction current induced in the PD per unit input optical power.

The flow of the bias current $I_{\rm b,PD}$ through $R_{\rm f}$ will create a static dc bias voltage. Hence, it is essential to include a zeroing function in the OD-BE to ensure that the output signal $v_{\rm out}$, driven by the dynamic signal current $i_{\rm PD}$, fluctuates around the ground reference potential, cf. Fig. 10. This process can be expressed as

$$\begin{aligned} &\{v_{\rm out}=V_{\rm z}-(I_{\rm b,PD}+i_{\rm PD})R_{\rm f}\}\overset{V_{\rm z}=I_{\rm b,PD}R_{\rm f}}{\Rightarrow} \\ &\{v_{\rm out}=-R_{\rm f}i_{\rm PD}=A_{\rm BE,LF}i_{\rm PD}\} \end{aligned} \tag{8}$$

where $A_{\rm BE,LF}$ is defined as the low-frequency gain, also known as the basic gain, of the OD-BE.

From (8) and Fig. 10, it can be observed that by adjusting the zeroing resistor $R_{\rm ZS}$, either automatically or manually, in a way that makes the output of the zeroing circuit $V_{\rm z}$ equal to $I_{\rm b,PD}R_{\rm f}$,

the OD-BE's output $v_{\rm out}$ will exhibit no additional dc bias and will solely rely on the dynamic signal current $i_{\rm PD}$.

In Fig. 10, when $i_{\rm PD} < 0$, it signifies a decrease in the total current "$I_{\rm b,PD} + i_{\rm PD}$" flowing through the PD. This reduction implies a decrease in the optical power received by the PD. However, it is essential to emphasize that the total current "$I_{\rm b,PD} + i_{\rm PD}$" cannot decrease to zero. If the PD has no current output, it means there is no optical power present in the optical path, which would result in the LD being turned OFF. This situation is not permissible during the normal operation of the OD.

Combining (8) with (6) and (7), $V_{\rm z}$ can be further determined by

$$V_{\rm z} = I_{\rm b,PD} R_{\rm f} = \beta P_{\rm b,LD} R_{\rm f} = \alpha\beta (I_{\rm b,LD} - I_{\rm th,LD}) R_{\rm f} \quad (9)$$

where the term $\alpha\beta$ represents the equivalent gain along the electro-optic-electro link. Introducing $V_{\rm z}$ is like applying a dc common-mode voltage to both the positive and negative input terminals of the op-amp. Consequently, if the current in the circuit diminishes to zero, $v_{\rm out}$ will progressively rise until it reaches $V_{\rm z}$. However, during the normal operation of the OD, where "$I_{\rm b,PD} + i_{\rm PD}$" is consistently greater than zero, $v_{\rm out}$ will always remain below $V_{\rm z}$. The zero setting principle depicted in Fig. 10 provides a clearer understanding of this concept.

Therefore, $V_{\rm z}$ determines the upper limit of the dynamic output of the OD-BE. To obtain the maximum dynamic output range, $R_{\rm f}$ should be adjusted so that $V_{\rm z}$ closely approaches the op-amp's common-mode input voltage upper limit, denoted as $V_{\rm IH}$. Based on (9), $R_{\rm f}$ can be determined as

$$\{V_{\rm z} = V_{\rm IH}\} \Rightarrow \{R_{\rm f} = V_{\rm IH}/[\alpha\beta(I_{\rm b,LD} - I_{\rm th,LD})]\}. \quad (10)$$

In conclusion, starting from (8) and tracing back to (5), after properly zeroing the system, the overall forward transmission gain of the OD from $v_{\rm in}$ to $v_{\rm out}$ is given by

$$\begin{aligned} v_{\rm out} &= -R_{\rm f} i_{\rm PD} = -\beta R_{\rm f} p_{\rm LD} = -\alpha\beta R_{\rm f} i_{\rm LD} = \alpha\beta \frac{R_{\rm f}}{R_{\rm b,LD}} v_{\rm in} \\ &= \alpha\beta A_{\rm FE,LF} A_{\rm BE,LF} v_{\rm in}. \end{aligned} \quad (11)$$

Upon examining (11), it becomes evident that integrating the OD into the original nonisolated measurement system, cf. Fig. 8, delivers exceptional galvanic isolation to the entire system while introducing a proportional gain of $\alpha\beta A_{\rm FE,LF} A_{\rm BE,LF}$. This gain is codetermined by the OD-FE's electrical gain $A_{\rm FE,LF}$, the electro-optic-electro link gain $\alpha\beta$, and the OD-BE's electrical gain $A_{\rm BE,LF}$.

C. Bandwidth Design Considerations of Optical Dock

1) Optical Dock Frontend: When the LD operates in the vicinity of its dc operating point, the voltage across the LD terminals, known as the LD forward operating voltage $V_{\rm op,LD}$, remains relatively stable. In contrast, the LD output current $i_{\rm LD}$ changes in response to variations in $v_{\rm in}$. Essentially, this behavior can be likened to that of a controlled voltage source. Consequently, during high-frequency analysis, it is important to account for the presence of parasitic inductance along the LD loop, denoted as $L_{\rm LD}$, as illustrated in Fig. 11.

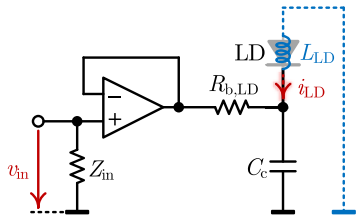

Fig. 11. High-frequency small-signal equivalent circuit of OD-FE.

In the absence of $C_{\rm c}$, the forward gain of the OD-FE $A_{\rm FE}$ from $v_{\rm in}$ to $i_{\rm LD}$ can be expressed as

$$\begin{aligned} A_{\rm FE} &= \frac{i_{\rm LD}}{v_{\rm in}} = -\frac{1}{R_{\rm b,LD} + sL_{\rm LD}} = \frac{-1/R_{\rm b,LD}}{L_{\rm LD}/R_{\rm b,LD} s + 1} \\ &= \frac{A_{\rm FE,LF}}{\tau s + 1} \end{aligned} \quad (12)$$

where $s = {\rm j}2\pi f$ stands for the complex frequency. $\tau = L_{\rm LD}/R_{\rm b,LD}$ is defined as the time constant of the first-order system. The bandwidth of the first-order system represented in (12), denoted as $f_{\rm BW,FE}^{\rm 1st}$, can be further calculated as

$$f_{\rm BW,FE}^{\rm 1st} = \frac{1}{2\pi\tau} = \frac{1}{2\pi} \frac{R_{\rm b,LD}}{L_{\rm LD}}. \quad (13)$$

Clearly, the presence of $L_{\rm LD}$ will have an impact on the high-frequency characteristics of $A_{\rm FE}$. To further improve the OD-FE's bandwidth, a compensating capacitance $C_{\rm c}$ is introduced in parallel to the LD terminals, cf. Fig. 11. In this scenario, $A_{\rm FE}$ undergoes further modification and can be expressed as

$$\begin{aligned} A_{\rm FE} &= \frac{i_{\rm LD}}{v_{\rm in}} = -\frac{\frac{1}{sC_{\rm c}} \parallel sL_{\rm LD}}{R_{\rm b,LD} + \frac{1}{sC_{\rm c}} \parallel sL_{\rm LD}} \Big/ sL_{\rm LD} \\ &= \frac{-1}{s^2 R_{\rm b,LD} L_{\rm LD} C_{\rm c} + sL_{\rm LD} + R_{\rm b,LD}} \\ &= \frac{-\frac{1}{R_{\rm b,LD}} \cdot \left(\frac{1}{\sqrt{L_{\rm LD}C_{\rm c}}}\right)^2}{s^2 + 2 \cdot \frac{1}{2R_{\rm b,LD}} \sqrt{\frac{L_{\rm LD}}{C_{\rm c}}} \cdot \frac{1}{\sqrt{L_{\rm LD}C_{\rm c}}} s + \left(\frac{1}{\sqrt{L_{\rm LD}C_{\rm c}}}\right)^2} \\ &= \frac{A_{\rm FE,LF}\omega_{\rm n}^2}{s^2 + 2\zeta\omega_{\rm n} s + \omega_{\rm n}^2} \end{aligned} \quad (14)$$

where ζ and $\omega_{\rm n} = 2\pi f_{\rm n}$ represent the damping ratio and natural angular frequency of the second-order system, respectively, and can be expressed as

$$\zeta = \frac{1}{2R_{\rm b,LD}} \sqrt{\frac{L_{\rm LD}}{C_{\rm c}}} \quad (15)$$

$$f_{\rm n} = \frac{\omega_{\rm n}}{2\pi} = \frac{1}{2\pi\sqrt{L_{\rm LD}C_{\rm c}}}. \quad (16)$$

Based on (14), it is evident that incorporating $C_{\rm c}$ transforms the OD-FE from a first-order system to a typical second-order system. Consequently, the system bandwidth $f_{\rm BW,FE}^{\rm 2nd}$ in this case can be calculated as

$$f_{\rm BW,FE}^{\rm 2nd} = f_{\rm n} \sqrt{1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}}$$

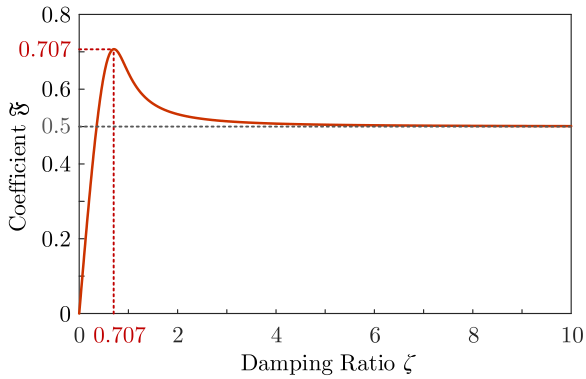

Fig. 12. Variation of coefficient $\mathfrak{F}$ with respect to damping ratio ζ.

$$= \frac{1}{\pi}\frac{R_{\mathrm{b,LD}}}{L_{\mathrm{LD}}}\zeta\sqrt{1-2\zeta^2+\sqrt{2-4\zeta^2+4\zeta^4}}. \quad (17)$$

To facilitate analysis, coefficient $\mathfrak{F}$ is introduced and defined as

$$\mathfrak{F} = \zeta\sqrt{1-2\zeta^2+\sqrt{2-4\zeta^2+4\zeta^4}}. \quad (18)$$

And the plot in Fig. 12 illustrates the variation of the coefficient $\mathfrak{F}$ with respect to the damping ratio ζ.

First, based on Fig. 12, a comparison between (13) and (17) demonstrates that the fundamental bandwidth of the OD-FE is determined by $R_{\mathrm{b,LD}}$ and L_{LD}. Minimizing the length of the LD loop to reduce the equivalent L_{LD} proves to be an effective approach for enhancing the bandwidth of the OD-FE.

Second, when the parameters $R_{\mathrm{b,LD}}$ and L_{LD} are determined, decreasing the compensating capacitance C_{c} corresponds to an increase in ζ, causing $f^{\mathrm{2nd}}_{\mathrm{BW,FE}}$ to approach $f^{\mathrm{1st}}_{\mathrm{BW,FE}}$. This process can be represented as

$$\lim_{C_{\mathrm{c}}\to 0} f^{\mathrm{2nd}}_{\mathrm{BW,FE}} = \lim_{\zeta\to\infty} f^{\mathrm{2nd}}_{\mathrm{BW,FE}} = \lim_{\mathfrak{F}\to 1/2} f^{\mathrm{2nd}}_{\mathrm{BW,FE}} = f^{\mathrm{1st}}_{\mathrm{BW,FE}}. \quad (19)$$

Hence, when adopting a conservative design approach, it is feasible to exclude the use of C_{c}. In such cases, the OD-FE can still attain a fundamental bandwidth $f^{\mathrm{1st}}_{\mathrm{BW,FE}}$, as defined in (13).

In order to attain a higher bandwidth, careful selection of C_{c} is necessary. To ensure that $f^{\mathrm{2nd}}_{\mathrm{BW,FE}}$ is always greater than $f^{\mathrm{1st}}_{\mathrm{BW,FE}}$, the following conditions must be satisfied:

$$\left\{f^{\mathrm{2nd}}_{\mathrm{BW,FE}} \geq f^{\mathrm{1st}}_{\mathrm{BW,FE}}\right\} \Rightarrow \{\mathfrak{F} \geq 1/2\} \Rightarrow \left\{\zeta \geq \sqrt{2}\Big/4\right\} \Rightarrow \left\{C_{\mathrm{c}} \leq \frac{2L_{\mathrm{LD}}}{R^2_{\mathrm{b,LD}}}\right\}. \quad (20)$$

Considering Fig. 12 and (20), it is evident that choosing an excessively large value of C_{c}, surpassing $2L_{\mathrm{LD}}/R^2_{\mathrm{b,LD}}$, not only fails to increase the bandwidth, but can also leads to a considerable degradation in system performance. When the damping ratio ζ is set to its optimum value, the corresponding appropriate value for the C_{c} can be determined accordingly as

$$\left\{\zeta = \frac{\sqrt{2}}{2}\right\} \Rightarrow \left\{C_{\mathrm{c}} = \frac{L_{\mathrm{LD}}}{2R^2_{\mathrm{b,LD}}}\right\}. \quad (21)$$

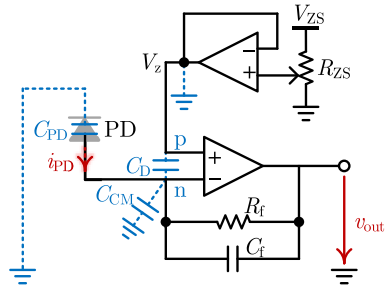

Fig. 13. High-frequency small-signal equivalent circuit of OD-BE.

In this scenario, the maximum value of $f^{\mathrm{2nd}}_{\mathrm{BW,FE}}$ is attained, which also represents the upper limit of the bandwidth achievable by the OD-FE, denoted as $f_{\mathrm{BW,FE}}$, and can be expressed as

$$f_{\mathrm{BW,FE}} = f^{\mathrm{2nd}}_{\mathrm{BW,FE}}\left(\zeta = \frac{\sqrt{2}}{2}\right) = \frac{\sqrt{2}}{2\pi}\frac{R_{\mathrm{b,LD}}}{L_{\mathrm{LD}}} = \sqrt{2}f^{\mathrm{1st}}_{\mathrm{BW,FE}}. \quad (22)$$

Upon comparing (13) and (22), it can be concluded that the addition of C_{c} has the potential to increase the OD-FE's system bandwidth by up to 41.4%, compared to the original $f^{\mathrm{1st}}_{\mathrm{BW,FE}}$.

2) Optical Dock Backend: Unlike the LD, PD operates at a fixed voltage of "$V_{\mathrm{b,PD}} - V_{\mathrm{z}}$" across its terminals when working at the dc operating point. However, its output current i_{PD} varies with the input optical power, resembling a controlled current source. Hence, during the high-frequency analysis, it becomes important to take into account the junction capacitance of the PD, represented as C_{PD}, cf. Fig. 13.

The open-loop gain of the op-amp utilized in the OD-BE is defined as

$$A_{\mathrm{ol}} = |A_{\mathrm{ol}}|\,\mathrm{e}^{\mathrm{j}\varphi_{\mathrm{ol}}} \quad (23)$$

where $|A_{\mathrm{ol}}|$ and φ_{ol} denote the open-loop gain magnitude and phase, respectively. According to Fig. 13, the closed-loop gain A_{cl} of the OD-BE from i_{PD} to v_{out} can be expressed as

$$A_{\mathrm{cl}} = \frac{v_{\mathrm{out}}}{i_{\mathrm{PD}}} = \frac{-Z_{\mathrm{f}}}{1+\frac{G_{\mathrm{n}}}{A_{\mathrm{ol}}}} = \frac{-Z_{\mathrm{f}}}{1+\frac{1+Z_{\mathrm{f}}/Z_{\mathrm{g}}}{A_{\mathrm{ol}}}} \quad (24)$$

where $G_{\mathrm{n}} = 1+Z_{\mathrm{f}}/Z_{\mathrm{g}}$ represents the noise gain, and $A_{\mathrm{ol}}/G_{\mathrm{n}}$ is the loop gain. Z_{g} and Z_{f} signify the impedance along the input and feedback branch, respectively, and can be written as

$$Z_{\mathrm{g}} = \frac{1}{sC_{\mathrm{g}}} = \frac{1}{s(C_{\mathrm{PD}}+C_{\mathrm{D}}+C_{\mathrm{CM}})} \quad (25)$$

$$Z_{\mathrm{f}} = R_{\mathrm{f}} \parallel \frac{1}{sC_{\mathrm{f}}} = \frac{R_{\mathrm{f}}}{sR_{\mathrm{f}}C_{\mathrm{f}}+1} \quad (26)$$

where $C_{\mathrm{g}} = C_{\mathrm{PD}} + C_{\mathrm{D}} + C_{\mathrm{CM}}$ represents the total equivalent input capacitance. C_{D} refers to the differential input capacitance of the op-amp, which also corresponds to the parasitic capacitance between the p and n ports in Fig. 13. C_{CM} indicates the common-mode input capacitance of the op-amp, which also represents the parasitic capacitance relative to ground for a single input port, i.e., p or n. R_{f} and C_{f} denote the feedback resistance and capacitance of the op-amp, respectively.

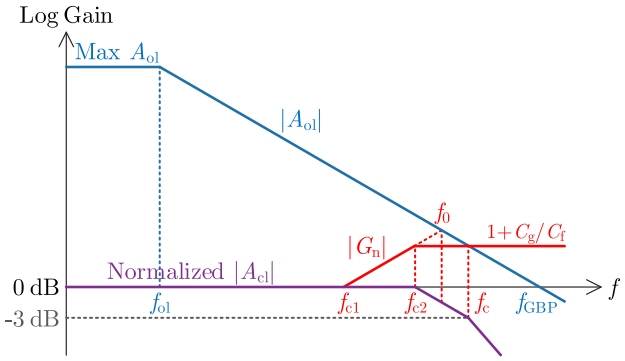

Fig. 14. Magnitude characteristics of open-loop gain $|A_{ol}|$, noise gain $|G_n|$, and normalized closed-loop gain $|A_{cl}|$ of OD-BE.

G_n can be further expanded based on (25) and (26) as

$$G_n = 1 + \frac{Z_f}{Z_g} = \frac{sR_f(C_g + C_f) + 1}{sR_fC_f + 1}. \tag{27}$$

As the frequency f increases, G_n can be approximately divided into segments, cf. Fig. 14, as

$$\begin{aligned} \underline{f < f_{c1}}, G_n &= 1 \\ \underline{f_{c1} \le f < f_{c2}}, G_n &= sR_f(C_g + C_f) \\ \underline{f \ge f_{c2}}, G_n &= 1 + C_g/C_f \end{aligned} \tag{28}$$

where f_{c1} and f_{c2} signify the first and second corner frequencies of G_n, respectively, and can be expressed as

$$f_{c1} = \frac{1}{2\pi R_f(C_g + C_f)} \tag{29}$$

$$f_{c2} = \frac{1}{2\pi R_fC_f}. \tag{30}$$

By referring to Fig. 14, additional definitions can be established for the central frequency f_0 and cut frequency f_c, which can be expressed as

$$f_0 = \sqrt{f_{c1}f_{GBP}} = \sqrt{\frac{f_{GBP}}{2\pi R_f(C_g + C_f)}} \tag{31}$$

$$f_c = \frac{f_{GBP}}{|G_n(f = f_c \ge f_{c2})|} = \frac{f_{GBP}}{1 + C_g/C_f} \tag{32}$$

where f_{GBP} represents the gain bandwidth product of the op-amp.

By combining (24) and (28), along with the information provided in Fig. 14, closed-loop gain A_{cl} can be approximately divided into segments as

$$\begin{aligned} \underline{f < f_{c2}}, A_{cl} &= -R_f/1 = -R_f = A_{BE,LF} \\ \underline{f_{c2} \le f < f_c}, A_{cl} &= -\frac{1}{sC_f}\Big/1 = -\frac{1}{sC_f} \\ \underline{f \ge f_c}, A_{cl} &= -\frac{1}{sC_f}\Big/\frac{G_n}{A_{ol}} = -\frac{A_{ol}}{sC_f}\Big/\frac{C_g + C_f}{C_f} \\ &= -\frac{A_{ol}}{s(C_g + C_f)}. \end{aligned} \tag{33}$$

According to (33) and Fig. 14, it can be observed that $|A_{cl}|$ transitions from a constant gain $A_{BE,LF}$ to a decay rate of -20 dB/dec at f_{c2} and further to a decay rate of -40 dB/dec at f_c. Therefore, the frequency range from f_{c2} to f_c determines the bandwidth of $|A_{cl}|$. In this context, the amplitude margin coefficient k is introduced to constrain the frequency range over which $|A_{cl}|$ decays at a rate of -20 dB/dec, and defined as

$$k = \frac{f_{c2}}{f_0} = \frac{f_0}{f_c} = \sqrt{\frac{f_{c2}}{f_c}} \le 1. \tag{34}$$

It is worth noting that a higher value of k, approaching 1, suggests that $|G_n|$ is more likely to intersect $|A_{ol}|$ with a slope of $+40$ dB/dec, potentially increasing the system's tendentiousness to instability.

By utilizing (30) and (32), (34) can be further expanded as

$$k^2 = \frac{f_{c2}}{f_c} = \frac{1}{2\pi R_fC_f}\Big/\frac{f_{GBP}}{1 + C_g/C_f}. \tag{35}$$

After further simplification, it can be obtained that

$$2\pi R_f f_{GBP} k^2 C_f^2 - C_f - C_g = 0. \tag{36}$$

Given $C_f > 0$, there exists a unique solution for (36), namely

$$C_f = \frac{1 + \sqrt{1 + 8\pi R_f f_{GBP} k^2 C_g}}{4\pi R_f f_{GBP} k^2}. \tag{37}$$

Upon examining (37), it can be observed that C_f is exclusively determined by k. To attain the highest possible bandwidth while maintaining system stability, the cut frequency f_c is selected as the -3 dB point of $|A_{cl}|$, marking the transition from a decay rate of -20 dB/dec to -40 dB/dec. By incorporating the insights presented in Fig. 14, we can further derive

$$\left\{20\lg\frac{f_{c2}}{f_c} = -3\right\} \Rightarrow \left\{\frac{f_{c2}}{f_c} = \frac{1}{\sqrt{2}}\right\} \Rightarrow \left\{k = \sqrt{\frac{f_{c2}}{f_c}} = 0.84\right\}. \tag{38}$$

Substituting k further into (37), C_f can be finally determined as

$$C_f = \frac{1 + \sqrt{1 + 4\sqrt{2}\pi R_f f_{GBP} C_g}}{2\sqrt{2}\pi R_f f_{GBP}} \tag{39}$$

where f_{GBP} and C_g are determined by the specific parameters of the op-amp and PD being used, while R_f is determined by (10), all of which are known in this context. Therefore, by utilizing these known values and determining the necessary C_f based on (39), we can calculate the theoretical bandwidth of the OD-BE denoted as $f_{BW,BE}$, which is given by

$$f_{BW,BE} = f_c = \frac{f_{GBP}}{1 + C_g/C_f}. \tag{40}$$

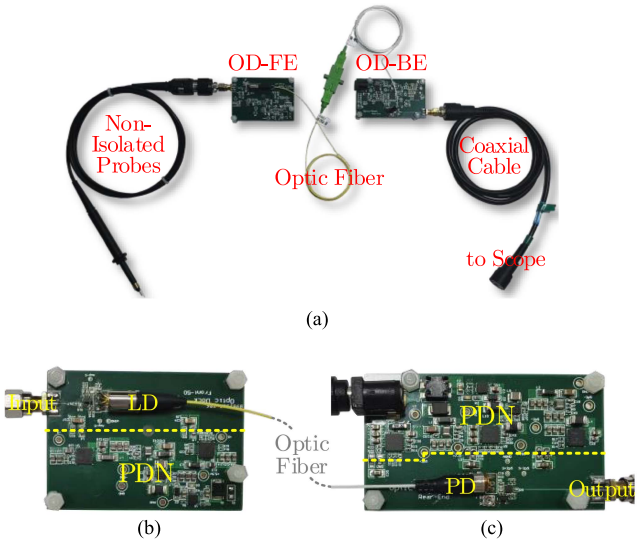

Fig. 15. (a) Experimental prototype of proposed PIE OD. (b) OD-FE zoom-in. (c) OD-BE zoom-in.

IV. Frequency-Domain Performance Characterization

A. Design Parameters and Theoretical Performance of Developed Optical Dock

Based on the principles illustrated in Fig. 9, an OD prototype was constructed, cf. Fig. 15, comprising three parts: 1) OD-FE, 2) optical fiber, and 3) OD-BE.

First, the output of nonisolated probes/systems is directly linked to the input of the OD-FE. The input impedance Z_{in} of the OD-FE can be switched flexibly between 50 Ω and 1 MΩ, accommodating various common nonisolated probes/systems output connection requirements. *Second*, the OD acts as a high-performance galvanically isolated buffer between front-end power stage and back-end signal stage. It effectively eliminates potential CM current paths, minimizing the effects of v_{CM} and dv/dt on the measurement results. *Finally*, the output of the OD-BE is connected to the 50-Ω input of the oscilloscope using a 50-Ω coaxial cable, ensuring impedance matching for the optimal design bandwidth performance.

To guarantee that the main circuit in Fig. 9 attains its design goals and maximizes system performance, a high-performance power distribution network is essential for providing support, as demonstrated in Fig. 15(b) and (c).

Specifically, OD-FE requires three voltage rails: two for the ±5-V op-amp supply and another for the +5-V LD bias supply, $V_{\text{b,LD}}$. The positive supply for the OD-FE op-amp and the LD bias supply share a common rail. On the other hand, OD-BE requires four voltage rails: besides the ±2.5-V op-amp supply, it also needs a +7-V PD bias supply, $V_{\text{b,PD}}$, and a +2.5-V zero-setting supply, V_{ZS}. Likewise, the positive supply for the OD-BE op-amp and the zero-setting supply share a common rail.

To ensure a high-quality system power supply, each voltage rail, post rectification by a switched-mode power supply (SMPS) to the desired voltage level, is additionally paired with a low dropout regulator characterized by ultralow noise and a very high power supply rejection ratio for enhanced noise elimination and filtering. This step is crucial for reducing the impact of SMPS switching ripple on the electro-optic-electro link depicted in Fig. 9.

TABLE I
Design Parameters of Optical Dock Frontend (OD-FE)

Parameters	Symbol	Value
Input Impedance of OD-FE	Z_{in}	50 Ω/1 MΩ
Operating Wavelength of LD	λ	1550 nm
Bias Voltage for LD	$V_{\text{b,LD}}$	5.0 V
Forward Voltage of LD	$V_{\text{op,LD}}$	1.2 V
Bias Resistance for LD	$R_{\text{b,LD}}$	100 Ω
Low-Frequency Gain of OD-FE	$A_{\text{FE,LF}}$	−0.01
Threshold Current of LD	$I_{\text{th,LD}}$	10 mA
Bias Current for LD	$I_{\text{b,LD}}$	38 mA
Slope Efficiency of LD	α	0.20 W/A
Parasitic Inductance of LD Loop	L_{LD}	11.6 nH
Compensated Capacitance	C_{c}	1.3 pF
Damping Ratio	ζ	0.47
Natural Frequency	f_{n}	1.30 GHz
Theo. Bandwidth of OD-FE	$f_{\text{BW,FE}}$	1.69 GHz

TABLE II
Design Parameters of Optical Dock Backend (OD-BE)

Parameters	Symbol	Value
Gain Bandwidth Product of OPA855	f_{GBP}	8 GHz
Bandwidth of PD	f_{PD}	2.5 GHz
Bias Voltage for PD	$V_{\text{b,PD}}$	7.0 V
CM Input Upper Limit of OPA855	V_{IH}	2.1 V
Zero Setting Range of OD-BE	V_{z}	0–2.5 V
Responsivity of PD	β	0.95 A/W
Feedback Resistance	R_{f}	400 Ω
Low-Frequency Gain of OD-BE	$A_{\text{BE,LF}}$	−400
Junction Capacitance of PD	C_{PD}	1.2 pF
Input Capacitance of OPA855	C_{D}+C_{CM}	0.8 pF
Total Input Capacitance	C_{g}	2.0 pF
Feedback Capacitance	C_{f}	0.4 pF

Tables I and II present the comprehensive design parameters for OD-FE and OD-BE, respectively. For specific details regarding the parameters and technical specifications of the Fabry–Perot/distributed feedback analog LD utilized in the OD-FE, as well as the InGaAs PD employed in the OD-BE, please refer to [25].

The TI LMH6559 [26] is used as the unit gain buffer in OD-FE, offering a bandwidth of 1.75 GHz. As specified in Table I, the bias resistor for the LD $R_{\text{b,LD}}$ is configured as 100 Ω, while the loop inductance of the LD, L_{LD} is calibrated to 11.6 nH using a vector network analyzer Agilent E5061B.

Initially, without the addition of C_{c}, the bandwidth of OD-FE can be calculated as $f_{\text{BE,FE}}^{1\text{st}} = 1.37$ GHz using (13). To further enhance the system bandwidth, (20) suggests that the damping ratio ζ of the system, after incorporating C_{c}, should not be less than 0.35, while C_{c} should not exceed 2.32 pF. By selecting an appropriate value for C_{c} to achieve the optimal damping ratio, it is determined to be 0.58 pF. At this value, the upper limit of the bandwidth for OD-FE can be established as $f_{\text{BW,FE}} = 1.94$ GHz. The impact of incorporating C_{c} on the enhancement of OD-FE bandwidth is visually demonstrated in Fig. 16.

However, it is important to note that the damping ratio ζ in this article is not set to its optimal value, as listed in Table I. This is due to the design of OD-BE shown in Fig. 14, where the

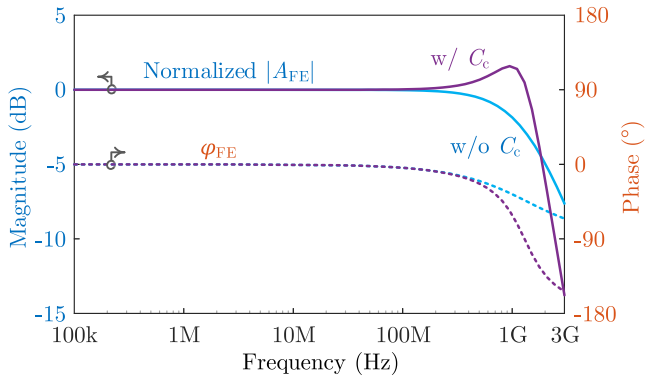

Fig. 16. Forward gain A_{FE} of OD-FE, comprising normalized amplitude $|A_{FE}|$ and phase φ_{FE}, with and without the inclusion of C_c.

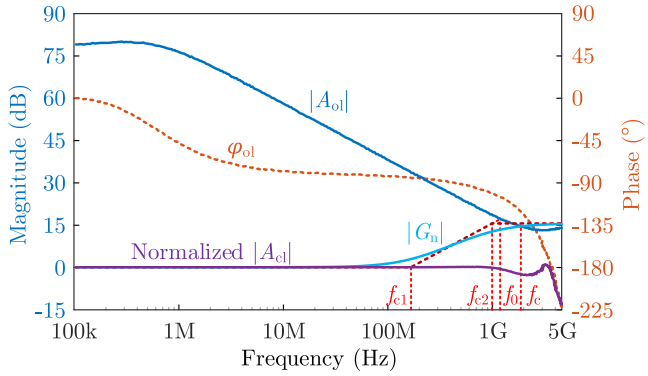

Fig. 17. Open-loop gain A_{ol} of employed OPA855 [27], including amplitude $|A_{ol}|$ and phase φ_{ol}. Noise gain magnitude $|G_n|$, and normalized closed-loop gain magnitude $|A_{cl}|$ of OD-BE.

TABLE III
THEORETICAL PERFORMANCE OF OPTICAL DOCK BACKEND (OD-BE)

Parameters	Symbol	Value
Corner Frequency 1	f_{c1}	0.17 GHz
Corner Frequency 2	f_{c2}	0.99 GHz
Central Frequency	f_0	1.17 GHz
Cut Frequency	f_c	1.91 GHz
Close-Loop Gain at f_c	$\lvert A_{cl}(f_c)\rvert$	−2.51 dB
Phase Margin	φ_m	58.7°@ f_c
Theo. Bandwidth of OD-BE	$f_{BW,BE}$	2.12 GHz

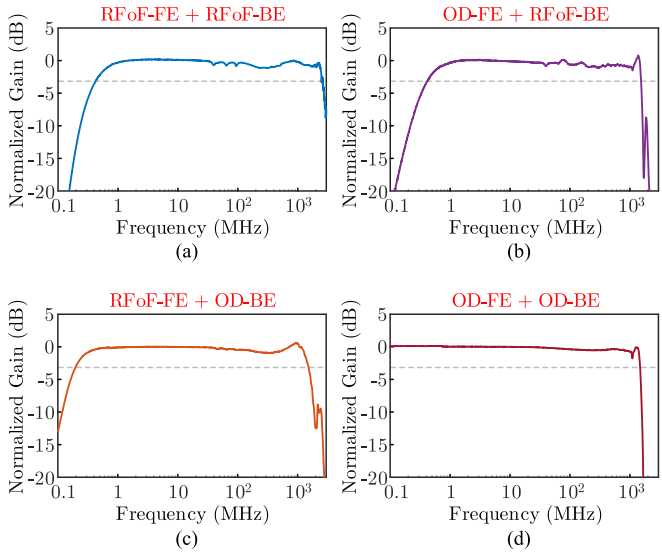

Fig. 18. Measured normalized forward gain of (a) RFoF, (b) OD-FE + RFoF-BE, (c) RFoF-FE + OD-BE, and (d) OD.

closed-loop gain A_{cl} is established with a smooth attenuation in the higher frequency range. Consequently, in the design of OD-FE, it becomes feasible to reduce the actual ζ from the optimum damping ratio, thereby creating a high-frequency gain peak to counteract the smooth attenuation characteristics of the OD-BE. This optimization process further enhances the overall flatness high-frequency gain of the PIE OD. Section IV-B provides additional explanations and visual validation of this approach.

The op-amp used in the OD-BE is TI OPA855 [27]. By substituting the design parameters from Table II into (29)–(32), the theoretical values of the four critical frequencies can be calculated as $f_{c1} = 0.17$ GHz, $f_{c2} = 0.99$ GHz, $f_0 = 1.15$ GHz, and $f_c = 1.33$ GHz, respectively. Moreover, by taking into account the open-loop gain A_{ol} provided in OPA855 datasheet, along with (24)–(26) and Table II, it is possible to plot the closed-loop gain A_{cl} of the OD-BE to obtain further insights. Refer to Fig. 17 for a visual representation of these results.

In comparison of Fig. 17 with Fig. 14, the presence of $|A_{ol}|$ distortion in the OPA855 at higher frequencies results in the actual bandwidth of OD-BE being slightly larger than the calculated theoretical value. By referring to Fig. 17, we can ascertain the specific values for several key frequencies: $f_{c1} = 0.17$ GHz, $f_{c2} = 0.99$ GHz, $f_0 = 1.17$ GHz, and $f_c = 1.91$ GHz. Moreover, at f_c, the phase margin φ_m is 58.7°, guaranteeing the overall stability of the system. The theoretical performance parameters of the OD-BE are summarized in Table III.

B. Forward Gain Characteristics Calibration of Optical Dock

To calibrate the frequency characteristics of the developed PIE OD, the forward transmission coefficient S_{21} is measured with the vector network analyzer Agilent E5061B.

In order to assess the performance of the FE and BE submodules in the developed OD, a programmable radio frequency over fiber (RFoF) module [28] with an operating frequency range from 0.5 MHz to 2.5 GHz is utilized. Just like the OD, the RFoF can be divided into three components: 1) RFoF front-end, 2) back-end, and 3) optical fiber. By integrating each of these components with their corresponding submodules in the OD, the independent validation and optimization of each submodule can be conducted, leading to an optimal overall design outcome, cf. Fig. 18.

Fig. 18(a) illustrates the normalized forward gain of the "RFoF-FE + RFoF-BE". The frequency range covers from 0.5 MHz to 2.5 GHz, which corresponds to the specified values in the RFoF datasheet. This indicates that RFoF can be utilized to calibrate the forward gain characteristics of the OD submodules within the frequency range of 0.5 MHz to 2.5 GHz.

Fig. 18(b) showcases the normalized forward gain of the "OD-FE + RFoF-BE". The frequency range below 0.5 MHz

predominantly depends on the characteristics of RFoF-BE. A minor gain peak of 0.7 dB is observed near 1.35 GHz, which closely aligns with the natural frequency f_n of 1.30 GHz shown in Table I. This gain peak is primarily attributed to a reduced design damping ratio ζ of 0.47. Consequently, the actual bandwidth of the OD-FE is 1.54 GHz, slightly lower than the theoretical value of 1.69 GHz. This difference may be because this theoretical bandwidth value is in close proximity to the nominal bandwidth of the LMH6559 buffer, which is 1.75 GHz.

Fig. 18(c) illustrates the normalized forward gain of the "RFoF-FE + OD-BE". Similar to Fig. 18(b), the frequency range below 0.5 MHz is influenced by the characteristics of RFoF-FE. At approximately 1.0 GHz, the gain exhibits a smooth decline at a rate close to −20 dB/dec, which closely aligns with the f_{c2} value of 0.99 GHz provided in Table III. The final calibrated bandwidth of OD-BE is determined to be 1.55 GHz, and around this frequency, the gain decay transitions from a rate of −20 dB/dec to a steeper rate of −40 dB/dec. The actual bandwidth of 1.55 GHz falls between the theoretical value of 1.33 GHz and the derived value of 2.12 GHz based on the open-loop characteristics A_{ol} as provided in the OPA855 datasheet. This discrepancy can still be attributed to the A_{ol} distortion of the OPA855 in the high-frequency range.

Fig. 18(d) showcases the normalized forward gain of the "OD-FE + OD-BE". Through an appropriate reduction of ζ of the OD-FE, a gain peak around 1.3 GHz is introduced, partially compensating for the smooth attenuation characteristics of the OD-BE at higher frequencies. Consequently, the developed OD achieves a remarkable measurement bandwidth of up to 1.53 GHz, while exhibiting highly flat properties across the spectrum, allowing for accurate capture of ultrafast switching edges with rise times as low as 1 ns.

C. Performance Parameters Comparison Between Cutting-Edge Galvanically Isolated Probes/Systems and Optical Dock

The developed OD is further compared to the state-of-the-art galvanically isolated probes/systems in terms of the normalized forward gain, measurement bandwidth, and broadband CMRR, as illustrated in Figs. 19 and 20. From Fig. 19, it is evident that OD exhibits an exceptionally high measurement bandwidth of up to 1.5 GHz and outstanding wideband gain flatness. This enables accurate characterization of ultrafast switching edges in next-generation WBG power devices, even with rise times as low as a few nanoseconds.

Fig. 20 reveals that using nonelectrical isolation techniques effectively prevents potential CM current paths within the entire measurement system when compared to traditional high-performance differential measurement methods. This leads to a significant improvement in the system's wideband CMRR, with an average enhancement of over 40 dB. Consequently, the system's immunity to dv/dt disturbances undergoes a significant improvement of more than a hundredfold, enabling accurate capturing of the high-side switching characteristics of next-generation WBG power devices.

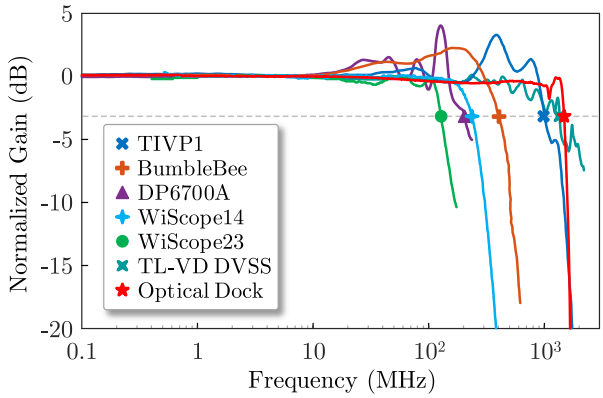

Fig. 19. Comparative analysis of measured normalized forward gain between cutting-edge galvanically isolated probes/systems and PIE OD.

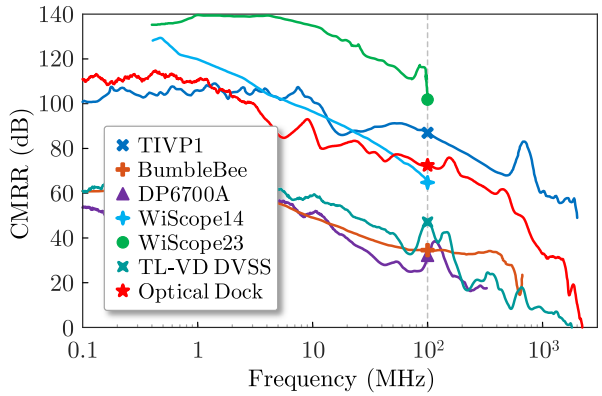

Fig. 20. Comparative analysis of measured CMRR between cutting-edge galvanically isolated probes/systems and PIE OD.

TABLE IV
KEY PERFORMANCE PARAMETERS COMPARISON BETWEEN CUTTING-EDGE GALVANICALLY ISOLATED PROBES/SYSTEMS AND DEVELOPED PIE OD

Probes/ Systems	Type	Dynamic Range	Bandwidth	CMRR @100MHz	dv/dt Immunity
TIVP1	Iso.	± 2.5 kV	1.00 GHz	87 dB	7.0 kV/ns
BumbleBee	Dif.	± 2.0 kV	0.40 GHz	34 dB	16 V/ns
Tl-Vd Dvss	Dif.	± 2.0 kV	1.30 GHz	48 dB	79 V/ns
DP6700A	Dif.	± 7.0 kV	0.10 GHz	32 dB	13 V/ns
WiScope14	Iso.	± −*	0.20 GHz	65 dB	560 V/ns
WiScope23	Iso.	± −*	0.13 GHz	102 dB	40 kV/ns
PIE OD	Iso.	± −*	1.53 GHz	72 dB	1.3 kV/ns

*Depending on the specifics of their front-end input connection.

The developed OD boasts an exceptional CMRR of 72 dB at 100 MHz, providing remarkable dv/dt immunity of up to 1.25 kV/ns. This capability enables highly effective mitigation of ultrafast dv/dt transients, including those encountered in the cutting-edge 10-kV SiC MOSFET power modules, which can reach speeds of up to 250 V/ns [1].

To facilitate a more intuitive comparison, the performance parameters of the state-of-the-art galvanically isolated probes/systems are consolidated in Table IV. Upon analyzing the results, it can be concluded that the developed PIE OD successfully satisfies the performance demands specified in Section II-B for advanced testing systems targeting next-generation WBG

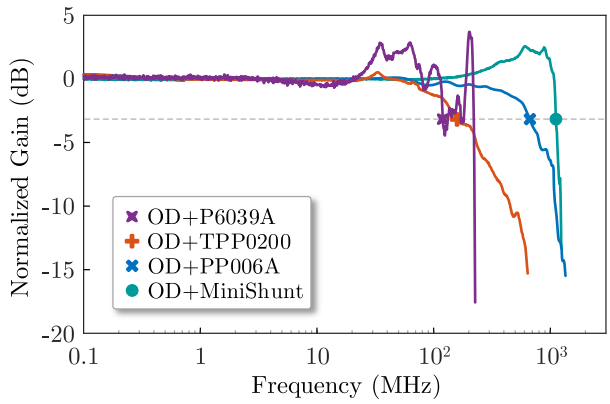

Fig. 21. Comparative analysis of measured normalized forward gain among nonisolated probes/systems extended with PIE OD.

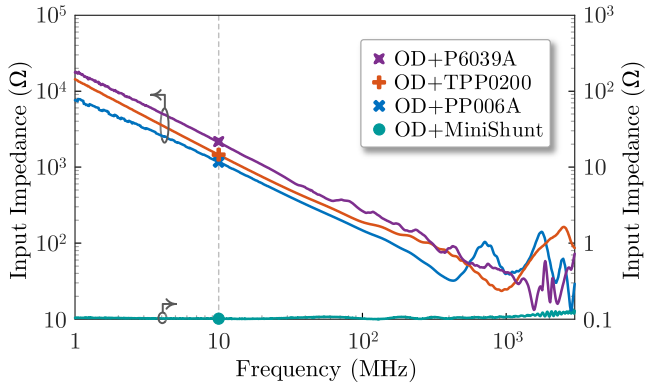

Fig. 22. Comparative analysis of measured input impedance among nonisolated probes/systems extended with PIE OD.

power devices, serving as a robust alternative solution to address the measurement concerns associated with next-generation WBG and even ultra-WBG applications.

D. Extended Performance of Commonly Used Nonisolated Probes/Systems With Optical Dock

To further confirm the effectiveness of the developed PIE OD in extending traditional nonisolated probes/systems, the OD was used to extend the MV single-ended attenuator P6039A, passive probe TPP0200 and PP006A, as well as current shunt MiniShunt [29], following the connection configuration shown in Fig. 15. Among these, the P6039A, TPP0200, and PP006A utilize a 1-MΩ input stage, while the MiniShunt employs a 50-Ω stage to maximize its bandwidth performance. The extended nonisolated probes were then evaluated and compared in terms of the forward gain characteristics, measurement bandwidth, and input impedance. The comparative results are provided in Figs. 21 and 22.

Upon analyzing Figs. 21 and 22, it is evident that the nonisolated probes/systems, following isolation extension through OD, have preserved their exceptional electrical attributes, such as high bandwidth and low parasitics, while also gaining the galvanic isolation and dv/dt immunity capabilities. These traits allow them to precisely capture and reproduce the ultrafast switching behaviors of the WBG power devices in challenging CM interference, i.e., v_{CM} and dv/dt, testing environments.

Among them, the "OD+P6039A" setup stands out with its remarkable features. It provides a dynamic testing range of ±39 kV, a measurement bandwidth of 120 MHz, and a complete galvanic isolation between the front and back stages. This configuration not only ensures high-level safety protection for the back-end, but also effectively mitigates CM grounding loop and eliminates potential zero-drift issues, contributing to the device design and characterization, advanced packaging and power module development, and industry applications of the next-generation MV SiC MOSFETs.

The performance parameters of the evaluated and compared nonisolated probes/systems, after being extended with the PIE OD, are summarized in Table V.

TABLE V
KEY PERFORMANCE PARAMETERS SUMMARY OF NONISOLATED PROBES/SYSTEMS EXTENDED WITH PROPOSED PIE OD

OD + ~	Target Signal	Dynamic Range	Bandwidth	Parasitics @10MHz
P6039A	v_{ds}	± 39 kV	0.12 GHz	7.5 pF
TPP0200	v_{ds}, v_{gs}	± 0.6 kV	0.16 GHz	11.3 pF
PP006A	v_{ds}, v_{gs}	± 0.6 kV	0.65 GHz	12.3 pF
MiniShunt	i_{d}	± 0.1 kA	1.10 GHz	~0 pH

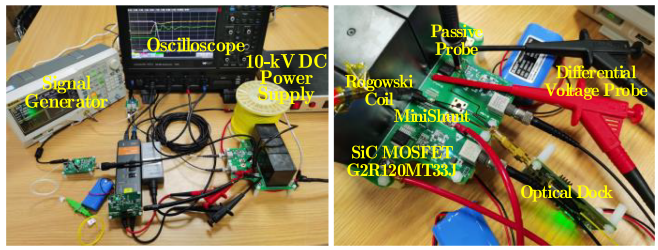

Fig. 23. Test setup for high-side DPT with SiC MOSFET G2R120MT33J.

V. TIME-DOMAIN COMPREHENSIVE VERIFICATION BASED ON HIGH-SIDE DOUBLE PULSE TEST WITH 3.3-KV SIC MOSFET

To thoroughly validate the flexibility, expandability, high bandwidth, galvanic isolation, and wideband CMRR performance, as well as dv/dt immunity of the proposed PIE OD, extensive comparisons with the state-of-the-art commercial galvanically isolated probe, Tektronix TIVP1, were conducted under the most challenging dynamic testing conditions, namely the high-side DPT with the MV SiC MOSFETs, in terms of the high-side gate-source voltage $v_{\mathrm{gs,HS}}$, high-side drain-source voltage $v_{\mathrm{ds,HS}}$, and high-side drain current $i_{\mathrm{d,HS}}$. The high-side DPT test setup, based on the principle and configuration illustrated in Fig. 2, is depicted in Fig. 23, where the Lecroy 715Zi (1.5 GHz, 20 GS/s) and GeneSiC Semiconductor SiC MOSFET G2R120MT33J (3.3 kV, 24 A) were utilized.

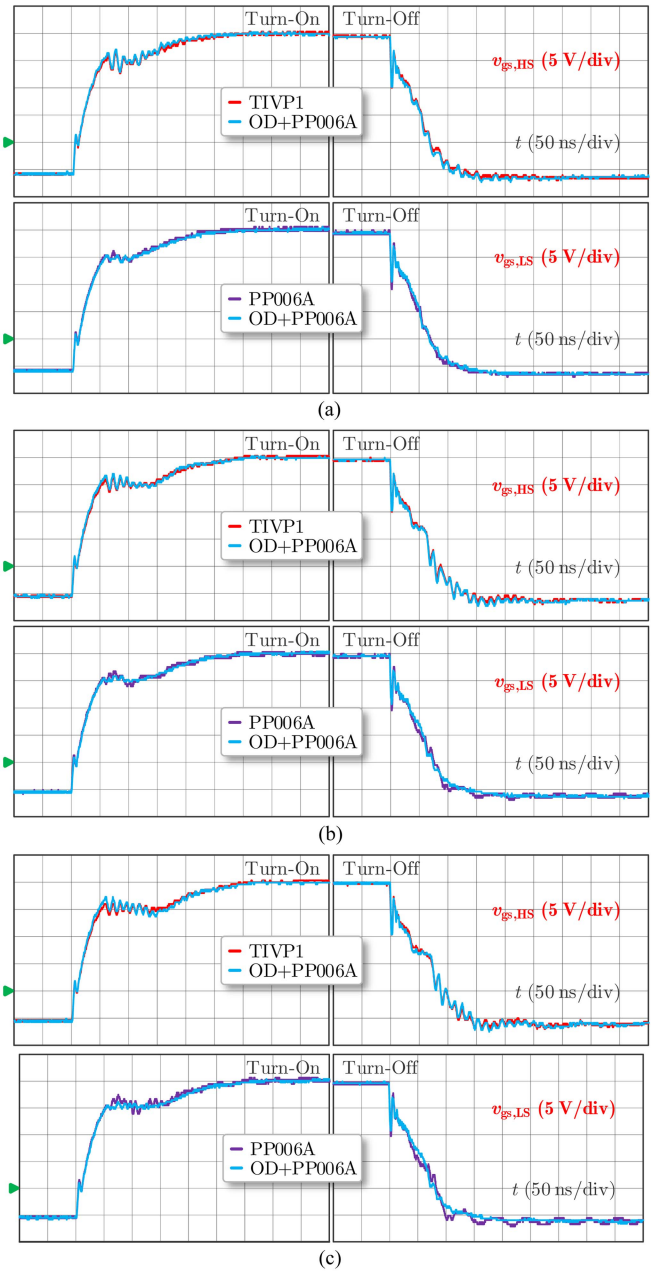

Fig. 24. High-side gate-source voltage $v_{\mathrm{gs,HS}}$ measured with TIVP1 and "OD + PP006A," as well as low-side gate-source voltage $v_{\mathrm{gs,LS}}$ measured with PP006A and "OD + PP006A" at $I_{\mathrm{d}} = 24$ A and (a) $V_{\mathrm{dc}} = 0.5$ kV, (b) $V_{\mathrm{dc}} = 1.5$ kV, and (c) $V_{\mathrm{dc}} = 2.5$ kV.

A. High-Side and Low-Side Gate-Source Voltage, $v_{gs,HS}$ and $v_{gs,LS}$

First, to validate the wideband CMRR of the developed OD in suppressing high-frequency CM noise dv/dt, the high-side gate-source voltage $v_{\mathrm{gs,HS}}$ were measured and compared between TIVP1 and "OD + PP006A," under a fixed I_{d} of 24 A and varying V_{dc} of 0.5, 1.5, and 2.5 kV. The results are presented in Fig. 24.

Thanks to the exceptional dv/dt immunity of TIVP1 and OD, reaching up to 7.0 kV/ns and 1.3 kV/ns, respectively, the impact of high-frequency CM noise dv/dt on the testing results can be effectively suppressed. Notably, the $v_{\mathrm{gs,HS}}$ waveforms obtained from both systems exhibit remarkable similarity, and as V_{dc} increases, the Miller plateau extends further. These measurement results serve as a strong basis for aspects, such as gaining deeper insights into the switching dynamics of high-side power devices, optimizing the design of high-side driving circuits, and developing ultrafast and robust protection designs.

In addition, to validate the galvanic isolation capabilities provided by OD to the nonisolated measurement system and suppress low-frequency CM noise v_{CM}, the low-side gate-source voltage $v_{\mathrm{gs,LS}}$ was also measured using the passive probe PP006A and compared between with and without the inclusion of OD, under a fixed I_{d} of 24 A and varying V_{dc} of 0.5, 1.5, and 2.5 kV. The results are depicted in Fig. 24.

When V_{dc} is relatively low, it can be observed that the $v_{\mathrm{gs,LS}}$ waveforms before and after adding OD are smooth and almost indistinguishable, indicating minimal CM issues associated with lower V_{dc} levels. However, as V_{dc} increases rapidly, the CM issues stemming from v_{CM} have a more pronounced impact on the backend. Without the inclusion of OD, the measured $v_{\mathrm{gs,LS}}$ waveforms exhibit noticeable low-frequency fluctuations, leading to a significant degradation of driving waveform quality. Conversely, the addition of OD results in remarkably smoother measured $v_{\mathrm{gs,LS}}$ waveforms, even when subjected to a 2.5-kV V_{dc}, showcasing a more realistic and reliable driving condition.

In conclusion, the inclusion of OD offers a straightforward and efficient solution to mitigate the adverse effects of the high- and low-frequency CM noise sources on the traditional nonisolated test systems. This achievement establishes a robust practical basis for precise characterization and comprehension of the dynamic properties of WBG devices, along with the optimization of their driving and protection circuit designs. As a result, PIE OD stands as an exceptionally appealing and remarkable solution targeting to the next-generation WBG measurements.

B. High-Side Drain-Source Voltage, $v_{ds,HS}$

To validate the proposed OD's flexibility and high scalability, the MV single-ended probe PPE6KV was extended with the OD to create the "OD + PPE6KV" configuration. This system offers a dynamic testing range of ±6.0 kV, a testing bandwidth of 400 MHz, and a complete galvanic isolation between the front and back stages, specifically designed to characterize the high-side drain-source voltage $v_{\mathrm{ds,HS}}$ of a 3.3-kV SiC MOSFET.

To thoroughly evaluate the system's performance, the $v_{\mathrm{ds,HS}}$ waveforms were measured using TIVP1, DP6700A, and "OD + PPE6KV," under a fixed I_{d} of 24 A and varying V_{dc} from 0.5 kV to 2.5 kV. The results are depicted in Fig. 25.

Based on the observation, all three testing systems meet the bandwidth requirements, leading to highly similar measured waveforms. It is worth noting that despite the DP6700A having a dv/dt immunity of only 13 V/ns, the influence of the high-frequency CM noise dv/dt on the system output becomes less significant due to the extensive dynamic range of the actual testing, reaching several kilovolts. Consequently, when characterizing $v_{\mathrm{ds,HS}}$, the measurement bandwidth becomes more critical than CMRR and dv/dt immunity in this context.

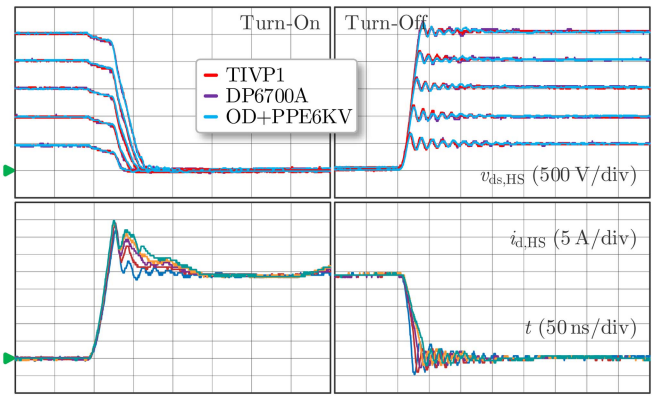

Fig. 25. High-side drain-source voltage $v_{ds,HS}$ measured with TIVP1, DP6700A, and "OD + PPE6KV" at $I_d = 24$ A and V_{dc} from 0.5 kV to 2.5 kV.

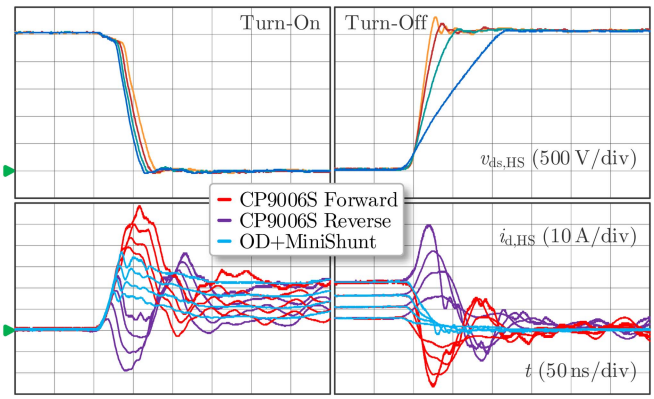

Fig. 26. High-side drain current $i_{d,HS}$ measured with "RC CP9006S in forward connection," "RC CP9006S in reverse connection," and "OD + MiniShunt" at $V_{dc} = 2.5$ kV and I_d from 5 A to 24 A.

C. High-Side Drain Current, $i_{d,HS}$

Compared to the Rogowski coil, the current shunt provides a much higher measurement bandwidth and better immunity to interference, making it a popular choice for the dynamic current characterization of WBG power devices. By extending the MiniShunt [29] with the OD, the inherent limitations of nonisolated measurements in traditional shunts can be addressed, allowing for a precise capture of the high-side drain current $i_{d,HS}$.

To comprehensively validate the system's performance, the $i_{d,HS}$ waveforms were compared between the "OD + MiniShunt," configuration and commercial RC CP9006 in both forward and reverse connections, under a fixed V_{dc} of 2.5 kV and four different I_d from 5 A to 24 A. The results are presented in Fig. 26. It is important to highlight that, the manual compensation for the accumulated zero-drift errors of the RC discussed in Section II-A was implemented to provide a more intuitive portrayal and comparison of the dv/dt impact on the RC CP9006.

The results clearly demonstrate that "OD + MiniShunt," with its extended galvanic isolation and CM rejection capabilities, successfully captures and reproduces the $i_{d,HS}$ characteristics. In contrast, the CP9006 is significantly affected by dv/dt, resulting in valid waveforms being nearly obscured by interference noise. Furthermore, when the connections are switched, the distortion in RC waveforms becomes reversed, and distortion oscillations exhibit a primarily symmetric distribution in comparison to the waveforms obtained by the "OD + MiniShunt". This suggests that combining the output waveforms obtained from the RC in both direction connections can partially mitigate the impact of dv/dt. Therefore, a potential approach to address the CM issues caused by dv/dt could be the utilization of a differential RC method.

In addition, taking into account the excellent characteristics of RC, such as floating measurements, ease of integration, and high current testing capability, it is commonly employed in the integrated overcurrent protection for MV SiC MOSFETs [15]. Nevertheless, given the insights gained from the results and discussion presented in this section, there is still an immediate need to conduct further research into advanced RC topologies and testing methodologies, aiming to achieve high-performance integrated current measurements and overcurrent protection schemes, prioritizing robust dv/dt immunity, for the upcoming generation of WBG power devices.

VI. Conclusion

Next-generation WBG semiconductor devices possess high blocking voltage capabilities reaching MV levels and exhibit fast switching speeds in the nanosecond range. Leveraging advanced packaging techniques, they can achieve exceptional dv/dt of up to 250 V/ns. To accurately capture and faithfully reproduce the rapid switching transients in the presence of intense CM interferences, there is an urgent demand for next-generation galvanically isolated testing systems that offer a minimum measurement bandwidth of 500 MHz, a CMRR of at least 50 dB at 100 MHz, and a dv/dt immunity of no less than 100 V/ns.

Given the successful performance of traditional nonisolated testing systems in meeting the requirements for dynamic range and measurement bandwidth, the PIE concept is introduced to address their inherent limitations associated with nonisolation. Expanding on the PIE concept, the OD is presented as a practical and high-performance implementation of PIE. By incorporating compensating capacitor C_c for OD-FE and feedback capacitor C_f for OD-BE, while also tuning and optimizing circuit parameters, the bandwidth performance of OD can be maximized within its design boundaries. These advancements have resulted in the development of a high-performance PIE OD. It features a flexible input load that can be switched between 50 Ω and 1 MΩ, outstanding galvanic isolation based on an optical link, an impressive bandwidth of 1.53 GHz, a high CMRR of 72 dB at 100 MHz, and a robust dv/dt immunity of 1.3 kV/ns. Therefore, this OD can effectively be used in combination with various nonisolated probes/systems, such as passive probes, medium-voltage single-ended attenuators, and current shunts, to meet the requirements of diverse testing scenarios that demand reliable galvanic isolation.

The contributions presented in this article successfully address the demanding requirements for dynamic testing in next-generation WBG semiconductor devices. Moreover, the proposed PIE concept goes beyond the OD and provides a

foundation for exploring advanced approaches to further extend isolation capabilities. Finally, this article serves as a valuable reference for guiding the design of future high-performance testing systems, analyzing CM interference in dynamic testing, and designing driving and protection circuits for WBG devices.

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