Dynamic Interleaving Strategy to Reduce DC-Link Ripple of Dual Three-Phase Permanent Magnet Synchronous Machine Drives by Using Discontinuous Space Vector Modulation

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***Abstract*—A dynamic interleaving method is proposed in this article to reduce the dc-link ripple for dual three-phase permanent synchronous machine drive systems. Existing literature covers the constant interleaving approach, where the interleaving angle is fixed, which is incapable of reducing the dc-link ripple significantly. During the overlapping condition of the dc-link currents of the two three-phase subsystems, the proposed method uses an interleaving angle of π while the rest of the time it is 0. As the proposed method is dynamically varying the interleaving angle, it is called the dynamic interleaving approach. All the dominant harmonics in the dc-link ripple are reduced through the proposed strategy, whereas the constant interleaving cannot reduce all the harmonics. The performance of the proposed strategy is compared to constant interleaving and noninterleaving approaches. Through the proposed method, the dc-link ripple is significantly reduced compared to other approaches, and thus, it improves the power density of the system. Simulation and experimental results are provided to validate the performance of the proposed strategy.**

***Index Terms*—DC-link ripple, dual three-phase, interleaving, permanent magnet synchronous machine (PMSM), pulsewidth modulation (PWM), space vector PWM (SVPWM).**

I. Introduction

MULTIPHASE permanent magnet synchronous machine (PMSM) drive systems are drawing attention in different industrial sectors due to their increased power and torque density, fault-tolerant characteristics, and high reliability [1], [2], [3]. The dual three-phase PMSM (DTP-PMSM) drive system is the most popular multiphase system where the neutrals of the two three-phase subsystems are isolated [4], [5], [6]. The conventional angular displacements between the two three-phase subsystems are 0, $\pi/3$, or $\pi/6$ [7]. DTP-PMSM system with $\pi/6$ angular displacement shows lower torque ripple, higher back electro-motive force constant, and lower magnetomotive force harmonic components compared to the other angular displacements [7]. However, the design and control of the DTP-PMSM system with $\pi/6$ angular displacement can be challenging because of the mutual coupling between the two three-phase subsystems [8], [9], [10].

Two control methods are explored extensively in the literature for the DTP-PMSM drive system. They are 1) the vector space decomposition (VSD) method and 2) the double *dq* synchronous reference frame-based control [11], [12]. Comparison between these two controllers is explored in the literature [13]. Although the VSD method shows better performance over the harmonic control of the phase current, conventional off-the-shelf three-phase pulsewidth modulation (PWM) strategies, e.g., space vector PWM (SVPWM) can be directly implemented in the double *dq* method. As a result, it will be easier to implement in industrial applications [13]. Conventionally, the DTP-PMSMs are driven by two three-phase voltage source inverters (VSI). This method requires a high number of switches for the inverter to reduce its power density. The PWM signals of the two inverter systems can be interleaved by applying a phase shifting between the PWMs. The phase shift angle between the PWM signals is called the interleaving angle. The interleaving strategy is explored in the literature to reduce the dc-link ripple and the dc-link capacitor requirement, improving the system's power density. The interleaving method is well-established for dc–dc converters to reduce the pulsating voltage and currents [14], [15]. An interleaving control for the three-level neutral point clamped dual three-phase drive system is proposed for the DTP-PMSM, where the equivalent sampling and control frequency are increased through the interleaving strategy [16]. An interleaved PWM carrier strategy is proposed for the multiphase-controlled integrated modular drives to simultaneously reduce the dc-link and the stator current ripple [17]. A constant interleaving angle is used for the DTP-PMSM system to reduce the dc-link capacitor current and the dc-link current ripple [18]. Selective torque harmonics are reduced through the interleaving approach for the DTP- PMSM system [19]. When the displacement angle of the two three-phase subsystems is 0, an optimum interleaving angle of π is found and for a displacement angle of $\pi/6$, an optimum interleaving angle is found at $\pi/2$ in [19]. A constant interleaving angle π is proposed to reduce the noise, vibration,

Received 25 December 2023; revised 29 March 2024, 12 June 2024, and 23 July 2024; accepted 16 August 2024. Date of publication 23 September 2024; date of current version 12 December 2024. This work was supported by the Power America Institute. Recommended for publication by Associate Editor D. G. Xu. *(Corresponding author: Yilmaz Sozer.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3456708.

Digital Object Identifier 10.1109/TPEL.2024.3456708

and dc-link current ripple for the DTP-PMSM system in [20], [21], and [22]. A constant $\pi/2$ interleaving angle is proposed for the DTP-PMSM system to improve the vibrational performance, reduce the dc-link current ripple, and reduce the high-frequency component in the phase currents and the torque ripple [23], [24], [25]. The optimal carrier phase shift angle is analyzed to reduce the harmonic iron loss for the DTP-PMSM system while considering different operating conditions [26]. All the literature explored above uses a constant interleaving angle, which cannot reduce the dc-link ripple of the DTP-PMSM drive system significantly as the two three-phase subsystems are displaced. A phase collaborative switching strategy is proposed for the flux-adjustable hybrid DTP-PMSM drive system to reduce the dc-link current ripple, and the performance is compared to the interleaving method in [27]. Although the proposed topology improves performance compared to the interleaving approach, it is very complex. The proposed dynamic interleaving method is taken as a baseline and modified the algorithm further to reduce the dc-link current ripple in [28]. Instead of applying dynamic interleaving for all modulation index values, the concept in [28] switches between the dynamic interleaving method and $\pi/2$ interleaving angle. For some of the PWM methods, the interleaving method is used as a function of the modulation index.

This article proposes a dynamic interleaving method for the DTP-PMSM drive system. Compared to the conventional constant interleaving strategy, the interleaving angle is not fixed in the proposed method. The proposed strategy is implemented for the double *dq* method, where the conventional three-phase SVPWM methods can be implemented. The proposed strategy applies to any discontinuous SVPWM (DPWM) method. In DPWM methods, the inverter switches' duty ratio becomes completely 1 or 0 to reduce the switching loss of the system. When the duty ratio of any two nearby phases becomes equal, inverter currents of the two three-phase subsystems overlap and increase the dc-link current ripple of the system. While the rest of the time, they do not overlap. As a result, during the overlapping condition, the interleaving angle is used as π, while the rest of the time, it is used as 0. As for the continuous PWM method (CPWM), the switches' duty ratio does not become completely 1 or 0, the proposed method is not applicable to the CPWM method.

The rest of the article is described as follows: in Section II, DTP-PMSM drive system and control method is described. Section III describes the conventional DPWM methods and inverter currents due to the DPWM methods. The proposed dynamic interleaving strategy is described in Section IV and the analysis of the inverter current of DTP-PMSM system for interleaving methods is presented in Section V. Simulation and experimental results are shown and described in Sections VI and VII, respectively. Finally, the conclusion is drawn in Section VIII.

II. DTP-PMSM Drive System

A DTP-PMSM system with its two parallel VSIs and the overall control topology is shown in Fig. 1. Two three-phase subsystems are displaced and the angle between them is $\pi/6$

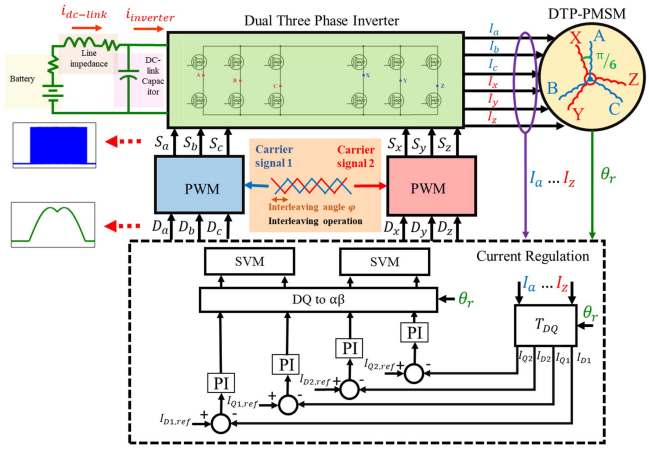

Fig. 1. DTP-PMSM system with two parallel interleaved voltage source inverters.

as shown in Fig. 1. For control purpose, six-phase currents are converted into double *dq* synchronous reference frame [12] using (1), (2) and (3) where I_a, I_b, I_c, I_x, I_y, and I_z are six phase currents, θ_r is the rotor position, I_{D1}, I_{Q1}, I_{D2}, and I_{Q2} are the synchronous reference frame currents. From the currents, voltage equations can be derived from the following (4)–(7) where V_{D1}, V_{Q1}, V_{D2}, and V_{Q2} are the stator voltages, R_s is the phase resistance, L_{D1}, L_{Q1}, L_{D2}, and L_{Q2} are the synchronous inductances, ω_r is the angular frequency and λ_{PM} is the permanent magnet flux linkage of the machine. As shown in (4)–(7), there is no coupling between two *dq* synchronous frames and as a result, it is called decoupled double *dq* synchronous control [12]. In the decoupled double *dq* synchronous reference frames, the first *dq* subspace reflects the torque component as given in (8), while the second subspace reflects the leakage components [8], [12]. Although there is a mutual coupling between the two three-phase subsystems, if the windings and the impedances are identical for both subsystems, there will be no coupling between two *dq* synchronous frames in this conversion, and as a result, it is called decoupled double *dq* synchronous control [8], [12]. As the asymmetric impedances of the two three-phase subsystems of the machine are outside the scope of this article, hence decoupled double *dq* synchronous control is considered here

$$\begin{bmatrix} I_{D1} \\ I_{Q1} \\ I_{D2} \\ I_{Q2} \end{bmatrix} = T_{DQ} \begin{bmatrix} I_a & I_b & I_c & I_x & I_y & I_z \end{bmatrix} \tag{1}$$

$$T_{DQ} = \frac{1}{\sqrt{3}} T_{rot} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2} & \frac{1}{2} & -1 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{1}{2} & 1 \\ -1 & \frac{1}{2} & \frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \end{bmatrix} \tag{2}$$

$$T_{rot} = \begin{bmatrix} \cos\theta_r & \sin\theta_r & 0 & 0 \\ -\sin\theta_r & \cos\theta_r & 0 & 0 \\ 0 & 0 & \cos\theta_r & \sin\theta_r \\ 0 & 0 & -\sin\theta_r & \cos\theta_r \end{bmatrix}. \tag{3}$$

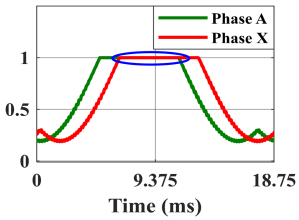

Fig. 2. Duty ratio of phase A and phase X for DPWMMax strategy.

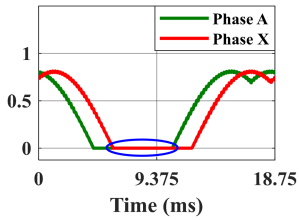

Fig. 3. Duty ratio of phase A and phase X for DPWMMin strategy.

In the closed-loop control, feedback and reference currents are fed to the proportional integral controller to generate the stator voltages. After that, voltages are converted to the static reference frame $\alpha\beta$ and conventional three-phase space vector modulations are generated, which is the duty ratio ($D_a \ldots D_z$) of the switches as shown in Fig. 1. Further, they are compared to the high-frequency triangular pulses to finally generate the SVPWM switching pulses ($S_a \ldots S_z$), as shown in Fig. 1. As the two three-phase subsystems use separate PWM pulses, a phase shift between the PWM pulses denoted as interleaving angle φ in Fig. 1, can eliminate the switching harmonics in dc-link ripple

$$V_{D1} = R_s I_{D1} + L_{D1}\frac{dI_{D1}}{dt} - \omega_r L_{Q1} I_{Q1} \tag{4}$$

$$V_{Q1} = R_s I_{Q1} + L_{Q1}\frac{dI_{Q1}}{dt} + \omega_r L_{D1} I_{D1} + \omega\sqrt{3}\lambda_{PM} \tag{5}$$

$$V_{D2} = R_s I_{D2} + L_{D2}\frac{dI_{D2}}{dt} - \omega_r L_{Q2} I_{Q2} \tag{6}$$

$$V_{Q2} = R_s I_{Q2} + L_{Q2}\frac{dI_{Q2}}{dt} + \omega_r L_{D2} I_{D2} \tag{7}$$

$$\tau_e = p\left(\sqrt{3}\lambda_{PM} I_{Q1} + (L_{D1} - L_{Q1})\, I_{D1} I_{Q1}\right). \tag{8}$$

III. DSVPWM Methods and Inverter Current

A. DSVPWM Methods

Conventional three-phase DPWM methods can be directly implemented for the DTP-PMSM systems. For the DPWM methods, switches are clamped either to the upper dc rail (duty ratio 1) or lower dc rail (duty ratio 0) for some time during the electrical cycle. As for these PWM methods, the switching action is not continuous. This is called the DSVPWM method [29]. They are popular for reducing the switching count, switching losses, and increasing the efficiency of the drive system [29]. In $2\pi/3$ DPWM methods, switches are continuously clamped to the upper dc rail (DPWMMax) or lower dc rail (DPWMMin) for one-third of the electrical cycle, as shown in Figs. 2 and 3. For the in-phase $\pi/3$ DPWM method (DPWM1), switches are locked alternatively to the upper and lower dc rails, as shown in Fig. 4, for consecutive one-third of the electrical cycle. For the DPWM1 method, switches are unmodulated during the fundamental reference voltage's positive or negative peaks, and the line-to-line switch voltages are symmetrical compared to the DPWMMax and the DPWMMin method [29]. For $\pi/6$ lagging $\pi/3$ DPWM method (DPWM2), unmodulated periods are $\pi/6$ delayed by the positive or negative peaks of the reference voltage, as shown in Fig. 5. For the $\pi/6$ leading $\pi/3$ DPWM method (DPWM3), unmodulated periods are $\pi/6$ leading as shown in Fig. 6. For these $\pi/3$ DPWM methods, the switches' thermal stress is more balanced than the $2\pi/3$ DPWM methods [29]. Another DPWM method is $\pi/6$ DPWM method (DPWM4), where switches are clamped to the upper or lower dc rail in every $\pi/3$ segment, as shown in Fig. 7. The duty ratio of phase A and phase X become

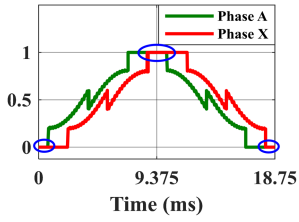

Fig. 4. Duty ratio of phase A and phase X for DPWM1 strategy.

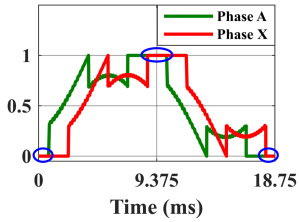

Fig. 5. Duty ratio of phase A and phase X for DPWM2 strategy.

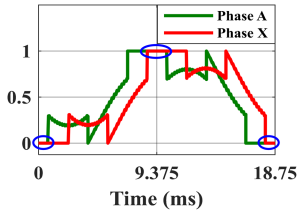

Fig. 6. Duty ratio of phase A and phase X for DPWM3 strategy.

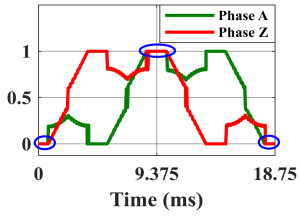

Fig. 7. Duty ratio of phase A and phase Z for DPWM4 strategy.

TABLE I
DUTY RATIO AND PHASE CURRENTS OF THE PHASE A, B, C

	Phase A	*Phase B*	*Phase C*
Duty ratio ($-\pi/6 < \theta_r < \pi/6$)	1	$1 - Mcos(\theta_r + \frac{\pi}{6})$	$1 + Mcos(\theta_r + \frac{5\pi}{6})$
Phase current	$Icos\theta_r$	$Icos(\theta_r - \frac{2\pi}{3})$	$Icos(\theta_r + \frac{2\pi}{3})$

TABLE II
DUTY RATIO AND PHASE CURRENTS OF THE PHASE X, Y, Z

	Phase X	*Phase Y*	*Phase Z*
Duty ratio ($-\pi/6 < \theta_r < 0$)	$Mcos(\theta_r)$	0	$-Msin(\theta_r - \frac{\pi}{6})$
Duty ratio ($0 < \theta_r < \pi/6$)	1	$1 - Mcos(\theta_r)$	$1 + Mcos(\theta_r + \frac{2\pi}{3})$
Phase current	$Icos(\theta_r - \frac{\pi}{6})$	$Icos(\theta_r - \frac{5\pi}{6})$	$Icos(\theta_r + \frac{\pi}{2})$

equal and overlap for some of the DPWM methods as shown in Figs. 2–6. However, for the DPWM4 method, the duty ratio of phase A and phase Z becomes equal and overlap. As a result, overlapping and nonoverlapping conditions will be created due to the nature of the DPWM methods.

B. Inverter Current Due to DPWM Methods

As explained in the previous section, the duty ratios of the phases overlap each other for the DPWM methods. During these overlapping conditions, inverter currents of the two three-phase subsystems overlap, and the rest of the time, they do not overlap. To explain the overlapping and nonoverlapping scenario, the DPWM1 method is chosen. The duty ratio and the phase currents of phases A, B, and C are shown in Table I for a range of rotor positions, θ_r [29], where M is the modulation index, and I is the peak of the phase current. The equations are taken from [29], which can be directly implemented for the DTP-PMSM system. Similarly, the duty ratio and the phase currents of the phases X, Y, and Z can be derived as shown in Table II for the same range of rotor position, θ_r [29]. As shown in Tables I and II, during certain rotor positions ($-\pi/6 < \theta_r < 0$), there is no overlap of duty ratio between the phases; however, for some other rotor positions ($0 < \theta_r < \pi/6$) there is an overlap of duty ratio between Phase A and Phase X. If a rotor position is chosen for no overlapping condition, e.g., $\theta_r = -\pi/12$, duty ratio, and the leg current of the inverter system for each phase can be derived from Tables I and II for $M = 0.25$. The duty ratio and the leg currents of different phases for $\theta_r = -\pi/12$ are given in Table III. The inverter currents are the summation of the multiplication of the duty ratio and the leg currents. The leg currents are derived by multiplying the phase current and the duty ratio. A graphical representation of the inverter currents of the two inverters and the total system is shown in Fig. 8 for $\theta_r = -\pi/12$. As shown in Fig. 8(c), the total inverter currents of the inverter system are reduced because of the nonoverlapping nature of the currents

TABLE III
DUTY RATIO AND LEG CURRENTS OF THE INVERTER FOR $M = 0.25$

	θ_r = -π/12		θ_r = π/12	
	Duty Ratio	Leg Currents	Duty Ratio	Leg Currents
Phase A	1	0.966I	1	0.966I
Phase B	0.758	-0.707I	0.823	-0.258I
Phase C	0.823	-0.258I	0.758	-0.707I
Phase X	0.241	0.707I	1	0.966I
Phase Y	0	-0.966I	0.758	-0.707I
Phase Z	0.176	0.258I	0.823	-0.258I

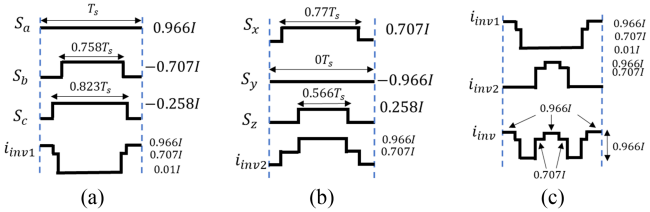

Fig. 8. For $M = 0.25$ and $\theta_r = -\frac{\pi}{12}$. (a) switching sequences and the DC-link currents of the phase A, B, C. (b) Switching sequences and the inverter currents of the phase X, Y, Z. (c) Total inverter currents of the inverter.

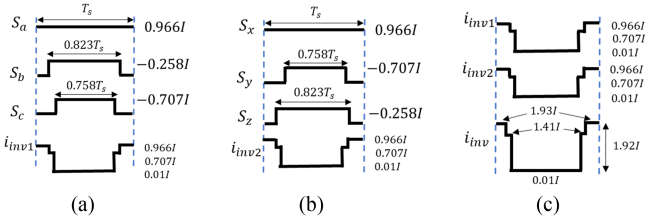

Fig. 9. For $M = 0.25$ and $\theta_r = \frac{\pi}{12}$. (a) Switching sequences and the DC-link currents of the phase A, B, C. (b) Switching sequences and the inverter currents of the phase X, Y, Z. (c) Total inverter currents of the inverter.

of the two three-phase subsystems. Similarly, the duty ratio and the leg currents of different phases for $\theta_r = \pi/12$, which is an overlapping region, are given in Table III for $M = 0.25$. This validates low inverter currents during the overlapping region.

A graphical representation of the inverter currents of the two inverters and the total system is shown in Fig. 9 for $\theta_r = \pi/12$. As shown in Fig. 9, the inverter currents of the two inverters completely overlap, and the total inverter current is two times higher than the nonoverlapping condition. This validates the high inverter currents due to the nonoverlapping nature. Similarly, this can apply to any other rotor position and current value. Inverter currents of the two individual three-phase inverters and the total inverter currents of the drive system from MATLAB-Simulink simulations are shown consecutively in Figs. 10 and 11 to validate the graphical analysis described above. In this simulation, the DPWM1 method and $M = 0.25$ is considered. The dc-link currents of the two inverters overlap each other, and the total dc-link current of the drive increases due to the reasons described earlier. Duty ratio and the leg currents for the inverter for a higher value of $M = 0.85$ are given in Table IV for both overlapping and nonoverlapping conditions. Graphical representation of the inverter currents for

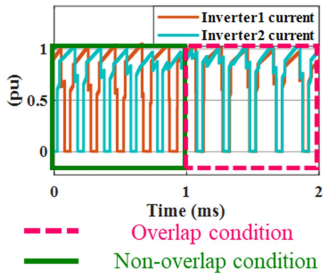

Fig. 10. Inverter currents of the individual two three-phase inverters.

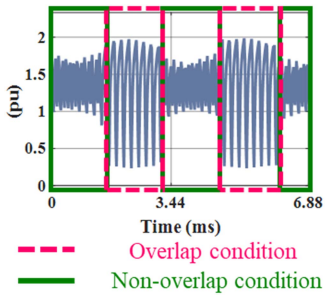

Fig. 11. DC-link current of the DTP-PMSM drive system.

TABLE IV
DUTY RATIO AND LEG CURRENTS OF THE INVERTER FOR $M = 0.85$

	θ_r = -π/12		θ_r = π/12	
	Duty Ratio	Leg Currents	Duty Ratio	Leg Currents
Phase A	1	0.966I	1	0.966I
Phase B	0.179	−0.707I	0.399	−0.258I
Phase C	0.399	−0.258I	0.179	−0.707I
Phase X	0.821	0.707I	1	0.966I
Phase Y	0	−0.966I	0.179	−0.707I
Phase Z	0.601	0.258I	0.399	−0.258I

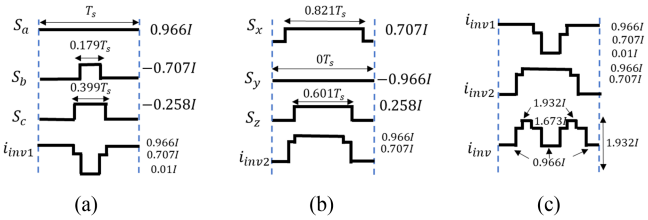

Fig. 12. For $M = 0.85$ and $\theta_r = -\frac{\pi}{12}$. (a) Switching sequences and the DC-link currents of the phase A, B, C. (b) Switching sequences and the inverter currents of the phase X, Y, Z. (c) Total inverter currents of the inverter.

the nonoverlapping condition ($\theta_r = -\pi/12$) of the inverters are shown in Fig. 12, where the inverter currents have changed compared to Fig. 8, and the inverter currents overlap each other, although it is a nonoverlapping condition. For the higher value of M (>0.8), the duration of the zero-voltage vector is small, which makes it difficult to place the inverter current completely out of phase [26]. As a result, the impact of the interleaving approach will be reduced, and the dc-link current will not be reduced significantly. A graphical representation of the inverter currents

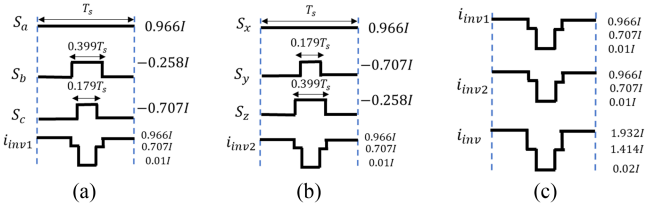

Fig. 13. For $M = 0.85$ and $\theta_r = \frac{\pi}{12}$. (a) Switching sequences and the DC-link currents of the phase A, B, C. (b) Switching sequences and the inverter currents of the phase X, Y, Z. (c) Total inverter currents of the inverter.

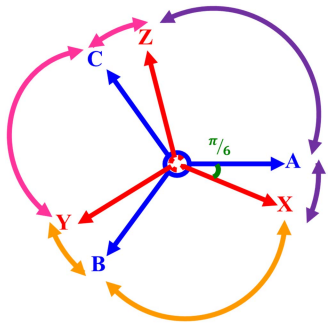

Fig. 14. Phase sequence diagram of DTP-PMSM system.

for the overlapping condition is shown in Fig. 13, where the inverter currents overlap. As a result, for both overlapping and nonoverlapping conditions for higher M value, inverter currents will overlap. As a result, the impact of the interleaving method will be much less for the higher modulation index (M) values.

IV. DYNAMIC INTERLEAVING STRATEGY

The phase sequence of the DTP-PMSM system is shown in Fig. 14 where any phase has two nearby phases. For the DPWM methods, the duty ratio of any phase becomes equal and overlaps with its nearby phases. The proposed method uses an interleaving angle of π during the overlapping regions, while the rest of the time, it is kept at 0. As shown in Fig. 14, the nearby phases of Phase A are Phase X and Phase Z. Similarly, the nearby phases of Phase B are Phase Y and Phase X, nearby phases of Phase C are Phase Z and Phase Y. As a result, overlapping moments can happen for any following conditions (Phase A, Phase X), (Phase A, Phase Z), (Phase B, Phase Y), (Phase B, Phase X), (Phase C, Phase Z), (Phase C, Phase Y) depending on the DPWM methods. During any conditions, individual three-phase inverter currents and hence the dc-link current overlap each other while the rest of the time, they do not overlap, as shown in Figs. 10 and 11 and explained in the previous section. The proposed method determines the interleaving angles of π or 0 depending on the overlapping and nonoverlapping conditions. As the proposed method uses a varying interleaving angle, it is called the dynamic interleaving method. The flow chart of the proposed method is shown in Fig. 15. As shown in Fig. 15, whenever there is a duty ratio overlap between the nearby phases, as explained in Tables I and II, the gate pulses are interleaved and when there is no overlapping between the nearby phases the gate pulses are

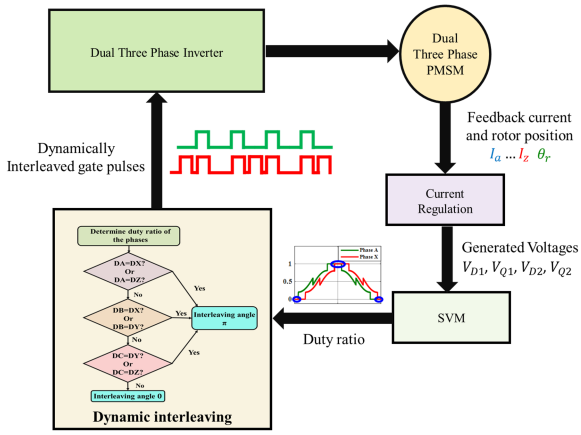

Fig. 15. Flow chart of the proposed dynamic interleaving method.

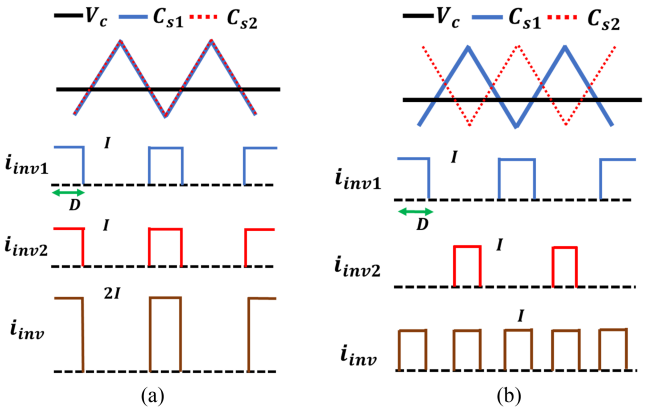

Fig. 16. Generic representations of the inverter currents due to same duty ratio. (a) 0 phase shift between the carrier signal. (b) π phase shift between the carrier signal.

not interleaved. Generic representations of the inverter currents due to the same duty ratio in the phases are shown in Fig. 16(a) where V_c is the commanded signal, C_{s1} and C_{s2} are the carrier signals [28]. The total inverter current i_{inv} is increased due to the overlapping nature of the duty ratio and the inverter currents i_{inv1} and i_{inv2}. However, with a similar duty ratio, if the phase shift between the carrier signal is π, the overall inverter currents will be less as the individual inverter currents are phase-shifted as shown in Fig. 16(b). As a result, during the same duty ratio, an interleaving angle of π is required to reduce the inverter current and, hence, the dc-link current of the drive.

V. Analysis of Inverter Current for Interleaving Methods

Two VSI share the same dc-bus to drive the DTP-PMSM system, as shown in Fig. 17. The total inverter current is the sum of the two inverter currents, as shown in Fig. 17. Inverter currents can be expressed as in (9) and (10), where $i_{\text{sw}A}$, $i_{\text{sw}B}$, and $i_{\text{sw}C}$ are the upper switches' current, i_A, i_B, and i_C are the phase currents, and S_{Au}, S_{Bu}, and S_{Cu} are the control signals of the upper switches. Similarly, the second inverter current can be

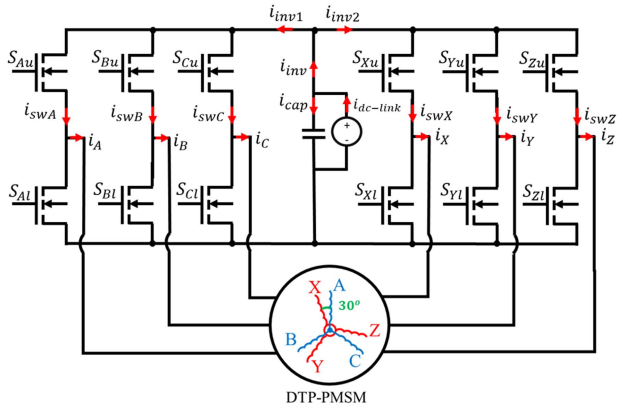

Fig. 17. Two parallel voltage source inverters for the DTP-PMSM system.

expressed as in (11) and (12)

$$i_{\text{inv1}} = i_{\text{sw}A} + i_{\text{sw}B} + i_{\text{sw}C} \tag{9}$$

$$i_{\text{sw}A} = S_{Au} \cdot i_A$$

$$i_{\text{sw}B} = S_{Bu} \cdot i_B$$

$$i_{\text{sw}C} = S_{Cu} \cdot i_C \tag{10}$$

$$i_{\text{inv2}} = i_{\text{sw}X} + i_{\text{sw}Y} + i_{\text{sw}Z} \tag{11}$$

$$i_{\text{sw}X} = S_{Xu} \cdot i_X$$

$$i_{\text{sw}Y} = S_{Yu} \cdot i_Y$$

$$i_{\text{sw}Z} = S_{Zu} \cdot i_Z. \tag{12}$$

The control signal S_{Au} can be expressed as in (13), and the phase current i_A as in (14) considering the sinusoidal phase current flowing through the machine

$$S_{Au} = A_m e^{j(m\omega_c t + n\omega_r t)} \tag{13}$$

$$i_A = I e^{j\omega_r t} \tag{14}$$

where A_m is a harmonic component of the control signal, ω_c is the angular carrier frequency, ω_r is the electrical angular frequency of the rotor, m is the harmonic order of the switching frequency, n is the harmonic order of the electrical angular frequency of the rotor, I is the peak of the phase current. Similarly, the control signal of Phase B and Phase C will be the time-shifted version of Phase A and can be written as

$$S_{bu} = A_m e^{j\left(m\omega_c t + n\left(\omega_r t - \frac{2\pi}{3}\right)\right)} \tag{15}$$

$$i_B = I e^{j\left(\omega_r t - \frac{2\pi}{3}\right)} \tag{16}$$

$$S_{cu} = A_m e^{j\left(m\omega_c t + n\left(\omega_r t + \frac{2\pi}{3}\right)\right)} \tag{17}$$

$$i_C = I e^{j\left(\omega_r t + \frac{2\pi}{3}\right)}. \tag{18}$$

In order to obtain the inverter currents, (9) and (11) need to be used. To get the first inverter current i_{inv1}, (13)–(18) need to be placed in (9) and (19) can be derived from there. All the phase currents and switching currents, as stated in (13)–(18) can be phase-shifted by $\frac{\pi}{6}$ to derive the phase current and the switching

TABLE V
HARMONIC CANCELLATION FOR CONSTANT INTERLEAVING ANGLE

$m = 1, n = -2, \varphi = \frac{\pi}{2}, \theta_{ps} = \pi$	Harmonics cancelled
$m = 1, n = 2, \varphi = \frac{\pi}{2}, \theta_{ps} = 0$	Harmonics not cancelled

TABLE VI
HARMONIC CANCELLATION FOR PROPOSED METHOD

$m = 1, n = \pm 2, \varphi = 0, \theta_{ps} = \pi$ Overlapping region	Harmonics cancelled
$m = 1, n = \pm 2, \varphi = \pi, \theta_{ps} = \pi$ Non-Overlap region	Harmonics cancelled

function for the second inverter. To derive the second inverter current, i_{inv2} phase current and the switching function need to be placed in (11) and (20) can be derived from there, where $\alpha = \frac{\pi}{6}$, the displacement angle between the two three phases

$$\begin{aligned} i_{\text{inv1}} &= A_m e^{j(m\omega_c t + n\omega_r t)}.Ie^{j\omega_r t} \\ &\quad + A_m e^{j\left(m\omega_c t + n\left(\omega_r t - \frac{2\pi}{3}\right)\right)}.Ie^{j\left(\omega_r t - \frac{2\pi}{3}\right)} \\ &\quad + A_m e^{j\left(m\omega_c t + n\left(\omega_r t + \frac{2\pi}{3}\right)\right)}\, Ie^{j\left(\omega_r t + \frac{2\pi}{3}\right)} \\ &= \left(A_m I + A_m.Ie^{-j(n+1)\frac{2\pi}{3}}\right. \\ &\quad \left. + A_m.Ie^{j(n+1)\frac{2\pi}{3}}\right) e^{j(m\omega_c t + (n+1)\omega_r t)} \end{aligned} \tag{19}$$

$$\begin{aligned} i_{\text{inv2}} &= A_m e^{j(m(\omega_c t + \varphi) + n(\omega_r t - \alpha))}.Ie^{j(\omega_r t - \alpha)} \\ &\quad + A_m e^{j\left(m(\omega_c t + \varphi) + n(\omega_r t - \alpha - \frac{2\pi}{3})\right)}.Ie^{j(\omega_r t - \alpha - \frac{2\pi}{3})} \\ &\quad + A_m e^{j\left(m(\omega_c t + \varphi) + n(\omega_r t - \alpha + \frac{2\pi}{3})\right)}.Ie^{j(\omega_r t - \alpha + \frac{2\pi}{3})} \\ &= \left(A_m I + A_m.Ie^{-j(n+1)\frac{2\pi}{3}} + A_m.Ie^{j(n+1)\frac{2\pi}{3}}\right) \\ &\quad \times e^{j(m(\omega_c t + \varphi) + (n+1)(\omega_r t - \alpha))}. \end{aligned} \tag{20}$$

Total phase shift θ_{ps} between the two inverter currents can be expressed as in (21), deriving from (19) and (20). Similarly, for the negative values of n, phase shift angle θ_{ps} can be derived as in (22). To cancel the harmonics, θ_{ps} should be π. For a specific DPWM method, values of m and n are fixed. The only variable in (21) and (22) is φ to cancel a harmonic. For a constant interleaving angle $\varphi = \frac{\pi}{2}$, it is impossible to cancel all the harmonics, as shown in Table V.

However, during the overlapping region, both inverter currents overlap each other, and the value of α is 0. At that time, to cancel the $m = 1$, $n = \pm 2$ harmonic, value of φ should be π to make the θ_{ps} value as π. And for the nonoverlap region, the value of α is π, to cancel the $m = 1$, $n = \pm 2$ harmonic, value of φ should be 0 to make the θ_{ps} value as π. The summary of the harmonic's cancellation for the proposed method is given in Table VI. As a result, the proposed method can cancel all the harmonics while the constant interleaving method can not

$$\theta_{\text{ps}} = m\varphi - (n+1)\,\alpha \tag{21}$$

$$\theta_{\text{ps}} = m\varphi - (n-1)\,\alpha. \tag{22}$$

TABLE VII
KEY PARAMETERS

Name	*Value*
Pole pair	4
D_1-axis inductance	1 pu
Q_1-axis inductance	1.8 pu
D_2-axis inductance	0.15 pu
Q_2-axis inductance	0.18 pu
Phase resistance	12.5 mΩ
No-load flux linkage	0.061 Wb
Rated speed	4500 rpm
Rated torque	445 Nm
DC-link capacitor	2400 μF
Switching frequency	10 kHz

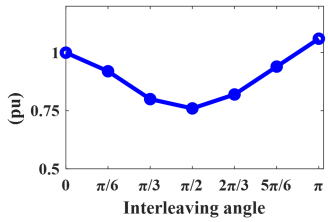

Fig. 18. Impact of different interleaving angle on DC-link current ripple for DPWM1 method.

The required amount of dc-link capacitor and the capacitor current can be written as [30]

$$C \geq \frac{5.5424\, I_{\text{cap}}}{21\, f_c\, \Delta V_{\text{pp}}} \tag{23}$$

where I_{cap} is the rated continuous current of the dc capacitor, ΔV_{pp} is the peak-to-peak voltage ripple. If everything else in (23) is considered constant, then the required amount of the dc-link capacitor is directly proportional to the capacitor current. With the reduced amount of the dc-link ripple, the capacitor current also reduces, which should reduce the amount of the dc-link capacitor. The maximum dc-link capacitance value entirely depends on the battery chemistry, the quality of the dc-link capacitors, and the application. However, in general, if the dc-link current ripple and the capacitor rms current are reduced, the amount of dc-link capacitors should be reduced.

VI. SIMULATION RESULTS

MATLAB/Simulink simulation is performed to validate the proposed method's performance. The key parameters of the system are shown in Table VII. For comparison purposes, without interleaving and constant interleaving approaches are also simulated. The impact of different constant interleaving angles for the DPWM1 method on dc-link current ripple is shown in Fig. 18. As the minimum dc-link current ripple is found for the interleaving angle of $\pi/2$, it is considered a constant interleaving strategy for comparison purposes. A comparison of dc-link current ripple for different interleaving methods is shown in Fig. 19 for 800 r/min 70 N·m torque. The dc-link current ripple

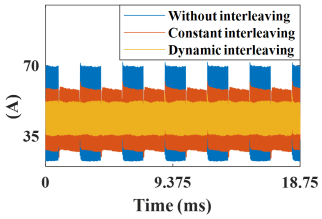

Fig. 19. Impact of different interleaving method on DC-link current ripple at 800 r/min 70 N·m torque.

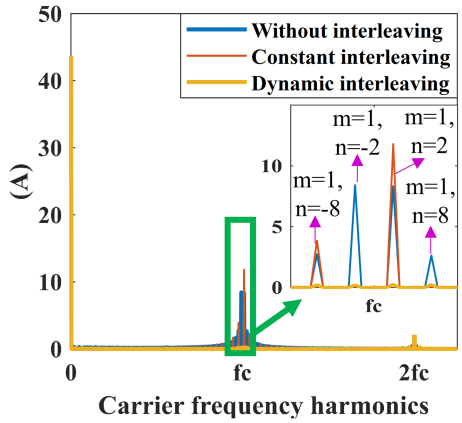

Fig. 20. FFT of the DC-link current ripple for different interleaving method at 800 r/min 70 N·m torque.

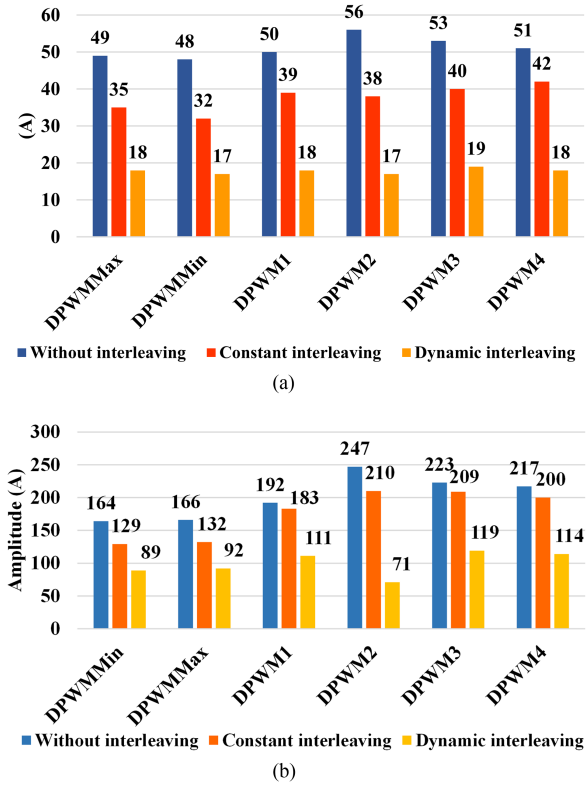

Fig. 21. Impacts of different interleaving method on DPWM methods for different operating conditions. (a) 800 r/min 70 N·m torque. (b) 4500 r/min 445 N·m torque.

is reduced significantly for the proposed strategy compared to the without interleaving and the constant interleaving strategies, as shown in Fig. 19. Moreover, the zoomed FFT of the dc-link current ripple is demonstrated in Fig. 20, where f_c is the carrier frequency. As shown in Fig. 20, all the harmonics of the dc-link current ripple are reduced through the proposed strategy, and some of the harmonics are reduced for the constant interleaving strategy, as discussed earlier. The impact of different interleaving methods on every DPWM method at 800 r/min 70 N·m torque and 4500 r/min 445 N·m torque are shown in Fig. 21. The dc-link current ripple is reduced significantly through the proposed strategy compared to the without interleaving and the constant interleaving strategies for every DPWM method and for both rated and underrated operating conditions. Impacts of the modulation index (M) on the performance of the different interleaving methods at 800 r/min 70 N·m torque is shown in Fig. 22, where the value of M is controlled by changing the dc bus voltage value. As shown in Fig. 22, the dc-link ripple is reduced significantly for the proposed strategy for a wide range of values of M. For higher M values, the impact of interleaving strategies is similar compared to the without interleaving method as described earlier. According to [30], the worst-case scenario of the dc-link current stress and the dc-link voltage stress appears when the M is between 0.55 and 0.65 which aligns with the simulation results. However, with the proposed method, the dc-link ripple is reducing more than 60% compared to the without interleaving strategy during this region. That means the proposed method works better during

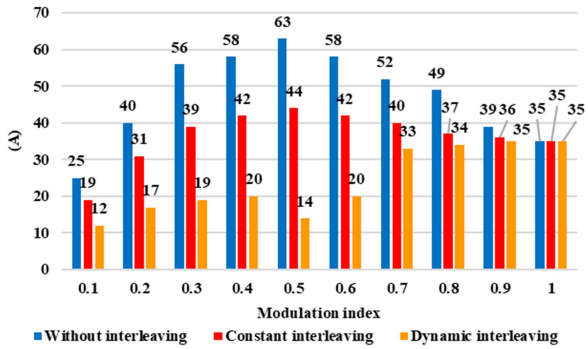

Fig. 22. Impacts of the modulation index on the performance of the interleaving methods for DPWM1 method at 800 r/min 70 N·m torque.

the maximum stress condition of the dc-link capacitor condition which relieves the stress from the capacitor and improves the longevity of the capacitances. From Fig. 22, it can be observed the maximum dc-link current ripple is 35 A for the dynamic interleaving strategy while for the without interleaving strategy it is 63 A, and the constant interleaving strategy it is 44 A. If 35 A is assumed to be the maximum allowed dc-link current ripple, then the without interleaving strategy would require 44% and the constant interleaving strategy would require 20% more dc-link capacitances compared to the dynamic interleaving strategy.

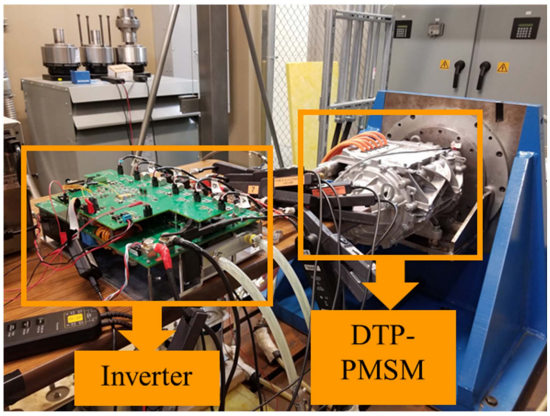

Fig. 23. Experimental setup of the DTP-PMSM drive system.

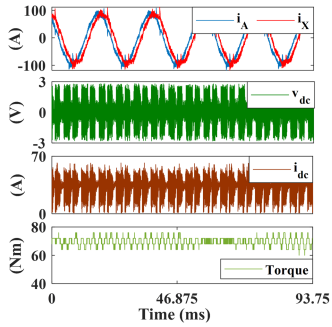

Fig. 24. Without interleaving method at 800 r/min 70 N·m for DPWM1 method ($M = 0.25$).

VII. Experimental Results

The experimental setup of the DTP-PMSM drive system is shown in Fig. 23. The control methods are implemented in the TMS320F28377D digital signal processor. Experimental analysis is performed under several operating conditions to validate the performance of the proposed method and compared to the without interleaving and constant interleaving methods. For the dc bus voltage measurement, a Tektronix THDP0200 is used. For the dc-link current and the phase current measurement, a Tektronix A622 is used. For speed measurement, high-resolution high-speed optical encoders are used by the dyno. Phase currents, dc-link voltage, dc-link current, and the output torque for without interleaving, constant interleaving, and dynamic interleaving are consecutively shown in Figs. 24 –26 at 800 r/min 70 N·m for the DPWM1 method and low modulation index ($M = 0.25$). As a torque measuring device, HBM T40 is used during the experimentation, and the bandwidth of this sensor is low, which does not allow measuring high-frequency ripple in the output torque. For all experimental results, dc-link voltages are shown in the ac coupling mode of the oscilloscope to focus on the ripple on the dc-link voltage. As a result, the average of the dc-link voltage is zero. As shown in the figures, both the dc-link current and the dc-link voltages are reduced for the proposed method compared to the without interleaving and constant interleaving methods. However, the total harmonic

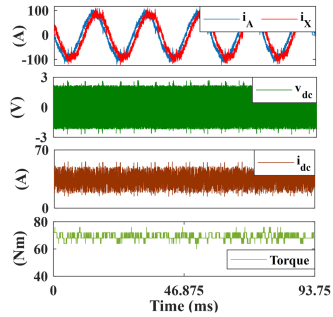

Fig. 25. Constant interleaving method at 800 r/min 70 N·m for DPWM1 method ($M = 0.25$).

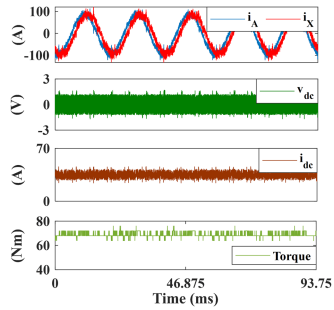

Fig. 26. Dynamic interleaving method at 800 r/min 70 N·m for DPWM1 method ($M = 0.25$).

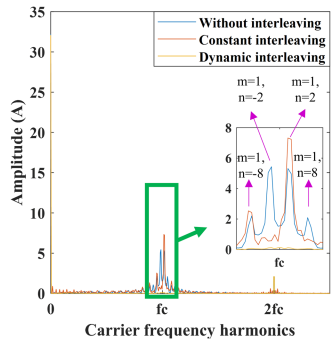

Fig. 27. FFT comparison of the DC-link currents for DPWM1 method and different interleaving strategies.

distortion (THD) of the phase currents is increased because of the interleaving methods, as there is a strong mutual coupling between the two three-phase subsystems. This phenomenon is well explained in the literature [24], [25], and [26] and is valid for both the constant interleaving and dynamic interleaving strategy. FFT comparison of the dc-link current ripple for different interleaving methods is shown in Fig. 27, where some of the carrier frequency harmonics are canceled through the constant interleaving strategy. In contrast, all the harmonics are canceled through the dynamic interleaving strategy. This validates the mathematical analysis and the simulation results of the proposed strategy. The same operating condition for the DPWMMax method and low modulation index ($M = 0.25$) for without interleaving, constant interleaving, and dynamic interleaving

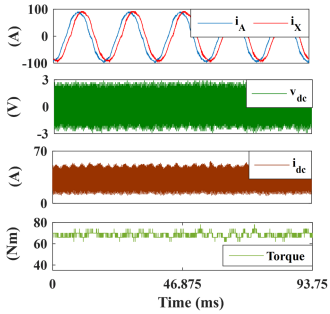

Fig. 28. Without interleaving method at 800 r/min 70 N·m for DPWMMax method ($M = 0.25$).

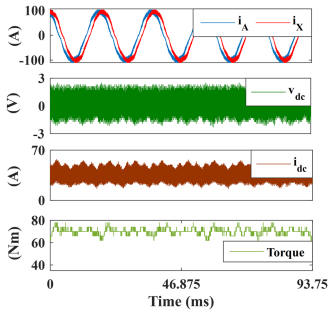

Fig. 29. Constant interleaving method at 800 r/min 70 N·m for DPWMMax method ($M = 0.25$).

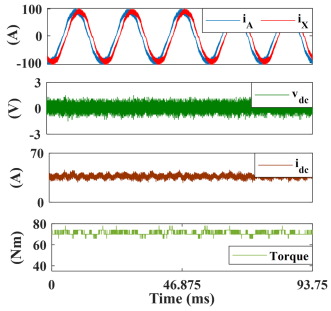

Fig. 30. Dynamic interleaving method at 800 r/min 70 N·m for DPWMMax method ($M = 0.25$).

TABLE VIII
COMPARISON OF THD VALUES OF THE PHASE CURRENT

	Without interleaving	*Constant interleaving*	*Dynamic interleaving*
DPWM1	5.22%	7.47%	8.07%
DPWMMax	9.43%	11.99%	13.19%

strategies are shown in Figs. 28 –30; the dc-link voltage and current ripples are reduced for the dynamic interleaving method. FFT comparison of the dc-link current ripple for the DPWMMax method and different interleaving strategies is shown in Fig. 31. Similar to the previous strategy, the carrier frequency harmonics are completely canceled through the proposed method, while for the constant interleaving method it is partially canceled. Table VIII compares the phase current THD values due to different interleaving strategies for DPWM1 and DPWMMax methods. The THD of the phase current is increased due to

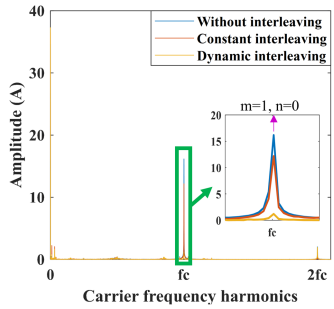

Fig. 31. FFT comparison of the DC-link currents for DPWMMax method and different interleaving strategies.

TABLE IX
COMPARISON OF DC-LINK CURRENT RIPPLE DIFFERENT INTERLEAVING STRATEGIES FOR DPWM METHODS AT 800 R/MIN 70 N·M

Modulation index	*DPWM methods*	*Interleaving strategies*		
		Without interleaving	Constant interleaving	Dynamic interleaving
$M = 0.25$	DPWMMax	47	37	17
	DPWMMin	46	40	13
	DPWM1	61	51	32
	DPWM2	60	50	33
	DPWM3	62	49	31
	DPWM4	61	50	32
$M = 0.5$	DPWMMax	73	52	21
	DPWMMin	72	49	22
	DPWM1	81	65	31
	DPWM2	84	70	28
	DPWM3	86	66	31
	DPWM4	84	67	29
$M = 0.8$	DPWMMax	65	54	42
	DPWMMin	63	50	41
	DPWM1	71	57	50
	DPWM2	68	55	48
	DPWM3	73	59	52
	DPWM4	72	54	49
$M = 0.9$	DPWMMax	54	51	50
	DPWMMin	56	54	54
	DPWM1	59	56	54
	DPWM2	59	57	57
	DPWM3	58	56	55
	DPWM4	60	58	57

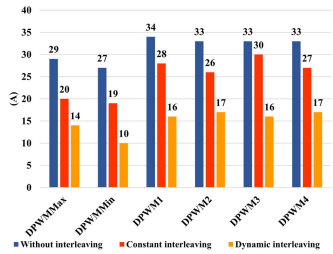

Fig. 32. DC-link current ripple at 400 r/min 70 N·m torque.

the interleaving strategies. Table IX compares dc-link current ripple for different DPWM methods and interleaving strategies for different modulation index values. DC-link current ripple is reduced for the proposed method compared to the without interleaving method and constant interleaving strategy for a wide range of modulation index values. Moreover, for every DPWM method, dc-link current ripple is reduced, validating the proposed method's versatility. At medium modulation index

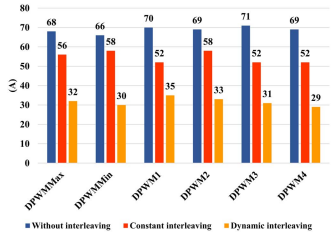

Fig. 33. DC-link current ripple at 1500 r/min 70 N·m torque.

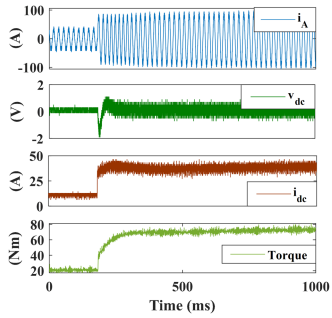

Fig. 34. Torque transient response of the proposed method from 20 to 70 N·m at 800 r/min.

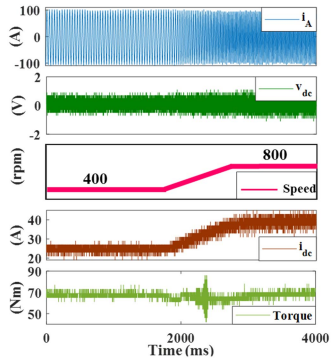

Fig. 35. Speed transient response of the proposed method from 400 to 800 r/min at 70 N·m.

value ($M = 0.5$), dc-link current ripples are reduced significantly through the proposed strategy, which validates the trend followed in the simulation result. The dc-link ripple is still reduced through the proposed method for a high modulation index value ($M = 0.8$). The dc-link ripple for the higher modulation index value ($M = 0.9$) is also shown where the impact of the interleaving methods reduces further as expected and explained in the previous sections. Experimentation is performed at two other operating points to validate the universality of the proposed method. DC-link current ripple comparison at 400 r/min 70 N·m ($M = 0.25$) for every DPWM method and interleaving methods are shown in Fig. 32. Similar comparisons for 1500 r/min 70 N·m ($M = 0.7$) are shown in Fig. 33. The performance of the proposed dynamic interleaving strategy is experimentally validated for multiple operating points and multiple modulation index values.

The torque transient of the proposed method from 17 to 70 N·m at 800 r/min is shown in Fig. 34. Speed transient response of the proposed method for 400 to 800 r-/min at 70 N·m output torque and 400 r/min/s ramp speed is shown in Fig. 35. Figs. 34 and 35 validate the stability of the proposed method during the transient response of the system.

VIII. Conclusion

A dynamic interleaving strategy is proposed in this article for the DTP-PMSM system to reduce the dc-link ripple. The proposed strategy is universal for any DPWM method and works for a wide range of modulation index values. The effect of the conventional constant interleaving angle and the proposed dynamic interleaving angle on the dc-link ripple is analytically derived. The cancellation of all carrier frequency harmonics due to the dynamic interleaving method is mathematically analyzed. Simulation results are provided to validate the performance of the proposed method and mathematical derivation. The proposed dynamic interleaving method is experimentally verified in a dyno test bench setup to validate the mathematical derivation and simulation results. At a medium index value ($M = 0.5$), the dc-link current ripple is reduced by more than 60% than the without interleaving strategy, and by 55% compared to the constant interleaving strategy. Moreover, the transient stability of the proposed method is also proved. The proposed method does not require any additional hardware, making it feasible to implement in any conventional DTP-PMSM drive system. The proposed algorithm reduces dc-link ripple significantly, reducing the dc-link capacitor requirement by a similar amount as dc-link ripple and improving the power density of the drive system.

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