Design and Characterization of Bus Bars for 1-MVA Three-Level ANPC Inverters in Aerospace Applications

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***Abstract*—Bus bars play a crucial role in connecting components and are widely utilized in high-power inverters. Efforts have been made in the past to reduce the stray inductance of bus bars. In the case of multilevel inverters, which involve more complex commutation loops than their two-level counterparts, the physical layout and parasitic parameters of bus bars are particularly important. Furthermore, for novel and more demanding applications such as aerospace, bus bars need to be designed to be lightweight while ensuring a partial discharge (PD)-free insulation performance. Given the challenging cooling condition in aerospace applications, the thermal design and cooling performance of bus bars also warrant considerable attention. This article presents a comprehensive design approach of a laminated bus bar for a 1.5-kV 1-MVA three-level active neutral-point-clamped (ANPC) inverter for electrified aircraft propulsion. With the proposed design methodologies, 29.4- and 48.8-nH inductance for short and long commutation loops, PD-free insulation, and satisfactory thermal performance are achieved with an only 1.77-kg layout. Experimental results confirm that the efficiency of the 1-MVA ANPC inverter can reach 98.97% under half-load conditions with the designed bus bar.**

***Index Terms*—Bus bars, electric aircraft, insulation design, multilevel inverters, thermal design, transportation electrification.**

I. Introduction

ELECTRIC aircraft propulsion has become a topic with increasing interest in the industry in recent years. The onboard power demand for next-generation electric aircraft is dramatically rising, and the need of MVA-level inverters is, therefore, becoming imperative. The National Aeronautics and Space Administration (NASA) has proposed ambitious goals for future aircraft propulsion drives, targeting higher power density and efficiency [1]. Initiated by the NASA and its collaborators, the design of lightweight and high-efficiency 1-MVA inverters for aerospace applications has been extensively pursued [2], [3], [4], [5], [6], [7], [8].

With their power density and efficiency advantages, three-level inverters have been considered the enabling technology for advanced aircraft electric propulsion systems [9]. Among various three-level topologies, the active neutral-point-clamped (ANPC) inverter stands out as a promising candidate in high-power propulsion drive, due to its lower switching voltage and balanced power loss distribution. Several ANPCs have been designed and prototyped for electric aircraft applications [2], [3], [4], [5]. In these prototyped ANPCs, wide-bandgap (WBG) devices such as silicon carbide (SiC) were adopted, significantly improving the inverter efficiency. However, the application of WBG devices poses technical challenges for aerospace inverters. Compared to conventional insulated-gate bipolar transistors, the faster switching speed of WBG devices leads to higher di/dt, inducing larger voltage overshoot across the switches during turn OFF, thereby causing severe risks to inverter safety. To mitigate the voltage overshoot during the turn-OFF transient, reducing the commutation loop inductance becomes critical for ANPCs in aerospace applications.

As an essential component of inverters, bus bars serve as connectors for different components, e.g., semiconductor switches, dc-link capacitors, electromagnetic interference (EMI) filters, etc. In comparison to cables, bus bars are particularly preferred by high-power inverters due to their higher current ampacity and more effective heat dissipation. As bus bars perform the interconnection function, their parasitic inductance strongly influences voltage overshoot. Without well-controlled parasitic inductance, the commutation loop inductance of high-power ANPCs can easily exceed 100 nH, which can induce an over 1000-V spike with the high-speed WBG devices and damage the inverter [10]. Therefore, designing a low-stray inductance bus bar is one of the fundamental requirements for aerospace inverters. Besides low-stray inductance, lightweight bus bars

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are also desirable, as bus bars can substantially contribute to the inverter total mass, and their weight reduction helps achieve higher power density, eventually leading to more cost-effective propulsion units [9]. In addition, at higher altitudes where air density and pressure decrease, the likelihood of partial discharge (PD) increases. Heat transfer also becomes a greater concern due to the degraded airflow and cooling efficiency. Both PD and overheating can lead to direct failure or accelerated aging of the insulation materials, threatening the inverter safety. Hence, PD-free and adequate thermal designs are particularly important for aerospace inverter bus bars.

To conclude, key metrics of bus bars in aerospace applications include low-stray inductance, light weight, PD-free, and cooling efficiency. Several studies have been conducted to address these challenges in bus bar design, many of which focus solely on physical layout optimization and loop inductance reduction [11], [12], [13], [14], [15]. Despite the improvements, some proposed designs still have more than 100-nH loop inductance, which is insufficient to match the fast switching speed of WBG devices. Some studies have also considered the insulation [16], [17], [18], [19] and thermal [20], [21], [22] performance of bus bars during the design process. Nevertheless, a comprehensive design approach that integrates loop inductance, weight, insulation, and thermal performance for aerospace bus bars has yet to be developed. The interaction of these different design metrics has not been clearly revealed either. A few articles have presented multiobjective optimized designs for other three-level topologies, such as T-type inverters [23], [24], [25], [26]. However, the commutation loop of T-type inverters differs from that of ANPC inverters and does not suffer from asymmetric commutation loop issues, making the design methodology inapplicable.

In this article, the design of the bus bar for a 1-MVA three-level aerospace ANPC is presented. The major contributions of this article are summarized as follows.

1) A comprehensive design approach of aerospace bus bars is introduced, considering the integration and interaction of different design metrics. The proposed approach can be used as a guideline for bus bar designs in different scenarios.
2) For the thermal design, a new heat transfer model is proposed, highlighting the significant effect of heat transfer from power modules and their cooling systems on bus bar thermal performance, which was ignored in previous studies.
3) Using the introduced approach, a laminated bus bar is designed and prototyped for the 1-MVA three-level ANPC inverter. Its performance, including stray inductance, insulation, and thermal characteristics, is quantitatively validated through both simulations and experiments. With the measured switching losses, the ANPC inverter can achieve up to 98.97% efficiency under half-load conditions.

The rest of this article is organized as follows. Section II analyzes commutation loops in three-level ANPCs. Section III presents the optimization design of bus bar conductor plates. Insulation design is elaborated in Section IV. The heat transfer characteristics of the designed bus bar are analyzed in Section V. A summary of the proposed design methodologies is presented in Section VI. Experimental characterization of the bus bar performance is presented in Section VII. Finally, Section VIII concludes this article.

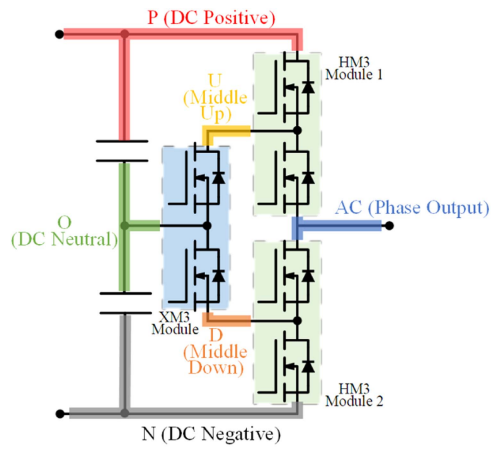


Fig. 1. Three-level ANPC.

TABLE I
MAJOR SPECIFICATIONS OF DESIGNED ANPC

Parameters	Values
Maximum output power	1 MVA
DC-link voltage	1.5 kV
Maximum fundamental frequency	1 kHz
Coolant temperature	70 °C
Inverter peak efficiency	≥98%

TABLE II
SWITCHING STATES OF THREE-LEVEL ANPC [27]

Switching state	Output voltage	S1	S2	S3	S4	S5	S6
+	$V_{DC}/2$	1	1	0	0	0	1
0U1	0	0	1	0	1	1	0
0U2		0	1	0	0	1	0
0L1		1	0	1	0	0	1
0L2		0	0	1	0	0	1
–	$-V_{DC}/2$	0	0	1	1	1	0

II. ANPC COMMUTATION LOOP ANALYSIS

The three-level ANPC topology and the major specifications for the designed ANPC are presented in Fig. 1 and Table I, respectively. Two SiC half-bridge power modules with the HM3 package from Wolfspeed are adopted as phase-leg switches, and another XM3 package SiC half-bridge module with a lower current rating is used for active clamping switches. Based on the power module selection, the interconnection that requires bus bars is also labeled in Fig. 1.

The switching states of three-level ANPC are listed in Table II. Since the designed ANPC aims to work with a high power factor, Type 1 and 3 commutations are used to achieve a balanced power loss distribution [27]. Consequently, there will be four possible commutation states, i.e., the inverter commutates between the switching state "+" and states "0L1" or "0U2" when phase voltage is positive and commutates between state "–" and "0U1" or "0L2" when phase voltage is negative.

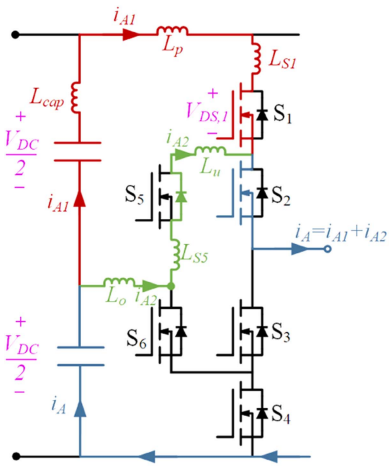


Fig. 2. Commutation of three-level ANPC from state "+" to "0U2."

Fig. 2 shows the commutation process when it occurs between states "+" and "0U2." Since the voltage is positive when this specific commutation occurs and the power factor is high, the output phase current i_A should also be positive. When the switching state changes from "+" to "0U2," S_1 will turn OFF, and S_5 will turn ON. In this case, the current i_{A1} will gradually decrease from i_A to zero, while current i_{A2} will increase from zero to i_A. According to KVL, following equation can be obtained:

$$V_{\mathrm{DS},1} = \frac{V_{\mathrm{DC}}}{2} + (L_{\mathrm{cap}} + L_P + L_{S1})\left|\frac{di_{A1}}{dt}\right| + (L_U + L_O + L_{S5})\left|\frac{di_{A2}}{dt}\right| \quad (1)$$

where L_P, L_U, and L_O are the stray inductances of bus bars P, U, and O in Fig. 1, respectively, L_{S1} and L_{S5} are the parasitic inductances of switches S_1 and S_5, respectively, and L_{cap} is the equivalent series inductance (ESL) of the dc-link capacitor, of which the voltage is $V_{\mathrm{DC}}/2$. For simplicity, the mutual inductance between each item is neglected. Since i_A can be assumed as constant during commutation transient, $|di_{A1}/dt| = |di_{A2}/dt|$. Therefore, (1) can be rewritten as

$$V_{\mathrm{DS},1} = \frac{V_{\mathrm{DC}}}{2} + (L_{\mathrm{cap}} + L_P + L_{S1} + L_U + L_O + L_{S5})\left|\frac{di_{A1}}{dt}\right|. \quad (2)$$

According to (2), there will be a voltage overshoot on S_1 caused by the voltage across the stray inductances during commutation. The commutation loop inductance in Fig. 2 can, thus, be written as follows:

$$L_{\mathrm{Loop},1} = L_{\mathrm{cap}} + L_P + L_{S1} + L_U + L_O + L_{S5}. \quad (3)$$

For commutations between other switching states, the analysis procedure is similar and will not be repeated here. In conclusion, for the three-level ANPC, depending on the voltage and current polarities, there will be four different commutation loops, as shown in Fig. 3. As can be observed from Fig. 3, the commutation loops of three-level ANPC are asymmetric, which

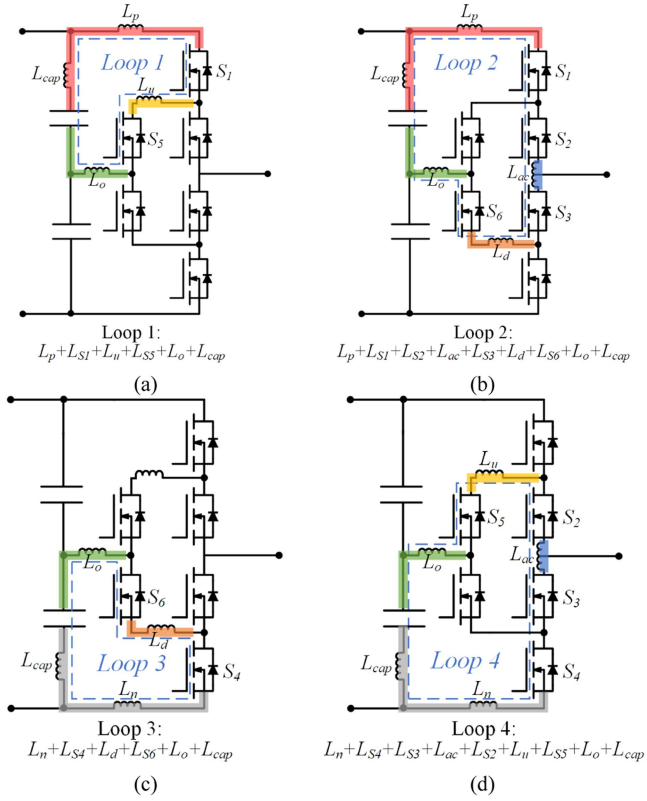


Fig. 3. ANPC commutation loops (single phase leg). (a) Loop 1 (between "+" and "0U2"). (b) Loop 2 ("+" and "0L1"). (c) Loop 3 ("–" and "0L2"). (d) Loop 4 ("–" and "0U1").

can be categorized into "short loops" (Loops 1 and 3) and "long loops" (Loops 2 and 4). In long loops, more bus bar pieces and switching devices are involved. As a result, a higher loop inductance and a voltage spike are expected when the inverter commutates along the long loops.

III. Conductor Plate Design and Optimization

A. Power Stage Layout

As the bus bar fulfills the interconnection of the power stage, its layout highly relies on the placement of power modules and dc-link capacitor banks. To design the bus bar, the power stage layout should be discussed first.

For aerospace inverters, a power-dense design is preferred. On the other hand, the manufacturability of the layout should also be considered. Fig. 4 shows three different proposals of one phase leg. For the power density reason, Fig. 4(a) is not preferred since it has the largest surface area. In terms of power density, Fig. 4(c) is preferred over Fig. 4(b) as the surface area is smaller. However, with the dimension specified in Fig. 4(c), the cold plate underneath the XM3 module will interfere with the cooling channel outlets of two HM3 modules. Without increasing the distance between the HM3 modules, the channels under HM3 modules will need a bending, making the cold plate machining more challenging and increasing the pressure drop. In contrast to Fig. 4(c), the layout in Fig. 4(b) is a more practical

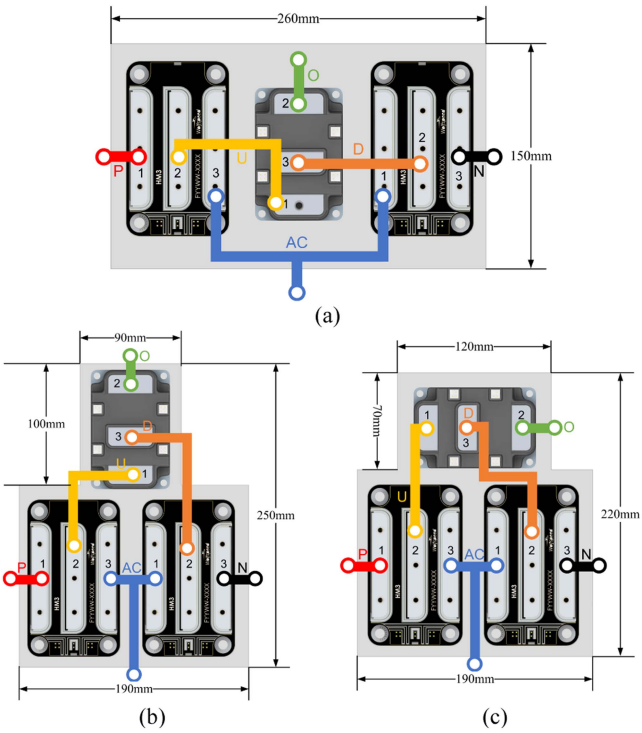


Fig. 4. (a)–(c) Three layout proposals of the power stage of three-level ANPC (single phase leg).

proposal due to easier cold plate manufacturing. Eventually, Fig. 4(b) is selected for the tradeoff between power density and manufacturability.

B. Bus Bar Lamination

The laminated bus bar is a well-known technique to reduce the stray inductance. The lamination of bus bar layers with opposite current flow direction will generate magnetic fluxes canceling each other, thus inducing negative mutual inductance to reduce the overall commutation loop inductance [16]. For traditional two-level inverters, the sequence of bus bar lamination is relatively simple, as the laminated bus bar will have up to three nodes, i.e., dc positive, dc negative, and ac phase output. However, for multilevel inverters with more nodes, the design of lamination becomes a greater concern.

A rule of thumb to design laminated bus bars is to select one copper layer which is shared by most of the commutation loops as the "returning path" [28]. For the selected returning path, its surface area should be maximized to fully overlap with other bus bar layers, so that the magnetic flux cancellation effect can be maximized. Another rule is that each conductor plate is preferred to occupy a big enough area on its own layer, so that the section area is large enough to achieve a low self-inductance and reasonable current density. Generally, the width of each conductor plate is preferred to be 40%–50% of the layer total width [29]. The self-inductance and mutual inductance between two laminated conductor plates can be calculated as [30], [31]

$$L = \frac{\mu_0 \mu_r l}{\pi}\left(\frac{1}{8} + \frac{2t}{t+w}\right) \tag{4}$$

$$M = \frac{\mu_0 \mu_r l t}{\pi\sqrt{4(d+t)^2 + kw^2}} \cos\emptyset \tag{5}$$

where l, w, and t are the length, width, and thickness of each plate, respectively, d is the distance between two laminated plates, μ_0 and μ_r are the vacuum permeability and the relative permeability of the insulation material, respectively, k is the correction coefficient, and ϕ is the angle between the current direction of two plates. Equation (5) indicates that the distance d between two plates shall be kept as small as possible to maximize the negative mutual inductance. In other words, to fully utilize the flux cancellation effect, the returning and outgoing paths of the bus bar should be placed in proximity.

According to the aforementioned rules, the neutral bus bar O is selected as the returning path for the designed laminated bus bar and occupies one single layer, since all the four commutation loops share O in three-level ANPC. For the other five nodes, i.e., P, N, U, D, and ac, based on the rules of plate width, they can be assigned to at most three different layers. Therefore, the number of layers will vary from two to four. Accordingly, three preliminary layouts of the ANPC bus bar are proposed, as shown in Fig. 5. Comparing the three proposals, the two-layer layout [28] maximizes the cancellation effect among all the outgoing paths and the returning path O since only one insulation layer is needed, and the distance d is, thus, minimized. Nevertheless, the five outgoing paths have the smallest section area, much less than the desirable 40%–50% of the total layer width. Furthermore, due to the layout of the XM3 module, bus bars U and D in the two-layer layouts have to make turns to avoid interfering with each other, reducing the effective conducting section area of both the bus bars. As a result, the current density of U and D in the two-layer layouts will be much higher than the desirable 5 A/mm^2 [16].

Unlike the two-layer layouts, the three-layer layout in Fig. 5(b) puts the bus bars U and D on two different layers. This compromises the cancellation effect between U and P, as there is an extra layer (O) in between, and d is, thus, increased. Nevertheless, since P and U will only be involved in the same loop when the commutation occurs along the short loops, which intrinsically have lower inductance, increasing the distance between them causes less severe problems. In contrast, the four-layer layout in Fig. 5(c) puts the ac bus bar on one separate layer, which compromises the flux cancellation effect in long commutation loops and makes the bus bar thicker and heavier. To achieve the balance between loop inductance and current density, the three-layer design is finally adopted.

C. Returning Path Optimization

As the returning path being shared among all the commutation loops, the self-inductance and mutual inductance of bus bar O greatly affect commutation loops. Therefore, the design of O is critical, and its stray inductance should be fully optimized.

The baseline design of bus bar O for one phase is shown in Fig. 6(a). During commutations, the current through XM3 module's terminal will flow along the middle branch on bus bar O and then to the capacitor banks (left-side capacitor bank in Loop 1).

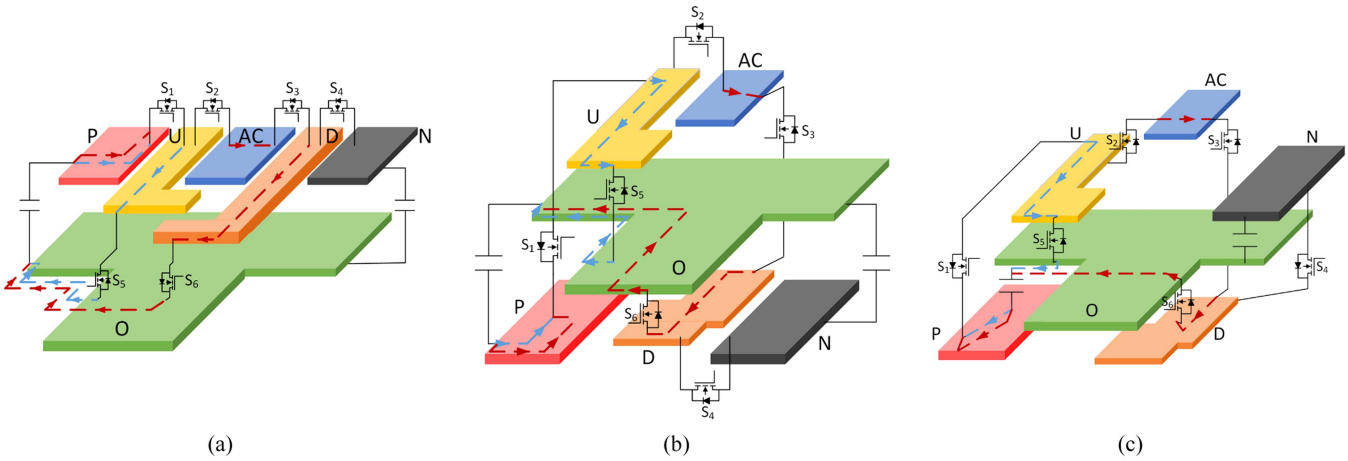


Fig. 5. Three proposals of bus bar lamination (single phase leg). (a) Two layers [28]. (b) Three layers. (c) Four layers. Blue dashed lines refer to short-loop commutation paths, and red dashed lines for long-loop paths.

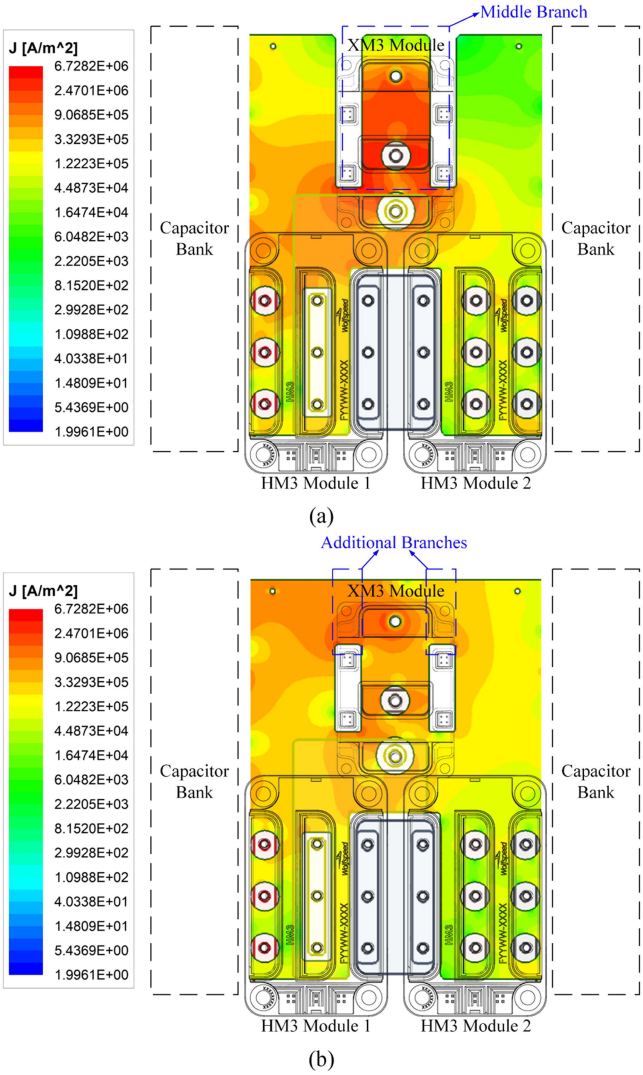


Fig. 6. Different designs of the returning path and its current distribution in Loop 1 commutation. (a) Baseline design. (b) Improved design.

TABLE III
SELF-INDUCTANCE AND MUTUAL INDUCTANCE OF RETURNING PATH WITH DIFFERENT LAYOUTS

Fig. 6 (a): baseline						
Inductance	L_O	$M_{O,P}$	$M_{O,N}$	$M_{O,U}$	$M_{O,D}$	$M_{O,AC}$
Value [nH]	23.53	−0.2	−0.2	−7.28	−4.46	−0.22
Fig. 6 (b): improved						
Inductance	L_O	$M_{O,P}$	$M_{O,N}$	$M_{O,U}$	$M_{O,D}$	$M_{O,AC}$
Value [nH]	10.47	−0.14	−0.14	−4.39	−1.90	−0.14

*Self-inductance of bus bar O (L_O) is highlighted in blue.

In this case, *O*'s current direction will be almost exactly opposite of middle bus bars *U* and *D*, leading to the strongest cancellation effect between these pieces. Nonetheless, this is not necessarily the best case for the global optimization of the loop inductance. An improved design of bus bar *O* is shown in Fig. 6(b), which adds two additional branches to connect the left and right sides of the middle branch. As can be observed in Fig. 6(b), the additional branches effectively increase the conducting area as they provide extra paths, reducing the current density on the middle branch. As a result, a lower self-inductance can be expected based on (4). This has been further verified by FEA results from Ansys Q3D in Table III. As can be seen, although the negative mutual inductance between bus bar *O* and other pieces becomes lower, the self-inductance of *O* in the improved design is also lower than the baseline design. Consequently, the loop inductance is optimized with the improved design.

Another important concern of returning path optimization is the dc-link capacitor placement. In the designed ANPC, film capacitors from Panasonic [32] are used as the dc-link capacitors for its high power density. Multiple capacitors are paralleled on each side of the inverter to form the upper and lower capacitor banks, reducing the capacitor banks' ESL. Based on the capacitor bank configuration, the capacitor terminals of the bus bar can be placed in two different ways. The first way is to place all the capacitor leads with the same polarity at one side and connect them to the same conductor plate (*P*/*N*/*O*), as shown in Fig. 7(a); the other way is to adopt an interleaving placement, i.e., put the

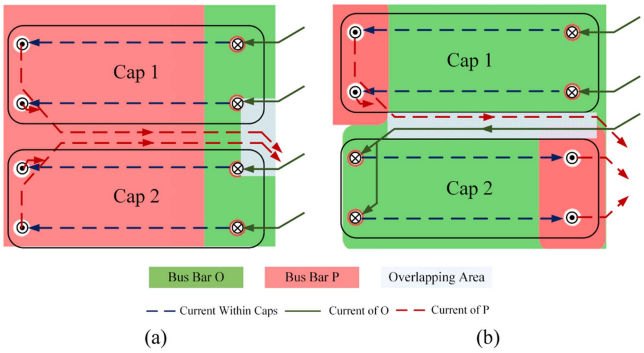


Fig. 7. DC-link capacitor placement methods. (a) One-sided placement. (b) Interleaving placement.

two capacitors with the opposite polarity next to each other, as shown in Fig. 7(b). In terms of loop inductance, the interleaving placement in Fig. 7(b) will have advantages over Fig. 7(a), since it increases the overlapping area of bus bars *P*/*N* and *O*, making the cancellation effect stronger. Moreover, the layout of *O* in Fig. 7(a) also negatively affects the design of bus bar *P*. If *O* is designed as Fig. 7(a), *P* will need a long row of through holes to let the capacitor leads pass through and connect to *O*. The big through holes on *P* cut the width of the conducting section, increasing the self-inductance of *P* and leading to a higher loop inductance.

IV. Bus Bar Insulation Design

With the optimized conductor plate layout, the overall bus bar design is demonstrated in Fig. 8. For bus bars *P* and *N*, three terminals are placed on each side to distribute the high dc current and reduce the current density at each terminal. Copper standoffs are used to connect the bus bars to the corresponding power module terminals. Two layers of insulation films are put in the middle of two conductor plates to avoid scratches and accidental break of any insulation layer. 3D-printed insulation rings are put in the center of conductor through holes to strengthen the insulation. All the edges of the bus bar are filled with epoxy to prevent contamination and moisture. In the following section, a more detailed elaboration of the bus bar insulation design is to be presented.

A. Clearance and Creepage Dimensioning

To design the bus bar insulation, the standard that is to be followed needs to be specified first. Current standards for the aviation industry focus on 28-V dc and 115-V ac system design without going for a higher bus voltage [33], [34]. Therefore, in this article, the design of bus bar insulation follows the IEC 60664-1 [35], one of the most adopted standards for equipment insulation. IEC 60664-1 complies with devices supplied by voltage up to 1-kV rms ac or 1.5-kV dc, and operating frequency up to 30 kHz, both of which satisfy the targeted specifications of the designed ANPC. According to IEC 60664-1, the bus bar insulation is classified as functional insulation, with the overvoltage category (OVC) II and pollution degree 2. With the

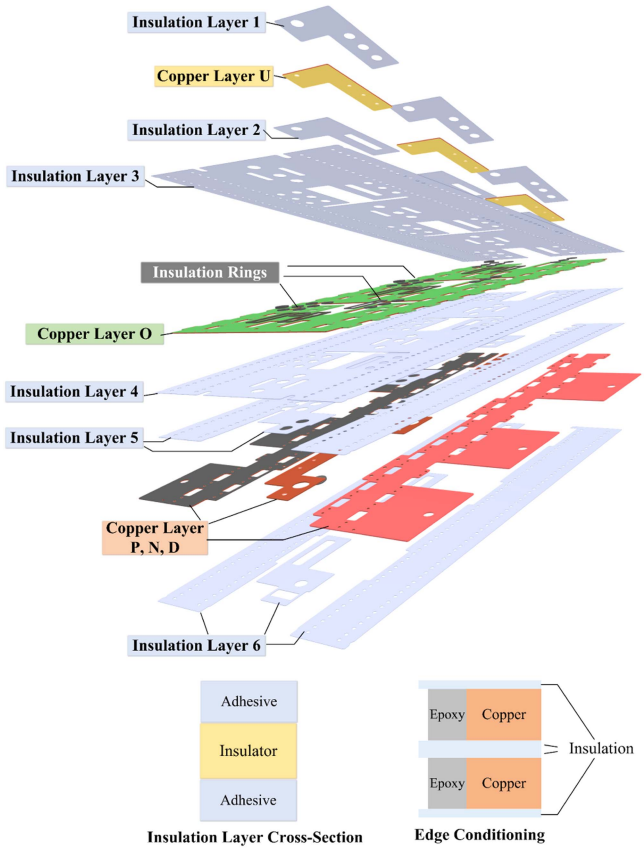


Fig. 8. Exploded view of the designed bus bar with insulation films.

specified insulation standard, the clearance and creepage of the bus bar can then be dimensioned.

In IEC 60664-1, the clearance is determined by both the OVC level and the pollution degree. According to the standard, the rated impulse voltage of the designed bus bar under OVC II should be 6 kV. At pollution degree 2, the minimum clearance for 6-kV impulse voltage is 5.5 mm at sea level. Since the clearance should be dimensioned proportionally to the equipment operating altitude, the 5.5-mm clearance is multiplied by a 1.48 correction factor for 5000-m altitude operation. Therefore, the final calculated clearance is 8.14 mm and is rounded to 8.2 mm for a larger safe margin. Fig. 9 demonstrates how the bus bar should be dimensioned based on the obtained clearance value. As shown in Fig. 9, the distance between two exposed spots on different conductor plates should be no less than 8.2 mm. Accordingly, the extension distance of insulation films and the distance between two adjacent capacitor terminals are designed.

The creepage of bus bar insulation depends on the voltage level and is also affected by the pollution degree and the comparative tracking index (CTI) of insulating materials. According to IEC 60664-1, for materials in CTI group 1 at pollution degree 2, the minimum creepages at 750-V dc ($V_{\mathrm{DC}}/2$) and 1500-V dc (V_{DC}) are 3.8 and 7.5 mm, respectively, both of which are smaller than the dimensioned 8.2-mm clearance. Since the clearance is the minimum distance between two exposed conductors and the creepage between the same two spots will naturally be

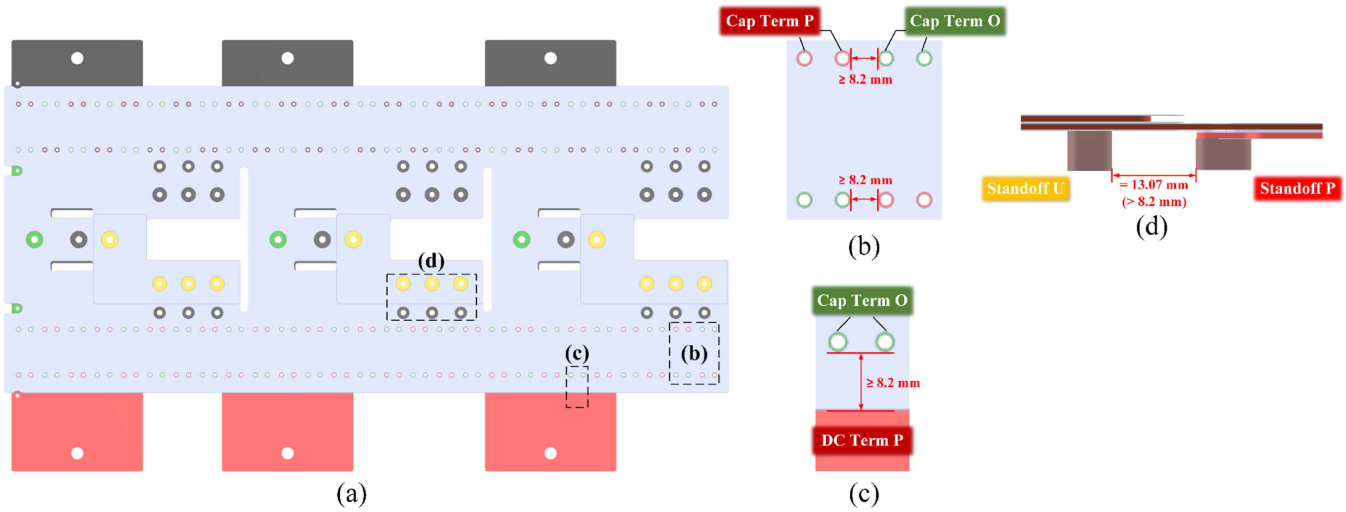


Fig. 9. (a) Clearance dimensioning at different spots. (b) Clearance between capacitor terminals. (c) Clearance between the edges of *P* and *O*. (d) Clearance between standoffs.

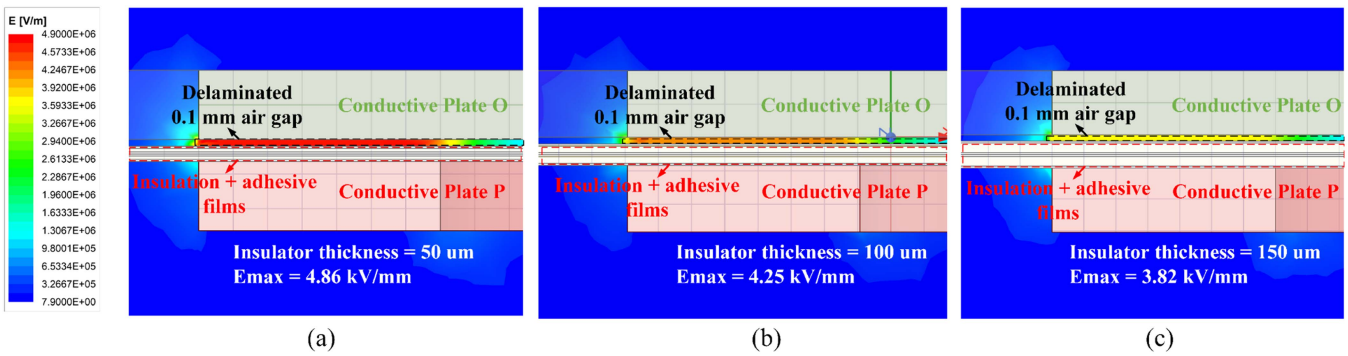


Fig. 10. Electric field distribution in the 100-μm delaminated air gap with different insulation film thicknesses: (a) 50 μm, (b) 100 μm, and (c) 150 μm.

longer than clearance, dimensioning the insulation with 8.2-mm clearance can intrinsically guarantee the creepage requirements specified by IEC 60664-1. Therefore, specific attention is not needed for the creepage dimensioning in the designed bus bar insulation.

B. Insulation Material and Thickness

Regarding the bus bar insulation material, standard options are Nomex, polyimide (Kapton), polyester (PET), and polyvinyl fluoride (PVF), with their major characteristics listed in Table IV. All the insulation materials have good dielectric strength, theoretically allowing them to withstand the nominal 1.5-kV voltage with a low thickness. Among the available options, Kapton is preferred for its high dielectric strength and better thermal conductivity. Its high dielectric constant also increases the parasitic capacitance between conductor plates, reducing the E-field intensity on insulation films [17] and having stronger filtering of EMI noises [16]. The major drawback of Kapton is that it lacks the flexibility to be elongated. If bending of bus bars is necessary, more flexible materials, such as PET and PVF, can also be used. The selection of adhesive material between the conductor and insulation layers has been discussed in [17] in detail. Given the availability of off-the-shelf products, acrylic is often used as the adhesive layer of insulation films.

TABLE IV
PROPERTIES OF MAJOR INSULATION MATERIALS

Materials	DuPont Nomex 410	Kapton	PET (Mylar)	PVF (Tedlar)
Dielectric strength	18–34 kV/mm	154–303 kV/mm	60–320 kV/mm	130 kV/mm
Dielectric constant	1.6–3.7	3.4–3.5	2.8–3.7	8.5–11
Thermal conductivity	0.1–0.17W/m·K	0.2W/m·K	0.15W/m·K	N/A
Elongation	10%–21%	72%–83%	120%–150%	130%–358%

For the required thickness of insulation layers, a thinner layer is generally preferred as long as it offers enough insulation strength. A thinner insulation layer (i.e., smaller distance between layers) will increase the cancellation effect between

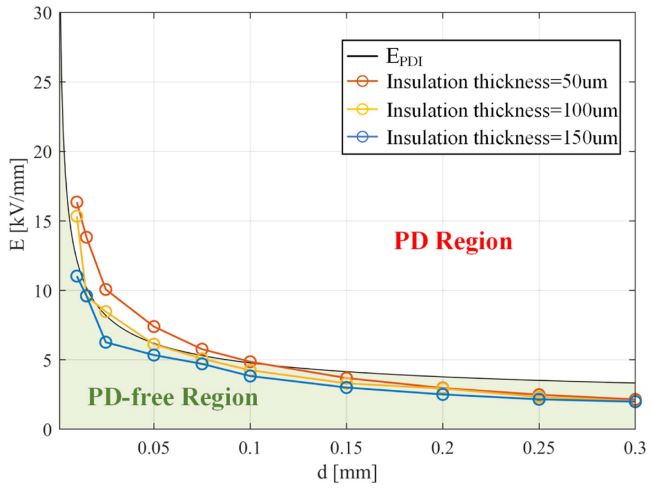


Fig. 11. Electric field intensity of the delaminated gap with different air gap distances (d) and insulation film thicknesses.

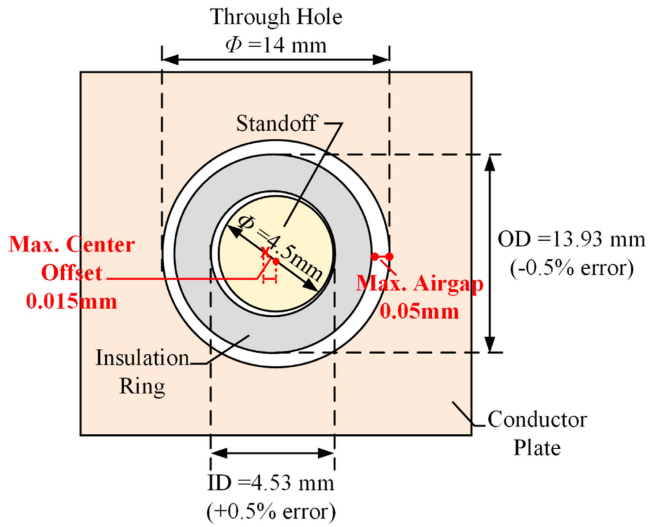


Fig. 12. Demonstration of insulation ring offset inside the bus bar through holes caused by manufacturing tolerance.

laminated conductors and reduce the loop inductance. Parasitic capacitance will also increase with reduced insulation thickness. Thinner insulation can also transfer the heat more efficiently, benefiting bus bar thermal management. However, the insulation layer cannot be too thin either, as it will increase the risk of PD. In aerospace applications, PD will be more prone to occur and should be avoided carefully [36]. This article determines the minimum insulation layer thickness to ensure a PD-free bus bar design.

The PD inception electric field intensity E_{PDI} is calculated as [37]

$$E_{\mathrm{PDI}} = \frac{(E_1/p)_{cr} p \left[1 + \frac{B}{(pd)^n}\right]}{f} \tag{6}$$

where $(E_1/p)_{cr}$, B, and n are the ionization parameters of the air, p is the air pressure, d is the air gap distance, and f is the field enhancement factor. For air, $(E_1/p)_{cr} = 25$ V/(Pa·m), $B = 5.9$ $\mathrm{Pa}^{0.5}\mathrm{m}^{0.5}$, $n = 0.5$, and $f = 1$. At targeted 5000-m altitude, $p =$ 54 000 Pa. As can be observed from (6), E_{PDI} depends on the air gap dimension and air pressure, which varies with the operating altitude.

One critical scenario that can induce PD on the laminated bus bar is the delamination between adhesive layers and conductors [23]. This can happen after a long-term operation of the inverter caused by vibration and thermal fatigue of adhesive films. The effect of delamination is elaborated with a case study, where the edges between two bus bar layers are delaminated, and a 100-μm air gap appears between the conductor and its adhesive layer. The electric field distribution in the analyzed area is shown in Fig. 10. It can be found that the E-field intensity decreases as the insulation films become thicker. With the insulator thickness increased from 0.05 to 0.15 mm, the maximum E-field can be reduced by 21%. Fig. 11 depicts the E-field curves of the bus bar with different air gap distances and insulator thicknesses. To design the insulation that will not induce PD with delamination, the E-field in the air gap should be lower than E_{PDI} with any air gap distances, i.e., the entire curve should remain inside the green PD-free operating region. According to Fig. 11, a 150-μm-thick insulator film can guarantee PD-free operation with any extent of delamination.

Another case of PD on the bus bar is the air gap caused by the tolerance of insulation rings. As shown in Fig. 12, due to the manufacturing tolerance, insulation rings that fill the conductor through holes can have an alignment offset from the hole center. As a result, there will be a tiny air gap between the insulation rings and the conductor plates. For the designed bus bar, given that all the insulation rings are 3-D printed and a $\pm 0.5\%$ accuracy is realized, the air gap between the insulation ring and the conductor plate can be up to 50 μm. Fig. 13 shows another case study on the E-field distribution of a 20-μm air gap with different insulator film thicknesses, and the E-field curves with different air gap distances and insulator thicknesses are plotted in Fig. 14. As can be seen, a design to avoid PD due to insulation ring offset can be ensured when insulator thickness is no less than 250 μm.

Considering both the delamination and insulation ring offset cases, the minimum thickness of each insulator layer is finally determined as

$$d_{\mathrm{min}} = \mathrm{Max}\ (d_{\mathrm{delamination}},\ d_{\mathrm{offset}}) = 250\,\mu\mathrm{m}. \tag{7}$$

As shown in Fig. 8, there are two insulation (insulator + adhesive) layers between the conductor plates. With the 30-μm acrylic adhesive layers, the final distance between two conductor plates is 0.62 mm.

V. Bus Bar Thermal Characteristics

To avoid overheating insulation materials and attached components, the thermal characteristics of bus bars need careful verification. In this article, an FEA-based numerical model of the designed laminated bus bar is adopted. A demonstrative model with major paths of bus bar heat transfer is shown in Fig. 15. As can be seen, the bus bar has natural convection with the air

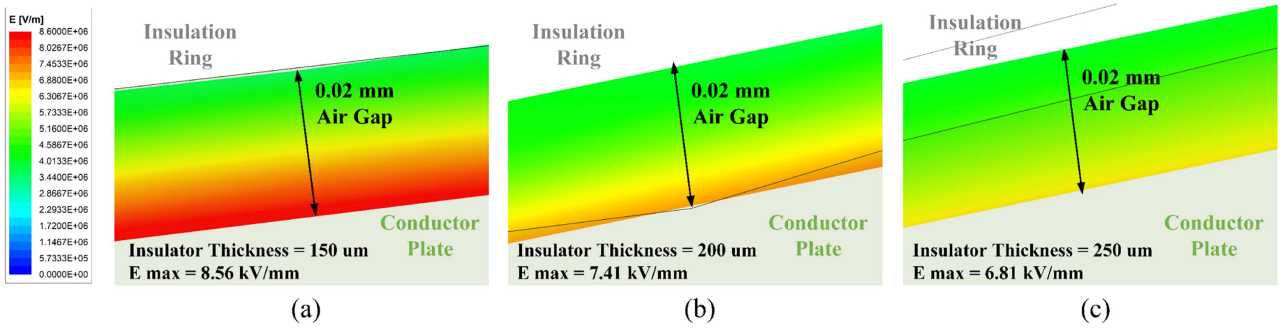


Fig. 13. Electric field distribution in the 20-μm unaligned air gap with different insulation film thicknesses. (a) 150 μm. (b) 200 μm. (c) 250 μm.

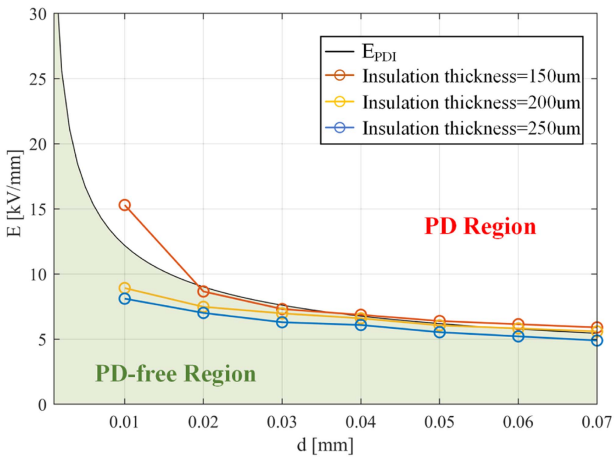


Fig. 14. Electric field intensity of the unaligned ring gap with different air gap distances (d) and insulation film thicknesses.

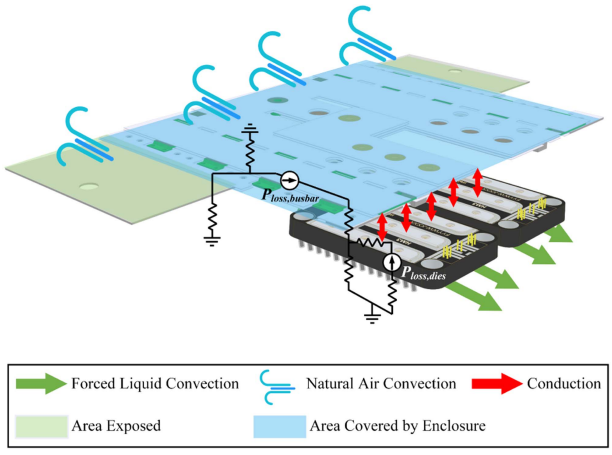


Fig. 15. Single-phase model for the thermal FEA and its major heat transfer paths with the equivalent thermal network.

on the top surface. Meanwhile, there simultaneously exists the heat transfer between the bus bar and power modules through the physical contact of terminals and bus bar standoffs. For high-power inverters, power modules typically generate more losses than bus bars; as a result, bus bar temperature is significantly affected by heat transfer between bus bars and power modules.

TABLE V
CONVECTION PARAMETERS IN THE FEA MODEL

Area	$G_rL P_r$	C	m	h (W/m°C)
Exposed terminals (top surface)	*[2×10^4, 8×10^6]	0.54	1/4	11.3
	[8×10^6, 1×10^{11}]	0.15	1/3	
Exposed terminals (bottom surface)	[10^5, 10^{11}]	0.27	1/4	5.6
Enclosed bus bar	*[7×10^3, 3.2×10^5]	0.21	1/4	2.6
	>3.2×10^5	0.61	1/3	
HM3 modules	Not applicable for liquid-cooled forced convection			8000
XM3 modules				4500

* Range applied to the designed bus bar

Nevertheless, the heat transfer between power modules and bus bars is ignored in previous studies, where the bus bar is often assumed as an isolated system [20], [21], [22]. In this section, the impact of power modules on bus bar heat transfer is revealed with the FEA.

Due to the symmetry of three phases and computationally expensive feature of FEA numerical models, the FEA is conducted on the single-phase geometry in Fig. 15. An electrical–thermal co-modeling method is adopted in the FEA. The bus bar current profile and power module losses are obtained from PLECS simulation as the FEA inputs. To simulate the worst case for thermal design, the current profile is obtained at the ANPC's operating point with peak output power, where the highest power losses are generated on both bus bars and power modules.

As shown in Fig. 15, natural convection of the bus bar will occur around its exposed dc terminals. Simultaneously, another portion of natural convection takes place between the top surface of the bus bar and the inverter enclosure. The natural convection can be empirically calculated as [38]

$$N_{uL} = C(G_{rL}P_r)^m \tag{8}$$

where N_{uL} is the Nusselt number, and the subscript L refers to the ratio of the area to the perimeter. P_r is the Prandtl number; its value depends on the physical properties of the air. C and m are constants depending on convection conditions. For exposed and enclosed parts, values of C and m are different and are given

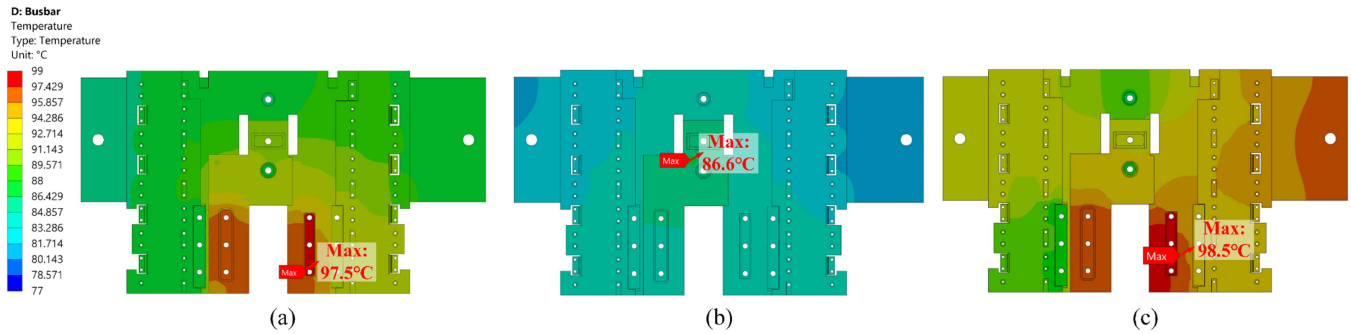


Fig. 16. Bus bar temperature distribution from the thermal FEA. (a) With power modules and air convection. (b) With air convection but without power modules. (c) With power modules but without air convection.

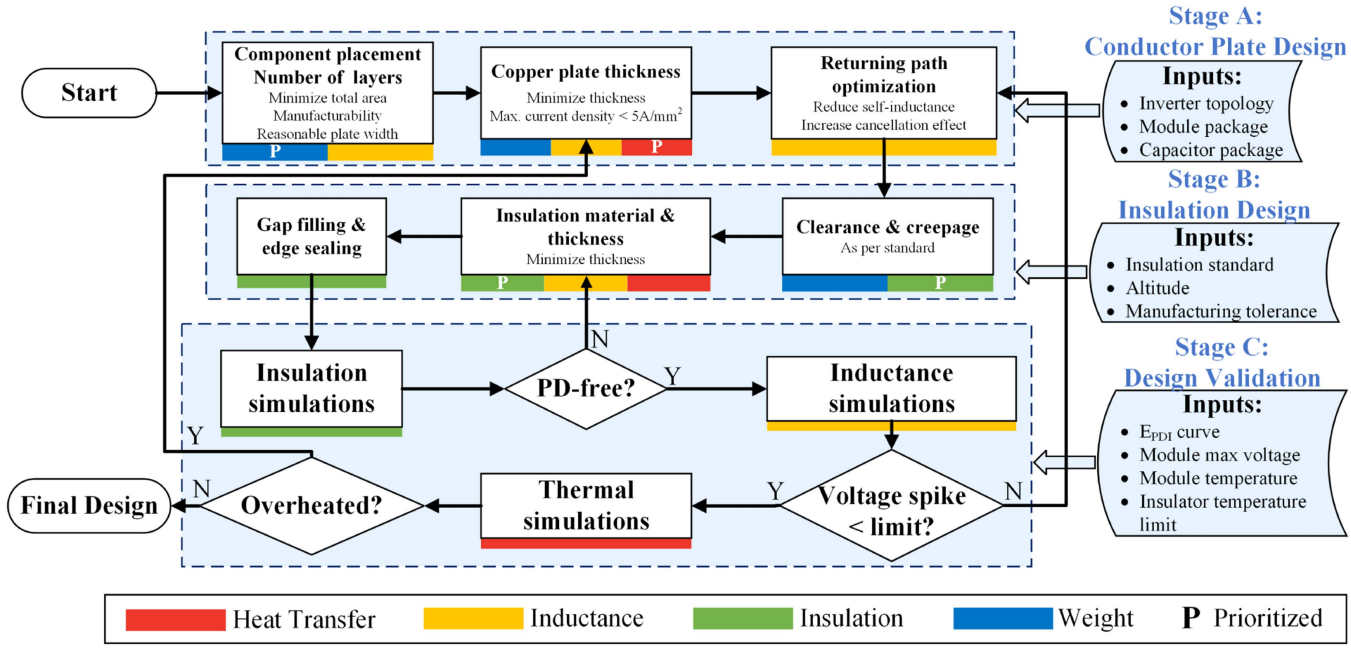


Fig. 17. Flowchart of the bus bar design methodology.

in Table V. G_{rL} is the Grashof number and can be calculated as

$$G_{rL} = \frac{g\beta\left(T_b - T_a\right)L^3}{v^2} \tag{9}$$

where g is the gravity constant, $\beta = 1/T_f$, and $T_f = (T_a + T_b)/2$ is the air film temperature. v is the kinematic viscosity of air film at T_f. L is the characteristic dimension. For convection on the exposed area, L refers to the ratio of the exposed area to its perimeter; for the enclosed area, L is the distance between the bus bar and the enclosure. With N_{uL} calculated, the heat transfer coefficient h can be expressed as

$$h = \frac{N_{uL}k}{L} \tag{10}$$

where k is the thermal conductivity of the air at T_f. The calculated h values for different parts in the geometry are summarized in Table V. The equivalent h values for power modules are estimated from separate computational fluid dynamics (CFD) simulations.

The thermal FEA result of the bus bar is shown in Fig. 16(a). As the result shows, the maximum temperature of the bus bar is around 97.5 °C, well below the glass transition temperature of the insulator (360 °C), the operating temperature of adhesive materials (110 °C), and the power module case temperature limit (125 °C). Compared to the FEA results with power modules in Fig. 16(a), the maximum temperature in Fig. 16(b) is reduced by 10.9 °C, showing the significant effect of power module temperature on bus bar cooling. The FEA without natural convection on the bus bar surfaces is also conducted and shown in Fig. 16(c). As the result shows, the natural convection changes the temperature distribution, especially on the exposed terminals where natural convection is stronger, but the bus bar maximum temperature is only affected by 1 °C. It further confirms that the effect of the coolant is significantly stronger than that of the natural convection of the bus bar itself. A properly designed

inverter cooling system not only dissipates power modules' losses but also helps with bus bar cooling. The cooling path, heat generation, and corresponding temperature field of the bus bar and its connected devices should be coupled and comodeled.

VI. Summary of Design Methodology

The proposed design methodology is summarized and presented as a flowchart in Fig. 17. The complete procedure can be divided into three stages, i.e., conductor plate design, insulator design, and design validation. These stages will be introduced in this section in detail.

A. Conductor Plate Design

Stage A involves designing the bus bar conductor plates, including their placement, shape, thickness, and number of conduction layers. These characteristics are determined based on the inverter topology and specifications and the package of selected components. For aerospace applications, the objective of conductor plate design is to achieve the lowest possible conductor weight and inductance while ensuring an allowable current density to avoid overheating.

B. Insulation Design

In this stage, the insulation design is determined, including the material and thickness of insulation films, gap filling and edge sealing techniques, and the areas that need to be covered to maintain enough clearance and creepage between conductors. The standard to be followed shall be established before designing the insulation. For aerospace applications, the operating altitude should also be known to determine the altitude correction factor of clearance and creepage. The goal of this stage is to minimize the thickness of insulation materials for a PD-free design. A minimized insulation thickness facilitates the inductance reduction and heat transfer.

C. Design Validation

After Stages A and B, the initial bus bar design is ready but still requires validation. Stage C involves simulations to verify the design's performance regarding insulation, inductance, and heat transfer. The design is finalized only when all the metrics meet the designers' requirements. If any of the metrics fail to satisfy the requirements, Stages A and B are iterated until a design that meets all the requirements is realized.

As shown in Fig. 17, each step of the procedure is integrated with one or multiple color bars. These color bars indicate which metrics are affected by each specific step in the design process. As can be seen, some parameters, such as the conductor and insulator thickness, influence different metrics simultaneously, illustrating the interaction between these metrics.

When there is a tradeoff between metrics, designers can prioritize certain metrics and use them as the design boundary conditions based on their targeted applications. For example, during clearance and creepage dimensioning, insulation capability needs to be given higher priority than weight, as violating the minimum clearance or creepage can cause direct failure of bus bar insulation, which is more critical than having a heavier bus bar. In general, design metrics that can directly lead to the malfunction of bus bars, such as thermal and insulation performance, should be prioritized and used as boundary conditions. On the other hand, when there is a less critical tradeoff between metrics, such as weight and inductance, designers can choose different metrics to prioritize based on their specific needs. This also indicates that the proposed approach is not limited to a specific application, inverter topology, or power level. By adjusting the priority of different metrics, the proposed approach can be implemented to optimize bus bar design in various scenarios.

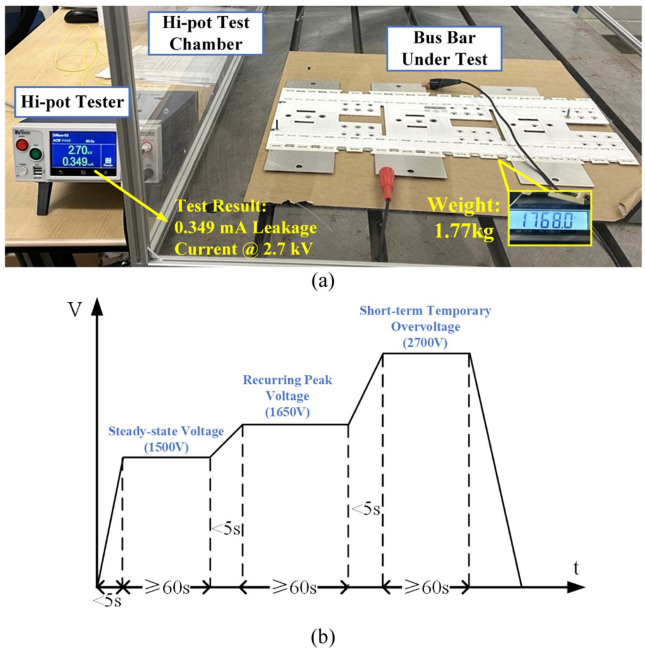


Fig. 18. (a) Bus bar prototype under hi-pot tests. (b) Test procedure specified by IEC 60664-1.

VII. Experimental Characterization

The designed bus bar was prototyped, as shown in Fig. 18(a), to characterize its practical performance. The total mass of the bus bar, including all the standoffs, is 1.77 kg, which is a light weight for high-power converter bus bars and makes the design specifically competitive for aerospace applications. An exploded demonstration of the inverter assembly with the designed bus bar is shown in Fig. 19.

To verify the insulation capability of the designed bus bar, hi-pot tests are carried out in the laboratory. The hi-pot test procedure specified by IEC 60664-1 is shown in Fig. 18(b). Based on the test procedure, the bus bar prototype was tested with voltage up to 2.7-kV ac for 60 s. During the hi-pot tests, no insulation breakdown or flashover occurred, and the leakage current of the bus bar under 2.7-kV test voltage is 0.349 mA, lower than the leakage current limit (10 mA) specified by the standard. Therefore, the insulation capability of the designed bus bar is confirmed. A PD test was also carried out by the bus bar manufacturer, with a 2.2-kV PD inception voltage and 1.75-kV

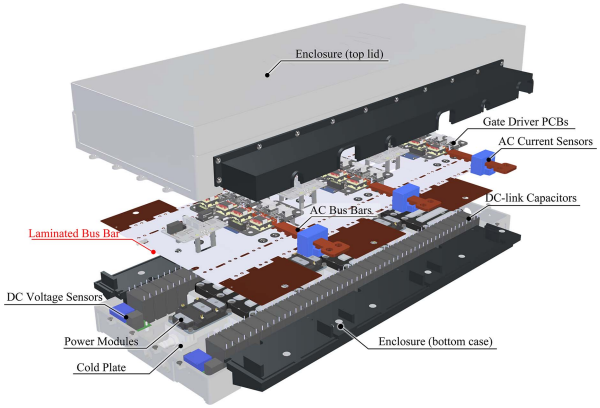
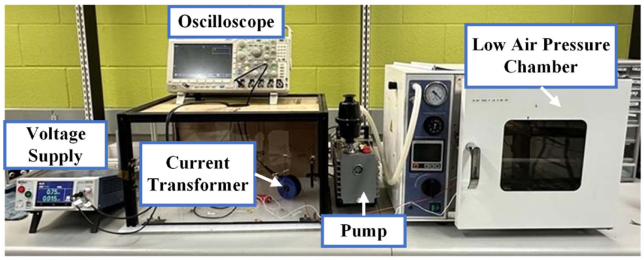
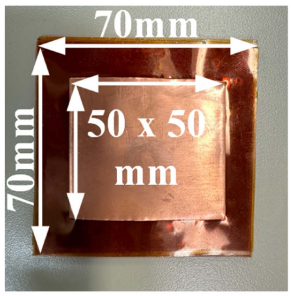


Fig. 19. ANPC inverter assembly with the designed bus bar.



(a)



(b)

Fig. 20. (a) Low-pressure PD test setup. (b) Sample for PD tests.

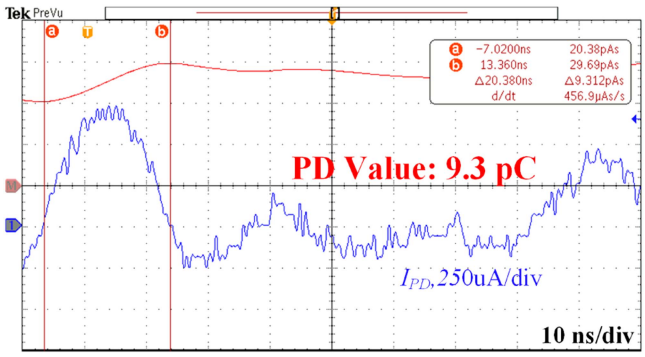
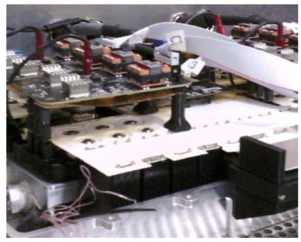
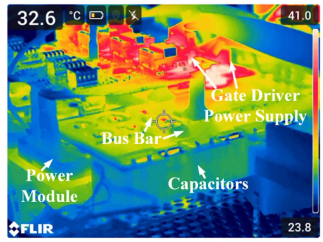


Fig. 21. Measured PD at 750 V.



(a)



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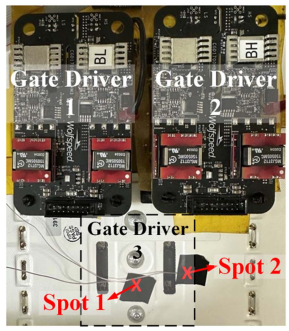

(c)

Fig. 22. (a) Regular and (b) thermal images of the bus bar with 250-kVA output power. (c) Spots of attached thermocouples.

extinction voltage, and measured discharge as 6.4 pC, lower than the specified 10-pC limit. The PD-free design concept is, thus, verified as well.

To further validate the PD performance at low air pressure, another PD test was performed in the laboratory, as shown in Fig. 20(a). During the test, the air pressure inside the chamber is reduced to 0.5 atm by a pump, simulating the pressure at 5000-m altitude. Due to the chamber size limitation, a sample, as shown in Fig. 20(b), was manually made for the test, consisting of two copper sheets and a 0.5-mm-thick Kapton film in between. A high bandwidth current transformer was used to measure the pulse current during the PD tests, and the PD value is then calculated by integrating the measured current. The test result is shown in Fig. 21, where the measured PD is 9.3 pC at 750 V, i.e., the rated voltage between two adjacent copper plates. Given that the sample has multiple imperfections as it was manually assembled, the test result is sufficient to validate the capability of the 0.5-mm-thick insulator in terms of PD-free characteristics.

The thermal performance of the bus bar prototype is validated through a power test on the three-level ANPC inverter. During the power test, the inverter operated continuously at 250-kVA output power until all the components reached the thermal steady state. The tests were conducted at an ambient temperature of 24 °C, with 32.7 °C coolant flowing through the cold plate. An image captured by the thermal camera during the power test is presented in Fig. 22(b), showing the temperature distribution of the bus bar under such conditions. The bus bar exhibited a maximum temperature rise of less than 10 °C from the coolant temperature at 250-kVA power. In addition, two T-type thermocouples from OMEGA were attached to the bus bar top surface during the tests. The measured temperatures are compared with the FEA results obtained under the same operating conditions, as shown in Table VI. It can be found that the measured temperature aligns well with the FEA results, with a maximum error of less than 7%. The possible causes of this error could be the heating of the air between the bus bar and the gate driver, which

TABLE VI
THERMOCOUPLE MEASUREMENT AND FEA RESULTS

Spots	Measured [°C]	FEA [°C]	Error
1	39.54	38.02	4.0%
2	38.07	35.62	6.9%

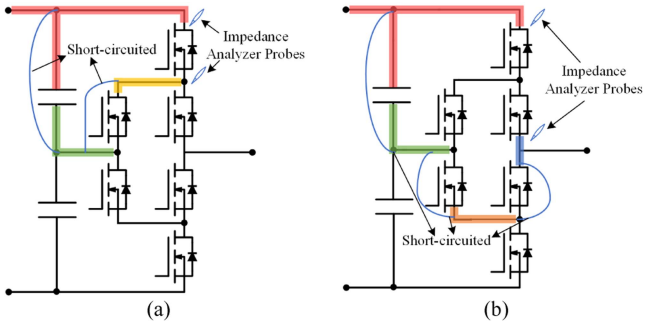

Fig. 23. Demonstrative diagrams of (a) circuit connection for short- and (b) long-loop measurements.

TABLE VII
MAJOR SPECIFICATIONS FOR DPT SETUP AND EQUIPMENT

Parameters	Values/Part numbers
Test voltage	V_{DC} = 1.5 kV
Peak current	$I_{load} \geq$ 700 A
Load inductance	35 μH
Oscilloscope	Tektronix MDO4024C
Voltage probes	Tektronix THDP0200
Current probes	I_{load}: Tektronix TRCP3000 I_{DS}: Tektronix TRCP0600
Signal generator	Plexim RT Box 1

was neglected in the FEA. With a good alignment between the experimental and FEA results, the thermal performance of the bus bar and the accuracy of the FEA model are verified.

The stray inductance of the prototyped bus bar is measured with the Keysight E4990A impedance analyzer. To form a complete commutation loop, the bus bar was shorted by copper foils during the measurement. The additional impedance of the copper foils was then subtracted from the measured raw data. Demonstrative diagrams of the measurement connection for both the short and long commutation loops are shown in Fig. 23.

Fig. 24 shows the measured inductances of all the commutation loops together with the Q3D simulation results. The measured frequency range is 100 kHz to 5 MHz. As can be seen, the measured and simulated inductances of all the loops align well with each other within the measured frequency range, with a maximum error lower than 3 nH at any frequency point. According to the measurement results, at 5 MHz, the average bus bar stray inductances of short and long loops are 11.05 and 21.35 nH, respectively.

To further confirm the loop inductance of the designed bus bar, double-pulse tests (DPTs) are carried out on the designed bus bar and 1-MVA inverter. The DPT setup is shown in Fig. 25.

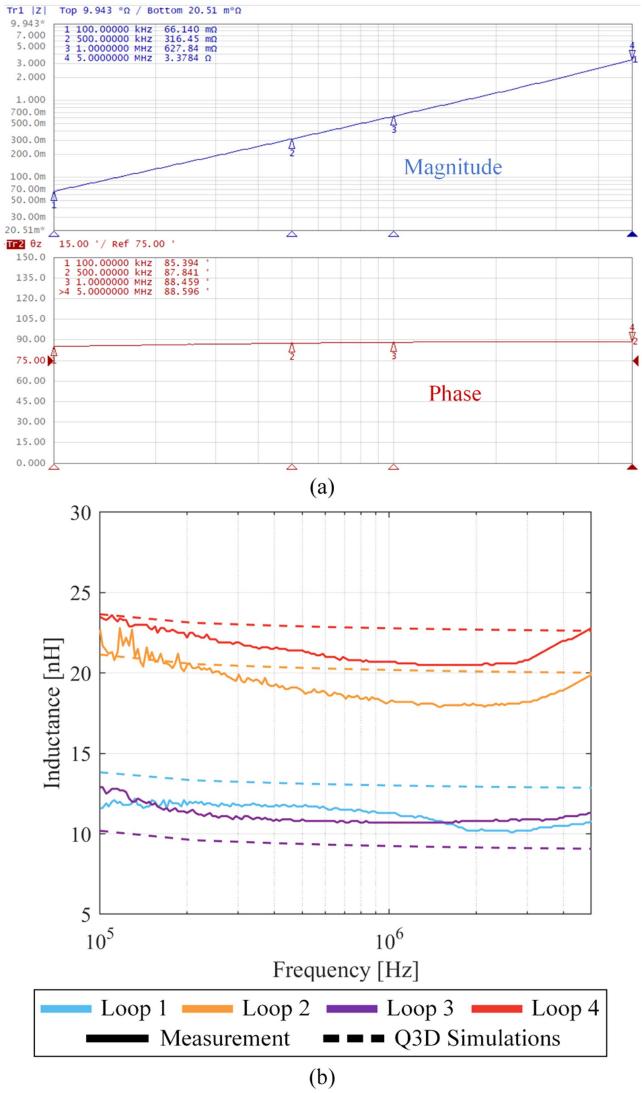

Fig. 24. Bus bar stray inductance measurement results. (a) Measured impedance response (Loop 1, raw data with copper foils). (b) Measured stray inductance (solid lines) of all the commutation loops and corresponding Q3D simulation results (dashed lines).

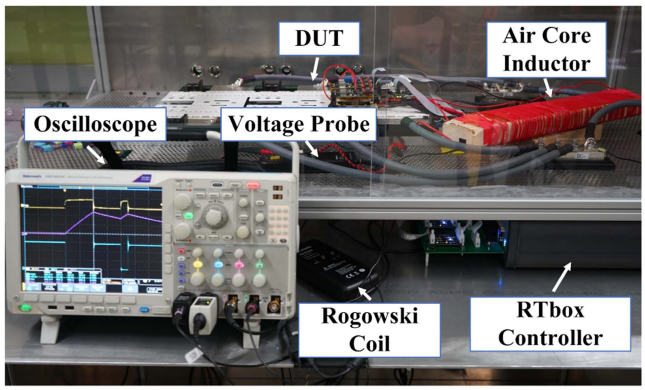

Fig. 25. DPT test setup.

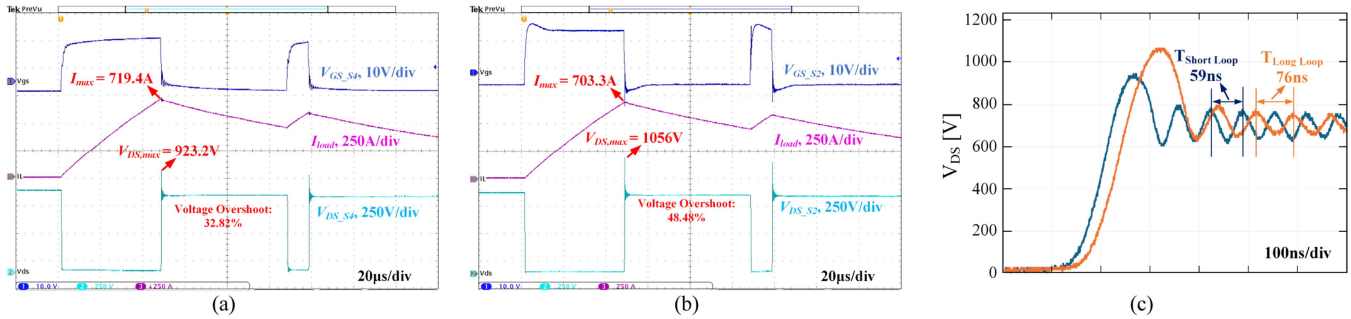

Fig. 26. DPT experimental waveforms. (a) Short loop. (b) Long loop. (c) Zoomed-in $V_{\rm DS}$ waveforms for short and long loops during turn-OFF transient.

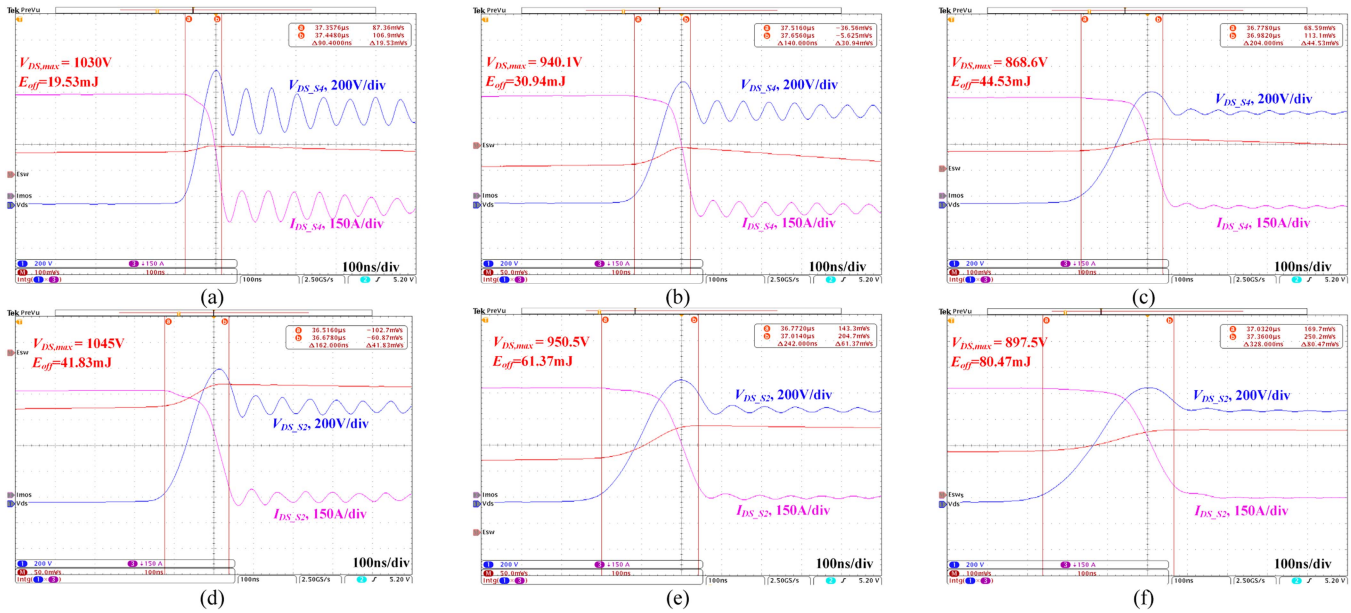

Fig. 27. $V_{\rm DS}$ and $I_{\rm DS}$ waveforms with different turn-OFF gate resistance. (a)–(c) For short loops. (d)–(f) For long loops. (a) $R_g = 1\ \Omega$. (b) $R_g = 2.5\ \Omega$. (c) $R_g = 5\ \Omega$. (d) $R_g = 2.5\ \Omega$. (e) $R_g = 5\ \Omega$. (f) $R_g = 7.5\ \Omega$.

Major specifications of the setup are listed in Table VII. The DPT waveforms of short and long commutation loops are shown in Fig. 26. During the tests, the dc-link voltage reached 1.5 kV, and the current was over 700 A, both meet the specifications of the designed inverter with the maximum output power. The measured voltage spikes for short and long commutation loops are 923.2 and 1051 V, respectively, with the overshoot percentage as 32.83% and 50.07%. It should be noted that the voltage spike values were obtained with a default 2.5-Ω external turn-OFF gate resistance, which will be tuned to minimize the overvoltage later. Fig. 26(c) shows the zoomed-in turn-OFF transient during DPTs. The measured resonant frequencies for short and long commutation loops are 16.95 and 13.16 MHz, respectively. According to the output capacitance value in the power module datasheet, the calculated loop inductances are 29.4 and 48.8 nH. It should be noted that the loop inductances obtained from DPTs include both the stray inductance of the bus bar and other components, i.e., power modules and dc-link capacitors, leading to a difference with the measured inductance in Fig. 24, which contains the bus bars only. If the simulated bus bar inductance is summed with the power module and capacitor stray inductance values from their datasheets, the theoretical loop inductances are 24.1 and 39.3 nH for short and long loops, respectively. Compared to the theoretical loop inductances, the accuracy of DPTs can be confirmed.

The effect of bus bar design and its loop inductance on inverter efficiency is also investigated. Fig. 27 shows the turn-OFF voltage and current waveforms of SiC switches when commutating along short and long loops. During DPTs, the external turn-OFF gate resistance was tuned to observe the switching performance, while the default 5-Ω turn-ON gate resistance remained unchanged. As Fig. 27 shows, since the switching speed slows down, the turn-OFF energy of switches increases with the increased gate resistance, and the voltage spike and the oscillation on $V_{\rm DS}$ are simultaneously damped. Fig. 28 depicts the switching energy and voltage overshoot curves of SiC switches in both the short and long loops. To ensure the safety of switches, a 200-V margin is left for the switch operating

TABLE VIII
SUMMARY AND COMPARISON OF ANPC BUS BAR DESIGNS

Ref.	Proposed	[3]	[12]	[13], [21]	[15]	[28]	[39]
Power (kVA)	1000	1000	750	250	3300	500	200
Voltage (kV)	1.5	2.4	2	1.1	5.6	1	1.2
Short loop (nH)	29.4	N/A	78	62.5	158	6.5	55
Long loop (nH)	48.8	115	208	102.9	231	17.5	135
PD-free?	Yes	No	No	No	No	Yes	No
Temperature rise	<10 °C (250 kVA)	N/A	N/A	10 °C (10% rated power)	N/A	N/A	N/A
Weight	1.77	8.8	N/A	N/A	N/A	3.9	N/A

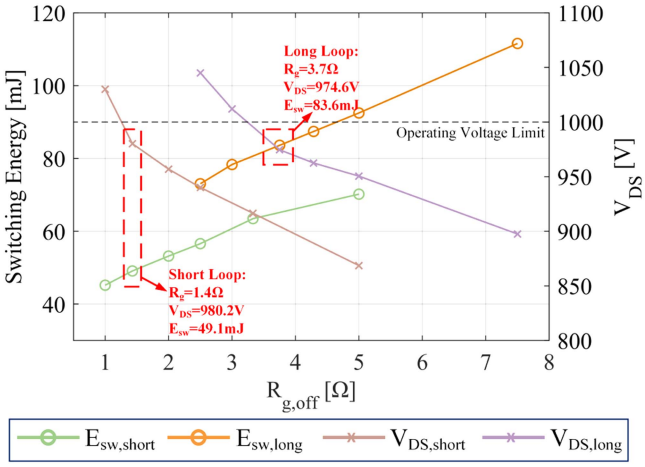

Fig. 28. Curves of measured switching energy and voltage overshoot with different R_g values.

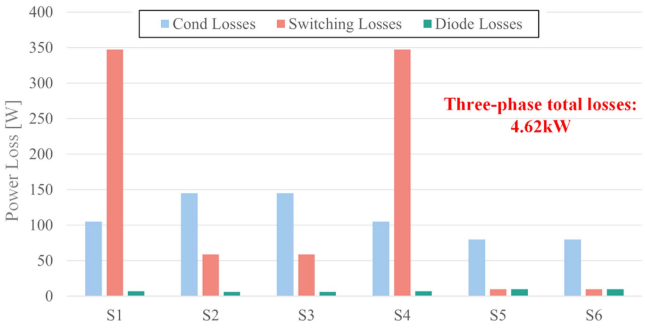

Fig. 29. Loss breakdown of switches in one phase leg under the half-load condition.

voltage; therefore, 1000 V is set as the limit. Based on this boundary condition, 1.4- and 3.7-Ω turn-OFF gate resistances are selected for short and long loops, respectively. Accordingly, the total switch energy will be 49.1 and 83.6 mJ. With the same modulation strategy as in [39], under half-load conditions of the 1-MVA inverter, the losses on the outer (S_1, S_4) and inner (S_2, S_3) phase-leg switches will approximately be 460 and 210 W, respectively, and the inverter's total loss will be 4.62 kW. A detailed loss breakdown is provided in Fig. 29. With the measured switching losses from DPTs, the expected efficiency of the designed inverter under half-load operation reaches 98.97%.

Finally, Table VIII summarizes the major features of the bus bars for high-power ANPCs designed in previous research. Compared to other designs, the bus bar designed in this article shows an overall superior performance in terms of loop inductance, insulation, heat transfer, and weight.

VIII. CONCLUSION

This article presents a comprehensive design approach for the bus bar of a 1-MVA three-level ANPC inverter in aerospace applications. With the proposed design methodology as a guideline, the performance of bus bars can be globally improved in terms of loop inductance, insulation capability, heat transfer, and weight. Through optimization efforts, the designed bus bar achieves a PD-free design, less than 10 °C temperature rise at 250-kVA power, 29.4- and 48.8-nH inductances for short and long commutation loops, and a total mass of only 1.77 kg. These features make the designed bus bar competitive for electric aircraft propulsion applications.

Being verified by DPTs, the voltage overshoot on SiC switches can be controlled under 1000 V when using 1.4- and 3.7-Ω gate resistances for short and long loops. With the low switching energy of SiC MOSFETs, the estimated efficiency of the 1-MVA ANPC inverter under half-load conditions reaches 98.97%, which is promising for MVA-level inverters.

At the end of this article, the introduced rules of bus bar design are summarized and listed as follows.

1) For a multilayer laminated bus bar, the conductor plate shared by most commutation loops should be selected as the returning path, and its surface area should be maximized to minimize self-inductance.
2) The thickness and width of each conductor plate should be maintained at reasonable values so that the current density on the bus bar is lower than the 5-A/mm^2 empirical limit.
3) Clearance and creepage dimensioning should follow the specified standards, with a correction factor for altitude considered. In a multiobjective design process, clearance and creepage should be used as boundary conditions and should not be violated.
4) The thickness of the insulation layer should be minimized. The minimum thickness can be determined based on PD-free design requirement.
5) When considering bus bar heat transfer, the effect of power modules and their cooling systems on bus bar temperature should be taken into account.

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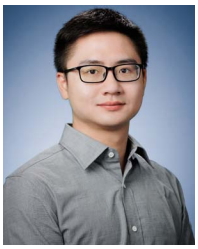

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