Compensating Frequency Converter Nonlinearity

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***Abstract*—Voltage and/or current of multiphase systems are usually controlled using frequency converters (FCs). Typically, these FCs consist of several half bridges and, due to their working principle, their output voltage will depend on the output current nonlinearly. Many well known compensation methods (CMs) rely on the assumption that the current is nearly constant during one switching cycle. However, with decreasing load inductances this assumption may not be fulfilled and therefore these methods may not succeed in achieving full compensation. This contribution provides a CM, which takes the so-called ripple current into account and is therefore especially useful when dealing with small load inductances.**

***Index Terms*—Compensation, dead time, distortion, half bridge model, IGBT, interlock time, nonlinearity.**

I. Introduction

FREQUENCY converters (FC) are widely used since several decades, thus the phenomenon of FC nonlinearity is already widely known. This nonlinear behavior causes problems in many areas including the fields of grid tied converters [1], [2], [3] and variable frequency drives [4], [5], [6].

One group of methods assumes that the current during one switching period is nearly constant. Jeong and Park [7] showed a method which only uses the sign of the load's current as an input quantity. Leggate and Kerkman [8] explained a pulse based compensation method (CM), expressed in the stator's reference frame, which also only depends on the sign of the load's current. Ben-Brahim [9] basically used the same method as [7], however, it tackles the behavior around zero current (called zero-crossing phenomenon) beneficially. Unlike the methods above, Zhao et al. [10] showed a compensation strategy that is expressed in the rotor's reference frame (d,q-coordinates) and tries to minimize the load currents harmonics. Park and Sul [11], [12] used trapezoidal voltages to compensate for the FC's nonlinearity. This compensation scheme only tunes one parameter, and thus is both easy to implement and easy to tune. Later, Wang et al. [13] extended this method by tuning two parameters, yielding a better compensation performance. All these methods are based on the assumption that the ripple current is negligibly small.

Another group of methods makes use of more sophisticated compensation strategies [14], [15], [16], [17]. The usage of repetitive control is shown in [14], [15], [16]. Although these methods provide very good results in stationary operation, they are disadvantageous in highly dynamic load situations, i.e., when the FC's output voltage or frequency changes quickly.

Tang and Akin [17] demonstrated a method based on an online adapting least mean squares (LMS) algorithm. However, it is very difficult to ensure that these self-learning methods are stable in every working condition.

Yang et al. [15] explained a method, which uses resonant controllers. Since resonant controllers focus on one specific frequency, usually several of them are connected in parallel [18]. This is necessary to achieve tracking of the fundamental frequency component while ensuring that the amplitudes of the harmonic frequencies are tending toward zero.

Ye et al. [19] provided a CM which adds harmonics to the output voltages until the measured load currents are sinusoidal. However, the authors point out that this method has limitations in case of load changes.

The method described in [20] makes use of additional sensing hardware. By direct integration of the FC's output voltage the authors could achieve a high grade of compensation. However, this method comes with the disadvantage of requiring additional hardware. Buchta and Bartik [21] and Kim et al. [22] have chosen a completely different approach by using disturbance observers to compensate for the FC's nonlinearity.

With increasing computational power another group of methods, which directly take the ripple current into account, were investigated. The computation of the ripple current can be accomplished as shown in [23], which makes use of several zones in the switching cycle and a single equivalent circuit. Depending on the switching order, the correct zones have to be chosen and lumped. This method was used afterward in [24] to obtain a CM which takes the ripple current into account. Around the same time also Futó et al. [25] came up with a relatively similar method.

Shen and Jiang [26], Schuetz et al. [27], Mannen and Fujita [28] also describe methods based on the idea of ripple current prediction. Shen and Jiang [26] neglect the zero current clamping phenomenon and thereby obtain quite simple equations for the compensation voltage. In contrast to [26], Schuetz et al. [27] take the zero current clamping phenomenon into account by using an adapted saturation function while Shen et al. [24] tackle this

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phenomenon using a lookup table and Mannen and Fujita [28] compute the output voltage error using three different models.

Once the current which shall be used for the compensation task is obtained, Zhang and Xu [29] provided a detailed mathematical description on how to compute the output voltage error. If the sampling frequency is very high compared to the switching frequency, it is possible to measure the output voltage error as well as the current around the moment of switching during operation, this method is described in [30].

This article's main contribution is a novel method for compensating the nonlinearity of FCs based on a lookup table. The proposed method takes the ripple current as well as the zero current clamping phenomenon into account. By feeding the current at the moment of switching into a 2-D lookup table, which is parametrized using a half bridge model, a high grade of compensation is achieved. The usage of a half bridge model to parametrize the lookup table introduces two major advantages compared with the state of the art.

1) A 2-D lookup table can be used, which not only maps the current during switching (first dimension), but also its slope (second dimension). This second dimension is especially important in the case of small inductances which lead to high ripple currents.
2) Instead of storing a voltage error $\Delta\bar{u}_X$, a correction voltage Θu_X which leads to $\Delta\bar{u}_X = 0\,\mathrm{V}$, is stored in the lookup table. Since an optimization problem has to be solved to obtain Θu_X, this is exclusively possible by using a half bridge model.

The rest of this article is organized as follows. Section II clarifies the used notation. Section III provides a brief comparison of the proposed CM with other state of the art methods. Afterward, Section IV shows the general setup, i.e., a FC interconnected with a load unit. This section also explains the impact of the interlock time (which is often referred to as dead time) on the output voltage. In Section V, the proposed CM is explained. After introducing the half bridge model, the generation of the lookup table is described. Subsequently, a ripple current prediction method is derived. Section VI provides a brief overview of the experimental setup. Afterward Section VII compares the proposed method with other state of the art CMs and demonstrates its effectiveness and real-time performance by showing experimental results. Finally, Section VIII concludes this article.

II. Notation

Voltages are denoted by u, currents are denoted by i. Small letters indicate that these quantities are usually interpreted as functions of time, e.g., $u = u(t),\ t \in \mathbb{R}$. Averaged values are indicated by a bar above and averaging is done over one discretization time step T_D, i.e., $\overline{u}_U = \frac{1}{T_D}\int_{t_0}^{t_0+T_D} u_U(\tau)\mathrm{d}\tau$. Voltages with a removed zero component are indicated by a superscripted star, i.e., u_U^*. Time intervals are denoted by a capital T with a subscript and specific points in time, in contrast, are denoted by a lowercase t with a subscript. The three physical phases are denoted by U, V, and W, whereas the letters X, Y, and Z are used to point out that a relation is valid for any phase. The switches are denoted by Q. Table I gives an overview of the symbols used in this article as well as their units and the parameter values obtained in the experiment.

TABLE I
Symbol, Unit, and Parameter Overview

Symbol	Description	Value/Unit
T_D	discretization time (=half switching cycle)	50 µs
T_V	interlock time	≈ 1.4 µs
U_S	DC link voltage (=source voltage)	700 V
R	resistance	≈1 mΩ
$\tilde{R}$	scaled resistance	≈1.5 mΩ
L	inductance	25 µH
$\tilde{L}$	scaled inductance	37.5 µH
i_X	current in phase X	A
u_X	output voltage of phase X referred to GND	V
$\overline{u}_X$	averaged output voltage of phase X referred to GND	V
$\Delta\overline{u}_X$	averaged output voltage error	V
Θu_X	output voltage correction	V
u_X^*	zero-component-free voltage of phase X	V
u_X^{**}	voltage computed by using squared duty cycles of phase X	V
$u_{G,X}$	counter voltage of phase X	V
$u_{G,X}^*$	zero-component-free counter voltage of phase X	V
δ_X^*	difference between output and counter voltage of phase X	V
δ_X^{**}	difference between u_X^{**} and counter voltage of phase X	V
d_X	duty cycle for phase X	-
Δd_X	duty cycle error for phase X	-
Θd_X	duty cycle correction for phase X	-
$\{U, V, W\}$	physical phases	-
X	arbitrary phase $\in \{U, V, W\}$	-
Y	other arbitrary phase $\in \{U, V, W\} \setminus \{X\}$	-
Z	remaining phase $\in \{U, V, W\} \setminus \{X, Y\}$	-

III. Comparison of CMs

Because there are a lot of different CMs available in the literature, Table II gives a brief overview of some selected methods. The methods written in *italic* font are used for comparison in Section VI.

IV. Working Principle

A. Setup

The setup is shown in Fig. 1. The FC, shown in the blue dashed box, consists of three half bridges and each half bridge consists of two switches. The upper switches (Q_1, Q_3, and Q_5) are referred to as high side switches, the lower switches (Q_2, Q_4, and Q_6) are referred to as low side switches. The voltage of every phase X ($X \in \{U, V, W\}$) to GND is referred to as u_X, the phase currents are referred to as i_X.

The load unit, shown in the red dashed box, consists of a resistor with the resistance R, an inductor with the inductance L, and a voltage source providing the voltage $u_{G,X}$. Please note that the voltage $u_{G,X}$ is not assumed to be constant and/or independent of the current i_X. Therefore, this general load unit

TABLE II
OVERVIEW OF CMS

Method #	Reference and Year	Description	Advantages	Disadvantages
CM 1	[7], 1991	adds $\Delta U = \text{sign}(i) U_{\text{Comp}}$	very simple	tends to overcompensation
CM 2	[29], 2014	adds precomputed $\Delta U = f(i)$	de-facto state of the art for industrial FC	-
CM 3	[24], 2020	adds precomputed $\Delta U = f(i_{\text{Sw}})$	uses the current at the moment of switching → Ripple prediction	-
CM 4	[30], 2016	adds measured $\Delta U = f(i)$	no parameter tuning required	high speed measurements and high computational power necessary
CM 5	[11],[12], 2012,2014	uses trapezoidal voltages	only need to tune one parameter	-
CM 5b	[13], 2022	further development of CM 5	better compensation performance than CM 5	additional parameters to tune
CM 6	[14]-[16], 2004,2018,2017	repetitive control	high grade of compensation no parameter tuning	disadvantageous in highly dynamic load situations
CM 7	[15],[18] 2008,2018	resonant control	easy controller structure	one controller per frequency required
CM 8	[20], 2020	uses additional sensing hardware to obtain the converters output voltage	high grade of compensation	additional hardware required

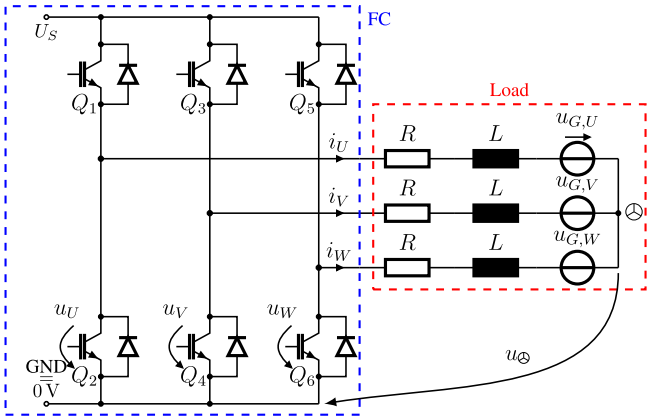

Fig. 1. Schematic of a FC interconnected with a load unit.

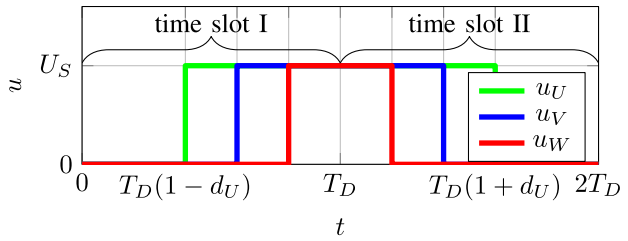

Fig. 2. Output voltages u_U, u_V, and u_W of the FC when $d_U \geq d_V \geq d_W$.

can represent loads such as induction machines, synchronous drives, and three phase filters. However, it is assumed that the load is balanced and its star-point (denoted ✇) is floating.

B. Frequency Converter

Fig. 2 shows a pulsewidth-modulated (PWM) sequence. Because a centered PWM mode is used, two updates of the demanded output voltage per PWM cycle are possible: the first at $t = 0\,\text{s}$ and the second at T_D. Therefore, the switching period with the length $2T_D$ needs to be separated into two subintervals. The subinterval $[0, T_D)$ contains all the rising edges of the output voltage and is referred to as time slot I. Consequently the subinterval $[T_D, 2T_D)$ contains all the falling edges and is referred to as time slot II.

For reasons of conciseness and consistency, all derivations in this document are shown for time slot I only. The derivations for all results in time slot II are analogous to those in time slot I. These results are shown in Table VII.

In order to generate the demanded output voltage shown in Fig. 2, by using the converter presented in Fig. 1, either the high side switch or the low side switch has to conduct. To guarantee short-circuit-free operation, a short time between each transition, the so-called interlock time T_V, is inserted. This interlock time guarantees that opening the desired switch is completed before the complementary switch can begin to conduct. During this interlock time, the output voltage u_X is not uniquely defined by the half bridge. However, the freewheeling diodes, which every half bridge contains, clamp the output voltage u_X. Therefore $u_X \in [-u_D, U_S + u_D]$, where u_D denotes the diodes forward voltage, holds always.

C. Reasons for Nonlinear Output Voltage Behavior

The voltage u_X was measured during switching at several currents to gain further knowledge about the causes of nonlinear behavior. Fig. 3 shows some representative measurements. It can be seen that the output voltage u_X, plotted in blue, depends on the corresponding current i_X. Although this figure only shows the critical region around the interlock time, the mean voltage error $\Delta\bar{u}_X$ over one time interval T_D is always in the following intervals:

$$\Delta\bar{u}_X \in \left[-\frac{T_V}{T_D}U_S, 0\right] = [-19.6\,\text{V}, 0\,\text{V}] \text{ in time slot I, or} \tag{1a}$$

$$\Delta\bar{u}_X \in \left[0, +\frac{T_V}{T_D}U_S\right] = [0\,\text{V}, +19.6\,\text{V}] \text{ in time slot II.} \tag{1b}$$

A detailed derivation of (1) is given in [31]. Since Urasaki et al. [31] do not consider the two time slots separately, $\Delta\bar{u}_X \in [-\frac{T_V}{2T_D}U_S, \frac{T_V}{2T_D}U_S]$ is obtained in that work. As typical voltage drops on semiconductors are in the range from 0.5 V to 3 V, the voltage error introduced by (1) is considered as the main effect of nonlinear FC behavior in this article.

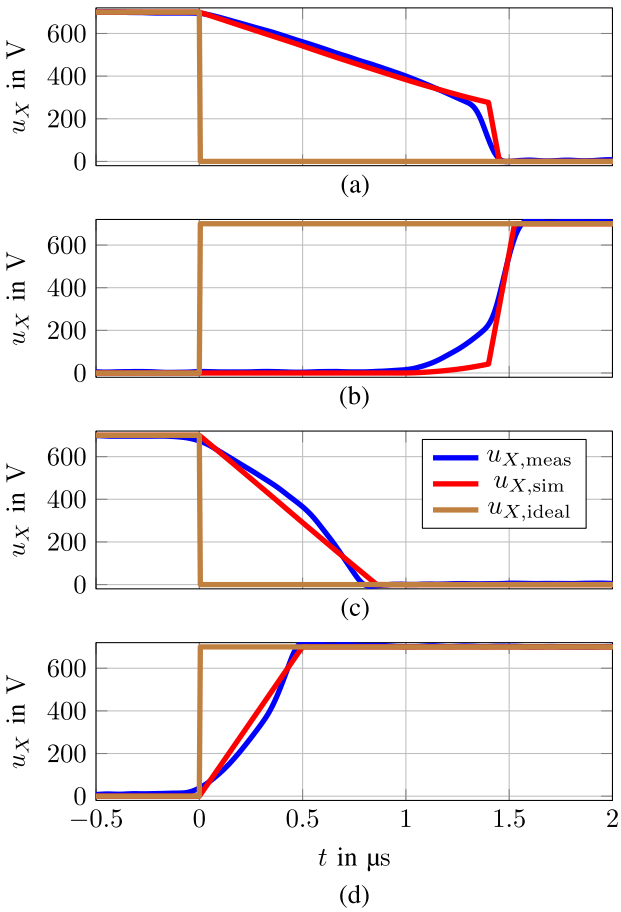

Fig. 3. Measured voltage u_X, depicted in blue, around the interlock time. A simulation result of the proposed half bridge model is shown in red. (a) $i_X \approx 10\,\text{A}$. (b) $i_X \approx 0\ A$. (c) $i_X \approx 30\,\text{A}$. (d) $i_X \approx -100\,\text{A}$.

For reasons of space also a simulation result of a half bridge model is shown in Fig. 3, plotted in red. This simulation model is explained in Section V-A, the simulation setup is discussed in Section V-B.

D. Load Unit Model

This section covers the description of the load unit shown in the red dashed box in Fig. 1. By using the voltage from the load's star point (denoted $u_{\text{⏢}}$) to GND and Kirchhoff's loop rule, the following equation is derived:

$$u_X = i_X R + \frac{\mathrm{d}i_X}{\mathrm{d}t} L + u_{G,X} + u_{\text{⏢}}. \tag{2}$$

Using Kirchhoff's node law in the load's star point, i.e., $i_U + i_V + i_W = 0\,\text{A}$, summing (2) over all phases leads to the star point voltage $u_{\text{⏢}}$, which is given by

$$u_{\text{⏢}} = \frac{1}{3}(u_X - u_{G,X} + u_Y - u_{G,Y} + u_Z - u_{G,Z}). \tag{3}$$

Reinserting (3) into (2) yields the finally used representation

$$\begin{aligned}\frac{\mathrm{d}i_X}{\mathrm{d}t} = &-\frac{R}{L} i_X + \frac{1}{3L}(2u_X - 2u_{G,X} + u_{G,Y} \\ &- u_Y + u_{G,Z} - u_Z).\end{aligned} \tag{4}$$

This equation is also obtained, when the output and counter voltages are used only and their corresponding mean values are subtracted, i.e.,

$$\frac{\mathrm{d}i_X}{\mathrm{d}t} = -\frac{R}{L} i_X + \frac{1}{L}[u_X - u_0 - (u_{G,X} - u_{G,0})] \tag{5}$$

where their mean values u_0 and $u_{G,0}$ are given by $u_0 = \frac{1}{3}\sum_{X\in\{U,V,W\}} u_X$ and $u_{G,0} = \frac{1}{3}\sum_{X\in\{U,V,W\}} u_{G,X}$, respectively. Therefore, (5) shows that the mean component of the output and counter voltages do not lead to any current flow. This is a direct consequence of the load's floating star point. Duesterhoeft et al. [32] provided a more general view of this topic. Following the notation used in this reference, the mean output voltage u_0 is referred to as the zero component of the voltage triple $\{u_U, u_V, u_W\}$. Consequently, the mean counter voltage $u_{G,0}$ is referred to as the zero component of the voltage triple $\{u_{G,U}, u_{G,V}, u_{G,W}\}$. Since these zero components do not lead to any current flow, a transformation which removes these zero components is used. However, it is worth mentioning that this transformation is applied to the averaged values $\{\overline{u}_U, \overline{u}_V, \overline{u}_W\}$ and $\{\overline{u}_{G,U}, \overline{u}_{G,V}, \overline{u}_{G,W}\}$, which are obtained by computing the mean over one discretization period T_D. After defining the transformation matrix $\mathbf{\Lambda}$ with

$$\mathbf{\Lambda} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{6}$$

the zero-component-free output voltages are given by

$$\begin{bmatrix} u_U^* & u_V^* & u_W^* \end{bmatrix}^T = \mathbf{\Lambda} \begin{bmatrix} \overline{u}_U & \overline{u}_V & \overline{u}_W \end{bmatrix}^T. \tag{7}$$

Applying the same transformation matrix $\mathbf{\Lambda}$ to the counter voltages $\overline{u}_{G,U}$, $\overline{u}_{G,V}$, and $\overline{u}_{G,W}$ yields zero-component-free counter voltages, which are computed using

$$\begin{bmatrix} u_{G,U}^* & u_{G,V}^* & u_{G,W}^* \end{bmatrix}^T = \mathbf{\Lambda} \begin{bmatrix} \overline{u}_{G,U} & \overline{u}_{G,V} & \overline{u}_{G,W} \end{bmatrix}^T. \tag{8}$$

Considering that the mean output voltage $\overline{u}_X$ is given by $\overline{u}_X = U_S d_X$, (7) can be expressed by direct use of duty cycles

$$\begin{bmatrix} u_U^* & u_V^* & u_W^* \end{bmatrix}^T = U_S \mathbf{\Lambda} \begin{bmatrix} d_U & d_V & d_W \end{bmatrix}^T. \tag{9}$$

Since $\boldsymbol{\rho}^T = [1 \quad 1 \quad 1]$ is a left eigenvector corresponding to the eigenvalue $\lambda_1 = 0$ of $\mathbf{\Lambda}$, these zero-component-free voltages have the property that their sum always equals zero

$$u_U^* + u_V^* + u_W^* = 0 \tag{10}$$

$$u_{G,U}^* + u_{G,V}^* + u_{G,W}^* = 0. \tag{11}$$

This property will be used extensively in Section V-E.

V. Compensation Approach

To compensate for the nonlinearity induced by the FC, a lookup table approach is proposed. As shown in Section IV-C, the voltage u_X mainly depends on the current i_X during the interlock time T_V. Since the current's evolution on an interval with length T_V cannot be used as a lookup table breakpoint, the current i_X at the beginning of the interlock time is used

instead. In the ongoing work, this current will be referred to as the current at the moment of switching, i.e., $i_X(T_D(1-d_X))$. In order to tackle the loss of information induced by retarding $i_X(t)$ where $t \in [T_D(1-d_X), T_D(1-d_X)+T_V)$ to $i_X(T_D(1-d_X))$, a second lookup table dimension is used. Section V-C will show that using a quantity proportional to the slope of $i_X(T_D(1-d_X))$ is a reasonable choice.

The lookup table's output quantity is an additive duty cycle correction Θd_X which is computed by using an additive voltage correction Θu_X, i.e., $\Theta d_X = \frac{\Theta u_X}{U_S}$. Therefore, the compensation idea is that after adding this duty cycle correction Θd_X to the desired duty cycle d_X, the nonlinear behavior disappears, i.e., the voltage error $\Delta\bar{u}_X = 0\,\mathrm{V}$. Unfortunately, this duty cycle correction Θd_X cannot be measured directly.

Therefore, a half bridge model, which allows the computation of this duty cycle correction, is presented in Section V-A. The generation of the lookup table is explained subsequently in Section V-C. The current i_X at the moment of switching is needed as recently explained; this topic is tackled in Section V-E. Subsequently, Section V-G briefly discusses how to use this CM and shows experimental results.

A. Half Bridge Model

As already mentioned in Section IV-C, the output voltage u_X depends on the corresponding phase current i_X during the interlock time T_V. Higher currents lead to higher gradients of the output voltage; this is commonly interpreted in the literature as a capacitive behavior, see [33]. The capacitance, which is often also referred to as parasitic capacitance, consists of the sum of the capacitances of the high side switch, the low side switch and the two freewheeling diodes' capacitances contained in every half bridge. At first it should be mentioned that this capacitive behavior is only detectable around the interlock time. Second it should be stated that this is not an ideal capacitor, but rather a result of the finitely fast processes occurring inside the switches and diodes. Therefore, direct measurement of this capacitance is not possible. In order to tackle the nonlinear behavior induced by the interlock time using a lookup table approach, it is necessary to develop a half bridge model which gives special attention to the behavior in this period. Based on (1) in Section IV-C, it was shown that voltage drops on all semiconductors are comparatively small. Voltage drops are thus neglected in this half bridge model.

Further, the resistance of all switches and diodes is assumed to be equal to $0\,\Omega$. Due to the capacitive behavior mentioned above, the voltage on the capacitance u_X is chosen as a state variable. For modeling the state of the half bridges, a current source providing the current $i_{S,X}$ is used. This current is set to $i_{S,X,\mathrm{on}}$ if the high side switch should conduct, $i_{S,X,\mathrm{off}}$ if the low side switch should conduct or to zero if no switch should conduct. The parameters $i_{S,X,\mathrm{on}}$ and $i_{S,X,\mathrm{off}}$ are constant and need to be determined from experimental data. The half bridge model consists of one integrator and is given by

$$\frac{\mathrm{d}u_X}{\mathrm{d}t} = \frac{1}{C}(i_{S,X} - i_X). \tag{12}$$

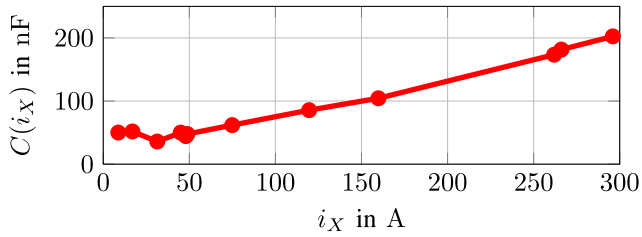

Fig. 4. Measurement of the capacitance for one half bridge.

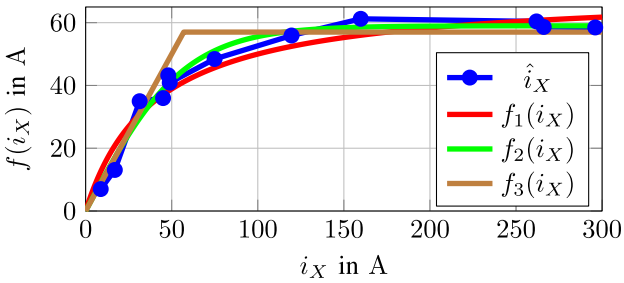

Fig. 5. Comparison of different scaling functions $f(i_X)$.

Because the voltage u_X can never exceed the source voltage U_S, the restriction $0 \le u_X \le U_S$ has to hold at all times.[1]

To find a suitable value for the capacitance, several measurements were performed and analyzed. It turns out that when using the system description shown in (12), a nonconstant capacitance that is a function of the current $C = f(i_X)$ is needed. Fig. 4 shows this capacitance, which is computed by $C(i_X) \approx i_X \frac{\Delta t}{\Delta u_X}$. The behavior observed in Fig. 4 is plausible since the capacitance C represents all processes occurring during switching. In [34, pp. 560–575], a detailed insight on the switching process of IGBTs is given. Schröder [34] also explains that the time for charging the capacitance C remains almost constant above a certain current, which depends on the specific IGBT and the gate drive circuit. Starting with this certain current, the capacitance needs to increase with current in order to keep the slope of the output voltage constant. As a consequence, (12) would need to be expanded by the derivative[2] $\frac{\mathrm{d}C}{\mathrm{d}t}$, as this simple structure only holds when the capacitance C is constant.

Another approach is used to maintain the description given in (12). As mentioned at the beginning of this section, the influence of this parasitic capacitance is only relevant during the interlock time. Because the control current $i_{S,X}$ is always zero during the interlock time, it is possible to obtain the same model behavior when using a scaled version $f(i_X)$ of the current i_X instead of scaling the capacitance C. A suitable scaling function $f = f(i_X)$ is needed to obtain the observed behavior. Several functions were investigated for this purpose, some of these functions are shown in Fig. 5 and are given by

$$f_1(i_X) = \frac{\alpha_1 i_X}{\alpha_2 + |i_X|} \tag{13a}$$

$$f_2(i_X) = \beta_1 \tanh\left(\frac{i_X}{\beta_2}\right) \tag{13b}$$

[1] The diode's forward voltage and resistance is neglected.

[2] With the charge $q = Cu$ one obtains $\frac{\mathrm{d}q}{\mathrm{d}t} = i = \frac{\mathrm{d}Cu}{\mathrm{d}t} = u\frac{\mathrm{d}C}{\mathrm{d}t} + C\frac{\mathrm{d}u}{\mathrm{d}t}$.

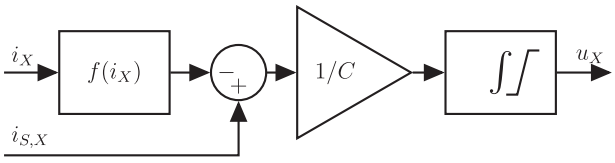

Fig. 6. Half bridge model – mathematical view.

$$f_3(i_X) = \begin{cases} i_{X,\max} & \text{if } i_{X,\max} < i_X \\ i_X & \text{if } i_{X,\min} \leq i_X \leq i_{X,\max} \\ i_{X,\min} & \text{if } i_X < i_{X,\min} \end{cases}. \tag{13c}$$

In order to find the parameters of these scaling functions the following approach is used: From the measurement, a virtual current $\hat{i}_X$ is computed by using $\hat{i}_X = C\frac{\Delta u_X}{\Delta t}$ with the constant capacitance C. Please note that $\hat{i}_X$ is a function of i_X because the measurements were performed at several different currents. This virtual current $\hat{i}_X$ is shown in Fig. 5, plotted in blue. The parameters of the scaling functions $f_1(i_X)$ to $f_3(i_X)$ are fitted in such a way that the scaling functions match with $\hat{i}_X$. To obtain the plots shown in Fig. 5, the following parameters were used:

$$\alpha_1 = 70, \qquad \alpha_2 = 40\,\text{A} \tag{14a}$$

$$\beta_1 = 60\,\text{A}, \qquad \beta_2 = 57\,\text{A} \tag{14b}$$

$$i_{X,\max} = 50\,\text{A}, \qquad i_{X,\min} = -i_{X,\max}. \tag{14c}$$

Putting together (12) and a scaling function leads to the representation shown in Fig. 6. From Fig. 6, it can be seen that $i_{S,X,\text{off}} < f(i_X) < i_{S,X,\text{on}}$ must always hold in order to guarantee controllability of this half bridge model. Otherwise, switching the half bridge model on and/or off with the control current $i_{S,X}$ is not possible because $i_{S,X}$ is dominated by the scaled load current $f(i_X)$.

The remaining parameters, $i_{S,X,\text{on}}$, $i_{S,X,\text{off}}$, and C, are also found using experimental data and given by: $i_{S,X,\text{on}} = 200\,\text{A}$, $i_{S,X,\text{off}} = -i_{S,X,\text{on}}$ and $C = 40\,\text{nF}$.

B. Half Bridge Model: Simulation Setup and Results

Some simulation results have already been shown initially in Fig. 3 and the simulation setup is discussed now. The measured current i_U is used as the half bridge model's input quantity, denoted i_X in Fig. 6.

The output quantity of Fig. 6 is denoted u_X and also plotted in Fig. 3, in red. Fig. 3 also shows that the presented half bridge model matches the measured overall behavior relatively well, even though there are slight deviations visible in Fig. 3(b).

C. Generating the Lookup Table

The goal is to find a universal lookup table, which can be used for every phase and also for every switching sequence; i.e., phase U is switching before phase V, phase V is switching before phase W or in any other order. However, as the dimension of the lookup table should be kept low, the case of simultaneous phase switching is not considered.

This section shows that then it is sufficient to perform the analysis in a single phase equivalent network. This single phase

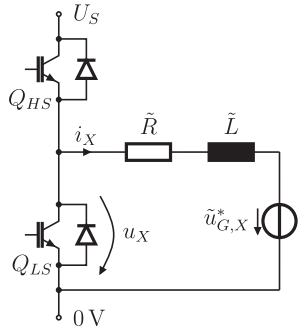

Fig. 7. Single phase equivalent circuit for generating the lookup table.

TABLE III
COUNTER VOLTAGE $\tilde{u}^*_{G,X}$ FOR DIFFERENT SWITCHING ORDERS

Order	$\tilde{u}^*_{G,U}$	$\tilde{u}^*_{G,V}$	$\tilde{u}^*_{G,W}$
$d_U \geq d_V \geq d_W$	$\frac{0}{2}U_S + \frac{3}{2}u^*_{G,U}$	$\frac{1}{2}U_S + \frac{3}{2}u^*_{G,V}$	$\frac{2}{2}U_S + \frac{3}{2}u^*_{G,W}$
$d_U \geq d_W \geq d_V$	$\frac{0}{2}U_S + \frac{3}{2}u^*_{G,U}$	$\frac{2}{2}U_S + \frac{3}{2}u^*_{G,V}$	$\frac{1}{2}U_S + \frac{3}{2}u^*_{G,W}$
$d_V \geq d_U \geq d_W$	$\frac{1}{2}U_S + \frac{3}{2}u^*_{G,U}$	$\frac{0}{2}U_S + \frac{3}{2}u^*_{G,V}$	$\frac{2}{2}U_S + \frac{3}{2}u^*_{G,W}$
$d_V \geq d_W \geq d_U$	$\frac{2}{2}U_S + \frac{3}{2}u^*_{G,U}$	$\frac{0}{2}U_S + \frac{3}{2}u^*_{G,V}$	$\frac{1}{2}U_S + \frac{3}{2}u^*_{G,W}$
$d_W \geq d_U \geq d_V$	$\frac{1}{2}U_S + \frac{3}{2}u^*_{G,U}$	$\frac{2}{2}U_S + \frac{3}{2}u^*_{G,V}$	$\frac{0}{2}U_S + \frac{3}{2}u^*_{G,W}$
$d_W \geq d_V \geq d_U$	$\frac{2}{2}U_S + \frac{3}{2}u^*_{G,U}$	$\frac{1}{2}U_S + \frac{3}{2}u^*_{G,V}$	$\frac{0}{2}U_S + \frac{3}{2}u^*_{G,W}$

representation of Fig. 1 is shown in Fig. 7. Please note that the values for the resistance $\tilde{R}$ and the inductance $\tilde{L}$ differ from R and L. When using $\tilde{R} = \frac{3}{2}R$ and $\tilde{L} = \frac{3}{2}L$, (4) can be rearranged, leading to

$$\frac{\mathrm{d}i_X}{\mathrm{d}t} = -\frac{\tilde{R}}{\tilde{L}}i_X + \frac{1}{\tilde{L}}u_X - \frac{1}{\tilde{L}}\tilde{u}^*_{G,X}. \tag{15}$$

Finally the voltage $\tilde{u}^*_{G,X}$, which also depends on the other half bridges voltages, is defined as follows:

$$\tilde{u}^*_{G,X} = u_{G,X} + \frac{1}{2}(u_Y - u_{G,Y} + u_Z - u_{G,Z}). \tag{16}$$

When assuming that the counter voltage $u_{G,X}$ is constant over one discretization time step T_D, $u_{G,X}$ equals $\overline{u}_{G,X}$ and therefore the zero-component-free voltages introduced in (8) can be used. By doing so, (16) can be expressed by

$$\tilde{u}^*_{G,X} = \frac{3}{2}u^*_{G,X} + \frac{1}{2}(u_Y + u_Z). \tag{17}$$

Table III is set up by interchanging the phases together with their corresponding duty cycles.

D. Generating the Lookup Table: Simulation Results

Once the equivalent single phase circuit is derived, the lookup table's entries are found using a simulation with the following assumptions:

1) The simulation is performed in time slot I.
2) Switching is scheduled to occur at $t^* = 2\,\mu\text{s}$ and simulation is performed for $t_E = 4\,\mu\text{s}$.
3) The dc-link voltage U_S is constant.

Fig. 8 shows the simulated voltage u_X and the simulated current i_X in blue. In addition, a reference signal is generated by using an ideal half bridge. This reference signal is plotted

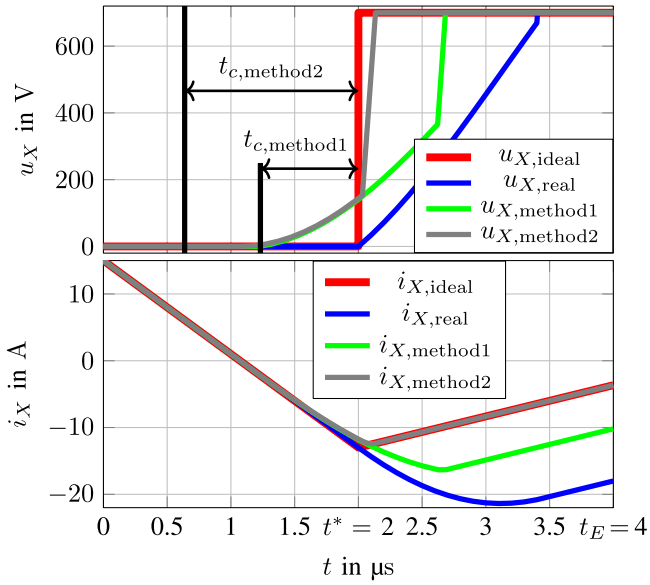

Fig. 8. Behavior of current and voltage around switching time.

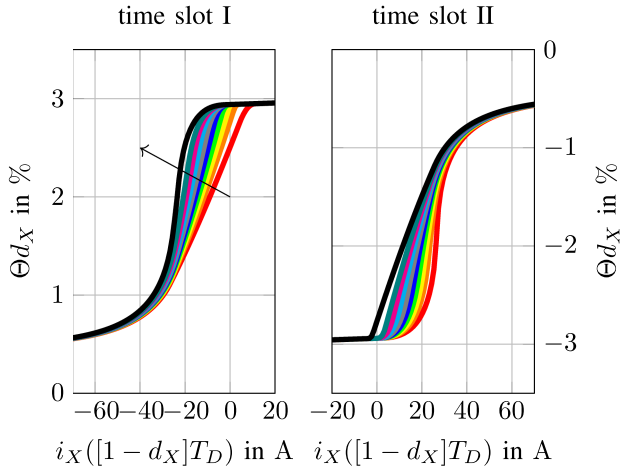

Fig. 9. Lookup table for both time slots, shown as an array of curves.

in red and will be further on referred to as *ideal* voltage and *ideal* current signal. It can be seen that at $t = t^*$ the low side switch opens and the high side switch starts conducting at $t = t^* + T_V \approx 3.4\,\mu$s. Due to the interlock time, there is some voltage-time area missing and this leads the current to differ from the *ideal* current. There are several ways to solve this problem, two of them are discussed in detail:

1) The missing voltage–time area $\Delta\Gamma_A = \int u_{X,\text{ideal}} - u_{X,\text{real}} \mathrm{d}\tau$ is computed. Now, switching is started earlier for $t_{c,\text{method 1}} = \frac{\Delta\Gamma_A}{U_S}$; this leads to opening the low side switch around $t = 1.23\,\mu$s. Fig. 8 shows this approach in green color. It can be seen that this method does not lead to a full compensation. The reason is that shifting the time instant of switching does not always have the same effect. The effectiveness of shifting is mainly dependent on the current during the interlock time. As the current's slope is proportional to $u_X - \tilde{u}^*_{G,X}$ (neglecting the resistance) it becomes plausible, that the voltage $\tilde{u}^*_{G,X}$ should get its own dimension in the lookup table. This is the direct consequence from retarding the problem of knowing $i_X(t)$, where $t \in [T_D(1-d_X), T_D(1-d_X)+T_V)$ to knowing $i_X(T_D(1-d_X))$, as explained in the beginning of this section.
2) This method takes the previously discovered effect into account. To ensure that the nonlinear behavior of the FC is fully compensated, the following approach is used: The time difference $t_{c,\text{method 2}}$ is searched in such a way that the *ideal* and the simulated current exactly match at the end of the simulation interval t_E, i.e.,

$$\underset{t_{c,\text{method 2}} \in (0,t^*)}{\text{find}} \; i_{X,\text{ideal}}(t = t_E) = i_{X,\text{real}}(t = t_E). \quad (18)$$

It is worth mentioning that method 1 needs one simulation per initial condition pair $(i_X, \tilde{u}^*_{G,X})$, in contrast to finding the solution of (18) for every initial condition pair. However, since this computation can be done offline, computational time is not a major concern. The results from using this approach are shown again in Fig. 8, plotted in gray. It can be seen that $i_{X,\text{ideal}}(t = t_E) = i_{X,\text{real}}(t = t_E)$ holds. This means that after completion of the switching process (this will certainly be before $t = t_E$), the current matches the *ideal* current exactly. Therefore, the influence of the switching process is perfectly compensated.

To generate the entries of the lookup table, the initial condition pair $(i_X(0), \tilde{u}^*_{G,X})$ is varied. The result of solving (18) is $t_{c,\text{method 2}}$. For calculating the duty cycle correction Θd_X, the following relation is used:

$$\Theta d_X = \frac{t_{c,\text{method 2}}}{T_D}. \quad (19)$$

The correction voltage Θu_X is calculated using

$$\Theta u_X = U_S \Theta d_X. \quad (20)$$

The result of this computation is shown in Fig. 9 as a array of curves. Each curve shown has the property that $\tilde{u}^*_{G,X} = const.$ holds. The impact of $\tilde{u}^*_{G,X}$ is clearly visible.

The duty cycle correction Θd_X is stored in a matrix $\boldsymbol{M}$, whose rows represent the ideal current at the moment of switching $i_X(T_D(1-d_X))$ and whose columns represent the counter voltage $\tilde{u}^*_{G,X}$. This matrix $\boldsymbol{M}$ with its corresponding base vectors will subsequently be referred to as the lookup table.

E. Currents at the Moment of Switching

As stated at the beginning of this section, the current i_X at the moment of switching is needed. At first, it is assumed that the current i_X at the time instant $t = 0\,$s, referred to as $i_X(0)$, is known. During the following derivation the property that $\sum_{X\in\{U,V,W\}} u^*_X = \sum_{X\in\{U,V,W\}} u^*_{G,X} = 0\,$V holds, as shown in (10) and (11), is used relatively often. Two assumptions are used for further reducing computational effort.

The first assumption is that the mean output voltage u^*_X is equal to the counter voltage $u^*_{G,X}$. The change of current when $u^*_X = u^*_{G,X}$ holds, is referred to as $\Delta\tilde{i}_X$. This assumption

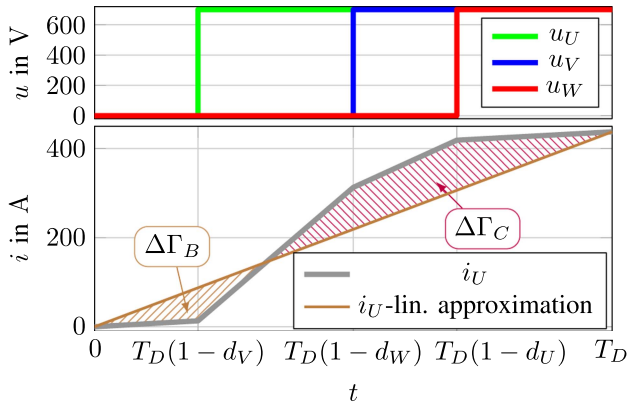

Fig. 10. Deriving the initial current $i_X(0)$ from its mean value $\bar{i}_X$.

will eventually be dropped during the derivation; the change of current when $u_X^* \neq u_{G,X}^*$ is then referred to as Δi_X.

The second assumption is that the resistance R is negligibly small; i.e., $R = 0\,\Omega$ is used. This leads to affine functions with respect to time instead of the solutions of (4), which are exponential functions. The error introduced by this assumption is relatively small because it is only used to approximate time intervals with a maximal length of T_D.

The timing can be seen directly from Fig. 10. As mentioned, the starting point of this calculation is at $t = 0\,\mathrm{s}$. The first switching process takes place in phase U at $t = T_D(1-d_U)$, the second switching process in phase V at $t = T_D(1-d_V)$ and the last switching process in phase W at $t = T_D(1-d_W)$. To derive the currents at the moment of switching, the voltage–time area of each phase X starting from 0 s to the corresponding time of switching $T_D(1-d_X)$ must be summarized. To accomplish this, the entire time interval $[0, T_D)$ must be split into subintervals in such a way that in every one of these subintervals all output voltages u_X are constant. The following equations show the way of computation:

1) $\Delta\tilde{i}_U$: Because the first switching occurs in phase U, there is only one time interval $[0, T_D(1-d_U))$ to consider. The FC's output voltages u_U, u_V, and u_W are zero. The counter voltage $u_{G,U}^*$ is assumed to be equal to the mean output voltage, this means $u_{G,U}^* = u_U^*$. Using these voltages in (4) leads to the following relation:

$$\Delta\tilde{i}_U = \frac{T_D}{L}\left(d_U u_U^* + \frac{3}{3}u_V^* + \frac{3}{3}u_W^*\right). \tag{21}$$

2) $\Delta\tilde{i}_V$: For phase V, the interval $[0, T_D(1-d_V))$ is split into two subintervals referred to as I_1 and I_2, respectively. During $I_1 = [0, T_D(1-d_U))$, all output voltages are zero again. However, during $I_2 = [T_D(1-d_U), T_D(1-d_V))$, u_U equals U_S. Analogous to the computation of $\Delta\tilde{i}_U$, it is assumed that $u_{G,V}^* = u_V^*$ holds. Using these voltages in (4) and summing up the influences of I_1 and I_2 leads to the following relation:

$$\Delta\tilde{i}_V = \frac{T_D}{L}\left(\frac{1}{3}u_U^* + d_V u_V^* + \frac{2}{3}u_W^*\right). \tag{22}$$

3) $\Delta\tilde{i}_W$: The same steps as shown previously are necessary. For calculating $\Delta\tilde{i}_W$ three subintervals are needed; $I_1 = [0, T_D(1-d_U))$, $I_2 = [T_D(1-d_U), T_D(1-d_V))$ and $I_3 = [T_D(1-d_V), T_D(1-d_W))$. Again the subintervals and their corresponding voltages are used in (4). This results in

$$\Delta\tilde{i}_W = \frac{T_D}{L}(d_W u_W^*). \tag{23}$$

By interchanging the phases U, V and W as well as their corresponding duty cycles, Table IV is filled up.

Now, the initially made assumption that u_X^* equals $u_{G,X}^*$ is dropped. The difference between u_X^* and $u_{G,X}^*$ is denoted δ_X^* and is given by

$$\delta_X^* = u_X^* - u_{G,X}^*. \tag{24}$$

For correcting the currents at the moment of switching, a straight line with the slope $\frac{\delta_X^*}{L}$ is added to $\Delta\tilde{i}_X$. This leads to

$$\Delta i_X = \Delta\tilde{i}_X + \frac{T_D}{L}(1-d_X)\delta_X^*. \tag{25}$$

This expression holds for all $X \in \{U, V, W\}$. The currents at the moment of switching can therefore be expressed by

$$\boxed{i_X(T_D(1-d_X)) = i_X(0) + \Delta i_X.} \tag{26}$$

F. Computing the Initial Current From Mean-Values

From (26), it can be seen that the initial current $i_X(0)$ is necessary to compute the current at the moment of switching $i_X(T_D(1-d_X))$. Depending on the used technique for current measurement, $i_X(0)$ may not be available directly. This section provides two methods for computing $i_X(0)$ in case that the mean value $\bar{i}_X$ is measured.

The first method assumes that the current changes linearly from $i_X(0)$ to $i_X(T_D)$. This results in a straightforward computation, which is presented in this section. As a result of the approximation used, however, the real current trajectory is neglected. This leads to an error that can be relatively high, depending on several parameters. For this reason, an exact solution is also presented in this article. However, the lengthy derivation cannot be shown here. For the change of current over a whole discretization time step, the following equation holds:

$$i_X(T_D) = i_X(0) + \frac{T_D}{L}\delta_X^*. \tag{27}$$

The evolution of the current $i_X(t)$ is therefore given by

$$i_X(t) = i_X(0) + \frac{t}{L}\delta_X^* \tag{28}$$

and this subsequently leads to

$$i_X(0) = \bar{i}_X - \frac{T_D}{2L}\delta_X^* \tag{29}$$

where $\bar{i}_X$ is the mean value. The linear approximation misses some current–time area, referred to as $\Delta\Gamma_B$ and $\Delta\Gamma_C$ in

TABLE IV
CHANGE OF CURRENT $\Delta\tilde{i}_X$ FOR DIFFERENT SWITCHING ORDERS

Order	$\Delta\tilde{i}_U$	$\Delta\tilde{i}_V$	$\Delta\tilde{i}_W$
$d_U \geq d_V \geq d_W$	$\frac{T_D}{L}(d_U u_U^* + \frac{3}{3}u_V^* + \frac{3}{3}u_W^*)$	$\frac{T_D}{L}(d_V u_V^* + \frac{1}{3}u_U^* + \frac{2}{3}u_W^*)$	$\frac{T_D}{L}(d_W u_W^* + \frac{0}{3}u_U^* + \frac{0}{3}u_V^*)$
$d_U \geq d_W \geq d_V$	$\frac{T_D}{L}(d_U u_U^* + \frac{3}{3}u_V^* + \frac{3}{3}u_W^*)$	$\frac{T_D}{L}(d_V u_V^* + \frac{0}{3}u_U^* + \frac{0}{3}u_W^*)$	$\frac{T_D}{L}(d_W u_W^* + \frac{1}{3}u_U^* + \frac{2}{3}u_V^*)$
$d_V \geq d_U \geq d_W$	$\frac{T_D}{L}(d_U u_U^* + \frac{1}{3}u_V^* + \frac{2}{3}u_W^*)$	$\frac{T_D}{L}(d_V u_V^* + \frac{3}{3}u_U^* + \frac{3}{3}u_W^*)$	$\frac{T_D}{L}(d_W u_W^* + \frac{0}{3}u_U^* + \frac{0}{3}u_V^*)$
$d_V \geq d_W \geq d_U$	$\frac{T_D}{L}(d_U u_U^* + \frac{0}{3}u_V^* + \frac{0}{3}u_W^*)$	$\frac{T_D}{L}(d_V u_V^* + \frac{3}{3}u_U^* + \frac{3}{3}u_W^*)$	$\frac{T_D}{L}(d_W u_W^* + \frac{2}{3}u_U^* + \frac{1}{3}u_V^*)$
$d_W \geq d_U \geq d_V$	$\frac{T_D}{L}(d_U u_U^* + \frac{2}{3}u_V^* + \frac{1}{3}u_W^*)$	$\frac{T_D}{L}(d_V u_V^* + \frac{0}{3}u_U^* + \frac{0}{3}u_W^*)$	$\frac{T_D}{L}(d_W u_W^* + \frac{3}{3}u_U^* + \frac{3}{3}u_V^*)$
$d_W \geq d_V \geq d_U$	$\frac{T_D}{L}(d_U u_U^* + \frac{0}{3}u_V^* + \frac{0}{3}u_W^*)$	$\frac{T_D}{L}(d_V u_V^* + \frac{2}{3}u_U^* + \frac{1}{3}u_W^*)$	$\frac{T_D}{L}(d_W u_W^* + \frac{3}{3}u_U^* + \frac{3}{3}u_V^*)$

TABLE V
EFFECT OF PARAMETER TOLERANCES ON THE THD

Parameter	rel. Change	add. THD
Half bridge model capacitance C	$\pm 20\,\%$	$< 1.6\,\%$
Every other half bridge model parameter	$\pm 20\,\%$	$< 2.2\,\%$
Load inductance L	$\pm 10\,\%$	$< 3.7\,\%$
Load inductance L	$\pm 5\,\%$	$< 1.4\,\%$

Fig. 10. If this approximation error is acceptable, putting together equation (25), (26) and (29) leads to the final result

$$\boxed{i_X(T_D(1-d_X)) = \Delta\tilde{i}_X + \bar{i}_X + \frac{T_D}{L}(\frac{1}{2} - d_X)\delta_X^*.} \quad (30)$$

As stated above, an exact solution for computing $i_X(0)$ is also shown in this article. Here, the current's correct trajectory is integrated from $t = 0\,\mathrm{s}$ to $t = T_D$. After introducing the squared, zero-component-free output voltages with

$$\begin{bmatrix} u_U^{**} & u_V^{**} & u_W^{**} \end{bmatrix}^T = U_S \mathbf{\Lambda} \begin{bmatrix} d_U^2 & d_V^2 & d_W^2 \end{bmatrix}^T \quad (31)$$

and the difference between u_X^{**} and $u_{G,X}^*$ with

$$\delta_X^{**} = u_X^{**} - u_{G,X}^* \quad (32)$$

the exact result

$$i_X(0) = \bar{i}_X - \frac{T_D}{2L}\delta_X^{**} \quad (33)$$

can be written in a form very similar to (30)

$$\boxed{i_X(T_D(1-d_X)) = \Delta\tilde{i}_X + \bar{i}_X + \frac{T_D}{L}\left[(1-d_X)\delta_X^* - \frac{1}{2}\delta_X^{**}\right].} \quad (34)$$

G. Using the Lookup Table

After computing $i_X(T_D(1-d_X))$ using (26), (30), or (34), Θd_X is found using the lookup table $\boldsymbol{M}$. Then the corrected duty cycle $d_{X,\mathrm{corr}} = d_X + \Theta d_X$ is assigned to the FC's output.

H. Parameter Tolerances

The proposed CM depends on many parameters. To investigate the effect of parameter tolerances, the authors performed a sensitivity analysis based on simulation. The simulation setup is similar as discussed in Section VI. Table V summarizes the results by providing the additional amount of Total Harmonic Distortion (THD) in case of different parameter variations.

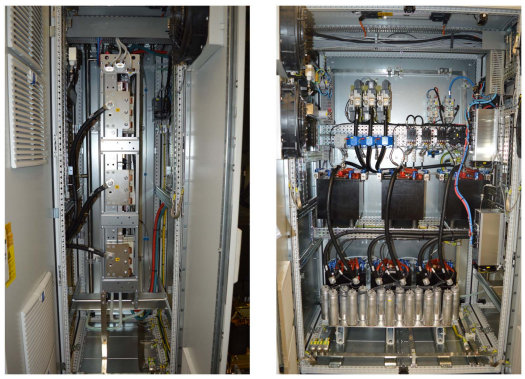

Fig. 11. The left picture shows the *Intelligent Power Module*. The picture on the right side shows the load unit which consists of inductors (center/cube/black) and capacitors (bottom/cylindrical/silver).

While the proposed method is fairly robust against variations in the half bridge model's parameters, it is important that the load unit's inductance is known relatively accurately.

VI. EXPERIMENTAL SETUP

The experimental setup is shown in Fig. 1. The counter voltage $u_{G,X}$ is generated using three capacitors, each with a capacitance of $C = 300\,\mu\mathrm{F}$. Fig. 11 shows the test hardware. The FC is based on an *Intelligent Power Module* called *SKiiP 4* produced by *Semikron*. This module consists of three half bridges, each half bridge itself consists of two 1200 V, 1800 A IGBTs. Current measurement is performed via the power module's built in current to voltage transducer.

The sampling of the analog signals as well as generating the PWM signal and the computation of the control algorithm is done on hardware manufactured by *dSpace*. The dc link voltage U_S is provided by a three phases power supply unit produced by *Siemens*.

All measurements shown in this manuscript are obtained using a 4-channel oscilloscope *WaveSurfer 4034HD* from *Teledyne Lecroy*. Since also the half bridges output voltage u_X and their gate control signal is necessary (see Fig. 3), only two phase currents are measured. Due to the floating star-point of the load the sum of all currents is zero anyway, thus the remaining phase current could be computed at any time. However, for reasons of consistence and to avoid overloading the figures, only two phase currents are shown.

Fig. 13 shows the oscilloscopes screen while operating without using a CM. It can be seen that due to the relatively high

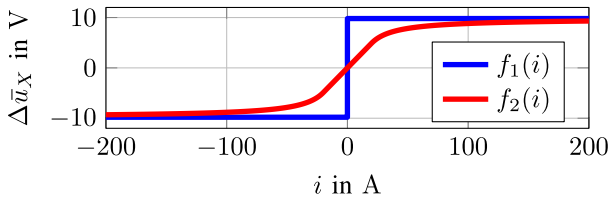

Fig. 12. Comparison of two often used functions for compensation: $f_1(i) = 9.8\,\mathrm{V}\,\mathrm{sign}\left(\frac{i}{1\,\mathrm{A}}\right)$ as in [7], $f_2(i)$ as discussed in [29, Table I].

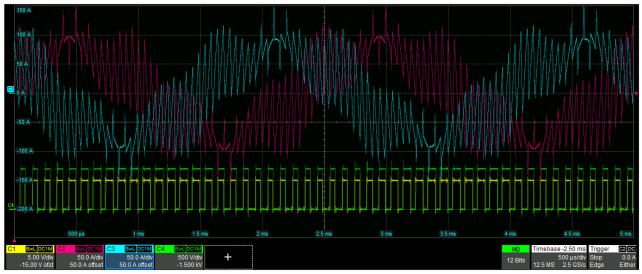

Fig. 13. Measurement of the phase currents i_V and i_W without a CM active. Performed at 400 Hz and 100 V. Channel 1 measures the gate drivers control signal on phase W, Channel 2 measures the current i_W, Channel 3 measures the current i_V and Channel 4 measures the half bridges output voltage referred to DC-.

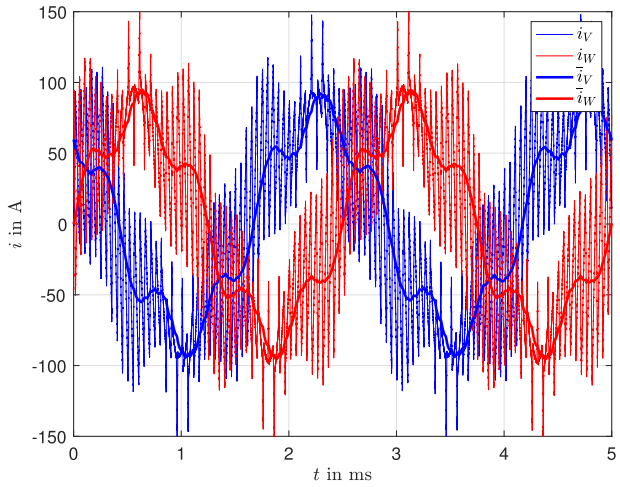

Fig. 14. Measured currents without compensation.

ripple current it is difficult to evaluate the mean current over one switching cycle. Therefore, the data shown in Fig. 13 is averaged using *MATLAB*. These averaged currents are shown in Fig. 14, plotted with thick lines. Fig. 14 also shows the unfiltered currents, plotted with thin lines.

Figs. 14 to 18 are all postprocessed in the same fashion, however, these figures show the current's trajectories when using different CMs.

VII. Experimental Comparison of CMs

This section provides a comparison of different CM using measured data obtained with the experimental setup explained in Section VI.

1) Fig. 15 shows the trajectory of the current when using the *CM 1*, which is explained in reference [7]. A voltage $\Delta\bar{u}_X = \frac{T_V}{2T_D} U_S\,\mathrm{sign}(i_X)$, which depends on the current's sign, is added to the reference voltage. This compensation function is shown as $f_1(i)$ in Fig. 12. The measurements show that *CM 1* tends to overcompensation and thus it cannot remove the distortions of the current. Therefore, the THD increases when using this method. This can be seen in Table VI.
2) *CM 2*, shown in Fig. 16, uses a more *smooth* function $\Delta\bar{u}_X = f(i_X)$ instead of the rectangular function used in

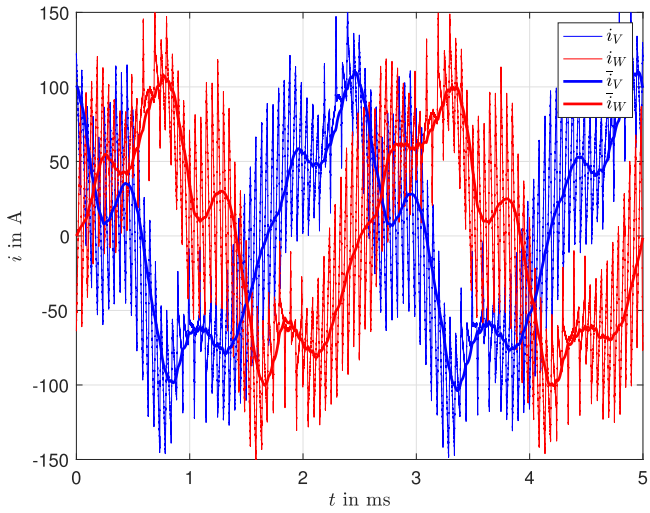

Fig. 15. Measured currents when using *CM 1* [7].

TABLE VI
Comparison of the THD

Method	Fig., Ref.	THD i_V	THD i_W	THD Avg.
none	Fig. 14, -	20.82 %	20.54 %	20.68 %
CM 1	Fig. 15, [7]	31.78 %	29.34 %	30.56 %
CM 2	Fig. 16, [29]	11.35 %	13.03 %	12.19 %
CM 3	Fig. 17, [24]	5.06 %	7.10 %	6.08 %
Proposed	Fig. 18, -	3.32 %	3.80 %	3.56 %

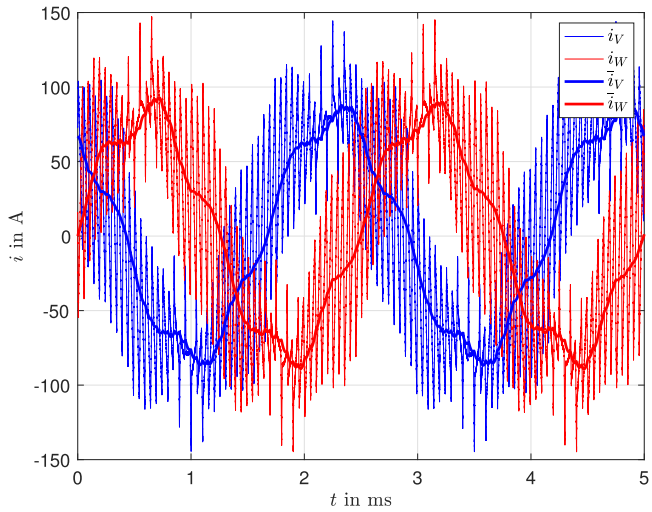

Fig. 16. Measured currents when using *CM 2* [29].

TABLE VII
COMPARISON BETWEEN THE EQUATIONS IN TIME SLOT I AND II

Ref.	Equation in time slot I	Equation in time slot II
(25)	$\Delta i_X = \Delta\tilde{i}_X + \frac{T_D}{L}(1-d_X)\delta_X^*$	$\Delta i_X = \Delta\tilde{i}_X + \frac{T_D}{L} d_X \delta_X^*$
(26)	$i_X(T_D(1-d_X)) = i_X(0) + \Delta i_X$	$i_X(T_D(1+d_X)) = i_X(T_D) + \Delta i_X$
(27)	$i_X(T_D) = i_X(0) + \frac{T_D}{L}\delta_X^*$	$i_X(2T_D) = i_X(T_D) + \frac{T_D}{L}\delta_X^*$
(29)	$i_X(0) = \bar{i}_X - \frac{T_D}{2L}\delta_X^*$	$i_X(T_D) = \bar{i}_X - \frac{T_D}{2L}\delta_X^*$
(30)	$i_X(T_D(1-d_X)) = \Delta\tilde{i}_X + \bar{i}_X + \frac{T_D}{L}(\frac{1}{2}-d_X)\delta_X^*$	$i_X(T_D(1+d_X)) = \Delta\tilde{i}_X + \bar{i}_X - \frac{T_D}{L}(\frac{1}{2}-d_X)\delta_X^*$
(33)	$i_X(0) = \bar{i}_X - \frac{T_D}{2L}\delta_X^{**}$	$i_X(T_D) = \bar{i}_X - \frac{T_D}{2L}(2\delta_X^* - \delta_X^{**})$
(34)	$i_X(T_D(1-d_X)) = \Delta\tilde{i}_X + \bar{i}_X + \frac{T_D}{L}[(1-d_X)\delta_X^* - \frac{1}{2}\delta_X^{**}]$	$i_X(T_D(1+d_X)) = \Delta\tilde{i}_X + \bar{i}_X - \frac{T_D}{L}[(1-d_X)\delta_X^* - \frac{1}{2}\delta_X^{**}]$

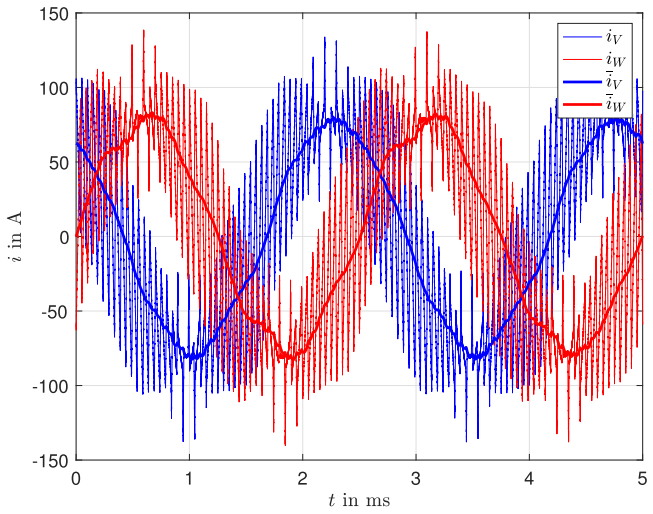

Fig. 17. Measured currents when using *CM 3* [24].

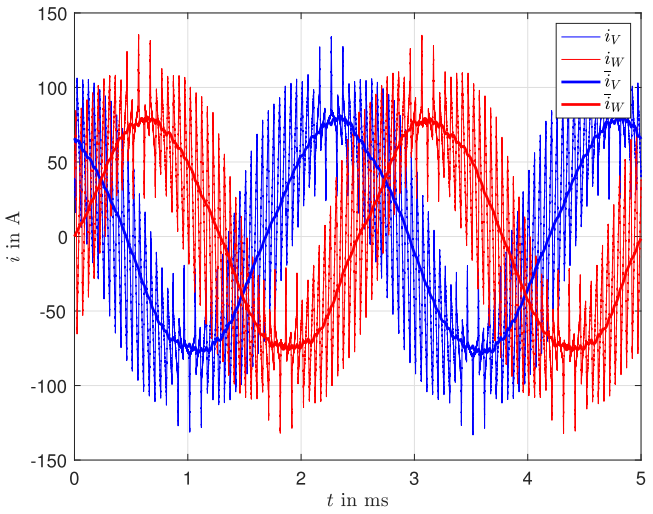

Fig. 18. Measured currents when using the *Proposed method*.

CM 1. This function can either be given in form of a mathematical expression [29] or in form of a lookup-table [30]. Due to the smoothed behavior around $i_X = 0\,\mathrm{A}$, overcompensation should not occur. The compensation function is again shown in Fig. 12, referred to as $f_2(i)$. This method is de-facto state of the art for many industrial FCs at the moment. The experiments show that *CM 2* manages to compensate for a good part of the distortions.

3) *CM 3*, shown in Fig. 17, uses the current at the moment of switching and a 1-D lookup table ($\Delta d_X = f(i_{\mathrm{Sw}})$), as described in [24]. By using the current at the moment of switching, *CM 3* leads to better compensation results. This fact can also be seen when comparing the THD of this method with the uncompensated case. Again, the THD values are provided in Table VI.
4) Finally, Fig. 18 shows the *Proposed method*. It uses the current at the moment of switching and the counter voltage inside a 2-D lookup table ($\Theta d_X = \tilde{f}(i_{\mathrm{Sw}}, u_{\mathrm{Counter}})$) which is filled up with duty cycle corrections Θd_X instead of duty cycle errors Δd_X.

The following summarizes the experimental results: *CM 1* and *CM 2* use the current at the latest available sample while *CM 3* and the *Proposed method* benefit from using the predicted current at the moment of switching. In addition, the *Proposed method* uses duty cycle corrections Θd_X instead of duty cycle errors Δd_X, which leads to a decrease of $41.4\,\%$ in THD compared to *CM 3*. All THD values are collected in Table VI.

VIII. CONCLUSION

This contribution has analyzed the voltage error of FCs with loads with small inductances. In accordance with the literature, it is found out that the main influence for nonlinear output voltage behavior is the interlock time. To gain knowledge about the mechanisms involved during the interlock time, a half bridge model is developed. Using this model leads to *two main results:*

The first new finding is that for lookup table based compensation approaches there are two quantities of interest: the current at the moment of switching and the current's slope around the moment of switching. While the former is already in use [23], [24], [25], using the latter is a completely novel approach.

The second new finding is used in the lookup table's entries which do not consist of duty cycle errors Δd_X, instead they consist of duty cycle corrections Θd_X. These corrections are added to the setpoint d_X to achieve zero output voltage error.

Since this lookup table has the current at the moment of switching as breakpoints, a method to compute this current directly is also presented in this manuscript. It should be noted that the results are provided for every switching sequence.

Subsequently the high effectiveness of the proposed method is shown using measured data.

IX. Results in Time Slot II

This section contains all time slot II results. Table VII contains a comparison between the equations in both time slots.

In time slot II, the sign of all results shown in Table IV needs to be changed.

References

[1] V. Mallemaci, F. Mandrile, E. Carpaneto, and R. Bojoi, "Dead–time effect on two–level grid–forming virtual synchronous machines," *IEEE Trans. Ind. Appl.*, vol. 59, no. 5, pp. 6103–6112, Sep./Oct. 2023.

[2] T. Messo, T. Roinila, A. Aapro, and P. Rasilo, "Evaluation of dead-time effect of grid-connected inverters using broadband methods," *IFAC-PapersOnLine*, vol. 51, no. 15, pp. 449–454, 2018.

[3] A. Mazaheri, F. Barati, and F. Ghavipanjeh, "Dead-time compensation in three-phase grid-tied inverters using LQG multivariable control," *Sci. Rep.*, vol. 13, no. 1, 2023, Art. no. 14851.

[4] A. Guha and G. Narayanan, "Impact of undercompensation and over-compensation of dead-time effect on small-signal stability of induction motor drive," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6027–6041, Nov./Dec. 2018.

[5] A. Guha and G. Narayanan, "Small-signal stability analysis of an open-loop induction motor drive including the effect of inverter deadtime," *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, pp. 242–253, Jan./Feb. 2016.

[6] S. Zhang, J. Kang, and J. Yuan, "Analysis and suppression of oscillation in V/F controlled induction motor drive systems," *IEEE Trans. Transport. Electrific.*, vol. 8, no. 2, pp. 1566–1574, Jun. 2022.

[7] S.-G. Jeong and M.-H. Park, "The analysis and compensation of dead-time effects in PWM inverters," *IEEE Trans. Ind. Electron.*, vol. 38, no. 2, pp. 108–114, Apr. 1991.

[8] D. Leggate and R. Kerkman, "Pulse based dead time compensator for PWM voltage inverters," in *Proc. 21st Annu. Conf. IEEE Ind. Electron.*, 1995, pp. 474–481.

[9] L. Ben-Brahim, "The analysis and compensation of dead-time effects in three phase PWM inverters," in *Proc. 24th Annu. Conf. IEEE Ind. Electron. Soc. (Cat. No.98CH36200)*, 1998, pp. 792–797.

[10] H. Zhao, Q. Wu, and A. Kawamura, "An accurate approach of nonlinearity compensation for VSI inverter output voltage," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1029–1035, Jul. 2004.

[11] Y. Park and S.-K. Sul, "A novel method utilizing trapezoidal voltage to compensate for inverter nonlinearity," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4837–4846, Dec. 2012.

[12] Y. Park and S.-K. Sul, "Implementation schemes to compensate for inverter nonlinearity based on trapezoidal voltage," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1066–1073, Mar./Apr. 2014.

[13] L. Wang, J. Xu, Q. Chen, Z. Chen, and R. Huang, "An improved trapezoidal voltage method for dead-time compensation in three-phase voltage source converter," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 8785–8789, Aug. 2022.

[14] L. Ben-Brahim, "On the compensation of dead time and zero-current crossing for a PWM-inverter-controlled ac servo drive," *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 1113–1118, Oct. 2004.

[15] Y. Yang, K. Zhou, H. Wang, and F. Blaabjerg, "Analysis and mitigation of dead-time harmonics in the single-phase full-bridge PWM converter with repetitive controllers," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5343–5354, Sep./Oct. 2018.

[16] Z. Tang and B. Akin, "Compensation of dead-time effects based on revised repetitive controller for PMSM drives," in *Proc. 2017 IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2730–2737.

[17] Z. Tang and B. Akin, "A new LMS algorithm based deadtime compensation method for PMSM FOC drives," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6472–6484, Nov./Dec. 2018.

[18] Z. Li et al., "A new digital control method for high performance 400 Hz ground power unit," in *Proc. 13th Int. Power Electron. Motion Control Conf.*, 2008, pp. 515–520.

[19] J. Ye et al., "An accurate dead time compensation method for SPWM voltage source inverters," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4894–4908, Apr. 2023.

[20] R. Ren, F. Zhang, B. Liu, F. Wang, Z. Chen, and J. Wu, "A closed-loop modulation scheme for duty cycle compensation of PWM voltage distortion at high switching frequency inverter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1475–1486, Feb. 2020.

[21] L. Buchta and O. Bartik, "Dead-time compensation strategies based on Kalman filter algorithm for PMSM drives," in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc.*, 2019, pp. 986–991.

[22] S.-Y. Kim, W. Lee, M.-S. Rho, and S.-Y. Park, "Effective dead-time compensation using a simple vectorial disturbance estimator in PMSM drives," *IEEE Trans. Ind. Electron.*, vol. 57, no. 5, pp. 1609–1614, May 2010.

[23] D. Jiang and F. Wang, "A general current ripple prediction method for the multiphase voltage source converter," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2643–2648, Jun. 2014.

[24] Z. Shen, D. Jiang, J. Chen, and Z. Liu, "A general dead time compensation method based on current ripple prediction and pulse delay measurement for voltage source inverter," in *Proc. 2020 IEEE Energy Convers. Congr. Expo.*, 2020, pp. 1927–1931.

[25] A. Futó, I. Varjasi, and Z. Sütő, "Current ripple calculation for dead time compensation in three phase PWM inverters," in *Proc. 2014 IEEE Int. Energy Conf.*, 2014, pp. 195–201.

[26] Z. Shen and D. Jiang, "Dead-time effect compensation method based on current ripple prediction for voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 971–983, Jan. 2019.

[27] D. A. Schuetz et al., "Dead-time compensation for grid-tied voltage source inverters with SVM^2 PC," *IEEE Trans. Ind. Appl.*, vol. 60, no. 4, pp. 6366–6379, Jul./Aug. 2024.

[28] T. Mannen and H. Fujita, "Dead-time compensation method based on current ripple estimation," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 4016–4024, Jul. 2015.

[29] Z. Zhang and L. Xu, "Dead-time compensation of inverters considering snubber and parasitic capacitance," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 3179–3187, Jun. 2014.

[30] B. Weber, T. Brandt, and A. Mertens, "Compensation of switching dead-time effects in voltage-fed PWM inverters using FPGA-based current oversampling," in *Proc. 2016 IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 3172–3179.

[31] N. Urasaki, T. Senjyu, T. Kinjo, K. Uezato, T. Funabashi, and H. Sekine, "Dead-time compensation strategy for permanent magnet synchronous motor drive taking zero current clamp and parasitic capacitor effects into account," in *Proc. 30th Annu. Conf. IEEE Ind. Electron. Soc.*, 2004, pp. 2718–2723.

[32] W. C. Duesterhoeft, M. W. Schulz, and E. Clarke, "Determination of instantaneous currents and voltages by means of alpha, beta, and zero components," *Trans. Amer. Inst. Elect. Eng.*, vol. 70, no. 2, pp. 1248–1255, 1951.

[33] L. M. Gong and Z. Q. Zhu, "Modeling and compensation of inverter nonlinearity effects in carrier signal injection-based sensorless control methods from positive sequence carrier current distortion," in *Proc. 2010 IEEE Energy Convers. Congr. Expo.*, 2010, pp. 3434–3441.

[34] D. Schröder, *Leistungselektronische Bauelemente*, vol. 2. Berlin, Germany: Springer-Verlag, 2005.

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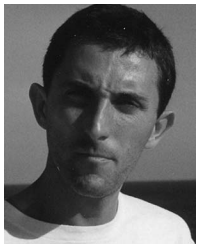

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