Asymmetrical Interleaved Switching Power Amplifier Based on Arm Multiplexing

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***Abstract*—Switching power amplifiers (SPAs) are commonly used as transmitters in sonar systems. They provide a low-distortion drive current with a wide bandwidth to the system. This article proposes an asymmetric interleaved SPA (AISPA) topology based on arm multiplexing. The topology combines active power decoupling and interleaving operation through arm multiplexing. The AISPA has both power decoupling mode and interleaving mode. The power decoupling mode effectively suppresses the dc-link voltage ripple, whereas the interleaved mode increases the equivalent switching frequency and reduces the total harmonic distortion (THD) of the output voltage. In addition, this article proposes a fundamental frequency current control method based on thermal stress balance. Furthermore, the impact of this current control method on the THD of the output voltage is examined, and the control loop for the AISPA is quantitatively derived. The parameters of the passive components are calculated. An experimental prototype has been constructed to verify the effectiveness and correctness of the proposed topology and control method.**

***Index Terms*—Active power decoupling (APD), interleaved, multiplexing, switching power amplifier (SPA).**

I. Introduction

THE sonar system is widely used in the fields of underwater resource detection, seabed topographic mapping, and seabed communication. It can meet the requirements of large-area, high-quality detection, and is the main method of underwater detection and communication with a wide application prospect [1], [2], [3], [4]. The switching power amplifier (SPA), as the transmitting equipment in the sonar system, is the key equipment of the system. The output band and distortion rate of the SPA directly affect the detection and communication performance of the whole system [5], [6]. The structure of the sonar system is shown in Fig. 1.

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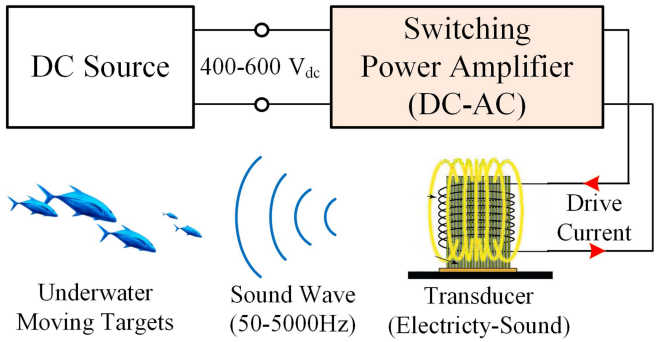

Fig. 1. Structure of the sonar system.

The lower the frequency of the sound wave, the slower the rate of decay underwater and the longer the detection distance [7]. With the development of transducer technology, it is now possible to detect sound waves with a lower frequency limit of less than 100 Hz [8]. However, lower-frequency sound waves have longer wavelengths, which reduces their ability to distinguish the shape of the detected target. To meet the requirements of the system under different working conditions, the transmitter must emit sound waves of various frequencies in a wide frequency band ($f_{\mathrm{outmax}}/f_{\mathrm{outmin}} \geq 100$) while maintaining a low harmonic distortion rate (THD$<$1%) across all frequencies [7].

For the fixed switching frequency SPWM, the carrier ratio decreases as the output frequency increases. The carrier ratio is equal to the equivalent switching frequency divided by the output frequency. To achieve a higher upper limit of output frequency and lower THD, researchers have added arms to the full-bridge inverter to form a multiphase parallel interleaved switching power amplifier (ISPA) [9], [10]. By increasing the number of arms, the equivalent switching frequency and the upper limit of the output frequency can be significantly increased. The topology of the ISPA is shown in Fig. 2.

The essence of the SPA is the single-phase inverter. Voltage ripple will appear on the dc link of the SPA without additional auxiliary circuitry. The amplitude of the voltage ripple will increase as the output power increases and the output frequency decreases, and this can have an effect on the reliability and output THD of the SPA. To lower the lower limit of output frequency, researchers have proposed and extensively studied active power decoupling (APD) technology to suppress dc-link voltage ripple [11], [12], [13], [14], [15], [16], [17], [18]. Fig. 3 shows several power decoupling circuit topologies. Power decoupling

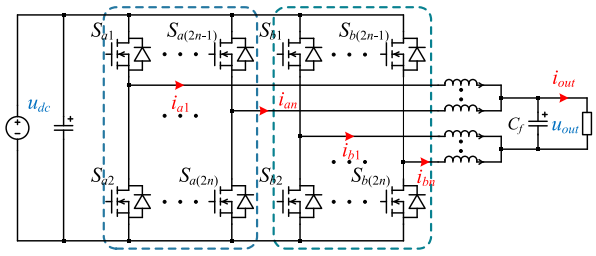

Fig. 2. Topology of multiphase parallel interleaved switching power amplifier.

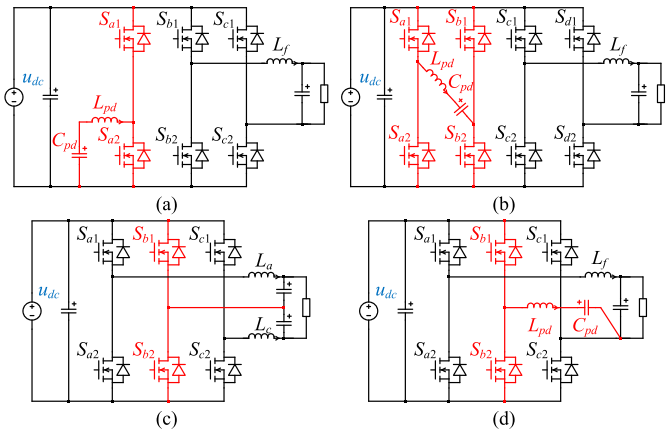

Fig. 3. Topologies of different power decoupling circuits. (a) Buck circuit adopted in [10]. (b) Full-bridge circuit adopted in [12]. (c) Enhanced single-phase inverter proposed in [15]. (d) Single-phase inverter with active power filter proposed in [16].

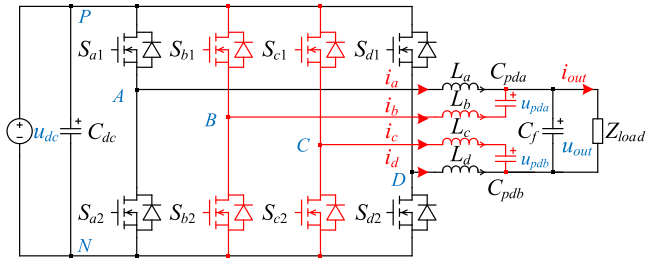

Fig. 4. Topology of the four-bridge arm asymmetric interleaved switching power amplifier.

circuits, which can be independent of the inverter circuit, are commonly implemented using bidirectional dc–dc converters such as buck and buck–boost [12], [13]. In [14] and [15], a full bridge is used as the power decoupling circuit. In [14], the power decoupling circuit is connected in parallel with the dc-link capacitor, whereas in [15], it is connected in series with the dc-link capacitor. Meanwhile, some power decoupling circuits are integrated with the inverter circuit [16], [17], [18]. Serban [16] used the differential inverter to increase output power by adjusting the common voltage of the output capacitor. Zhu et al. [17] proposed the enhanced single-phase full-bridge inverter topology, which adds an arm to create an additional current loop for the output capacitor. The single-phase inverter with active power filter (APF) topology is proposed in [18]. The double-frequency power of the inverter can be absorbed by controlling the power decoupling capacitor with a power decoupling arm.

Although the number of arms is increased, the existing APD topology does not increase the equivalent switching frequency of SPA as ISPA does. Similarly, ISPA also cannot solve the dc-link voltage ripple problem by increasing the number of bridge arms. Unlike grid-connected inverters, the output frequency of the SPA varies over a wide range. Both the amplitude of the dc-link voltage ripple and the carrier ratio are inversely proportional to the output frequency of the SPA. As the output frequency decreases for the same output power, the dc-link voltage ripple and carrier ratio gradually increases. This leads to an increased need for the SPA to suppress the dc-link voltage ripple and a decreased need to increase the equivalent switching frequency. Similarly, as the output frequency increases, the dc-link voltage ripple and carrier ratio decrease. This results in an increased need for the SPA to increase the equivalent switching frequency and a decreased need to suppress the dc-link voltage ripple. The analysis above shows that the SPA will not experience both low carrier ratio and high dc-link voltage ripple simultaneously due to the influence of the changing law of carrier ratio and voltage ripple.

Considering that adding both APD circuits and multiphase interleaved parallel bridge arms to the SPA increases the current complexity, a four-bridge arm asymmetric ISPA (AISPA) topology is proposed in this article. The topology of the AISPA is shown in Fig. 4. The bridge arms of the AISPA are not all the same, unlike conventional ISPAs. The phase B and phase C bridge arms are used as multiplexed bridge arms. AISPA operates in power decoupling mode to suppress dc-link voltage ripple by controlling the power decoupling capacitor voltages of the two multiplexed bridge arms. In interleaved mode, AISPA is increased by carrier phase shifting, which raises the equivalent switching frequency. This ensures that each bridge arm can effectively contribute to the AISPA at any output frequency. However, AISPA differs from conventional ISPA in terms of current stress and output harmonics due to its different bridge arms. In response to the above issues, this article analyzes the characteristics of the circuit in different operation modes and proposes a method for controlling the fundamental frequency current based on thermal stress balancing. The method aims to balance the thermal stress of the power switches. To achieve this, this article considers the difference in power switch models and suppresses the temperature difference of each power switch by adjusting the power decoupling capacitor voltage. In addition, this article analyzes the impact of power decoupling capacitors on switching frequency harmonics. It also determines the optimal carrier phase shift angle and evaluates the amplitude of switching frequency harmonics and THD.

The rest of this article is organized as follows. Section II describes the working principle of AISPA, explains the operating characteristics of power decoupled mode and interleaved mode, respectively, and compares AISPA with conventional ISPA in terms of current stress. To address the current stress characteristics of AISPA, the thermal stress balancing fundamental frequency current control is proposed in Section III. The implementation method of this current control method and its effect

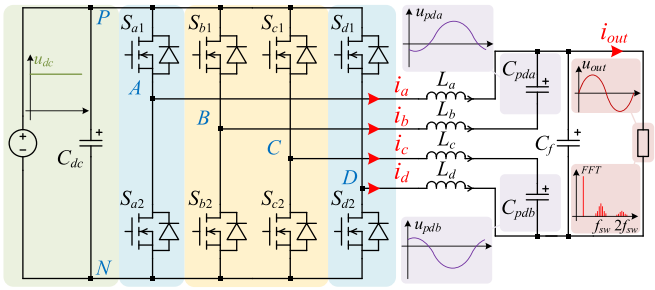

Fig. 5. Operating principle of the asymmetric interleaved switching power amplifier in power decoupling mode.

on the THD of the output voltage are explained in detail. The flowchart of the control method and the control block diagram of the whole AISPA at different output frequencies are shown. Section IV analyzes the impact of the mode-switching frequency on the performance of the AISPA and the specific calculation method of the mode-switching frequency is derived. To facilitate the subsequent design, the parameters of passive components in the circuit are also calculated. In Section V, an experimental prototype is designed to demonstrate that the AISPA and control methods proposed in the thesis are experimentally proven to be effective and correct. Finally, Section VI concludes this article.

II. Topology and Principal Analysis of AISPA Based on Arm Multiplexing

The AISPA consists of four half bridges, where $C_{\rm dc}$ represents the dc-link capacitor. S_{x1} and S_{x2} represent the power switches of each half bridge, where x can be a, b, c, and d. Similarly, L_x is the filter inductor. $C_{\rm pda}$ and $C_{\rm pdb}$ are the power decoupling capacitors, and C_f is the output filter capacitor. The AISPA has two modes of operation: power decoupling mode and interleaved mode. In power decoupling mode, the AISPA controls the reactive power of the power decoupling capacitor to suppress dc-link voltage ripple. In interleaved mode, the AISPA adjusts the carrier phase to improve the equivalent switching frequency and output waveform quality.

A. Power Decoupling Mode

The operation principle of power decoupling mode is shown in Fig. 5. In this mode, the arms of phase A and phase D function as regular arms of AISPA, whereas the arms of phase B and phase C serve as power decoupling arms. By adjusting the $u_{\rm BN}(t)$ and $u_{\rm CN}(t)$, the voltages of the power decoupling capacitors $u_{\rm pda}(t)$ and $u_{\rm pdb}(t)$ can be controlled to regulate the reactive power of the capacitors. If the sum of the instantaneous power of the power decoupling capacitor and the load remains constant, the voltage ripple in the dc-link will be suppressed significantly.

Since the switching power amplifier is a dc–ac converter, it is assumed that its output voltage $u_{\rm out}(t)$ and output current $i_{\rm out}(t)$ are expressed as the following equations:

$$\begin{cases} u_{\rm out}(t) = u_o \sin \omega_s t \\ i_{\rm out}(t) = i_o \sin(\omega_s t - \varphi) \end{cases} \tag{1}$$

where u_o and i_o represent the amplitude of the output voltage and output current, respectively. ω_s represents the angular frequency of the output voltage, and φ represents the impedance angle of the load. The instantaneous output apparent power $S_o(t)$ of the switching power amplifier can be expressed as

$$S_o(t) = u_{\rm out}(t) i_{\rm out}(t) = \frac{1}{2} u_o i_o \cos\varphi - \frac{1}{2} u_o i_o \cos(2\omega_s t - \varphi). \tag{2}$$

According to (2), the output power consists of two parts, namely the constant power $S_{\rm con}(t)$ and the fluctuating power $S_{\rm fl}(t)$. $S_{\rm con}(t)$ is equal to the average value of the active power on the load. The fluctuating power $S_{\rm fl}$(t) is equal to the difference between the instantaneous power $S_o(t)$ and the constant power $S_{\rm con}(t)$. The constant power and the fluctuating power can be expressed as

$$\begin{cases} S_{\rm con}(t) = \frac{1}{2} u_o i_o \cos\varphi \\ S_{\rm fl}(t) = -\frac{1}{2} u_o i_o \cos(2\omega_s t - \varphi). \end{cases} \tag{3}$$

The existence of fluctuating power is the core reason for the dc-link voltage ripple. In power decoupling mode, to eliminate the influence of the fluctuating power, the reactive power of the power decoupling capacitor can be controlled so that the total sum of the reactive power and fluctuating power is equal to zero. It is assumed that the power decoupling capacitors $C_{\rm pda}$ and $C_{\rm pdb}$ each carry half of the fluctuating power. The reactive power of power decoupling capacitors $S_{c1}(t)$ and $S_{c2}(t)$ is

$$\begin{cases} S_{c1}(t) = S_{c2}(t) = -\frac{1}{2} S_{fl}(t) = \frac{u_o i_o}{4} \cos(2\omega_s t - \varphi) \\ S_{c1}(t) = C_{\rm pda} u_{\rm pda}(t) \frac{d}{dt} u_{\rm pda}(t) \\ S_{c2}(t) = C_{\rm pdb} u_{\rm pdb}(t) \frac{d}{dt} u_{\rm pdb}(t). \end{cases} \tag{4}$$

To simplify the analysis, it is assumed that the capacitance of both power decoupling capacitors is C_p. Taking $C_{\rm pda}$ as an example, after simplifying (4), we can get

$$u_{\rm pda}(t) = \pm \sqrt{\frac{u_o i_o}{2\omega_s C_p} \sin^2\left(\omega_s t - \frac{\varphi}{2} + \frac{\pi}{4}\right) - \frac{u_o i_o}{4\omega_s C_p} + C_1}. \tag{5}$$

Equation (5) represents the generalized solution of $u_{\rm pda}(t)$. To reduce the voltage stress on the power decoupling capacitor, it is necessary to undertake a detailed analysis of the parameter values and the plus and minus signs in (5). C_1 is a constant generated by integral operations. To maximize the variation range of voltage of the power decoupling capacitor, its average voltage of $u_{\rm pda}(t)$ should be minimized. So C_1 should be equal to $u_o i_o / 4\omega_s C_p$. After simplifying (5), we can get

$$u_{\rm pda}(t) = \sqrt{\frac{u_o i_o}{2\omega_s C_p}} \sin\left(\omega_s t - \frac{\varphi}{2} + \frac{\pi}{4} + k\pi\right) \tag{6}$$

where k can take either 0 or 1. On the other hand, according to Kirchhoff's voltage law (KVL), the output voltage of phase B can be expressed as

$$u_{\rm BN}(t) = \frac{1}{2} u_{\rm dc} + \frac{1}{2} u_o \sin\omega_s t - u_{\rm pda}(t) - L_f C_p \frac{d^2}{dt^2} u_{\rm pda}(t) \tag{7}$$

where L_f is the inductance of the filter inductor. Since $u_{\rm BN}(t)$ cannot be higher than the dc-link voltage $u_{\rm dc}$. Therefore, the

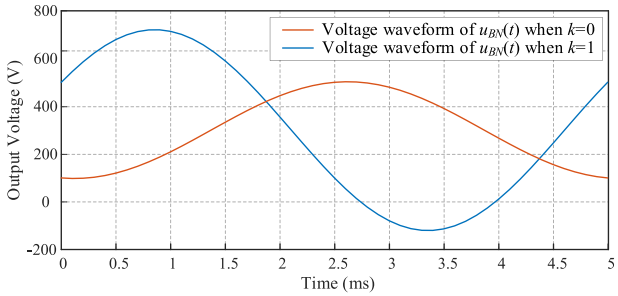

Fig. 6. Voltage waveform of $u_{\mathrm{BN}}(t)$ for different values of k. (u_o=340 V, i_o=17 A, ω_s=2π×200 rad/s, L_f=150 μH, C_p=28.2 μF, φ=0°).

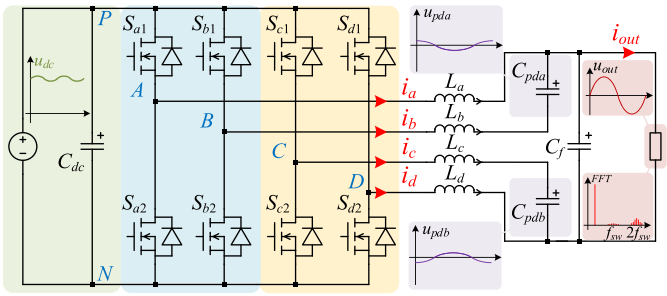

Fig. 7. Operating principle of the asymmetric interleaved switching power amplifier in interleaved mode.

reference value with a smaller amplitude should be selected. Two voltage waveforms of $u_{\mathrm{BN}}(t)$ can be obtained by substituting the two solutions of (6) into (7), respectively, as shown in Fig. 6. So, to reduce the demand for power decoupling capacitor and dc-link voltage, $u_{\mathrm{pda}}(t)$ and $u_{\mathrm{pdb}}(t)$ can be expressed as

$$\begin{cases} u_{\mathrm{pda}}(t) = \sqrt{\frac{u_o i_o}{2\omega_s C_p}} \sin\left(\omega_s t - \frac{\varphi}{2} + \frac{\pi}{4}\right) \\ u_{\mathrm{pdb}}(t) = \sqrt{\frac{u_o i_o}{2\omega_s C_p}} \sin\left(\omega_s t - \frac{\varphi}{2} - \frac{3\pi}{4}\right). \end{cases} \tag{8}$$

B. Interleaved Mode

In interleaved mode, the operating principle of AISPA is shown in Fig. 7. Different from the power decoupling mode, the AISPA in interleaved mode is no longer engaged in actively controlling the dc voltage ripple and the reactive power of the power decoupling capacitor. All bridge arms of the AISPA are now functioning as regular bridge arms. The AISPA can effectively suppress the harmonics of switching frequency and its multiples through the adjustment of the initial phase of the carrier in each bridge arm, thereby enhancing the equivalent switching frequency and the quality of the output waveform, similar to conventional ISPA.

At the switching frequency, the impedance of the power decoupling capacitor and filter capacitor is much smaller than the impedance of the filter inductor. The switching frequency equivalent circuit of the AISPA is shown in Fig. 8, which is consistent with that of the conditional ISPA. So the switching

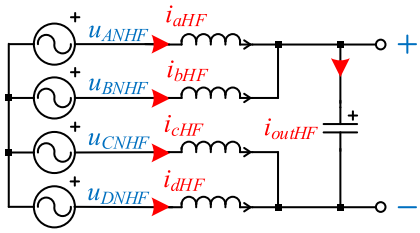

Fig. 8. Equivalent model of the asymmetric interleaved switching power amplifier at the switching frequency.

frequency and its multiples harmonics current in the filter inductor of phase A can be expressed as

$$i_{a\mathrm{HF}}(t) = \frac{1}{4L_f}\int 3u_{\mathrm{ANHF}}(t) - u_{\mathrm{BNHF}}(t) - u_{\mathrm{CNHF}}(t) - u_{\mathrm{DNHF}}(t)dt \tag{9}$$

where $u_{\mathrm{ANHF}}(t)$ represents the switching frequency and its multiples portion of the output voltage of phase A, and the same for the other bridge arms. According to Kirchhoff's current law (KCL), the sum of current harmonics of phase A and phase B can be expressed as

$$\begin{aligned} i_{\mathrm{outHF}}(t) &= i_{a\mathrm{HF}}(t) + i_{b\mathrm{HF}}(t) \\ &= \frac{1}{2L_f}\int u_{\mathrm{ANHF}}(t) + u_{\mathrm{BNHF}}(t) - u_{\mathrm{CNHF}}(t) - u_{\mathrm{DNHF}}(t)dt. \end{aligned} \tag{10}$$

To enhance the equivalent switching frequency, the AISPA adopts unipolar frequency doubling SPWM modulation with the carrier phase shifting technique. Referring to [19], based on the double Fourier transform, the switching frequency and its multiples voltage harmonics in phase A u_{ANHF} can be expressed as follows:

$$\begin{aligned} u_{\mathrm{ANHF}}(t) = {} & \frac{2u_{\mathrm{dc}}}{\pi}\sum_{m=1,3\ldots}^{\infty}(-1)^{m-1}\frac{J_0\left(\frac{mM\pi}{2}\right)}{m} \\ & \cos\left(m\omega_c t + m\theta_A\right) + \frac{2u_{\mathrm{dc}}}{\pi}\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty} \\ & (-1)^{m-1}\frac{J_n\left(\frac{mM\pi}{2}\right)}{m}\sin\left(\frac{m+n}{2}\pi\right) \\ & \cos\left(m\omega_c t + m\theta_A + n\omega_s t - \frac{n\pi}{2}\right) \end{aligned} \tag{11}$$

where M represents the modulation index, equal to the ratio of voltage amplitude to the dc-link voltage u_o/u_{dc}. ω_c is the switching angular frequency. $J_n(x)$ represents the Bessel function. θ_A is the initial phase angle of the carrier of phase A. According to the periodicity and symmetry of the trigonometric function, it is known that the harmonic amplitude of the output current in (10) can be reduced by reasonably setting the initial phase angles of the carriers of different bridge arms, thus improving the quality of the output waveform.

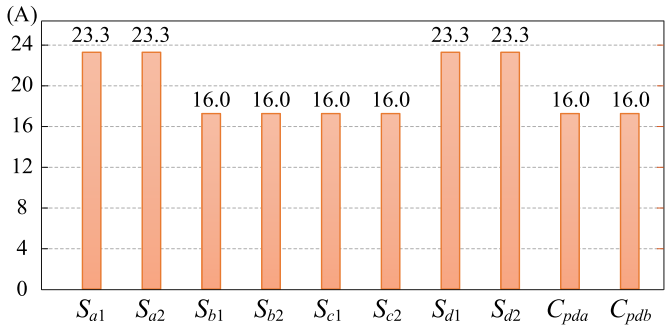

Fig. 9. Current stresses on the components of the asymmetric interleaved switching power amplifier. ($u_{\rm dc}$=600V, ω_s=2π×500 rad/s, u_o=340 V, i_o=17 A, C_p=28.2 μF).

C. Challenges From AISPA

AISPA has two different modes to cope with different operating conditions, but this also introduces some new problems. In power decoupling mode, the functions and current stresses of different bridge arms are different, which increases the difficulty of analyzing and calculating component parameters. In addition, unlike conventional ISPAs, the presence of power decoupling capacitors makes the impedance of each bridge arm of the AISPA different. This makes it impossible to spontaneously balance the fundamental frequency currents in each phase of the AISPA in interleaved mode and affects the composition of the output current harmonics.

When selecting power switches, the current stresses of the power switches in the AISPA must take into account the upper limits for both modes of operation. Since in interleaved mode, the output current of each bridge arm is less than the output current of the AISPA, the component stress calculation should be based on the power decoupling mode. In power decoupling mode, the current of the filter inductor of phase B can be calculated as follows:

$$i_b(t) = -C_p \frac{d}{dt} u_{\rm cpa}(t) = -\sqrt{\frac{u_o i_o \omega_s C_p}{2}} \cos\left(\omega_s t - \frac{\varphi}{2} + \frac{\pi}{4}\right). \tag{12}$$

According to KCL, it is possible to determine that the current of the phase A filter inductor is

$$i_a(t) = i_o \sin(\omega_s t - \varphi) + \sqrt{u_o i_o \omega_s C_p/2} \cos\left(\omega_s t - \frac{\varphi}{2} + \frac{\pi}{4}\right). \tag{13}$$

To ensure suitability for different loads, the current amplitude of $i_a(t)$ should be at its maximum when selecting a power switch, that is,

$$|i_a(t)|_{\max} = \sqrt{i_o^2 + u_o i_o \omega_s C_p/2}, \text{when} \varphi = -\pi/2. \tag{14}$$

Based on the KCL and the symmetry of topology, the current stresses on the power switches and passive components in the AISPA are shown in Fig. 9.

According to Fig. 9, it can be seen that there is a significant gap among the current stresses in different phases. This also means that the power models will not be the same when the power switches are selected.

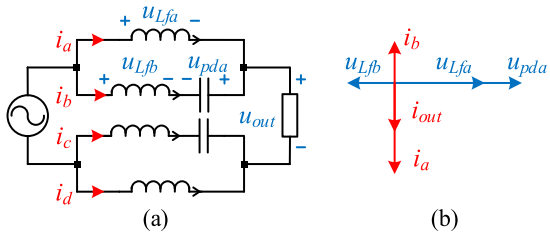

Fig. 10. The analyze of AISPA with the same modulation index of each phase. (a) Equivalent circuit. (b)Vector diagram of key voltage and current.

In terms of current control in interleaved mode, the output currents of the phases are no longer able to equal spontaneously due to the presence of the power decoupling capacitor. If the modulation indexes of the phases are identical, like conventional ISPA, the equivalent circuit of AISPA is shown in Fig. 10, along with the corresponding vector diagrams for phases A and B. Fig. 10 shows that when the modulation indexes are equal, the currents in each arm are not naturally equal, and the phases of the currents are opposite, resulting in circulating current. According to KVL, at the fundamental frequency, the relationship between the output currents of phase A and phase B can be expressed as

$$\left|\frac{i_a}{i_b}\right| = 1 - \frac{1}{\omega_s^2 L_f C_p}. \tag{15}$$

To suppress the circulating current in the interleaved mode and to balance the current stress between the phases, it is necessary to actively regulate the modulation index in phase B and phase C. However, the regulation of the modulation index changes the harmonic amplitudes at different frequencies in (11), which undoubtedly also affects the harmonics of the output current $i_{\rm out}(t)$.

Based on the above analysis, it can be seen that it is difficult to have the same model of power switches for AISPA to take into account the two modes. Moreover, in the interleaved mode, additional control of the fundamental frequency current of each bridge arm of the AISPA is required.

III. Characteristics Analysis and Control Strategy of Fundamental Frequency Current in Interleaved Mode

A. Fundamental Frequency Current Control With Thermal Stress Balancing

According to Fig. 7, the output voltage of phase B $u_{\rm BN}$ (t) can be expressed as

$$u_{\rm BN}(t) = \frac{1}{2}u_{\rm dc} + \frac{1}{2}u_o \sin\omega_s t + L_f \frac{d}{dt} i_b(t) + \frac{1}{C_p}\int_{t_0}^{t} i_b(t)dt. \tag{16}$$

It can be assumed that the output current of phase B $i_b(t)$ is α times the output current $i_{\rm out}(t)$, where α is the coefficient of shunt and $\alpha \in (0, 1)$. The output voltage of phase B can be rewritten as

$$
\begin{aligned}
&u_{\mathrm{BN}}(t)\\
&=\frac{1}{2}u_{\mathrm{dc}}+\frac{1}{2}u_o\sin\omega_s t+\alpha L_f\frac{d}{dt}i_{\mathrm{out}}(t)+\frac{\alpha}{C_p}\int_{t_0}^{t}i_{\mathrm{out}}(t)dt\\
&=\frac{1}{2}u_{\mathrm{dc}}+\frac{1}{2}u_o\sin\omega_s t+\alpha i_o\left(\omega_s L_f-\frac{1}{\omega_s C_p}\right)\cos(\omega_s t-\varphi).
\end{aligned}
\tag{17}
$$

So, the output voltage between phase B and phase C is

$$
\begin{cases}
u_{\mathrm{BC}}(t)=M_2u_{\mathrm{dc}}\sin(\omega_s t+\delta)\\
M_2=\frac{1}{u_{\mathrm{dc}}}\\
\sqrt{u_o^2+4\alpha u_o i_o(\omega_s L_f-\frac{1}{\omega_s C_p})+[2\alpha i_o(\omega_s L_f-\frac{1}{\omega_s C_p})]^2}\\
\delta=\arctan\frac{2\alpha i_o(\omega_s^2L_fC_p-1)\cos\varphi}{u_o\omega_s C_p+2\alpha i_o(\omega_s^2L_fC_p-1)\sin\varphi}.
\end{cases}
\tag{18}
$$

The derivation above shows that the bridge arms with power decoupling capacitors, namely phase B and phase C, must adjust the amplitude and phase angle of their modulation waves to regulate the current stress of each bridge arm.

As previously analyzed, the shunt coefficient α affects the current stress of power switches of each phase, and it has multiple available values. This section considers thermal stress as the key factor in determining the value of α. The current stress of power switches in phase A and phase D is larger than that of phase B and phase C in power decoupling mode. Therefore, the power switch model number for phase A and phase D is different from that of phase B and phase C. The ON-state resistance $R_{ds\ \mathrm{ON}}$ and switching energy E_{sw} of the power switches also differ. For each fundamental frequency cycle, the loss of power switch $P_{\mathrm{loss}}(t)$ can be expressed as

$$
\begin{cases}
P_{\mathrm{loss}}(t)=\frac{\omega_s}{2\pi}E_{\mathrm{loss}}(t)\\
E_{\mathrm{loss}}(t)=\int_{t_0}^{t_0+2\pi/\omega_s}i_{ds}^2(t)R_{ds\mathrm{ON}}dt+\sum E_{\mathrm{sw}}(u_{ds},i_{ds})
\end{cases}.
\tag{19}
$$

As demonstrated in (19), the loss P_{loss} is primarily influenced by the drain–source current i_{ds}, ON-state resistance $R_{ds\ \mathrm{ON}}$, and switching energy E_{sw}. Typically, for power switches of the same type, such as SiC MOSFET, there is a negative correlation between ON-state resistance $R_{ds\ \mathrm{ON}}$ and switching energy E_{SW}. Additionally, under equivalent heat dissipation conditions, the case temperature of the power switch is generally positively correlated with the loss P_{loss} of the power switch. If α is set to 0.5, the same as conventional ISPA, it will lead to a thermal stress imbalance between the power switches of phase A and phase B.

Considering the variability of device models, this article takes the thermal stress balance of power switches as the goal. With this goal, the loss of each switch in one fundamental frequency cycle should be the same. After determining parameters such as input voltage u_{dc}, power switch model, and drive resistance, the switching energy can be simplified to an expression related only to the drain–source current i_{ds} and (19) can be rewritten as

$$
\begin{cases}
P_{\mathrm{loss}}(i_{ds})=i_{ds\mathrm{rms}}^2R_{ds\mathrm{ON}}+P_{\mathrm{sw}}(i_{ds})\\
P_{\mathrm{sw}}(i_{ds})=\frac{\omega_s}{2\pi}\sum_{n=1}^{\omega_c/\omega_s}E_{\mathrm{sw}}(i_{ds}(t)).
\end{cases}
\tag{20}
$$

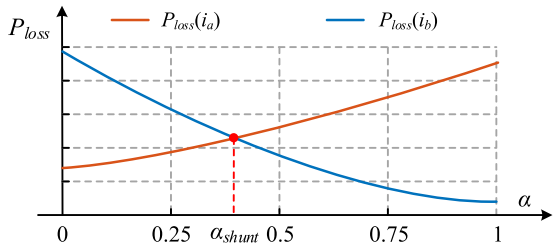

Fig. 11. Schematic diagram of the loss curves of power switches in phase A and phase B.

To calculate the loss of different phases, it is necessary to calculate i_{ds} of each phase. Taking phase A as an example, its drain–source current $i_{\mathrm{dsa}}(t)$ and $i_{\mathrm{dsb}}(t)$ can be expressed as

$$
\begin{cases}
i_{\mathrm{dsa}}(t)=(1-\alpha)i_{\mathrm{out}}(t)+i_{a\mathrm{HF}}(t)\\
i_{\mathrm{dsb}}(t)=\alpha i_{\mathrm{out}}(t)+i_{b\mathrm{HF}}(t)
\end{cases}.
\tag{21}
$$

When the output current is determined, the schematic diagram of the loss curves of power switches in phase A and phase B as α varies from 0 to 1 is shown in Fig. 11. Loss curves for different power switches can be obtained from datasheets or tests. On this basis, an offline table of the shunt coefficient α_{shunt} can be created for different output currents, so that it can be called up at any time when facing different operating conditions. Considering that the parameters of the power switch will change with the temperature and the thermal resistance of each power switch cannot be the same due to the influence of the air duct, a proportional link composed of the power switches' temperature is added to get the thermal balancing coefficient $\alpha_{\mathrm{thermal}}$. It can be expressed as

$$
\alpha_{\mathrm{thermal}}=\alpha_{\mathrm{shunt}}+k(T_{cjy}-T_{cjx})
\tag{22}
$$

where T_{cjx} and T_{cjy} represent the case temperature of power switches, measured by a negative temperature coefficient (NTC) resistor. The temperature changes slowly, and the NTC resistors do not measure the junction temperature of the power switch with high accuracy, so the proportional link needs to be adjusted slightly based on the value of $\alpha_{\mathrm{thermal}}$.

B. Analysis of Switching Frequency and Its Multiples Voltage Harmonics

The same modulation index makes voltage harmonics of different phases cancel each other out and improves the equivalent switching frequency. However, according to the analysis of fundamental frequency current, the modulation index of different phases cannot be the same in AISPA.

Since the modulation indexes of phase A and phase D are the same, when the carriers phase angles of phase A and phase D satisfy $\theta_{\mathrm{A}}=\theta_{\mathrm{D}}+180°$, the switching frequency and its multiples voltage harmonics $u_{\mathrm{ADHF}}(t)$ in $u_{\mathrm{AD}}(t)$ can be expressed as

$$
\begin{aligned}
&u_{\mathrm{ADHF}}(t)=u_{\mathrm{ANHF}}(t)-u_{\mathrm{DNHF}}(t)\\
&=\frac{4u_{dc}}{\pi}\sum_{m=2,4}^{\infty}\sum_{n=\pm1,\pm3}^{\pm\infty}(-1)^{\frac{m}{2}}\frac{J_n\left(\frac{mM\pi}{2}\right)}{m}\\
&\sin\left(m\omega_c t+m\theta_A+n\omega_s t\right).
\end{aligned}
\tag{23}
$$

To facilitate the distinction, the modulation index of phase A and phase D is M_1, which is equal to $u_o/u_{\rm dc}$, and the modulation index of phase B and phase C is M_2. The switching frequency part $u_{\rm BCHF}(t)$ in $u_{\rm BC}(t)$ can be expressed in the same way. By substituting (23) into (10), the equation can be rewritten as

$$\begin{aligned} i_{cf\rm HF}(t) &= \frac{1}{2L_f}\int u_{\rm ADHF}(t)+u_{\rm BCHF}(t)dt \\ &= \frac{2u_{\rm dc}}{\pi L_f}\sum_{m=2,4}^{\infty}\sum_{n=\pm1,\pm3}^{\pm\infty}\frac{(-1)^{\frac{m}{2}+1}}{m(m\omega_c+n\omega_s)} \\ &\quad\left[J_n\left(\frac{mM_1\pi}{2}\right)\cos\left(m\omega_c t+m\theta_A+n\omega_s t\right)\right. \\ &\quad\left.+J_n\left(\frac{mM_2\pi}{2}\right)\cos\left(m\omega_c t+m\theta_B+n\omega_s t\right)\right]. \end{aligned} \tag{24}$$

To simplify the analysis, it is assumed that the initial phase of the carrier in phase A is 0° and the initial phase of the carrier in phase B is θ. By simplifying (24), we get

$$\begin{cases} i_{cf\rm HF}(t)=\frac{2u_{\rm dc}}{\pi L_f}\sum_{m=2,4}^{\infty}\sum_{n=\pm1,\pm3}^{\pm\infty}\frac{(-1)^{m/2+1}A_{mn}(\theta)}{m(m\omega_c+n\omega_s)} \\ \cos(m\omega_c t+n\omega_s t+\gamma) \\ A_{mn}(\theta)= \\ \sqrt{J_n^2(\frac{mM_1\pi}{2})+J_n^2(\frac{mM_2\pi}{2})+2J_n(\frac{mM_1\pi}{2})J_n(\frac{mM_2\pi}{2})\cos m\theta} \\ \tan\gamma=J_n(\frac{mM_2\pi}{2})\sin m\theta/(J_n(\frac{mM_1\pi}{2}) \\ +J_n(\frac{mM_2\pi}{2})\cos m\theta) \end{cases}. \tag{25}$$

To minimize the amplitude of the switching frequency and its multiples voltage harmonics, it is necessary to minimize the value of $A_{mn}(\theta)$, where cos$m\theta$ equals -1. The harmonic amplitude decreases rapidly as m increases, and the decay property of the Bessel function is also taken into account. The amplitude of the lowest frequency harmonic, specifically at $m=2$, should be the main concern in terms of amplitude. The minimum value of $A_{2n}(\theta)$ is

$$\begin{aligned} &A_{2n}(\theta)= \\ &\sqrt{J_n^2(M_1\pi)+J_n^2(M_2\pi)+2J_n(M_1\pi)J_n(M_2\pi)\cos 2\theta} \\ &=|J_n(M_1\pi)-J_n(M_2\pi)|\ \text{when}\theta=\pi/2. \end{aligned} \tag{26}$$

It is worth mentioning that, from the results, the optimal phase shift angle of AISPA in interleaved mode is the same as that of the conventional ISPA. But the difference between the two is that the modulation index of each arm in conventional ISPA is consistent, so the harmonic at $m=2$, i.e., the switching doubling frequency harmonic can be eliminated. For the AISPA, the modulation index of each arm is not the same, and the switching doubling frequency harmonic is substantially reduced but still exists. Under no-load conditions, the switching frequency and its multiples voltage harmonics of the filter capacitor $u_{cf\rm HF}(t)$ can be expressed as

$$\begin{aligned} u_{cf\rm HF}(t) &= \frac{1}{C_f}\int i_{cf\rm HF}(t)dt \\ &= \frac{2u_{\rm dc}}{\pi L_f C_f}\sum_{m=2,4}^{\infty}\sum_{n=\pm1,\pm3}^{\pm\infty}\frac{(-1)^{m/2+1}A_{mn}(\pi/2)}{m(m\omega_c+n\omega_s)^2} \\ &\quad\sin(m\omega_c t+n\omega_s t+\gamma). \end{aligned} \tag{27}$$

To evaluate the switching frequency harmonic amplitude of the AISPA and to prevent the effects caused by the load parameters, the switching frequency and its multiples voltage harmonics of the filter capacitor under no-load conditions are used to calculate the voltage THD. The harmonic amplitude $u_{\rm har}(m,n)$ and corresponding voltage THD under different operating conditions are shown in Table I, where $L_f=150$ μH, $C_f=470$ nF, $\omega_s=2\pi\times5000$ rad/s, and $\omega_c=2\pi\times100$ krad/s. The effect of factors such as dead time on THD is ignored. From Table I, it can be seen that the waveform quality of the AISPA in interleaved mode is almost the same as that of the conventional ISPA.

C. Controller Implementation

In terms of the fundamental frequency current control method, accurate adjustment of the value of $\alpha_{\rm thermal}$ is a key factor in the effectiveness of current control. Considering the NTC resistor is not capable of accurately measuring the junction temperature of the power switch based on its characteristics. Therefore, in actual operation, the controller cannot directly obtain the accurate shunt coefficient. To tackle this issue, this article uses a blend of offline and online calculations to determine the shunt coefficient based on the power switch case temperature average. The shunt coefficient $\alpha_{\rm thermal}$ is calculated using NTC resistor measurements and data from the datasheet. It is then corrected using a proportional link to reduce the temperature difference between the case temperatures of different power switches. The operation flow is shown in Fig. 12. The calculation has the advantage of utilizing publicly available data from the datasheet to narrow the gap between initial and actual values of the shunt coefficient, reducing the time required for coefficient adjustment. Additionally, the coefficient can be fine-tuned based on the actual situation of the power switches, leading to a better reduction of temperature differences between them. To avoid a significant deviation of the shunt coefficient's initial value from the actual value, the maximum output result of the temperature loop should not exceed 10% of the initial value.

In terms of the control strategy of AISPA, the control block diagram of AISPA is shown in Fig. 13. For the output voltage loop, PI control is used to maintain the quality of the output voltage, regardless of the operating mode. In power decoupling mode, the duty cycle of phase B and phase C can be calculated by sampling the output voltage, output current, and output frequency by (8). In interleaved mode, the PI control is added to calculate the error of i_b. The carrier phase angle is set to 0 in power decoupling mode to reduce the circulating current between different phases and set to $\pi/2$ in interleaved mode to improve the equivalent switching frequency. During mode switching, the duty cycle references of phase B and phase C may change, potentially causing overvoltage and overcurrent conditions. To ensure smooth mode switching, a PI control and a low-pass filter have been added to the current loop.

TABLE I
HARMONIC AMPLITUDE AND CORRESPONDING VOLTAGE THD UNDER DIFFERENT OPERATING CONDITIONS

Operation condition	Harmonic amplitude	THD of filter capacitor voltage
Conventional ISPA	$u_{har}(m,n)=\frac{2u_{dc}}{\pi L_f C_f}\times\frac{1}{m(m\omega_c+n\omega_s)^2}\times[J_n(\frac{mM_1\pi}{2})+(-1)^{m+1}J_n(\frac{mM_1\pi}{2})]$	0.091 %
AISPA not in interleaved mode	$u_{har}(m,n)=\frac{2u_{dc}}{\pi L_f C_f}\times\frac{1}{m(m\omega_c+n\omega_s)^2}\times[J_n(\frac{mM_1\pi}{2})+J_n(\frac{mM_2\pi}{2})]$	0.945 %
AISPA in interleaved mode	$u_{har}(m,n)=\frac{2u_{dc}}{\pi L_f C_f}\times\frac{1}{m(m\omega_c+n\omega_s)^2}\times\left\lvert J_n(\frac{mM_1\pi}{2})+(-1)^{m+1}J_n(\frac{mM_2\pi}{2})\right\rvert$	0.101 %

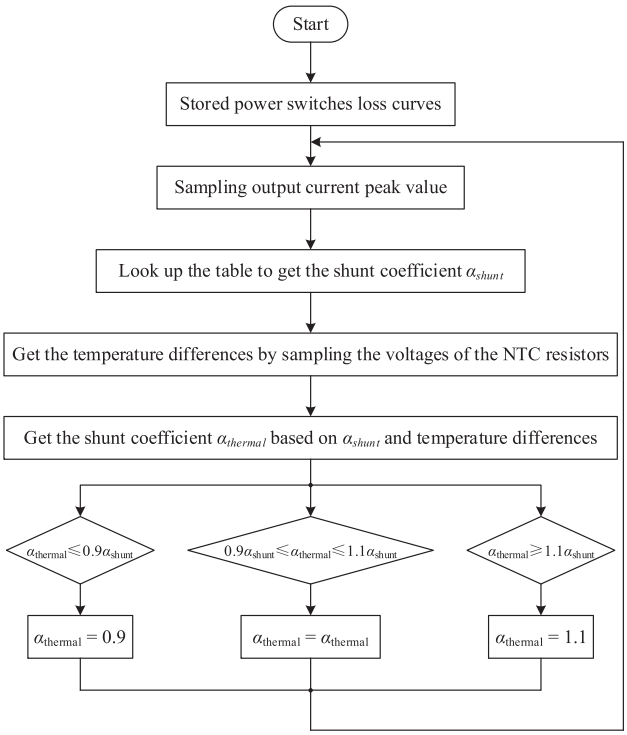

Fig. 12. Control block diagram of the asymmetric interleaved switching power amplifier.

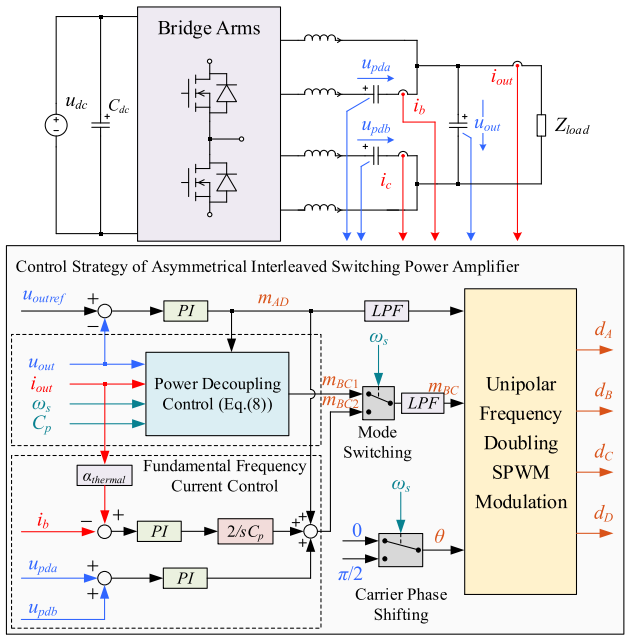

Fig. 13. Control block diagram of the asymmetric interleaved switching power amplifier.

This helps to smooth out changes in the output current of the power decoupling bridge arm by narrowing the bandwidth of the current loop. It is also believed that the voltage changes across the two power decoupling capacitors may not be completely symmetrical due to the sudden change in the duty cycle during mode switching. Therefore, PI control is applied to the voltage of the power decoupling capacitors to ensure that the voltage waveforms of the two capacitors are always symmetrical.

IV. MODE SWITCHING AND PARAMETER DESIGN

A. Mode Switching Condition

Since there are two modes of the AISPA, the mode switching conditions between modes and the overall control strategy affect the performance of the AISPA. The main purpose of the power decoupling mode is to reduce the voltage ripple amplitude of the dc link, whereas the main purpose of the interleaved mode is to reduce the THD of output voltage. With the same output power, the dc-link voltage ripple amplitude of the AISPA gradually decreases and the output voltage THD gradually increases as the output frequency increases. Therefore, in this article, the output frequency, a variable that is related to both voltage ripple amplitude and THD, is used as the switching variable between modes. When the output frequency is higher than the mode switching frequency, the AISPA switches from power decoupling mode to interleaved mode and vice versa.

The mode switching frequency affects the operating performance of the AISPA, such as dc-link voltage ripple, output voltage THD, and operating efficiency. In terms of dc-link voltage ripple, the AISPA is only affected by dc-link voltage ripple in the interleaved mode because the power decoupling mode actively suppresses dc-link voltage ripple. According to the research work presented in [20], if all the fluctuating power is borne by the dc-link capacitor, the peak value of dc-link voltage ripple Δu_{dc} can be expressed as

$$\Delta u_{\mathrm{dc}}=\frac{u_o i_o}{8\pi u_{\mathrm{dc}} f_{\mathrm{out}} C_{\mathrm{dc}}}. \tag{28}$$

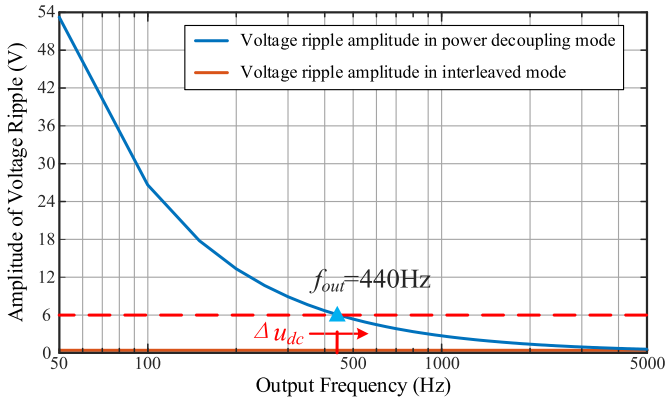

Fig. 14. Curve of the DC-link voltage ripple amplitude and output frequency of the asymmetric interleaved switching power amplifier with different modes.

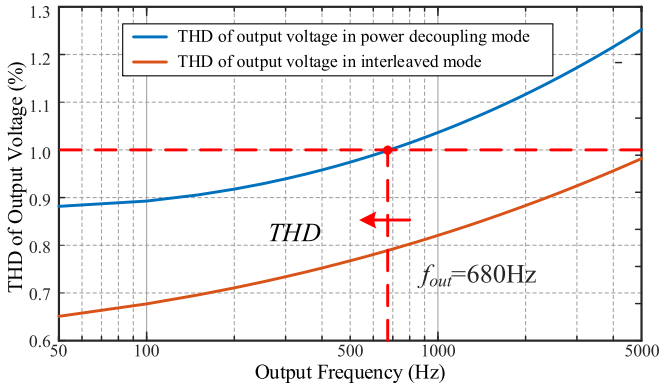

Fig. 15. Total harmonic distortion curve of the output voltage in different modes.

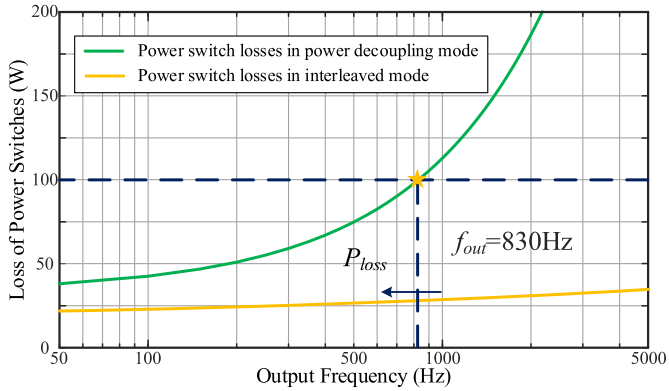

Fig. 16. Power switch loss curves of asymmetric interleaved switching power amplifier in different modes.

Therefore, the amplitude of the dc-link voltage ripple reaches its maximum value when the AISPA is output at full power and the output frequency is the lowest frequency of the interleaved mode. At full power output, based on the parameters of the prototype, the variation curve of the dc-link voltage ripple amplitude and output frequency is shown in Fig. 14. To reduce the capacitor current, the dc-link voltage ripple amplitude should not exceed 1% of the dc-link voltage, so the mode switching frequency should not be lower than 440 Hz.

In terms of THD of output voltage, the harmonic composition of the output voltage of the AISPA in different modes has been analyzed previously. Taking the power decoupling mode as an example, according to (23), it can be seen that the amplitude of the lower side frequency harmonics of the switching frequency increases with the increase of the output frequency, thus affecting the THD. With a resistive load, the gain of the output filter can be expressed as

$$G(\omega)=\left|\frac{u_{\text{out}}(\omega)}{u_{\text{AD}}(\omega)}\right|==\frac{1}{\sqrt{\left(1-\omega^2L_oC_o\right)^2+\left(\frac{\omega L_o}{R_{\text{load}}}\right)^2}} \tag{29}$$

where L_o and C_o denote the equivalent filter inductor and filter capacitor, respectively, and R_{load} denotes the resistance of the load. According to the defining equation of THD and (23), the filtered output voltage THD can be expressed as

$$\begin{aligned}\text{THD}&=\frac{1}{u_o}\sqrt{\sum_{n=2}^{\infty}u_n^2(n\omega_s)}\\&=\frac{1}{u_o}\sqrt{\sum_{n=2}^{\infty}\left|u_{\text{ADHF}}(n\omega_s)\right|^2G^2(n\omega_s)}.\end{aligned} \tag{30}$$

The THD expression in interleaved mode can be derived in the same way. In addition, considering the need to set the dead time for the power switches in practical applications. After setting the dead time to 200 ns, based on the parameters of the prototype, the THD curve of the AISPA output voltage in different modes can be obtained through simulation as shown in Fig. 15. To output the high-fidelity voltage waveform, THD should not be higher than 1%.

In terms of operating efficiency, according to (12), (13), and (21), it can be seen that in the power decoupling mode, the current stress in each bridge arm of the AISPA increases with the output frequency. In the interleaved mode, the fundamental frequency current stress of each bridge arm of the AISPA decreases substantially. The decrease in the drain–source current of the power switch can effectively reduce the conduction loss and switching loss. Based on (20) and the parameters of the prototype, the power switch loss curves in different modes can be calculated as shown in Fig. 16. To reduce the loss of AISPA, the loss of power switches should not be higher than 3% of output power.

Above all, the range of the mode switching frequency f_{switch} can be expressed as

$$\begin{cases}f_{\text{switch}}\geq 440\\ f_{\text{switch}}\leq 680\\ f_{\text{switch}}\leq 830\end{cases}\Rightarrow 440\leq f_{\text{switch}}\leq 680. \tag{31}$$

In practical application, it is considered that a certain margin should be left for the boundary conditions. Finally, the mode switching frequency is set to 500 Hz. When the output frequency is less than 500 Hz, the power amplifier operates in power decoupling mode. When the output frequency is above 500 Hz, the amplifier operates in interleaved mode.

B. Parameters of Passive Components

Passive components play a significant role in the performance of the AISPA. The parameters of the dc-link capacitor, power decoupling capacitor, filter inductor, and filter capacitor are analyzed in the following order.

The dc-link capacitor should be designed for the lowest output frequency of interleaved mode since the dc-link voltage ripple is extremely small in power decoupling mode. To decrease the capacitor current, the amplitude of the dc-link voltage ripple should not exceed 1% of the dc-link voltage, that, is

$$C_{\rm dc} \geq \frac{u_o i_o}{8\pi u_{\rm dc} f_{\rm out} \times 1\% u_{\rm dc}}. \tag{32}$$

For the power decoupling capacitor, the larger its capacitance, the more energy it can buffer. Since the amplitude of $u_{\rm BC}(t)$ cannot be higher than the dc-link voltage. Combining with (7), it can be known that

$$\begin{cases} \sqrt{u_o^2 - 4u_o Z\cos(\frac{\pi}{4} - \frac{\varphi}{2}) + 4Z^2} \leq u_{\rm dc} \\ Z = \omega_s L_f \sqrt{\frac{u_o i_o \omega_s C_p}{2}} - \sqrt{\frac{u_o i_o}{2\omega_s C_p}} \end{cases}. \tag{33}$$

Simplifying (32) gives the maximum value of C_p, which can be approximated as

$$C_p \geq \frac{2u_o i_o}{\omega_s(u_{dc}^2 - u_o^2)} {\rm when} \varphi = -\pi/2. \tag{34}$$

The filter inductor and filter capacitor affect the bandwidth and waveform quality of the AISPA. According to the circuit equivalent model, it is clear that the filter circuit of the AISPA is not coupled with the power decoupling circuit. Taking the output current i_a of phase A as an example, in one switching cycle, the switching frequency current $\Delta i_{a\rm hf}$ can be expressed as

$$\Delta i_{a\rm hf} = \frac{\pi u_{\rm dc}}{\omega_c L_f}\left[d_a(1-d_a) + \frac{1}{4}\right] \leq \frac{\pi u_{\rm dc}}{2\omega_c L_f}. \tag{35}$$

It is worth mentioning that the maximum value of the switching frequency current is the same for all filter inductors. To minimize losses caused by switching frequency current ripple, the inductor current's switching frequency ripple is typically limited to within 10% of the filter inductor's rated current [21]. Considering the rate current of phase B is smaller than that of phase A, the inductance value range of the filter inductor is

$$L_f \geq \frac{10\pi u_{\rm dc}}{\omega_c \sqrt{2u_o i_o \omega_s C_p}}. \tag{36}$$

The filter cutoff frequency is generally designed to filter out switching frequency harmonics without affecting the output bandwidth [21].

$$10\omega_{s\,\max} \leq 2\pi f_{\rm cutoff} \leq \omega_c/2. \tag{37}$$

Therefore, the value range of the filter capacitor is

$$\frac{4}{\omega_c^2 L_f} \leq C_f \leq \frac{1}{100\omega_{s\,\max}^2 L_f}. \tag{38}$$

V. Prototype Implementation and Experiment Result

An experimental prototype has been constructed, as shown in Fig. 17, to verify the topology and control method's correctness and feasibility. Table II shows the AISPA parameters, including the dc-link capacitor, which is the film capacitor SHB-700-145-4 GB1 from EACO, and the power decoupling capacitor, which is the film capacitor B32924Q3475M000 from TDK. The power switches for phase A and phase D are the SiC MOSFET C2M0025120D from Cree. The power switches for phase B and phase C are the SiC MOSFET C2M0040120D. The prototype uses a resistance voltage divider sampling circuit for the sampling and control circuits, with the ISO224 and AMC1302 from TI as the core chips. The core controller is the FPGA EP4CE10E22C8 from Altera.

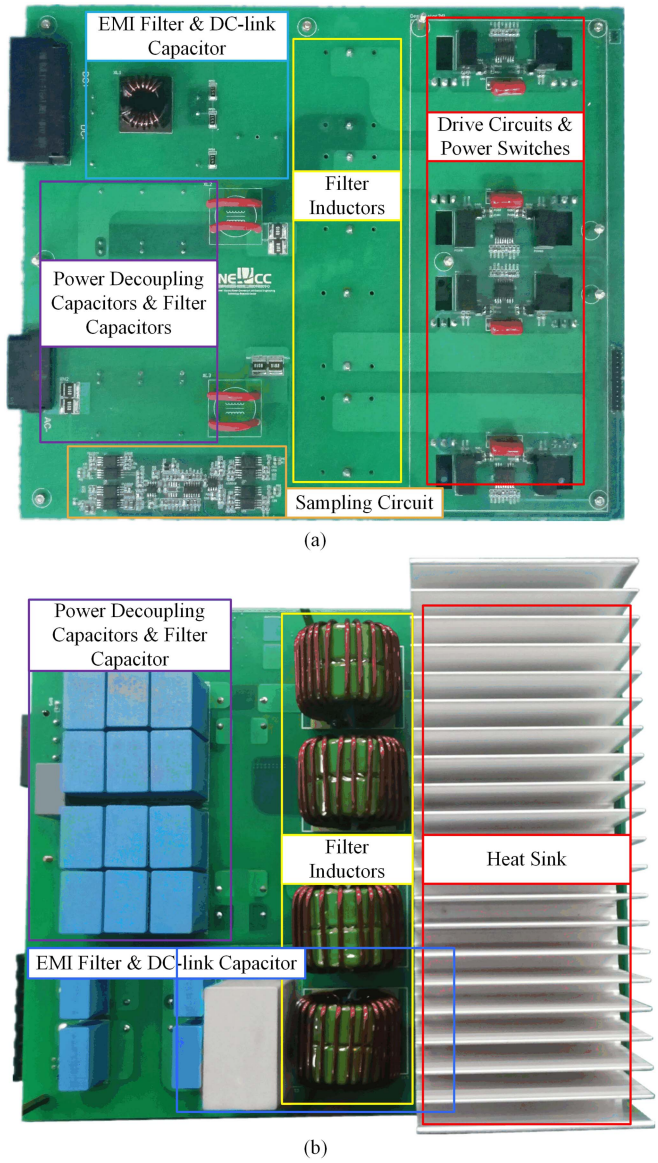

Fig. 17. Pictures of prototype. (a) Front of the prototype. (b) Back of the prototype.

When the output frequency is 50 Hz, the voltage waveforms of dc-link voltage $u_{\rm dc}(t)$, output voltage $u_{\rm out}(t)$, and power decoupling capacitor voltage $u_{\rm pda}(t)$ before and after the power decoupling operation are shown in Fig. 18(a) and (b). As can be seen from Fig. 18(a), before the power decoupling mode operation,

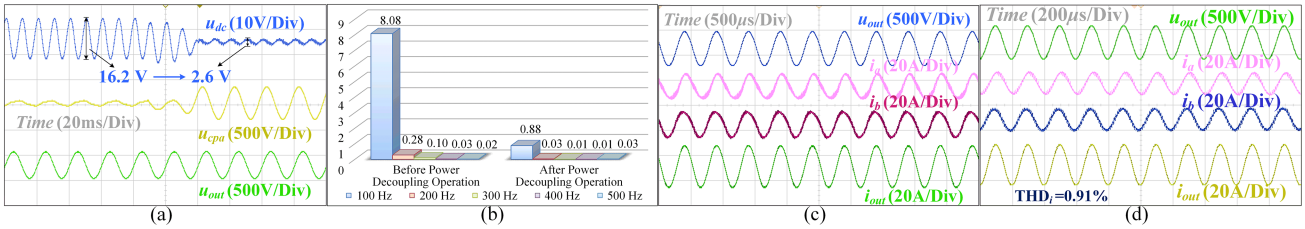

Fig. 18. Experiment waveforms of the prototype in power decoupling mode and interleaved mode. (a) Key voltage waveforms before and after power decoupling operation when the output frequency is 50 Hz. (b) Comparison of different frequency voltage ripple amplitude of $u_{\mathrm{dc}}(t)$ before and after power decoupling operation. (c) Key voltage and current waveforms when the output frequency is 2000 Hz. (d) Key voltage and current waveforms when the output frequency is 5000 Hz.

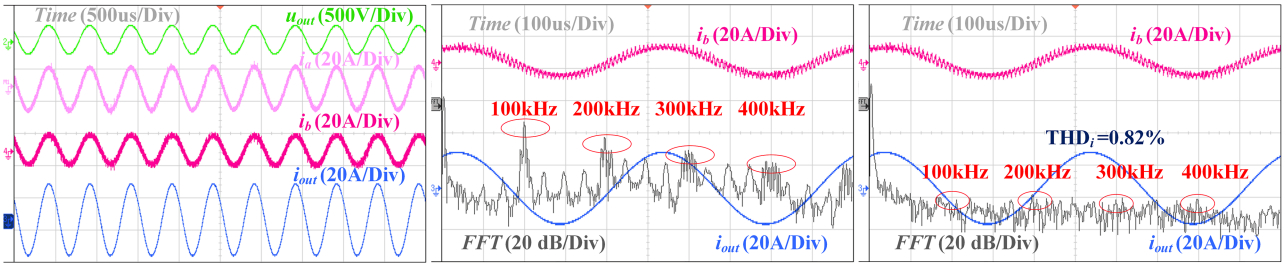

Fig. 19. Experiment waveforms of the prototype in interleaved mode ($f_{\mathrm{out}} = 2000$ Hz). (a) Key waveforms of the prototype in interleaved mode. (b) Current waveform and FFT result of the output current of phase B. (c) Current waveform and FFT result of the output current of the prototype.

TABLE II
PARAMETERS OF AISPA

Parameters	Value
Output power	3000 VA
DC-link capacitor voltage u_{dc}	600 V
DC-link capacitor C_{dc}	145 μF
Power decoupling Capacitor C_{pd}	4.7 × 6 μF
Filter inductor L_f	150 μH
Filter capacitor C_f	470 nF
Switching frequency	100 kHz
Output bandwidth f_{out}	50—5000 Hz
Mode switching frequency f_{switch}	500 Hz

the peak-to-peak value of the voltage ripple reaches 16.2 V. After the power decoupling mode operation, the peak-to-peak value of the voltage ripple is reduced to 2.6 V. The peak-to-peak value of the dc-link voltage ripple is reduced by 84.0% before and after the power decoupling operation. When the AISPA operates in interleaved mode, the voltage waveforms of output voltage $u_{\mathrm{out}}(t)$, the output current of phase A $i_a(t)$, the output current of phase B $i_b(t)$, and the output current of prototype $i_{\mathrm{out}}(t)$ are shown in Fig. 18(c) and (d) with output frequencies are 2000 Hz and 5000 Hz, respectively. The output current of arms and the fast fourier transform (FFT) results of $i_b(t)$ and $i_{\mathrm{out}}(t)$ are shown in Fig. 19. Due to the different models of power switches selected for phase A and phase B, the output currents of phase A and phase B are also different. As can be seen from the FFT results, similar to conventional ISPA, the harmonics of switching frequency and switching frequency multiples from 100 to 400 kHz are evident in the $i_b(t)$. However, the FFT result of $i_{\mathrm{out}}(t)$ shows that the harmonics of switching frequency and switching frequency multiples have been significantly suppressed.

Fig. 20 shows the process of mode switching. The experimental waveforms of AISPA switching from power decoupling mode to interleaved mode are shown in Fig. 20(a)–(c), whereas Fig. 20(d)–(f) shows the experimental waveforms of AISPA switching from interleaved mode to power decoupling mode. The experimental waveforms indicate that the current in each bridge arm fluctuates during mode switching, but the overshoot is minimal. To maintain optimal dynamic response performance and output bandwidth, the cutoff frequency of the current loop is designed to be four times the upper limit of the output frequency, rather than solely considering smooth mode switching.

Fig. 21 represents the current and temperature waveforms of the prototype before and after switching from power decoupling mode to interleaved mode. At first, there is a certain temperature difference between the switches due to the large difference in current stress. To show the effectiveness of the proposed control method, the prototype is first operated without thermal stress balancing, like the conventional ISPA. With this control target, a certain temperature difference between switches because of the inconsistent parameters. Then, it is switched to the thermal stress balancing case, where the thermal stress of the switches is further reduced.

To provide a more comprehensive comparison of the advantages and disadvantages of the different topologies, Table III lists the performance of the different topologies in terms of the number of power switches, equivalent switching frequency, current stress, size, cost, and other indicators. For comparison purposes, the switching frequency of all power switches is assumed to be the same fixed value. The table is denoted by ⋆ to indicate how well the topology works, with more ⋆ indicating better performance.

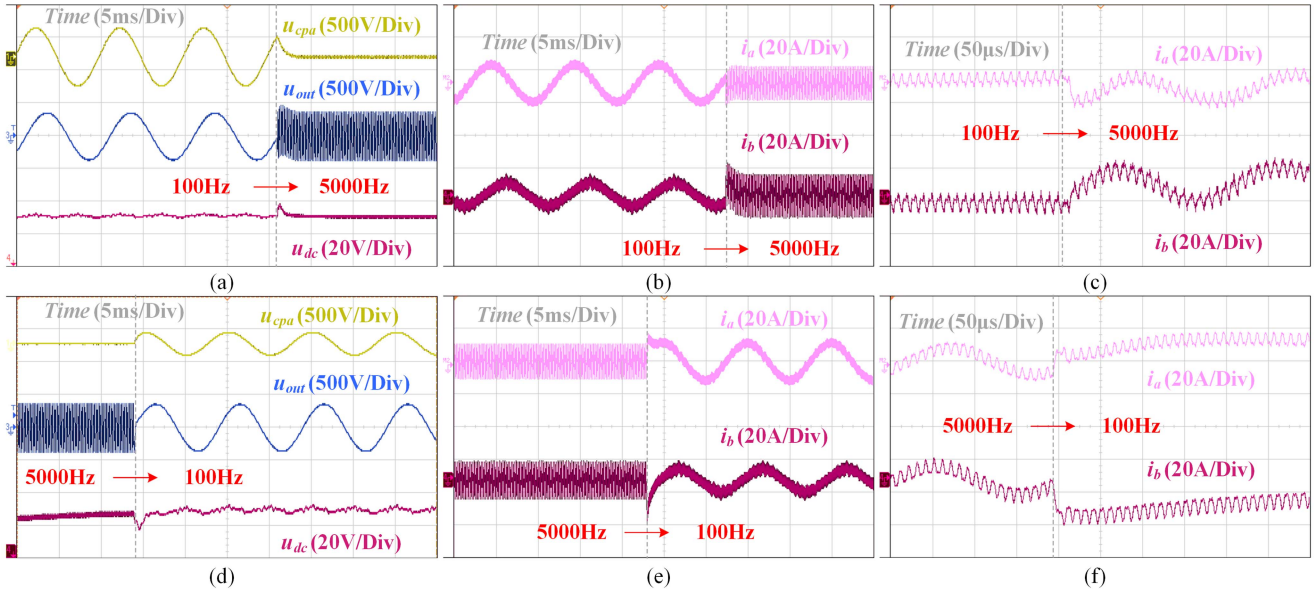

Fig. 20. Experiment waveforms of mode switching. (a)–(c) Key voltage and current waveforms of AISPA switching from power decoupling mode to interleaved mode. (d)–(f) Key voltage and current waveforms of AISPA switching from interleaved parallel mode to power decoupling mode.

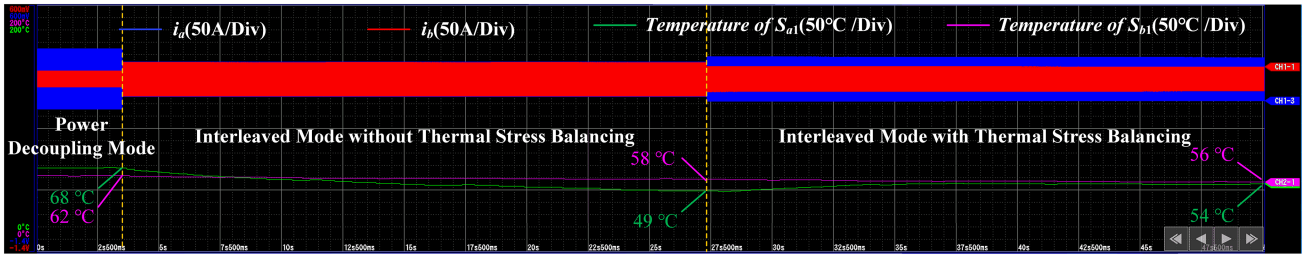

Fig. 21. Current and temperature waveforms of S_{a1} and S_{b1}.

TABLE III
MULTIFACETED PERFORMANCE COMPARISON OF DIFFERENT TOPOLOGIES

Topology	A. Single-phase inverter with buck-type power decoupling circuit	B. Single-phase interleaved inverter with buck-type power decoupling circuit	C. Enhanced single-phase inverter	D. Enhanced and interleaved single-phase inverter	E. Single-phase inverter with APF	F. Single-phase interleaved inverter with APF	G. AISPA
The number of power switches	6	10	6	10	6	10	8
Equivalent switching frequency	$2f_c$	$4f_c$	$2f_c$	$4f_c$	$2f_c$	$4f_c$	$4f_c$
Output bandwidth	★	★★	★	★★	★	★★	★★
Total current stress	★★★	★★★★	★	★★	★	★★	★★★
Power density	★★	★	★★★	★★	★★	★	★★★
Cost	★★★	★	★★★	★	★★	★	★★

In terms of efficiency, topologies with the same equivalent switching frequency are selected and compared in this article. The efficiency curves of the different topologies with respect to output frequency at rated power are shown in Fig. 22. For topology B, the efficiency of the buck power decoupling circuit decreases slightly with increasing frequency because the efficiency of the circuit is not sensitive to the voltage ripple frequency. For topologies D, F, and G, as the output frequency increases, the impedance of the power decoupling capacitor decreases, and the circulating current problem between the bridge arms gradually becomes more pronounced. Therefore, the efficiency of all three topologies decreases as the output frequency increases. However, after switching modes, all the arms of the AISPA are used to output current without the need for a power decoupling circuit. In this case, the efficiency of AISPA is slightly higher than that of topology A.

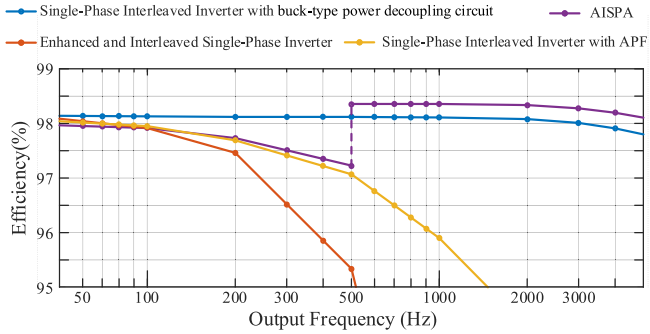

Fig. 22. Efficiency curves of different topologies with output frequency at rated power.

VI. Conclusion

This article proposes a topology for an AISPA based on arm multiplexing. The topology combines APD operation and interleaved parallel operation through the multiplexing of the arms. AISPA operates in power decoupling mode to suppress dc-link voltage ripple by controlling the power decoupling capacitor voltages of the two multiplexed bridge arms. In interleaved mode, AISPA is increased by carrier phase shifting, which raises the equivalent switching frequency. This guarantees that each bridge arm can effectively contribute to the AISPA at any output frequency. This article compares the differences between AISPA and conventional ISPA in terms of fundamental frequency current control and switching frequency current ripple. Additionally, it proposes a fundamental frequency current control strategy based on thermal stress balancing. This article also provides a detailed analysis of the control strategy and passive component parameters. The experimental prototype confirms the correctness and feasibility of the proposed topology and control method. However, to be compatible with different operating modes, AISPA needs to reserve more current stress margins in component selection, which increases the cost of AISPA.

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