An Asynchronous Geometric Sequence Array-Based Binary Search Digital Low-Dropout Regulator for $O(\log n)$-Complexity Coarse Searching Operations

Hyunjin Kim, *Graduate Student Member, IEEE*, Taehyeong Park, *Graduate Student Member, IEEE*, Seokjin Kim, *Graduate Student Member, IEEE*, Seokhee Han, *Graduate Student Member, IEEE*, Mingi Jeong, *Graduate Student Member, IEEE*, Jaekyun Kim, *Graduate Student Member, IEEE*, Inho Park, *Member, IEEE*, and Chulwoo Kim, *Senior Member, IEEE*

***Abstract*—This article presents a coarse search scheme for digital low-dropout regulators (DLDOs) that enables an $O(\log n)$-complexity of coarse searching operations. To address the effectiveness of the searching algorithm, the proposed DLDO conducts asynchronous coarse searching using the proposed binary search scheme and synchronous fine searching using a fixed-precision linear searching scheme. The chip was fabricated using a 28-nm process, and the proposed DLDO was designed to cover an output voltage (V_{OUT}) of 0.45–0.95 V with an input voltage (V_{IN}) of 0.5–1 V. The proposed DLDO regulates the output with a wide load range from 15 Ω to 450 kΩ at $V_{OUT} = 0.45$ V and $V_{IN} = 0.5$ V condition. Compared with the conventional binary search scheme, the proposed DLDO achieves an average coarse searching time improvement of 3.7 μs for light-to-heavy load-transition and 32 μs for heavy-to-light load-transition.**

***Index Terms*—Binary search, digital low-dropout regulator (DLDO), fast transient response, linear search, low-dropout regulator (LDO), power management.**

I. Introduction

In modern chip designs, as semiconductor manufacturing processes develop, the importance of fully integrated power management circuitry increases owing to increased transistor integration densities and operating speeds. Thus, process-scalable digital low-dropout regulators (DLDOs) have been widely studied to regulate the supply voltage with high current efficiency, even at low input voltage (V_{IN}).

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Hyunjin Kim, Taehyeong Park, and Seokhee Han are with the Department of Semiconductor System Engineering, Korea University, Seoul 02841, South Korea.

Seokjin Kim, Mingi Jeong, Jaekyun Kim, and Chulwoo Kim are with the Department of Electrical Engineering, Korea University, Seoul 02841, South Korea (e-mail: ckim@korea.ac.kr).

Inho Park is with the Department of Electronic Engineering, Inha University, Incheon 22212, South Korea.

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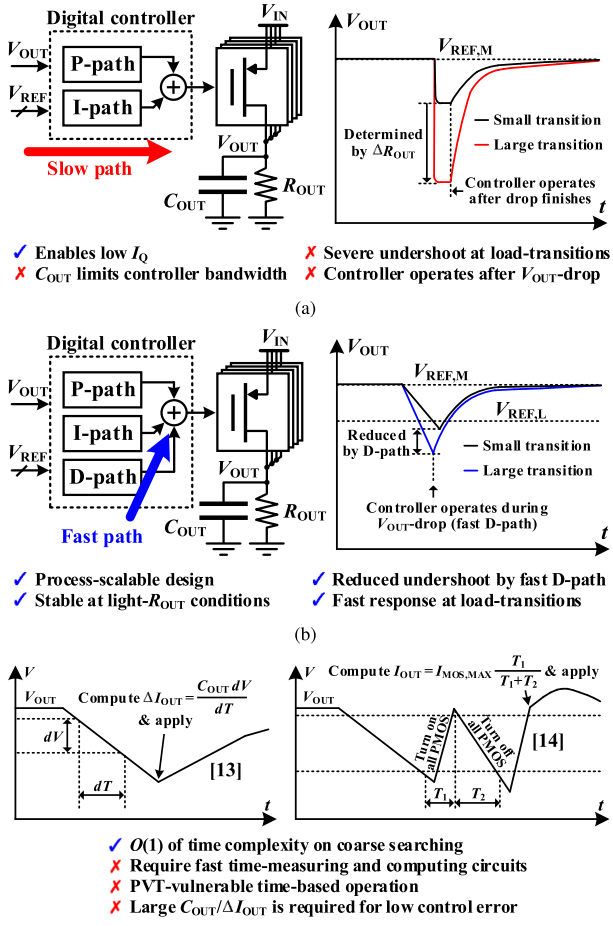

Fig. 1. Operation of the (a) DLDOs with PI control and (b) DLDOs with PID control. (c) DLDOs with computational logic [13], [14].

The operation of DLDOs can be approximated as a proportional–integral–derivative (PID) control model [1]. Thus, the conventional DLDOs are classified into two different types based on the existence of a digital derivative control loop. Fig. 1(a) shows the architecture and time-domain transient response of the proportional–integral (PI)-controlled DLDOs [2], [3], [4], [5], [6], [7], [8], [9]. Conventional DLDOs with PI

control loops were designed to achieve better figure-of-merit (FoM [10]), by using a pF-level output decoupling capacitor (C_{OUT}) along with relatively low quiescent current (I_{Q}); actually, this widely used FoM has been used to compare the performance of linearly operating analog LDOs, which is an inappropriate design metric for accurately evaluating the performance of capacitorless DLDOs. The PI-controlled DLDOs made the controllers respond after load-change events, causing large undershoots at output voltage (V_{OUT}) even for small changes in the load current (I_{OUT}). Thus, the conventional PI-controlled DLDOs reduced the V_{OUT}-drop by employing analog-assisted high-pass filters [2], [3], [6] or NMOS pass transistors [8], [9] but the V_{OUT} still drops severely under small load-transitions (only 3.5× [4] and 6× [2] load-transitions resulted in approximately 100 mV V_{OUT}-drops). In addition, for driving SRAM or digital circuits with large supply-line capacitance (>100 pF) [11], a dominant pole at the gate of the p-channel metal–oxide–semiconductor (PMOS) pass transistor requires a lowered bandwidth of their controller. Furthermore, the bandwidth of the controller should be designed by considering the stability of the lightest load condition of the DLDO, which worsens the transient response in practical applications.

Owing to the availability of response during load-change events, PID-controlled DLDOs exhibit several advantages over PI-controlled DLDOs, as shown in Fig. 1(b). First, the bandwidth of the digital controller and capacitance density of C_{OUT} increase with advancements in the CMOS fabrication process. Thus, the performance of DLDO naturally improves in modern CMOS processes. In addition, the dominant V_{OUT}-pole provides a high power-supply rejection ratio at high-frequency range [12], and a well-designed DLDO can be employed in many applications, because it operates stably under light-load conditions.

To maximize the transient-response performance over conventional DLDOs, several studies have introduced DLDOs that measure the transient V_{OUT}-slope and transform the slope into proper PMOS-codes using computational logic [13], [14], as shown in Fig. 1(c). However, they require accurate time measurements and computational logic circuits that operate within the RC-delay of the output load (R_{OUT}) and C_{OUT}, even under low-V_{IN} conditions.

To address this challenge, we propose a DLDO that activates asynchronous coarse searching with a time complexity of $O(\log n)$ in load-transient situations. The proposed DLDO also conducts synchronous fine-searching operations using a fixed 8 MHz clock, reducing the settling time (T_{settle}) by adopting a linear searching logic with 7-bit fixed precision.

The rest of this article is organized as follows. In Section II, we describe the proposed DLDO search scheme. Section III describes the top architecture of the DLDO and its circuit implementations, and Section IV presents the measurement results. Finally, Section V concludes this article.

II. Proposed Geometric Sequence Array-Based Binary Search Scheme

DLDOs were initially designed to find a suitable digital code for a PMOS array that makes the V_{OUT} close to a target reference voltage ($V_{\mathrm{REF,M}}$) by controlling the output current of the PMOS array using a linear search algorithm [7]. However, operating a DLDO with a linear search requires a high-frequency clock to operate $O(2^n)$ search cycles, where n denotes the number of digital bits of PMOS pass transistor array. Thus, this design methodology caused a strong tradeoff between the transient response and current dissipation of DLDO.

Therefore, several DLDOs have improved their transient responses by adopting fast and process-scalable binary search algorithms [15], [16], as shown in Fig. 2. These DLDOs employed binary-search-based algorithms as coarse-searching algorithms, which rapidly search the appropriate PMOS digital code during the load transient events. Thus, the digital-algorithm-based coarse search operations enabled the DLDOs to operate even under low-V_{IN} conditions with robustness in process, voltage, and temperature (PVT). However, the time complexity of these binary search schemes using a unary-weighted PMOS array is equivalent to that of the linear search algorithm using a binary-weighted PMOS array, which still has the worst case number of events as $O(n)$ [15].

Fig. 3(a) shows the operation principle of the proposed coarse search scheme. When designing the DLDO to cover the continuous R_{OUT} range by multiplying a certain width of the PMOS (W_{x}) by a constant k, the DLDO can cover a wide range of R_{OUT} values using geometric sequence PMOS-codes. If we define the R_{x} as the output resistance when V_{OUT} becomes $V_{\mathrm{REF,M}}$ with the PMOS width of W_{x}, the high and low R_{OUT} boundaries for the coarse search operation can be designed by dividing and multiplying the target-R_{OUT} of the range by $\sqrt{\mathrm{k}}$. Thus, the reference voltages that can be used for the proposed coarse search operation ($V_{\mathrm{REF,L}}$ and $V_{\mathrm{REF,H}}$) are derived by connecting the $R_{\mathrm{x}}/\sqrt{\mathrm{k}}$ and $\sqrt{\mathrm{k}}R_{\mathrm{x}}$ to the W_{x} width PMOS, and can be repetitively employed as voltage references at the overall operation range in proposed coarse search scheme. For example, when the width of the PMOS is k^3W_{x} and the V_{OUT} increases above $V_{\mathrm{REF,H}}$, the coarse search logic determines that the current R_{OUT} is larger than $R_{\mathrm{x}}/(k^2\sqrt{\mathrm{k}})$. Therefore, the proposed geometric sequence array-based binary search (GSABS) scheme enables a novel binary search scheme for DLDOs, using the $V_{\mathrm{REF,H}}$ and $V_{\mathrm{REF,L}}$ voltage references.

Fig. 3(b) illustrates the detailed coarse searching operation of the proposed DLDO. When the required width-range of PMOS changes from the k^6W_{x} range (heavy-load condition) to the k^2W_{x} range (light-load condition), V_{OUT} automatically increases above $V_{\mathrm{REF,H}}$ owing to the resistance division between on-resistance of the PMOS array and R_{OUT}. Once the load-transition is detected, the controller turns OFF all the PMOS transistors in the array to force V_{OUT} close to $V_{\mathrm{REF,M}}$ and starts the first coarse search operation with a PMOS width of k^3W_{x}. Then, owing to the larger output current of the PMOS array compared with the required I_{OUT}, V_{OUT} automatically increases above $V_{\mathrm{REF,H}}$. Thus, the controller turns OFF all the PMOS transistors again to force V_{OUT} close to $V_{\mathrm{REF,M}}$ and conducts a second search operation with a PMOS array of kW_{x} width. However, V_{OUT} drops below $V_{\mathrm{REF,L}}$ because of the insufficient width of the PMOS array, which causes the controller to turn ON a PMOS width of k^2W_{x} after resetting V_{OUT} to $V_{\mathrm{REF,M}}$.

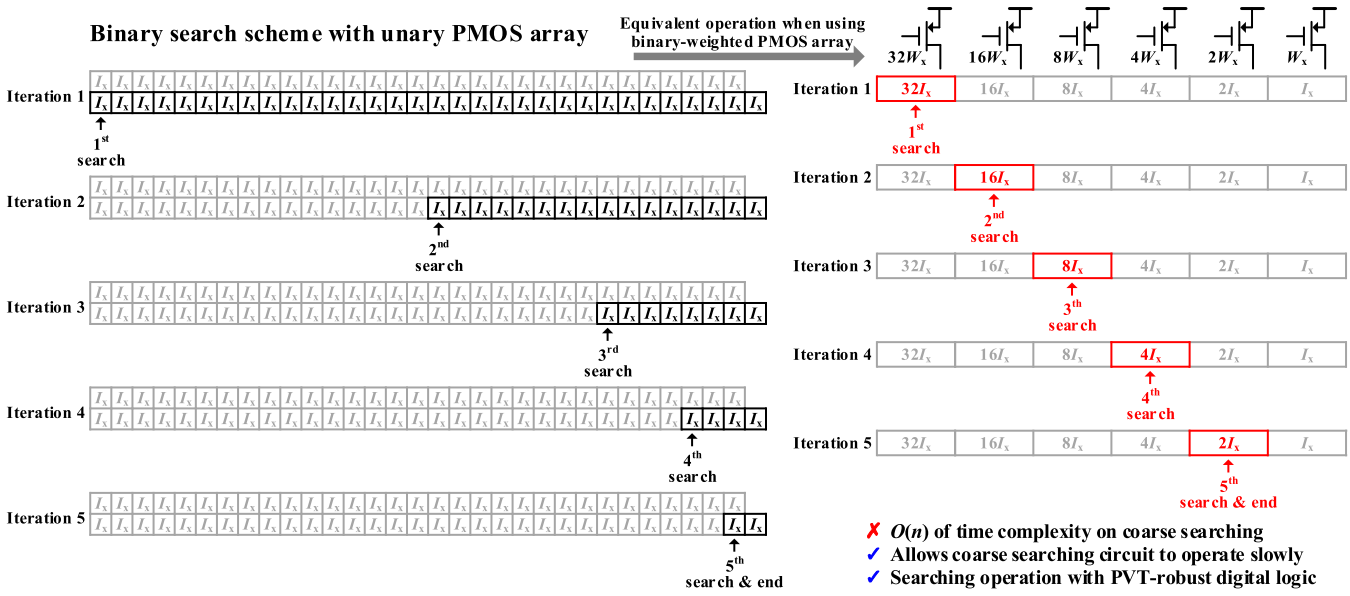

Fig. 2. Conventional binary search scheme [15], [16].

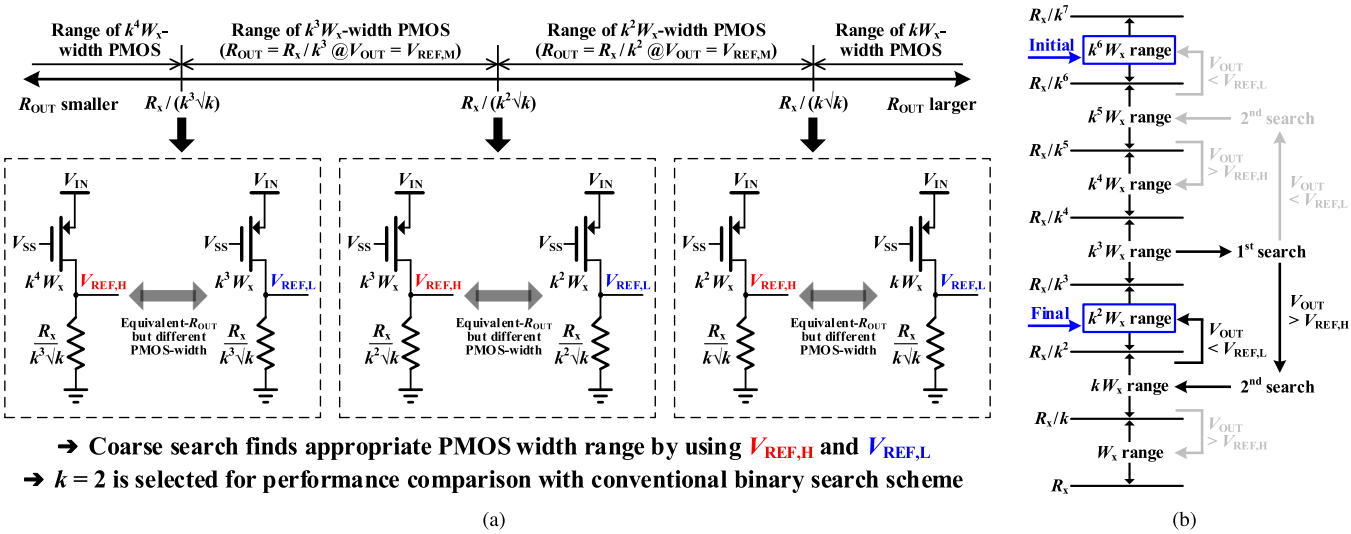

Fig. 3. (a) Operation principle of the proposed GSABS scheme. (b) Its example when the required PMOS width changes from k^6W_x to k^2W_x.

Therefore, V_{OUT} settles within the voltage window bounded by $V_{REF,L}$ and $V_{REF,H}$ within $O(\log_k n)$ event cycles. The constant k, which trades the transient response with a coarse voltage window, can be selected variously based on the target application. In this work, the proposed DLDO is implemented with $k = 2$ to directly compare the transient response performance with that of the conventional binary-search scheme.

Fig. 4 shows an operation example with a binary-weighted PMOS width from W_x to $64W_x$. Even when starting the coarse operation with an $8W_x$ range at load-transitions, the proposed GSABS scheme requires only two coarse search operations to cover a 128× wide load range. In this study, the DLDO is designed to regulate V_{OUT} with a 21-bit binary-weighted PMOS array, consisting of an effective 15-bit resolution for coarse searching operation and an additional 6-bit resolution for finer V_{OUT}-regulation. The 21-bit is determined to have the widest coarse range among comparable DLDOs, and to conduct up to four perfect coarse search cycles with the proposed GSABS scheme, while meeting small voltage ripples.

Fig. 5 shows the detailed operation of the proposed DLDO. Since the proposed GSABS scheme uses a sorted geometric sequence array, search operations can be initiated at the parent node of the binary search tree. Therefore, the operation cycles of the proposed GSABS scheme are further reduced, decreasing the coarse search time for certain light-to-heavy load-transitions (e.g., from 2^8W_x PMOS to $2^{11}W_x$ PMOS) and heavy-to-light load-transitions (e.g., from $2^{12}W_x$ PMOS to 2^7W_x PMOS). A test option for using the conventional most significant bit (MSB)-first binary search algorithm as a coarse searching scheme is also implemented in this study. This conventional

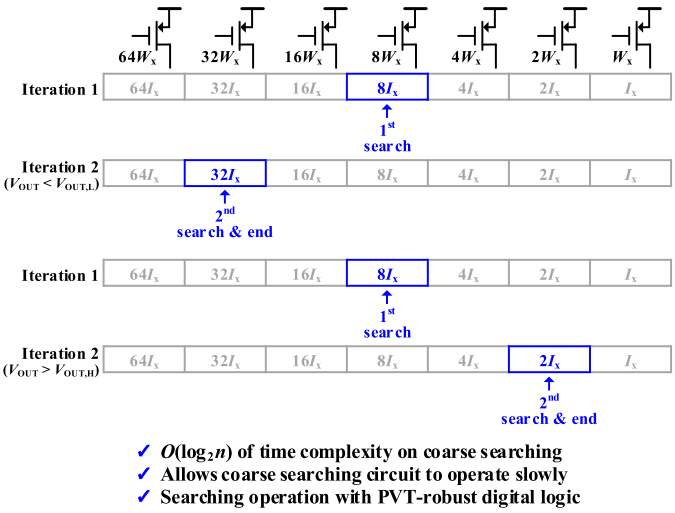

Fig. 4. Proposed GSABS scheme.

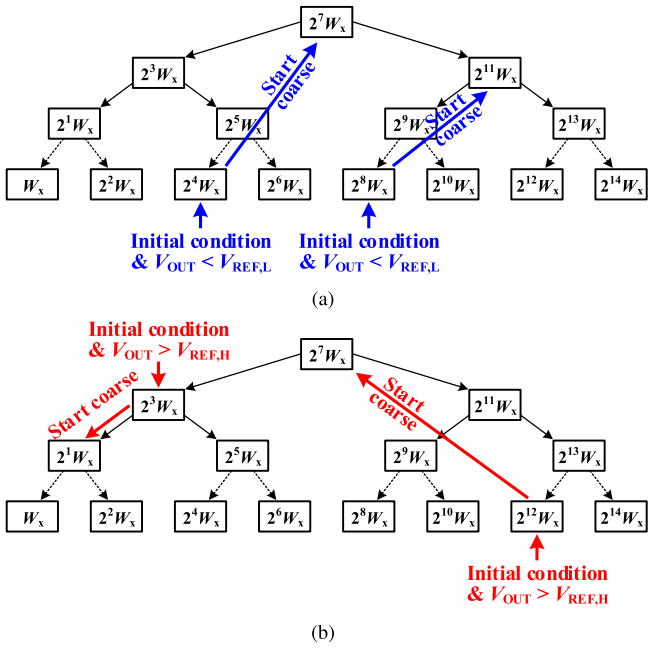

Fig. 5. Operation examples at the start of the GSABS scheme. (a) Under light-to-heavy load-transitions. (b) Under heavy-to-light load-transitions.

binary search algorithm is also designed to initiate the coarse searching operation from the parent node during heavy-to-light load-transitions.

The operation of the GSABS relies on decisions made by comparing V_{OUT} with $V_{REF,H}$ and $V_{REF,L}$. Thus, the process and temperature variations for the required $V_{REF,H}$ and $V_{REF,L}$ values of the PMOS pass transistors with widths of $2^{13}W_x$ were simulated and are plotted in Fig. 6. In this study, R_x is defined as $V_{OUT} = V_{REF,M}$ with a PMOS width of W_x. Thus, the absolute value of the required R_x automatically scales with the process and temperature variations of PMOS on-resistance. This mechanism makes the absolute values of $\sqrt{k}R_x$ and $R_x/\sqrt{k}$, which determine $V_{REF,H}$ and $V_{REF,L}$ using voltage divisions between

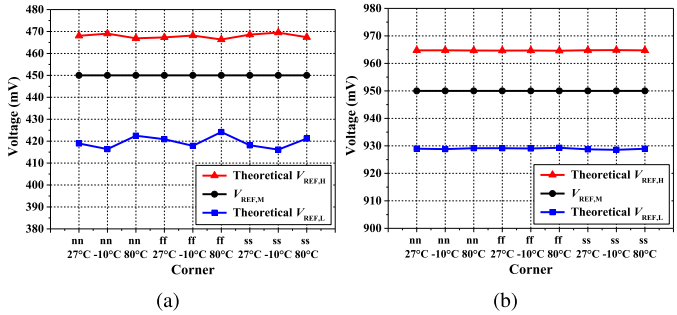

Fig. 6. Process and temperature simulations on required $V_{REF,H}$ and $V_{REF,L}$ with PMOS width of $2^{13}W_x$. (a) At $V_{REF,M} = 0.45$ V and $V_{IN} = 0.5$ V condition. (b) At $V_{REF,M} = 0.95$ V and $V_{IN} = 1$ V condition.

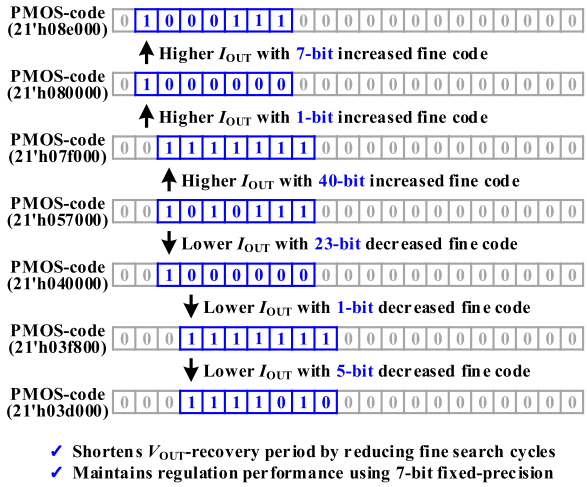

Fig. 7. Fixed-precision linear search for fine searching operation.

the PMOS array and R_{OUT}, also be scaled with the process and temperature variations. As a result, the simulation results reveal that the required $V_{REF,L}$ and $V_{REF,H}$ vary by ± 4.0 and ± 1.6 mV at $V_{IN} = 0.5$ V condition, respectively. These variations in the reference voltages are relatively smaller than the voltage window by $V_{REF,L}$ and $V_{REF,H}$, but also can cause a 1-bit searching error in the proposed algorithm. However, this small amount of voltage error during the GSABS still makes V_{OUT} close to $V_{REF,L}$ or $V_{REF,H}$, and the following fine search operation compensates the voltage error. In this work, for suppressing the additional coarse search caused by a small voltage error and increasing the timing margin of the DLDO with static comparators, 475 and 415 mV are selected as $V_{REF,H}$ and $V_{REF,L}$, respectively, at $V_{IN} = 0.5$ V and $V_{REF,M} = 0.45$ V condition. In addition, these variations decrease as V_{IN} increases, which are reduced down to ± 0.4 and ± 0.1 mV, respectively, at $V_{IN} = 1$ V condition.

Fig. 7 shows the fine search operation using a fixed-precision linear searching operation. Because coarse search operations have limited resolutions for rapid V_{OUT}-recovery, the V_{OUT} resulting from the final PMOS-code of the coarse search has a dc voltage error [15], [16]. Therefore, the synchronous linear search algorithm is performed immediately after the coarse search operation as in [16]. Although the linear search algorithm reduces

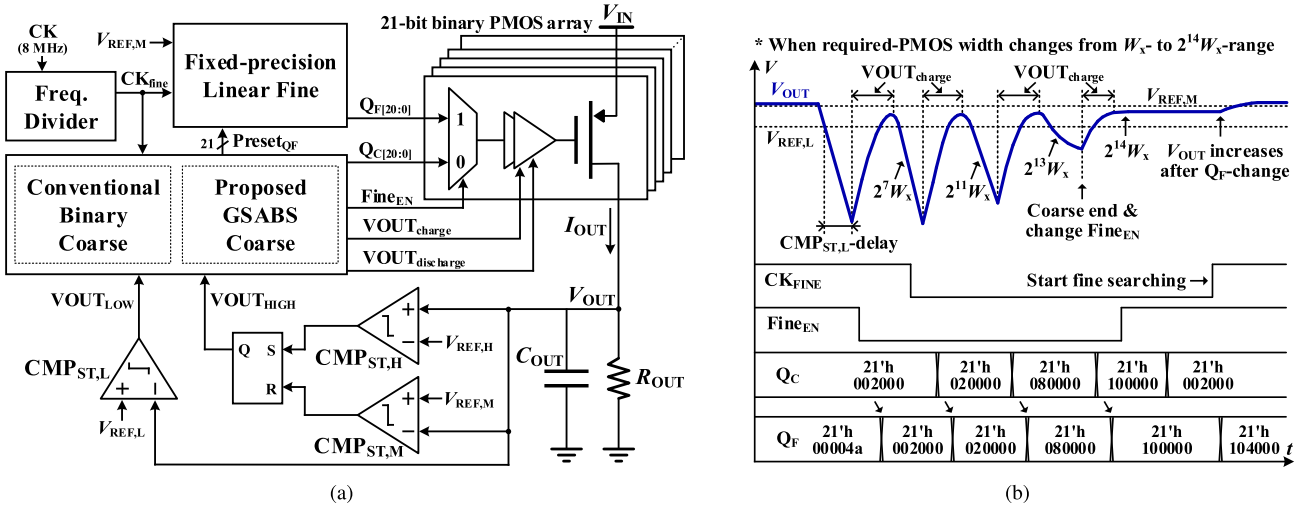

Fig. 8. (a) Top architecture. (b) Operating waveform of the proposed DLDO.

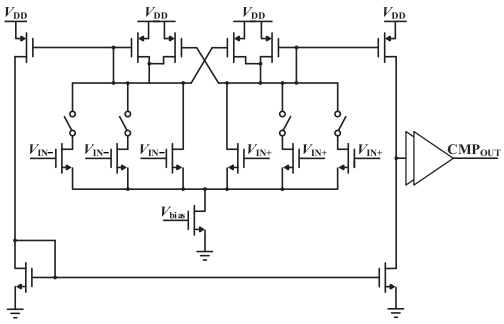

Fig. 9. Schematic diagram of the designed static comparator [17].

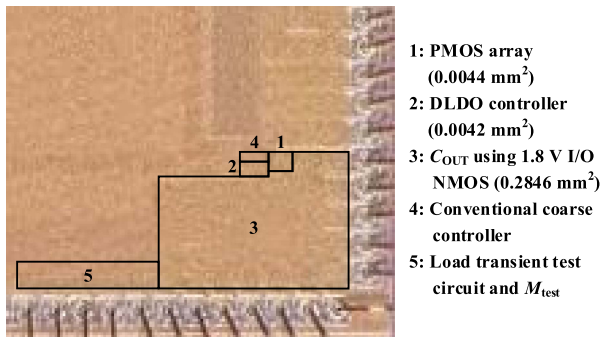

Fig. 10. Chip micrograph.

the steady-state voltage error and voltage ripples, conducting synchronous linear searching with a 21-bit PMOS array results in large T_{settle}, particularly under heavy-load conditions. Thus, the proposed DLDO conducts a regulation operation with an effective 7-bit PMOS-code and a fixed 8 MHz clock signal, targeting up to 2^{14} times faster V_{OUT}-recovery than the conventional linear search scheme [16]. In addition, for regulating V_{OUT} stably in light-load operations, a D flip-flop-based dynamic frequency divider dynamically generates an appropriate slower clock signal based on the current PMOS-code.

III. System Architecture and Circuit Details

Fig. 8(a) illustrates the overall architecture of the proposed DLDO. In the steady state, the DLDO operates with a dynamic comparator (CMP_{DY}) in a fine search circuit using the output signal of a frequency divider (CK_{fine}). At each rising edge of signal CK_{fine}, CMP_{DY} compares V_{OUT} with $V_{REF,M}$. Thus, based on the comparison results, the fine search logic circuit regulates V_{OUT} close to $V_{REF,M}$ by changing the 7-bit of total 21-bit PMOS-code. When a transient light-to-heavy (heavy-to-light) load-transition occurs, a reference voltage $V_{REF,L}$- ($V_{REF,H}$-)connected static comparator $CMP_{ST,L}$ ($CMP_{ST,H}$) detects the change in the load condition and stops the fine search by turning the $Fine_{EN}$ signal to zero. Simultaneously, the controller rapidly generates the signal $VOUT_{charge}$ ($VOUT_{discharge}$), which only turns ON the largest PMOS (turns OFF all PMOS) for fast recovery of V_{OUT}, until the signal $VOUT_{LOW}$ (signal $VOUT_{HIGH}$) becomes zero again. To start the next search operation with V_{OUT} close to $V_{REF,M}$ during heavy-to-light load-transitions, an additional $V_{REF,M}$-connected static comparator ($CMP_{ST,M}$) was employed. In addition, a 21-bit

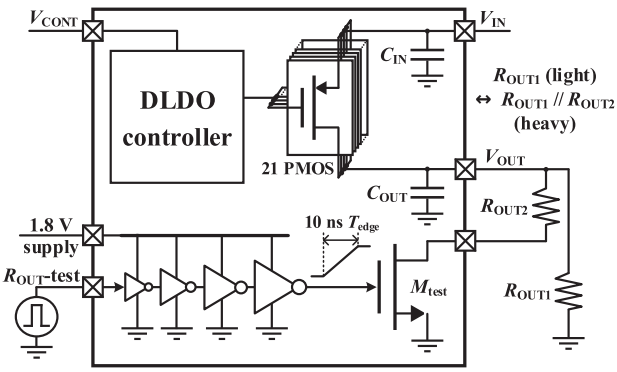

Fig. 11. Measurement setup.

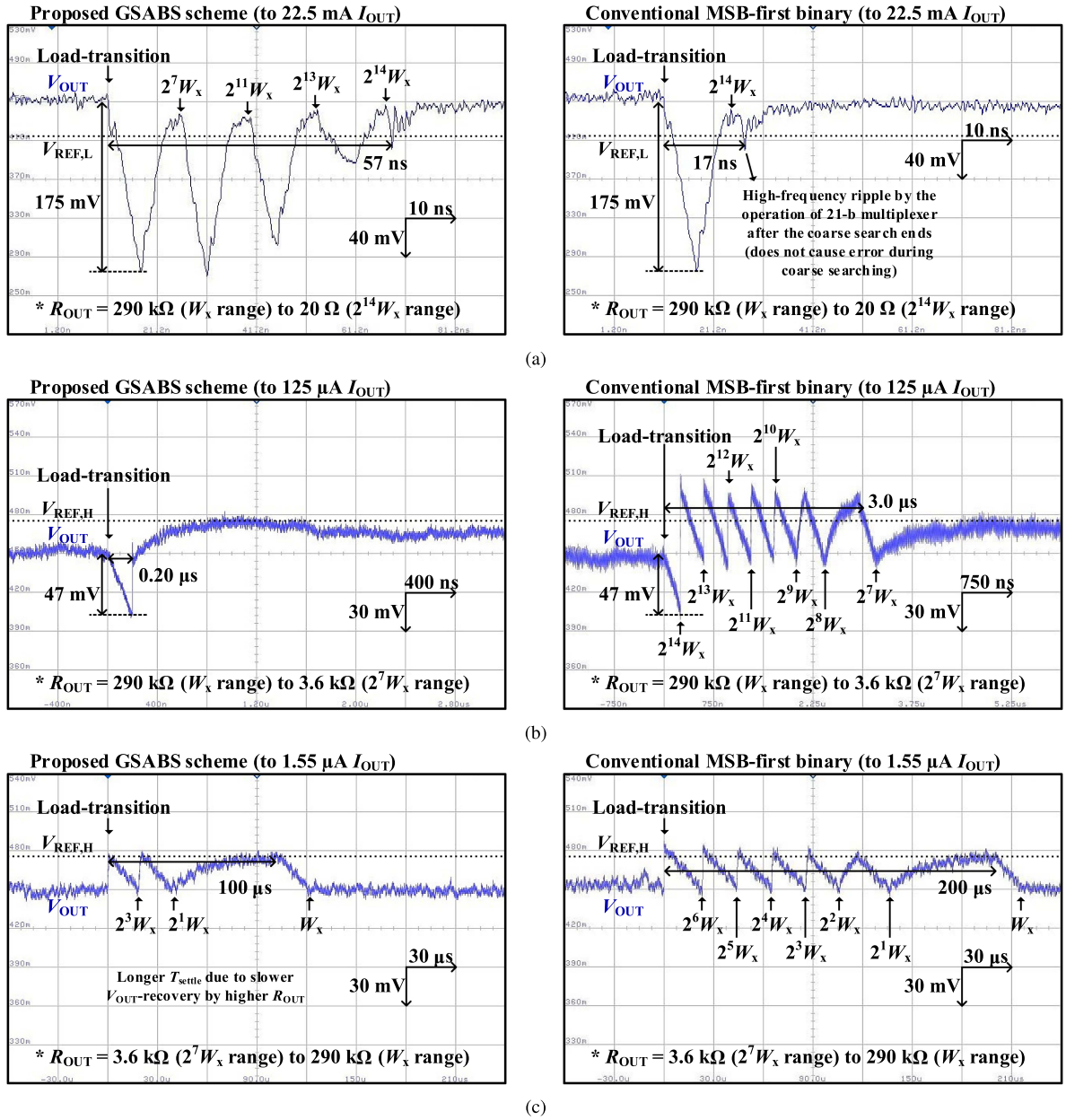

Fig. 12. Measured V_{OUT}-waveforms with conventional and proposed binary search schemes at 0.5 V V_{IN} condition under (a) 290 kΩ–20 Ω load-transition, (b) 290–3.6 kΩ load-transition, and (c) 3.6–290 kΩ load-transition.

digital multiplexer is employed to select an appropriate PMOS-code resulting from the coarse and fine search logic ($Q_{C[20:0]}$ and $Q_{F[20:0]}$) based on the $Fine_{EN}$ signal, enabling seamless mode transitions between the coarse and fine search operations.

Fig. 8(b) shows the detailed operating waveform of the proposed DLDO. Once $CMP_{ST,L}$ detects a voltage drop at V_{OUT}, the proposed DLDO recovers V_{OUT} using a $VOUT_{charge}$ signal and starts a coarse search. Thus, as shown in the waveform, the proposed DLDO starts a coarse search with 2^7W_x, but after V_{OUT} becomes lower than $V_{REF,L}$ with 2^7W_x of the PMOS pass transistor, the proposed DLDO restarts the coarse search with $2^{11}W_x$. However, V_{OUT} drops below $V_{REF,L}$ again, and the coarse search logic sets the PMOS width to $2^{13}W_x$. This coarse search is repeated once more, forcing the controller to set the PMOS width to $2^{14}W_x$. Subsequently, the controller presets the fine search logic with the PMOS-code of coarse search logic using a 21-bit signal $Preset_{QF}$, and retriggers the fine search operation by turning ON the signal $Fine_{EN}$. Fig. 9 shows a schematic diagram of the gain-boosted static comparator [17], which was employed as the $CMP_{ST,H}$, $CMP_{ST,M}$, and $CMP_{ST,L}$ in this study. The widths of the input transistors were calibrated manually to reduce the input offset voltage.

IV. Measurement Results

Fig. 10 shows a chip micrograph fabricated using 28 nm CMOS technology. To accurately measure the performance of the proposed DLDO even at light-load conditions, the 1.8 V I/O

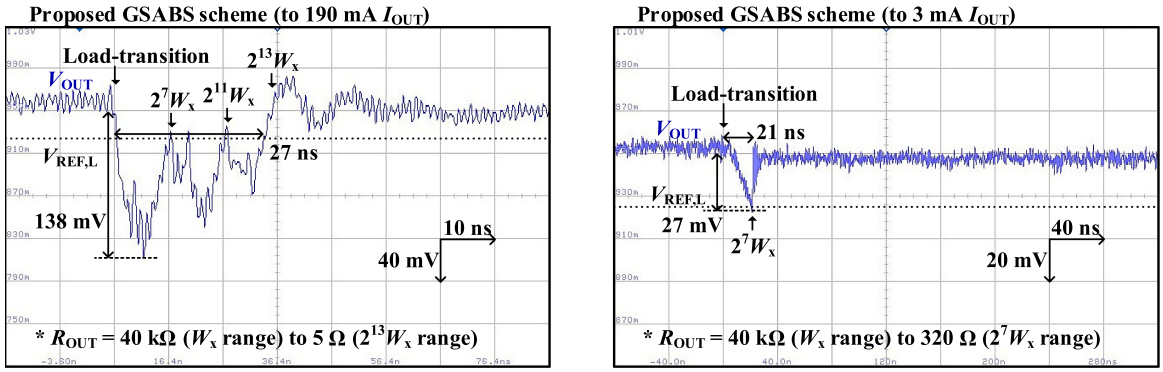

Fig. 13. Measured V_{OUT}-waveforms at 1 V V_{IN} condition.

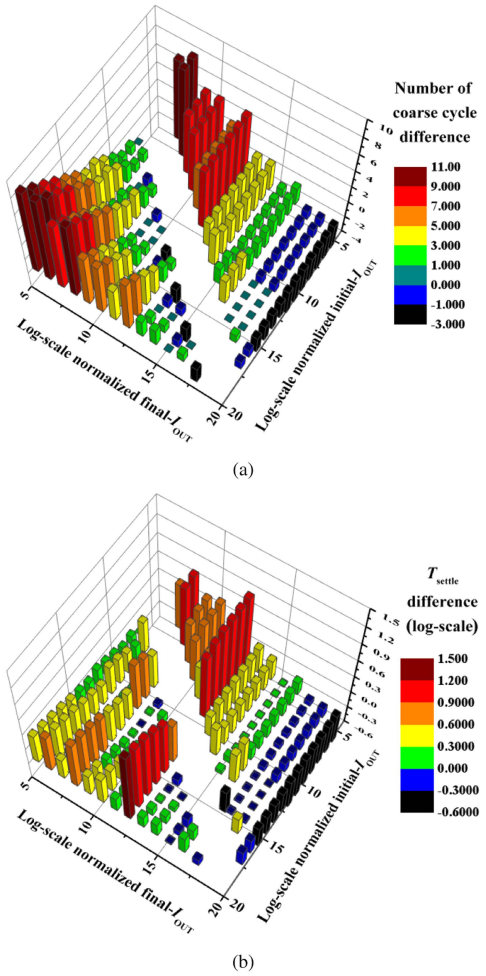

Fig. 14. Comparison between conventional and proposed binary search schemes with (a) Coarse search cycles. (b) T_{settle}.

NMOS was used as C_{OUT} to reduce the leakage current. Considering the mismatch variations between PMOS pass transistors, this work employed a 1-μm-width PMOS transistor as a unit transistor and generated lower I_{OUT} by stacking the transistors vertically. In addition, the common-centroid layout style [18] was adopted to reduce the mismatch variations. Furthermore, the 7-bit fixed-precision linear search of this work reduces the burden of matching the output current of the binary-sized PMOS pass transistors.

Fig. 11 shows the test setup used for measuring the proposed DLDO. To represent R_{OUT} during the load-transition operations, two different off-chip resistors (R_{OUT1} and R_{OUT2}) were employed. The supply voltage of the DLDO controller (V_{CONT}) was separated from the main current-path V_{IN}. During the transient performance measurement, a wide power switch (M_{test}) was turned ON to connect R_{OUT1} and R_{OUT2} in parallel. The off-chip R_{OUT2} is employed for more accurate performance measurement of the proposed DLDO. Since the R_{OUT2} is series-connected to the bond-wires, the RLC system by R_{OUT2}, bond-wire inductance, and C_{OUT} is strongly overdamped; thus, the parasitic inductance of bond-wires does not create LC-oscillation behavior at V_{OUT}. However, the limited on-chip decoupling capacitor (C_{IN}) and parasitic inductance of bond-wire cause LC-oscillation behavior at V_{IN} node [3], [6]. In particular, sharp load-transition operations within 1 ns edge time (T_{edge}) cause large peak-to-peak V_{IN}-ripples [3]. In order to measure clear V_{OUT}-waveforms, 10 ns T_{edge} and nF-level on-chip decoupling capacitor (C_{IN}) were employed. In addition, eight short bond-wires were connected in parallel to V_{IN} to suppress the LC-oscillation phenomenon. This non-DLDO effect is further reduced in practical applications due to the low inductance in flip-chip designs [3].

In this work, for measuring the various operations of the DLDO with high accuracy, four off-chip resistors were employed to implement $V_{REF,H}$, $V_{REF,M}$, and $V_{REF,L}$, through the resistive division from V_{IN}. The current consumption by these off-chip resistors is also included in the current consumption measurement. In practical applications, an on-chip resistive digital-to-analog converter can be employed to generate these reference voltages simultaneously, which can be controlled by a commander circuit that controls dynamic voltage scaling operation to produce the desired dropout voltage at each predesigned operation mode [19].

The measured waveforms of the proposed DLDO at 0.5 V_{IN} are displayed in Fig. 12. The proposed DLDO exhibits a 175 mV undershoot with 57 ns light-to-heavy T_{settle} when the R_{OUT} changes from 290 kΩ to 20 Ω. Since the MSB-first conventional binary search scheme requires one coarse search operation for this load transition case, the T_{settle} of the proposed GSABS

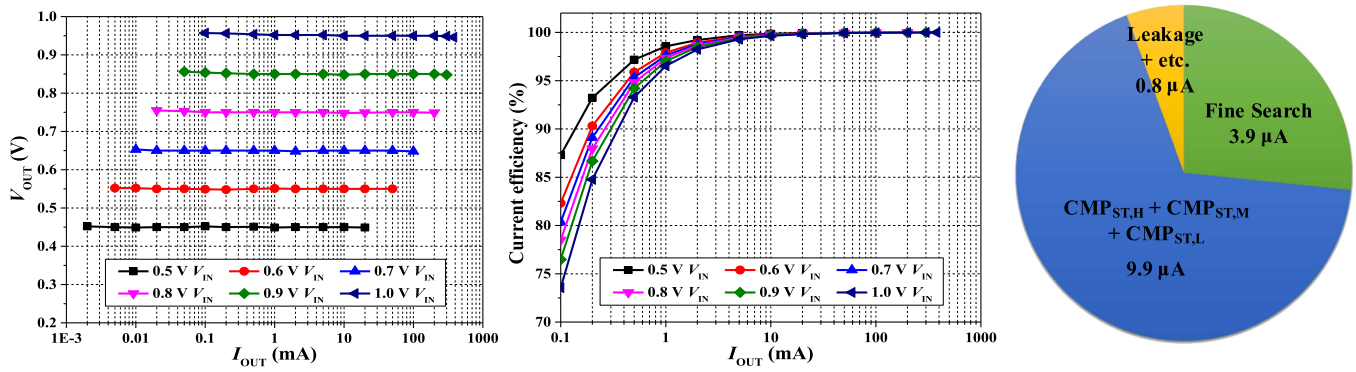

Fig. 15. (a) Measured V_{OUT} vs. I_{OUT}. (b) Measured current efficiency. (c) Measured I_Q-breakdown at $V_{OUT} = 0.45$ V and $V_{IN} = 0.5$ V.

scheme is 3.35 times longer than the conventional scheme. Nevertheless, the $O(\log n)$-complexity searching operations reduce the worst case coarse search cycles, resulting in shorter search periods in the other waveforms. Fig. 13 shows that the proposed DLDO can also regulate V_{OUT} close to $V_{REF,M}$ under the 1V V_{IN} condition. The second undershoot of the proposed DLDO was smaller than the first undershoot during the load transition from 40 kΩ to 5 Ω. This was occurred because the constant-transconductance bias condition of the $CMP_{ST,L}$, which was optimized at 0.5 V V_{IN} condition, rather aided the $CMP_{ST,L}$ in responding faster by using the first undershoot signal. This relatively low-transconductance bias condition did not cause measurement issues since the DLDO controller changes the PMOS-width after the V_{OUT} has recovered, and the static comparators respond only after V_{OUT} falls below $V_{REF,L}$ or rises above $V_{REF,H}$. In addition, as the initial and final states of V_{OUT} in each waveform are close to the $V_{REF,M}$, the waveforms indicate that the proposed DLDO successfully tracks $V_{REF,M}$ through fixed-precision fine search operations.

Fig. 14 shows the performance comparison between the binary-search-based coarse schemes. Fig. 14(a) shows the coarse search cycle difference by subtracting the number of coarse cycles of the proposed coarse scheme from that of the conventional scheme, and Fig. 14(b) indicates the T_{settle} difference by dividing the T_{settle} of the conventional scheme with that of the proposed scheme. The measurement results of 182 different load-transition cases show that the proposed GSABS scheme reduces the coarse search cycles in 126 cases and T_{settle} in 131 cases, respectively. Under the light-load to heavy-load transition scenarios, the proposed GSABS coarse search scheme has shorter search times at 55 out of 91 cases. In addition, since the conventional MSB-first search begins with the MSB PMOS-code, the conventional DLDO requires up to 10.3× coarse search time for a 4× load increase scenario. Consequently, the proposed GSABS scheme achieves an average coarse search time improvement of 3.7 μs for light-to-heavy load-transitions and 32 μs for heavy-to-light load-transitions. This performance results show that the proposed GSABS scheme is better suited for DLDO applications with wide output load ranges.

Fig. 15 shows the additional measured performance of the proposed DLDO. Fig. 15(a) shows that the DLDO successfully tracks V_{OUT} with the fine search in the steady-state conditions. In addition, the current efficiency of the proposed DLDO was measured to be up to 99.9% for every V_{IN} condition, as shown in Fig. 15(b). Fig. 15(c) presents the measured current consumption of the proposed DLDO at 0.5 V V_{IN}, 0.45 V V_{OUT}, and $R_{OUT} = 290$ kΩ condition. As the figure shows, the three static comparators predominantly consume I_Q.

Table I compares the proposed DLDO with previous DLDOs that can regulate 0.45 V V_{OUT} with a V_{IN} of 0.5 V. The proposed work is the first $O(\log_2 n)$ coarse searching DLDO that uses an asynchronous GSABS scheme with a binary-weighted PMOS array. Since the time complexity of the proposed DLDO is $O(\log_2 n)$, the number of required coarse cycles is smaller than those of other DLDOs [5], [8], [15], [16], [20] that operate without time-measurement-based computational logic. In addition, as discussed with Fig. 14(b), the proposed DLDO exhibited a relatively shorter average-T_{settle} than the conventional binary-search scheme [15], [16]. Furthermore, employing an asynchronous coarse search operation enabled the proposed DLDO to achieve a relatively better FoM than previous digital-derivative-control-based DLDOs [13], [15], [20]; the FoM value of [16] is relatively larger because of its low-I_Q-target design approach.

The computational DLDO [13] achieved a small ΔV_{OUT} with a short T_{settle}, but its time-measuring computation limited the maximum I_{OUT} ($I_{OUT,MAX}$). Moreover, the computational scheme causes control errors at light-to-heavy load-transitions; e.g., when the computational DLDO operates with 50 mV voltage window, the 0.5-V-operating time-measuring unit requires the resolution below 11.6 ps to distinguish between 5.6-mA-to-70-μA and 5.6-mA-to-140-μA I_{OUT}-transitions. In contrast, the binary-coarse search DLDOs exhibit relatively wide light-to-heavy and heavy-to-light coarse search ranges owing to their algorithm-based coarse search schemes.

Although DLDOs without digital derivative control achieved a better FoM [5], [8], the digital controllers of these DLDOs responded slowly after the sharp load-transition finished, resulting in a high V_{OUT}-drop (ΔV_{OUT}) at large and sharp load-transitions. In other words, the output digital loads require additional control schemes that suppress the I_{OUT}-scenario as consecutive but small load-step events. Then, the consecutive I_{OUT} increase

TABLE I
COMPARISON BETWEEN PREVIOUS DLDOS @$V_{IN} = 0.5$ V AND $V_{OUT} = 0.45$ V

	Y. Li TPEL'16 [20]	X. Ma TCAS1'20 [8]	J. Lee SSC-L'19 [5]	D. Kim VLSI'18 [13]	L. G. Salem JSSC'18 [15]	S. Li ISSCC'19 [16]	**This work**
Technology	130 nm	28 nm	65 nm	65 nm	65 nm	65 nm	**28 nm**
V_{IN} (V)	0.45–1.2	0.4–0.55	0.5–1	0.5–1	0.5–1	0.5–1	**0.5–1**
V_{OUT} (V)	0.35–1.15	0.35–0.5	0.45–0.95	0.45–0.95	0.3–0.45	0.4–0.95	**0.45–0.95**
Derivative control	Coarse linear*	NAND-loop (analog D-path)	N/A	TDC & Computation	Synchronous binary	Asynchronous binary	**Asynchronous GSABS**
Additional T_{settle} acceleration scheme	Synchronous binary	Coarse linear	Adaptive CK & Coarse linear	N/A	N/A	N/A	**Fixed-precision linear**
Big-O notation of coarse cycles	$O(2^n)$	$O(2^n)$	$O(2^n)$	$O(1)$	$O(n)$	$O(n)$	$\boldsymbol{O(\log_2 n)}$
Coarse cycles	1–8	1–20	1–31	1**	1–7	1–14	**1–4**
Coarse range	8×	68×	31×	255×**	255×	16,000×	**30,000×**
C_{OUT} (pF)	1,000	24	100	100	400	100,000	**1,100**
$I_{OUT,MAX}$ (mA)	1.5	40	25	5.6	1	0.27	**30**
I_Q (μA)	8.9	0.81	25	18.1	14	0.000745	**14.6**
T_{edge} (ns)	100	0.1	400	0.1	1	500	**10**
ΔV_{OUT} (mV) @ΔI_{OUT} (mA)	100 @1.48 (75×)	117 @20 (41×)	47 @20 (9×)	54.8 @2.3 (33.9×)	40 @1.06 (27.5×)	76.5 @0.27 (380,000×)	**47 @0.167 (80.6×) 175 @22.5 (14,500×)**
T_{settle} (ns)	1,600	9,000	1,200	26.4	100	48,000	**57**
FoM*** (ps)	406	0.0057	0.29	18.8	199	78.2	**5.6**

* D-path due to large $C_{OUT}/I_{OUT,MAX}$ ** Search causes errors at heavy-to-light transitions *** $C_{OUT}(\Delta V_{OUT}/\Delta I_{OUT})(I_Q/\Delta I_{OUT})$ [10]

scenarios will cost longer T_{settle} than those reported in the table.

In addition, the proposed GSABS scheme can be employed in parallel with conventional analog derivative loops [2], [8]. This analog–digital hybrid approach to derivative loops can further enhance the performance of the DLDO, which can be explored in future works.

V. CONCLUSION

This article proposed an $O(\log_2 n)$ coarse-searching DLDO that regulates $V_{OUT} = 0.45$–0.95 V with $V_{IN} = 0.5$–1 V. The proposed DLDO also adopts an asynchronous GSABS coarse search and a synchronous fixed-precision linear fine search to achieve both fast T_{settle} and small dc errors. The proposed DLDO achieved a T_{settle} of 57 ns and an FoM of 5.6 ps.

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Hyunjin Kim (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering and the M.S. degree in semiconductor system engineering in 2019 and 2021, respectively, from Korea University, Seoul, South Korea, where he is currently working toward the Ph.D. degree in semiconductor system engineering.

He has been working on power management integrated circuit design, especially low-power CMOS analog circuits, energy harvesting systems, switched-capacitor circuits, linear dropout regulators, and hybrid dc–dc converters. In addition, his Ph.D. Research includes a probabilistic computing system, prime factorization, and deep learning acceleration algorithms.

Taehyeong Park (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 2019, and the M.S. degree in semiconductor system engineering in 2022 from Korea University, Seoul, where he is currently working toward the Ph.D. degree in semiconductor system engineering.

His research interests include integrated power management system designs, low-power CMOS analog circuit designs, and dc–dc converters.

Seokjin Kim (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering in 2023 from Korea University, Seoul, South Korea, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include integrated power management system designs and low-power CMOS analog circuit designs.

Seokhee Han (Graduate Student Member, IEEE) received the B.S. degree in semiconductor system engineering in 2023 from Korea University, Seoul, South Korea, where he is currently working toward the M.S. degree in semiconductor system engineering.

His research interests include integrated power management system designs and low-power CMOS analog circuit designs, and dc–dc power converter.

Mingi Jeong (Graduate Student Member, IEEE) received the B.S. in industrial and management engineering and electronics engineering in 2023 from Korea University, Seoul, South Korea, where he is currently working toward the combined M.S./Ph.D. degree in semiconductor system engineering.

His research interests include integrated power management system designs and low-power CMOS analog circuit designs, and dc–dc power converter.

Jaekyun Kim (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering in 2024 from Korea University, Seoul, South Korea where he is currently working toward the M.S. degree in electrical engineering.

His research interests include integrated power management system designs and low-power CMOS analog circuit designs, and hybrid dc–dc power converters.

Inho Park (Member, IEEE) received the B.S. and Ph. D. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2016 and 2023, respectively.

Since 2023, he has been with the Department of Electronic Engineering, Inha University, Incheon, South Korea, where he is currently an Assistant Professor. In 2023, he was a Senior Enginner with Samsung Electronics, Suwon, South Korea. His research interests include integrated power management system designs, high-voltage siliconbased power converters, hybrid dc–dc converter topologies and methodologies, and energy-harvesting systems.

Dr. Park was the recipient of the IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award in 2021 and 2022 and the Honorable Mention Prize at 25th Humantech Paper Award hosted by Samsung Electronics in 2019.

Chulwoo Kim (Senior Member, IEEE) received B.S. and M.S. degrees in electronics engineering from Korea University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana–Champaign, IL, USA, in 2001.

Since 2002, he has been with the School of Electrical Engineering, Korea University, where he is currently a Professor. In 1999, he worked as a Summer Intern with the Design Technology, Intel Corporation, Santa Clara, CA, USA. In May 2001, he joined IBM Microelectronics Division, Austin, TX, USA, where he was involved in cell processor design. In 2012, he was a Visiting Professor with the University of California, Los Angeles, CA, USA, in 2008 and the University of California, Santa Cruz, CA. He has coauthored two books: *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 4th edition 2014) and *High-Bandwidth Memory Interface* (Springer, 2013). His current research interests include wireline transceivers, memory, power management, and data converters.

Dr. Kim was the recipient of the Samsung Humantech Thesis Contest Bronze Award in 1996, International Symposium on Low Power Electronics and Design (ISLPED) in 2001 and 2014, Design Automation Conference (DAC) Student Design Contest Award in 2002, Semiconductor Research Corporation (SRC) Inventor Recognition Awards in 2002, Young Scientist Award from the Ministry of Science and Technology, South Korea, in 2003, Seoktop Award for excellence in teaching (2006 and 2011), Asia and South Pacific (ASP)-DAC Best Design Award in 2008, Special Feature Award in 2014, and Korea Semiconductor Design Contest: Ministry of Trade, Industry, and Energy Award in 2013. From 2015 to 2016, he was selected as a Distinguished Lecturer of the IEEE Solid-State Circuits Society. He served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference. He served as a Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS. He serves on the Editorial Board for IEEE TRANSACTIONS ON VLSI SYSTEMS.