A Wide Pulse-Repetitive-Frequency Range Pulsed Power Supply With Improved Dynamic Response and Efficiency

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***Abstract*—The transmitter/receiver modules in active phased array radar systems is powered by a pulsed power supply (PPS). In this article, an active capacitor converter (ACC) based PPS is adopted for wide pulse repetition frequency (PRF) range, and the design method is presented to minimize the output capacitance and storage capacitance. Since the demand of the storage capacitance is inversely proportional to the PRF, the ACC is redundant at high PRF, and thus, a smart disabling control of the ACC is proposed to shut down the ACC at high PRF to improve the efficiency of the PPS. To suppress the PRF ripple in the input current, the bandwidth of the voltage loop of the PPS is designed to be very slow, which leads to poor dynamic response. To address this issue, the dynamic response enhancement control strategies are proposed, including the output current feedforward control and the output voltage limiting control. Finally, a prototype of the PPS with pulsed power of 2.8 kW and PRF ranging from 50 Hz to 2 kHz is fabricated and tested in the lab. The experimental results are provided to verify the effectiveness of the control strategies of the PPS with wide PRF range.**

***Index Terms*—Active capacitor converter (ACC), dynamic response, pulse repetition frequency (PRF), pulsed power supply (PPS).**

I. Introduction

THE active phased array radar (APAR) features high bandwidth, long detection range, and wide operational frequency band [1], and it is suitable for the applications such as navigation [2], positioning [3], and search and rescue [4]. The antenna array is one of the crucial components in the APAR, which is composed of thousands of antenna elements. Each antenna element contains transmitter/ receiver (T/R) modules and active power circuits [5]. The T/R module consumes high current during the pulse duration and almost no power during the pulse interval [6], so the power supply for the T/R module is a pulsed power supply (PPS) [7]. For different purposes, the APAR operates in different frequency bands. Specifically, for remote sensing, the operational frequency range is very wide, covering various bands such as L-band, C-band, and X-band [8]. Consequently, the pulse repetition frequency (PRF) of T/R modules is wide, ranging from a few hertz to several tens of kilohertz [9].

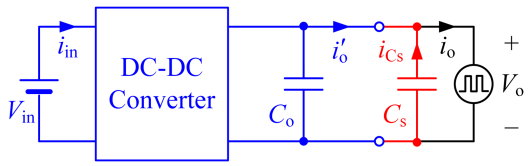

Fig. 1. Configurations of the PPS with large capacity storage capacitor.

In order to reduce the peak power of the power system, it is essential to prevent the PRF current ripple from propagating into the input side of the PPS. Thus, the input current of the PPS is flat [10], [11]. However, the output current of the PPS is pulsed. As a result, the instantaneous input and output power of the PPS is unequal, necessitating the use of energy storage units. The simple method is connecting storage capacitor C_s at the output side of the PPS, as shown in Fig. 1 [12], [13], [14]. For obtaining a high accuracy of the transmitted signal from the T/R modules, the output voltage of the PPS should have a very small drop and recover very fast [15], [16]. Thus, the storage capacitance is large. Particularly, if the PRF is very low, the required storage capacitance is very large, which is not suitable for the applications such as vessels, aviation and aerospace that have strict requirements on volume and weight.

In [17], [18], and [19], an active capacitor converter (ACC) is introduced into the PPS to replace the output storage capacitor, which is a kind of active power decoupling topology, as shown in Fig. 2. Since the storage capacitor C_s in the ACC is not connected at the output side of the PPS, its voltage ripple is not constrained by the output voltage drop, and can be intentionally increased. Thus, the storage capacitance could be greatly reduced, thereby reducing the size of the PPS.

During the operation of the APAR, the amplitude of the output signal is frequently changing, which imposes stringent requirements on the dynamic response of the PPS. Due to the small storage capacitance and low bandwidth of the voltage loop of the dc–dc converter, the dynamic response of the PPS is very poor. In addition, when the PRF range is wide, especially when it

Received 25 January 2024; revised 10 May 2024 and 20 July 2024; accepted 31 August 2024. Date of publication 4 September 2024; date of current version 12 December 2024. Recommended for publication by Associate Editor S. Kapat. *(Corresponding author: Xinbo Ruan.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3454384.

Digital Object Identifier 10.1109/TPEL.2024.3454384

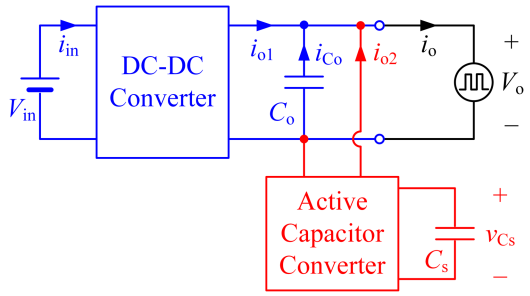

Fig. 2. Configurations of the ACC-based PPS.

covers both low and high PRF, the ACC- based PPS encounters some issues. First, the inductor in the ACC limits the tracking ability of the pulsed current, especially at high PRF. Second, the required storage capacitance is inversely proportional to the PRF, and it is relatively large at low PRF while it is very small at high PRF. So, the ACC is redundant at high PRF while bringing additional losses.

This article aims to address the aforementioned issues, and the major contributions are as follows.

1) The design method of the ACC is presented, and the minimum required output capacitance and the inductance in the ACC are derived to ensure the ACC can track the pulsed current.
2) A smart disabling control of the ACC is proposed to enhance the efficiency of the PPS at high PRF.
3) The dynamic response enhancement control strategies are proposed for the wide PRF range PPS during load transients, including the output current feedforward control and the output voltage limiting control.

The rest of this article is organized as follows. In Section II, the basic principles and circuit topology of the wide PRF range PPS is briefly introduced. In Section III, the relationship of the minimum required output capacitance and the inductance in the ACC are discussed, and the design method of the wide PRF range PPS is given. In Section IV, the redundancy of the ACC at high PRF is analyzed, and a smart disabling control of the ACC and its implementation circuit are given for enhancing the efficiency at high PRF. Additionally, the dynamic response enhancement control strategies including the output current feedforward control and the output voltage limiting control are proposed. In Section V, a prototype of the wide PRF range PPS is fabricated and tested in the lab, and the experiment results confirms the correctness of theoretical analysis and the effectiveness of the proposed control strategies. Finally, Section VI concludes this article.

II. Basic Principles and Circuit Topology of the Wide PRF Range PPS

Fig. 2 has given the configuration of the ACC-based PPS, which consists of a dc–dc converter and an ACC. The ACC is connected in parallel at the output side of the PPS to provide the pulsed power, and the dc–dc converter only supplies the average power.

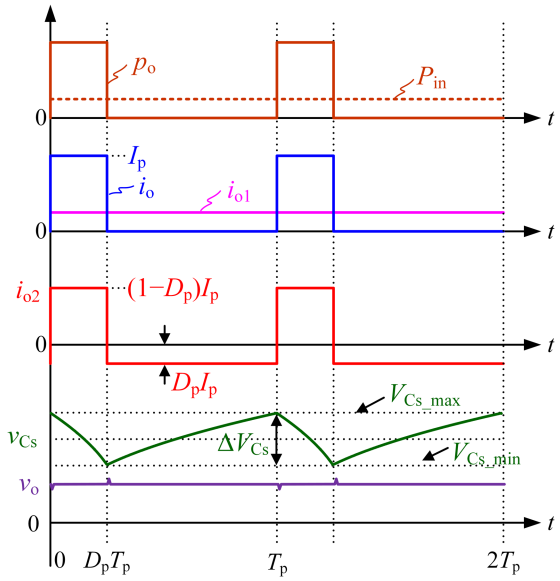

Fig. 3. Key waveforms of the ACC-based PPS.

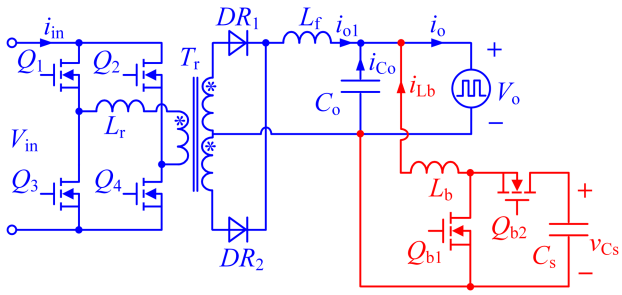

Fig. 4. Circuit of the wide PRF range PPS.

Fig. 3 shows the key waveforms of the ACC-based PPS, where P_{in} is the input power, p_o is the output power, i_o is the load current, i_{o1} is the output current of the dc–dc converter, i_{o2} is the ACC's port current, v_{Cs} is the storage capacitor voltage of the ACC, v_o is the output voltage, D_p is the duty cycle of the pulse, and T_p is the pulse repetition period. As shown, during $[0, D_pT_p]$, $P_{in} < p_o$, and storage capacitor C_s provides the deficient power and its voltage decays; during $[D_pT_p, T_p]$, $P_{in} > p_o$, and the excess power charges C_s through the ACC and the voltage of C_s increases.

For safety considerations, the PPS needs to have galvanic isolation. The *LLC* resonant converter and the phase-shifted full-bridge (PSFB) converter are the popular isolated dc–dc converters. The *LLC* resonant converter usually adopts pulse frequency modulation, which results in difficulties in optimizing the magnetic components. Here, the PSFB converter is chosen as the dc–dc converter. The ACC employs the simple buck/boost converter. Consequently, the circuit topology of the wide PRF range PPS is shown in Fig. 4.

TABLE I
SPECIFICATIONS OF THE WIDE PRF RANGE PPS

Symbol	Parameter	Value
V_{in}	input voltage	80-120 V
V_{in_norm}	normal input voltage	100 V
V_o	output voltage	28 V
I_p	load peak current	100 A
f_p	PRF	50-2000 Hz
D_p	duty cycle of the pulse	≤ 10%
t_p	pulse width time	10-2000 μs
V_{drop}	output voltage drop	≤ 3%
ΔI_{in}	input current ripple	≤ 10%

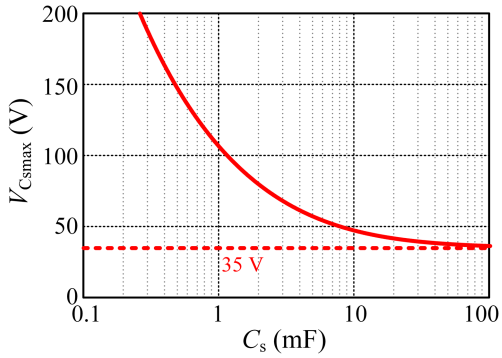

Fig. 5. Curve of V_{Csmax} versus C_s with $V_{Csmin} = 35$ V.

III. DESIGN OF THE WIDE PRF RANGE PPS

In this section, the parameter design for the wide PRF range PPS will be presented. Table I lists the specifications of the wide PRF range PPS.

A. Storage Capacitor in the ACC

The storage capacitance can be expressed as [20]

$$C_s = \frac{2V_oI_pD_p\left(1-D_p\right)}{f_p\left(V_{Csmax}^2 - V_{Csmin}{}^2\right)} = \frac{V_oI_pD_p\left(1-D_p\right)}{f_pV_{CS-\ ave}\,\Delta V_{Cs}} \quad (1)$$

where V_o is the output voltage of the PPS, I_p is the peak load current, V_{Csmax} and V_{Csmin} are the maximum and minimum voltages of C_s, respectively, $\Delta V_{Cs} = V_{Csmax} - V_{Csmin}$ is the voltage ripple of C_s, V_{Csave} is the average voltage of C_s, and f_p is the PRF. According to (1), C_s can be reduced by increasing V_{Csave} or ΔV_{Cs}. Moreover, it is evident that the lower the PRF, the larger the required C_s. Therefore, C_s should be designed at the minimum PRF.

The maximum voltage of the storage capacitor can be expressed as [20]

$$V_{Csmax} = \sqrt{\frac{2V_oI_p}{C_sf_p}D_p\left(1-D_p\right) + V_{Csmin}^2}\,. \quad (2)$$

TABLE II
SELECTION OF THE STORAGE CAPACITOR C_s

Type	Max. Voltage	Capacitance	Volume	Cost
UPW1J681MHD (63 V / 680 μF) × 12	50 V	7.91 mF	48 cm^2	$17.92
UPW2A331MHD (100 V / 330 μF) × 6	80 V	1.95 mF	24 cm^2	$10.10
UPW2C101MHD (160 V / 100 μF) × 7	128 V	0.67 mF	28 cm^2	$12.57

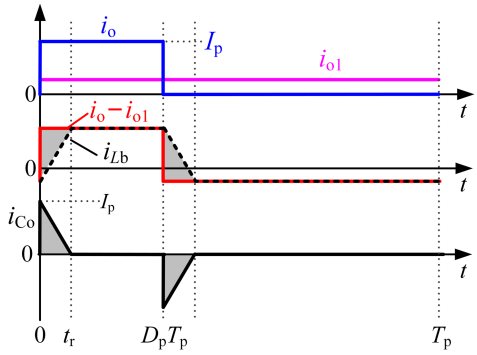

Fig. 6. Unbalanced charges when the pulse current comes and vanishes.

According to Fig. 4, to ensure normal operation of the ACC, V_{Csmin} needs to be higher than V_o, and $V_{Csmin} = 35$ V is chosen here. Substituting it with $D_p = 0.1$, $f_p = 50$ Hz, $V_o = 28$ V, and $I_p = 100$ A into (2), the curve of V_{Csmax} versus C_s can be plotted, as shown in Fig. 5. As seen, V_{Csmax} increases with the decrease of C_s. A too high V_{Csmax} will lead to increased voltage stress of the switches and losses in the ACC. Therefore, a compromise needs to be made when selecting C_s. Table II gives the possible options for the storage capacitor. For minimizing the volume and cost of the capacitors, $V_{Csmax} = 80$ V is chosen, and the corresponding C_s is 1.95 mF.

B. Inductor L_b in the ACC and Output Capacitor C_o

The inductor L_b in the ACC can be expressed as [21]

$$L_b = \frac{\left(v_{CS}(t) - V_o\right)V_0}{f_5 \cdot \Delta i_{Lb} \cdot v_{Cs}(t)} \quad (3)$$

where Δi_{Lb} is the current ripple of L_b. According (3), a larger L_b leads to smaller inductor current ripple and, thus, small losses in the ACC. However, the larger inductance will limit the slew rate of the ACC's port current, thereby increasing the requirement of output capacitance.

Fig. 6 shows the unbalanced charges when the pulse current comes and vanishes. As seen, when the pulse current comes, the inductor current i_{Lb} cannot rise abruptly, and the output capacitor C_o will provide the deficient current, resulting in output voltage drop. For proper operation of the ACC, the maximum duty cycle of the ACC is chosen as 0.9. So, the rise time t_r of

i_{Lb} can be expressed as

$$t_r = \frac{L_b I_p}{0.9\,(V_{Csmas} - V_o) - 0.1V_0}. \tag{4}$$

During $[0, t_r]$, the current provided by C_o is

$$i_{Co}(t) = I_p - \frac{I_p}{t_r}t. \tag{5}$$

Thus, the output voltage drop can be expressed as

$$V_{drop}(t) = i_{Co}r_{Co} + \frac{1}{C_o}\int_0^t i_{Co}dt \tag{6}$$

where r_{Co} is the equivalent series resistance (ESR) of C_o.

Substituting (5) into (6), we have

$$V_{drop}(t) = \frac{I_p}{2C_o t_r}\left[-t^2 + 2\,(t_r - C_o r_{C_o})\,t + 2C_o r_{CO_o} t_r\right]. \tag{7}$$

According to (7), the maximum output voltage drop is

$$V_{drop} = \begin{cases} I_p r_{Co} & t_r \le C_o r_{Co} \\ \frac{I_p}{2C_o t_r}(t_r - C_o r_{Co})^2 + I_p r_{Co} & t_r > C_o r_{Co} \end{cases}. \tag{8}$$

For an electrolytic capacitor, we have $C_o r_{Co} = 60\ \mu$s [22]. According to (8), $t_r < C_o r_{Co}$ is preferred to obtain a smaller output voltage drop, i.e., $V_{drop} = I_p r_{Co}$. By substituting $I_p = 100$ A, $V_{Csmax} = 80$ V, and $V_o = 28$ V into (4) and combining with $t_r \le C_o r_{Co} = 60\ \mu$s, we have $L_b \le 5.06\ \mu$H. Accordingly, the required C_o is

$$C_o = \frac{60\times10^{-6}}{r_{Co}} = \frac{60\times10^{-6} I_p}{V_{drop}} = \frac{100\times60\times10^{-6}}{28\times3\%} = 7.15(\text{mF}). \tag{9}$$

C. Components in the PSFB Converter

Since the PSFB converter only supplies the average power, conventional design methods can be employed.

The primary-secondary turns ratio of the transformer can be designed as [23]

$$K_{Tr} = \frac{N_p}{N_s} = \frac{V_{in\_min}(1 - D_{loss})}{V_o} \tag{10}$$

where V_{in_min} is the minimum input voltage, D_{loss} is the duty cycle loss resulted by the resonant inductor. Substituting $V_{in\_min} = 80$ V, $D_{loss} = 0.15$ and $V_o = 28$ V into (10) leads to $K_{Tr} = 2.43$. Here, $N_p = 7$ and $N_s = 3$ are chosen, and thus, $K_{Tr} = 2.33$.

The resonant inductance L_r can be designed as [23]

$$L_r = \frac{K_{Tr} V_{in\_min} D_{loss}}{4 I_{o\_ave} f_s} \tag{11}$$

where I_{o_ave} is the average output current. Substituting $K_{Tr} = 2.33$, $V_{in\_min} = 80$ V, $D_{loss} = 0.15$, $I_{o\_ave} = 10$ A, and $f_s = 100$ kHz into (11), $L_r = 7\ \mu$H is calculated.

The output inductance can be designed as [23]

$$L_f = \frac{V_o}{2 f_s \Delta I_{Lf}}\left(1 - \frac{V_o K_{Tr}}{V_{in\_max}}\right) \tag{12}$$

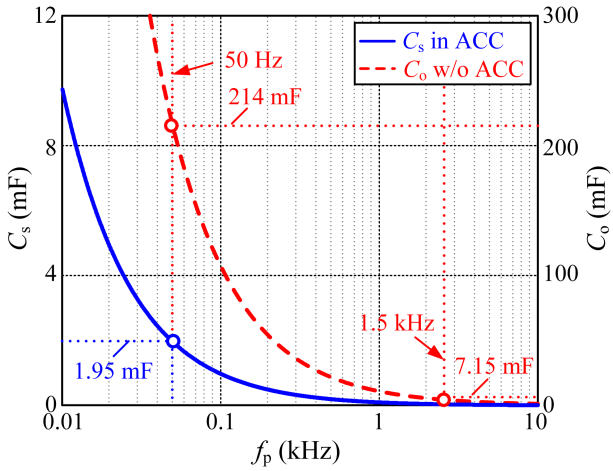

Fig. 7. Curves of the storage capacitance requirement versus the PRF.

where ΔI_{Lf} is the output inductor current ripple. For a tradeoff of the conduction loss and inductor size, ΔI_{Lf} is chosen as 20% of the average current. Substitution of $V_o = 28$ V, $K_{Tr} = 2.33$, $V_{in\_max} = 120$ V, $\Delta I_{Lf} = 20\% I_{o\_ave} = 2$ A, and $f_s = 100$ kHz into (12) leads to $L_f = 32.4\ \mu$H.

IV. Control Strategies for the Wide PRF Range PPS

A. Control Strategy at High PRF

In the wide PRF range PPS, the storage capacitance C_s in the ACC is designed at the lowest PRF. Substituting $V_o = 28$ V, $I_p = 100$ A, $D_p = 0.1$, $V_{Csmax} = 80$ V, and $V_{Csmin} = 35$ V into (1), the curve of the required C_s in ACC versus the PRF is depicted, as shown in Fig. 7 with the solid line. As observed, the required C_s is inversely proportional to the PRF. At high PRF, a very small C_s is needed, and the ACC is redundant. In addition, substituting $V_o = 28$ V, $I_p = 100$ A, $D_p = 0.1$, $V_{Csmax} = V_o = 28$ V, and $V_{Csmin} = V_o - 3\%V_o = 27.16$ V into (1), the curve of the required C_o without ACC versus the PRF can be depicted, as shown in Fig. 7 with the dashed line. As seen, at high PRF, if the ACC is not used, the required C_o is also very the pulsed power at high PRF, and the ACC could be shut small. Therefore, the existing output capacitor could provide down to save the loss in the ACC.

In Section III-B, the C_o is designed as 7.15 mF. By substituting $C_s = C_o = 7.15$ mF, $V_o = 28$ V, $I_p = 100$ A, $D_p = 0.1$, $V_{Csmax} = V_o = 28$ V, and $V_{Csmin} = V_o - 3\%V_o = 27.16$ V into (1), the corresponding PRF is 1.5 kHz. This means when the PRF is higher than 1.5 kHz, the ACC can be disabled.

Fig. 8 shows the smart disabling control circuit of the ACC. The sensed load current i_{o_s} is compared with the pulse threshold v_{th_ps} through comparator C1 to reshape the pulse signal. The generated pulse signal v_{ps} is sent to the D flip–flop to obtain a pulse signal with a 50% duty cycle and half the PRF frequency. Then, an *RC* charging circuit and a peak detection circuit are used to detect the pulse period. The generated signal v_{RPF} is proportional to the PRF pulse period. Finally, v_{RPF} is compared

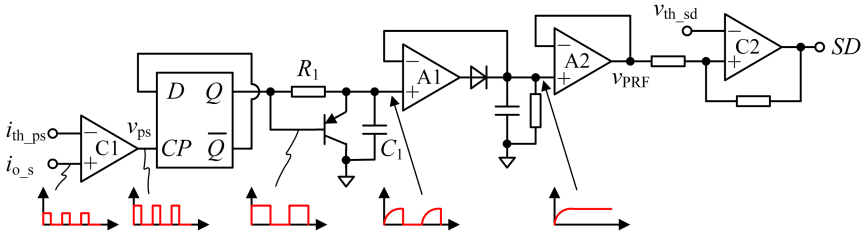

Fig. 8. Smart disabling circuit of the ACC.

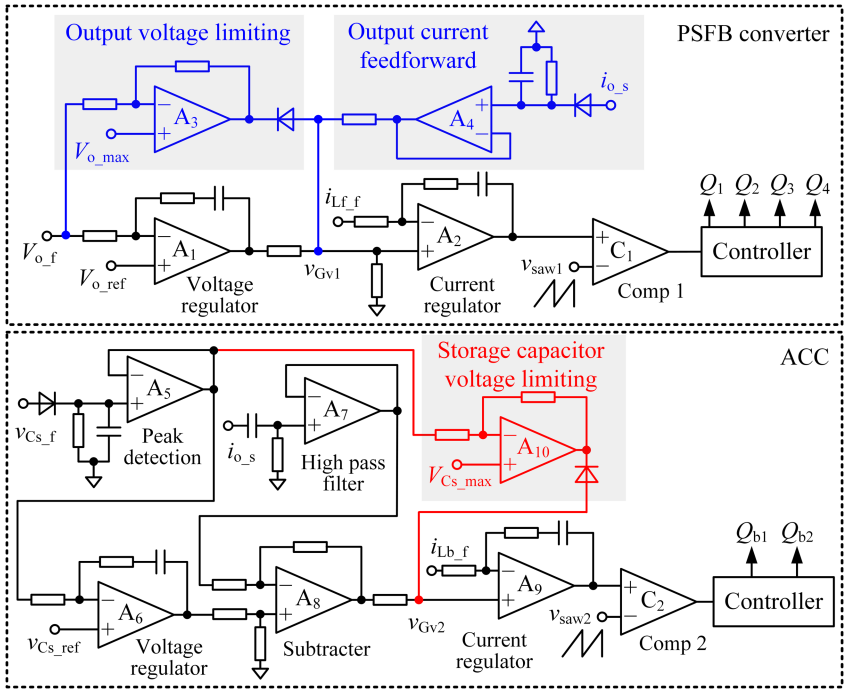

Fig. 9. Control circuit of the wide PRF range PPS.

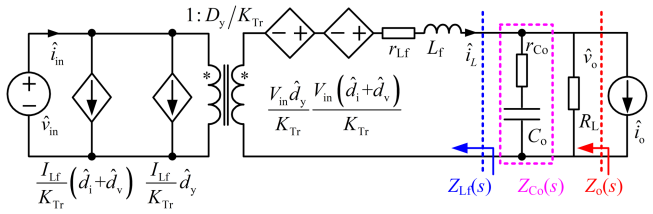

Fig. 10. Small-signal model of the PSFB converter.

with the shut-down threshold $v_{\mathrm{th\_sd}}$ through a hysteresis comparator. At high PRF, the signal *SD* is at low level to shut down the ACC.

B. Dynamic Response Enhancement Control Strategies

Fig. 9 shows the control circuit of the wide PRF range PPS. A dual-loop control is employed for the PSFB converter. In order to suppress the PRF current ripple at the input, the bandwidth of the voltage loop is generally designed to be 1/10 of the lowest PRF.

Fig. 10 shows the small-signal model of the PSFB converter [24], where, D_y is the duty cycle, I_{Lf} is the output inductor current, r_{Lf} is the ESR of the output inductor, R_{L} is the equivalent load resistance of the converter, $\hat{d}_{\mathrm{i}}$ and $\hat{d}_{\mathrm{v}}$ are the small signal disturbances caused by the resonant inductor, and expressed as [24]

$$\hat{d}_{\mathrm{i}} = -r_{\mathrm{d}}\frac{K_{\mathrm{Tr}}}{V_{\mathrm{in}}}\hat{i}_{\mathrm{L}} \tag{13}$$

$$\hat{d}_{\mathrm{v}} = r_{\mathrm{d}}\frac{1-D_{\mathrm{loss}}}{V_{\mathrm{in}}R_{\mathrm{L}}}\hat{v}_{\mathrm{in}} \tag{14}$$

where $r_{\mathrm{d}} = 4L_{\mathrm{r}}f_{\mathrm{s}} / {K_{\mathrm{Tr}}}^2$ is the equivalent resistance caused by the resonant inductor.

According to Fig. 9, the control block diagram of the PSFB converter can be obtained, as shown in Fig. 11(a), where, $Z_{\mathrm{o}}(s)$ represents the output impedance of the PSFB converter and $G(s)$ represents the equivalent transfer function. Fig. 11(a) can be equivalently transformed into Fig. 11(b), where the equivalent transfer function $G(s)$ can be derived as

$$G(s) = \frac{1}{H_{\mathrm{i}}}\frac{H_{\mathrm{i}}G_{\mathrm{c}}(s)G_{\mathrm{M}}G_{\mathrm{id}}(s)}{1+H_{\mathrm{i}}G_{\mathrm{c}}(s)G_{\mathrm{M}}G_{\mathrm{id}}(s)}Z_{\mathrm{Co}}(s) = \frac{1}{H_{\mathrm{i}}}\frac{T_1(s)}{1+T_1(s)}Z_{\mathrm{Co}}(s) \tag{15}$$

where $T_1(s) = H_{\mathrm{i}}G_{\mathrm{c}}(s)G_{\mathrm{M}}G_{\mathrm{id}}(s)$ is the transfer function of current loop, $G_{\mathrm{c}}(s) = k_{\mathrm{ic}}/s + k_{\mathrm{pc}}$ is the transfer function of the

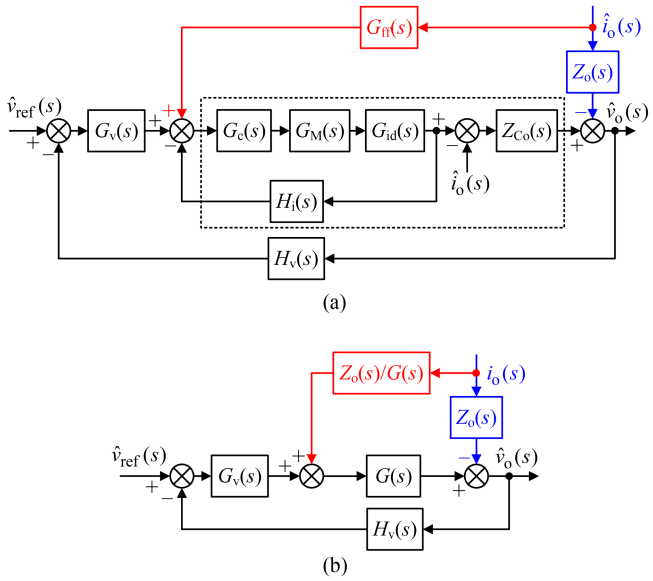

Fig. 11. Control block diagram of the PSFB converter. (a) Original block diagram. (b) Equivalent model.

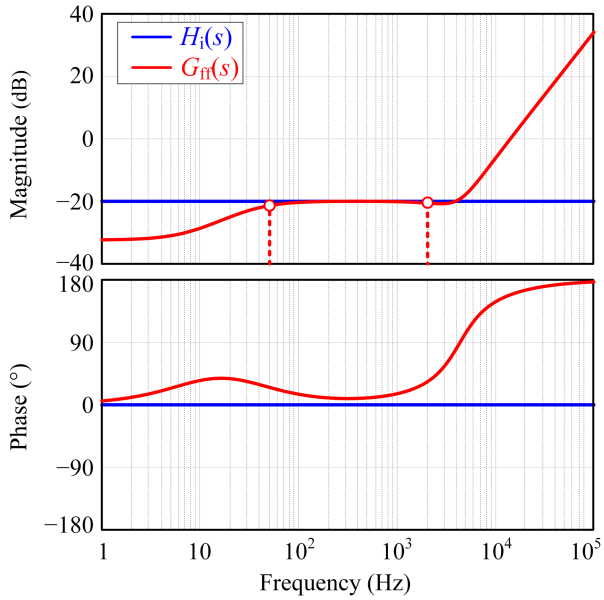

Fig. 12. Bode plot of $G_{ff}(s)$ and H_i.

current regulator, $G_M = 1/V_M$, and V_M is the amplitude of the saw-tooth carrier, $H_i = 0.1$ is the current sensing gain, $G_{id}(s)$ is the transfer function from the inductor current to the duty cycle, and $Z_{Co}(s)$ is the impedance of the output capacitor. The cut-off frequency of the current loop, f_c, is generally designed to 1/10 of the switching frequency ($f_s = 100$ kHz). So, $f_c = 10$ kHz is chosen. Thus, we have $\| T_1(j2\pi f_c) \| = 1$, and the phase margin of the current loop is set to 45°. Therefore, $k_{pc} = 2.5$ and $k_{ic} = 2000$ are obtained.

The transfer function $G_{id}(s)$ can be expressed as

$$G_{id}(s) = \frac{V_{in}}{K_{Tr} R_L} \frac{sC_o\left(r_{Co} + R_L\right) + 1}{\Delta(s)} \tag{16}$$

where $\Delta(s)$ is expressed as

$$\Delta(s) = \left(1 + \frac{r_{Co}}{R_L}\right) L_f C_o s^2 + \frac{r_{Lf} + r_d}{R_L} + 1 + \left[\left(1 + \frac{r_{Lf} + r_d}{R_L}\right) r_{Co} C_o + \left(r_{Lf} + r_d\right) C_o + \frac{L_f}{R_L}\right] s. \tag{17}$$

The equivalent impedance of the output capacitor can be expressed as

$$Z_{Co}(s) = r_{Co} + \frac{1}{sC_o} = \frac{1 + sC_o r_{Co}}{sC_o}. \tag{18}$$

The output impedance of the PSFB converter can be expressed as

$$Z_o(s) = Z_{Lf}(s) // Z_{Co}(s) // R_L = \frac{r_{Co} L_f C_o s^2 + \left[\left(r_{Lf} + r_d\right) r_{Co} C_o + L_f\right] s + r_{Lf} + r_d}{\Delta(s)}. \tag{19}$$

Since the bandwidth of the voltage loop is extremely low, the dynamic response of PPS is very poor. Moreover, the storage capacitance in the ACC is quite small, which cannot provide sufficient power when the load changes abruptly, leading to a large output voltage drop or overshoot, which affects the normal operation of T/R module.

To enhance the dynamic response during load transients, an output current feedforward control is adopted, as shown in Fig. 11(a). According to Fig. 11(b), the transfer function of the output current feedforward control can be expressed as

$$G_{ff}(s) = \frac{Z_o(s)}{G(s)} = H_i \frac{1 + T_1(s)}{T_1(s)} T_2(s) \tag{20}$$

where $T_2(s) = Z_o(s) / Z_{Co}(s)$.

Substituting $H_i = 0.1$, $k_{ic} = 2000$, $k_{pc} = 2.5$, $G_M = 1 / 2.15$, $V_{in} = 100$ V, $K_{Tr} = 2.33$, $C_o = 7.15$ mF, $r_{Co} = 2.5$ mΩ, $R_L = 2.8$ Ω, $L_f = 32$ μH, $r_{Lf} = 5$ mΩ, and $r_d = 0.88$ Ω into (20), the Bode plot of $G_{ff}(s)$ and H_i can be plotted, as shown in Fig. 12. As seen, the gain of $G_{ff}(s)$ is approximated as H_i within the PRF. First, the gain of $[1 + T_1(s)] / T_1(s)$ can be approximated as 1 because that the gain of the current loop is very large at low frequency ($\|T_1(j2\pi f) >> 1\|$ for $f << f_c$). Second, the gain of $T_2(s)$ can be approximated as 1. This is because that the impedance $Z_{Co}(s)$ is much smaller than the impedance $Z_{Lf}(s)$ within the PRF, which leads to the output impedance $Z_o(s) = Z_{Lf}(s) // Z_{Co}(s) \approx Z_{Co}(s)$.

Since the load current is pulsed, to avoid affecting the normal operation of the converter at steady state, a peak detection circuit is added to the load current feedforward path. When the load current changes, it can be quickly detected and compensated through the feedforward path. In addition, due to the low bandwidth of the voltage loop, when the load current suddenly vanishes, the output voltage will experience a significant overshoot. To prevent the excessive voltage overshoot, an output voltage limiting control is added. When the output voltage exceeds the voltage threshold, the output voltage limiting control will

TABLE III
MAIN PARAMETERS OF THE PROTOTYPE

Module	Parameters	Value	Type	Volume	Cost
PSFB Converter	Q_1-Q_4	/	BSZ900N20NS3G	0.01 cm^3 × 4	\$2.28 × 4
	T_r [K (N_p/N_s)]	2.33	DMEGC PQ40	22.4 cm^3	\$0.5
	L_r	7 μH	DMEGC PQ20	2.94 cm^3	\$0.3
	D_{R1}-D_{R2}	/	V20PW22C	0.08 cm^3 × 4	\$1.46 × 4
	L_f	32.4 μH	DMEGC PQ35	19.4 cm^3	\$0.4
	C_o (with ACC)	7.15 mF	UHD1H102MHD	5.03 cm^3 × 8	\$1.92 × 8
	C_o (without ACC)	214 mF	UHD1H102MHD	5.03 cm^3 × 214	\$1.92 × 214
	f_s	100 kHz	/	/	/
	Total (only with C_o)			1121.52 cm^3	\$427.04
	Total (with ACC)			85.34 cm^3	\$31.52
ACC	Q_{b1}-Q_{b2}	/	IPB026N10NF2S	0.45 cm^3 × 4	\$2.58 × 4
	L_b	5.06 μH	DMEGC PQ40	22.4 cm^3 × 2	\$0.5 × 2
	C_s	1.95 mF	UPW2A331MHD	5.03 cm^3 × 6	\$2.84 × 6
	Driver	/	UCC20225	0.025 cm^3 × 2	\$4.86 × 2
	Controller	/	UCC35702	0.09 cm^3	\$5.71
	f_s	100 kHz	/	/	/
	Total			76.92 cm^3	\$43.76

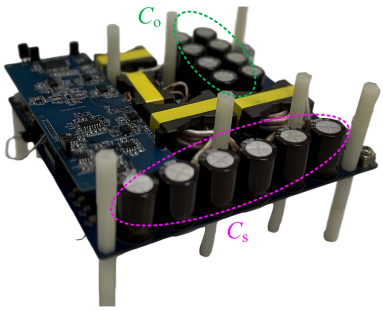

Fig. 13. Photograph of the wide PRF range PPS prototype.

limit the maximum output voltage. The implement circuits of the output current feedforward control and the output voltage limiting control are shown in Fig. 9.

V. EXPERIMENTAL RESULTS

To validate the proposed design method and control strategies, a prototype of the wide PRF range PPS is fabricated in the lab, which consists of a PSFB converter and an ACC, as shown in Fig. 13. The specifications of the prototype are provided in Table I, and the main parameters are listed in Table III.

Fig. 14 shows the steady-state experimental waveforms of the wide PRF range PPS. As can be observed, the maximum output voltage drop is 0.81 V, and the input current ripple is 0.24 A (7.6% of i_{in}). Meanwhile, with the increase of the PRF, both the output voltage drop and the input current ripple decrease, and the inductor current in the ACC becomes increasingly difficult to track the load current, which confirms the analysis.

Fig. 15 shows the experimental waveforms of the load transients without dynamic response enhancement control at 50 Hz PRF. As seen, the output voltage drop is 7.76 V when the load suddenly comes, and the voltage overshoot is 5.87 V when the load suddenly vanishes. The dynamic response of the PPS is very poor.

Fig. 16 gives the experimental waveforms of the load transients with the proposed dynamic response enhancement control at 50 Hz PRF. When the pulse load comes, due to the output current feedforward control, the output voltage drop decreases to 0.34 V, with a recovery time of only one pulse cycle. When the pulse load vanishes, the output voltage limiting control limits the voltage overshoot to 1.22 V.

Fig. 17 presents the experimental waveforms of the load transients with dynamic response enhancement control at 2 kHz PRF. It shows that the proposed control strategies can also improve the dynamic response of the PPS at high PRF. The experimental results in Figs. 16 and 17 demonstrate that the proposed dynamic response enhancement control can significantly enhance the dynamic response of the PPS, even with extremely low voltage loop bandwidth and extremely small storage capacitance.

Fig. 18 shows the experimental waveforms when the PRF changes. Fig. 18(a) shows the waveforms when the PRF suddenly increases from 50 Hz to 1.5 kHz. As seen, the ACC is shut down when the PRF increases, and the overshoot of output voltage is 2.02 V, which has a favorable dynamic response. Fig. 18(b)

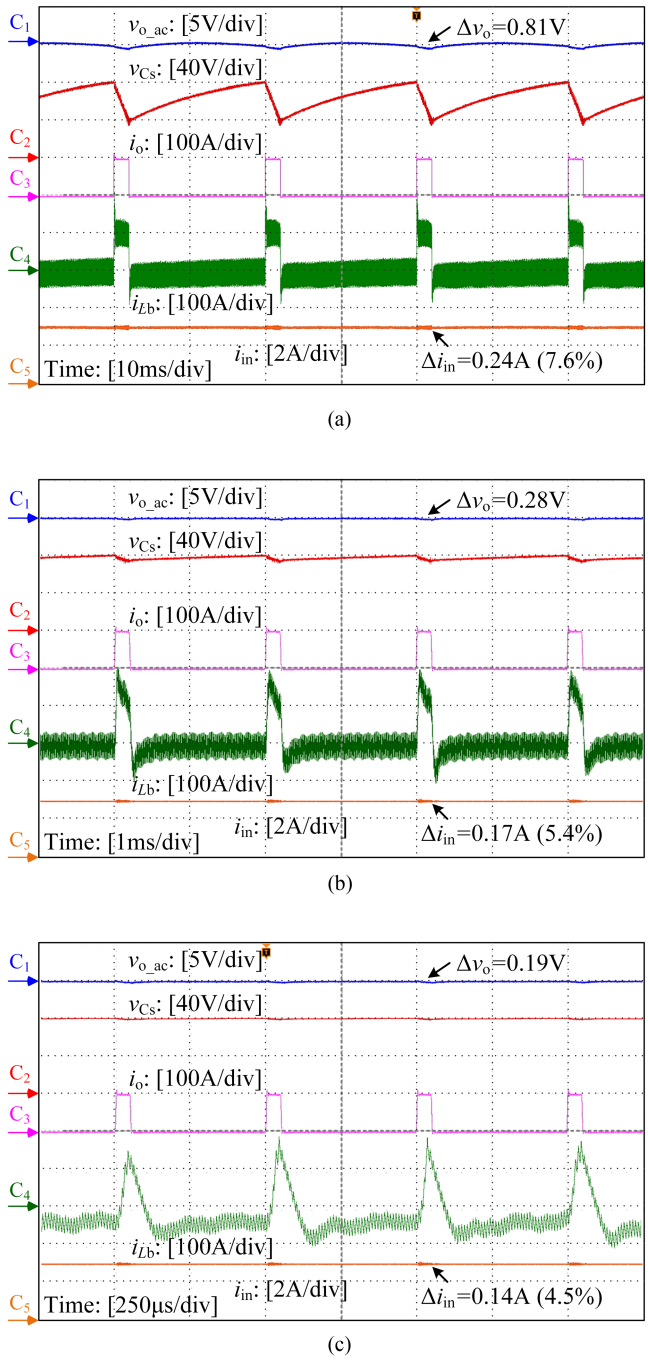

Fig. 14. Steady state experimental waveforms at (a) 50 Hz PRF, (b) 500 Hz PRF, and (c) 2 kHz PRF.

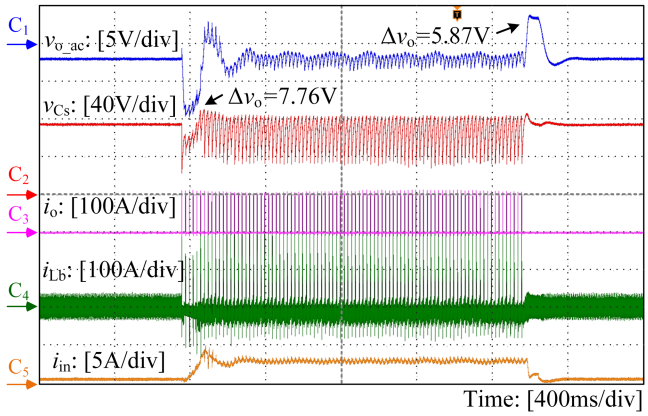

Fig. 15. Experimental waveforms of the load transient without dynamic response enhancement control at 50 Hz PRF.

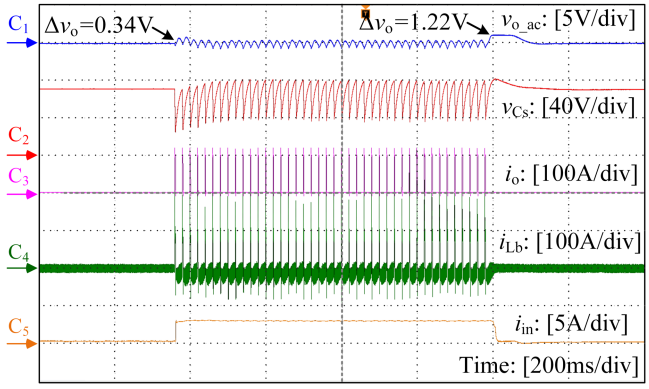

Fig. 16. Experimental waveform of the load transient with proposed dynamic response enhancement control at 50 Hz PRF.

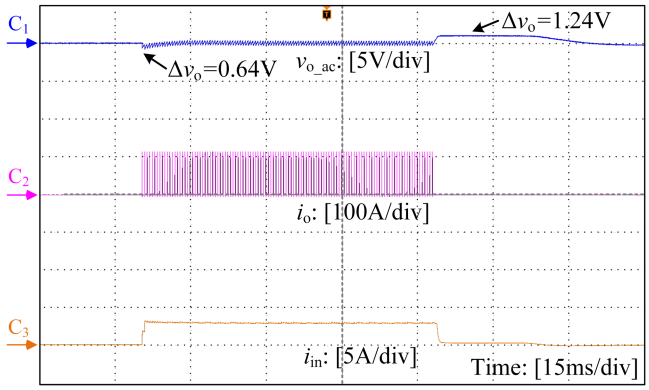

Fig. 17. Experimental waveform of the load transient with the proposed dynamic response enhancement control at 2 kHz PRF.

shows the waveforms when the PRF suddenly decreases from 1.5 kHz to 50 Hz. In this case, the ACC is rapidly switched on, providing the pulsed load current. Additionally, the presence of the storage capacitor voltage limiting loop limits the voltage and current overshoots in ACC during starting up.

Fig. 19 gives the measured efficiencies of the PPS with large capacity storage capacitor, the ACC-based PPS without smart disabling, and the proposed wide PRF range PPS. As seen, at the lowest PRF (50 Hz), the efficiency of the wide PRF range PPS is equal to the ACC-based PPS and the full-load efficiency is 92.8%. The full-load efficiency of the PPS with large capacity storage capacitor is 94.3%. When the PRF is 1.5 kHz, the efficiency of the ACC-based PPS with smart disabling is equal to the PPS with large capacity storage capacitor, and the full-load efficiency is 94.7%. The full-load efficiency of the ACC-based PPS without smart disabling is 93.2%. It is evident that disabling the ACC at high PRF improves the efficiency by nearly 1.5%.

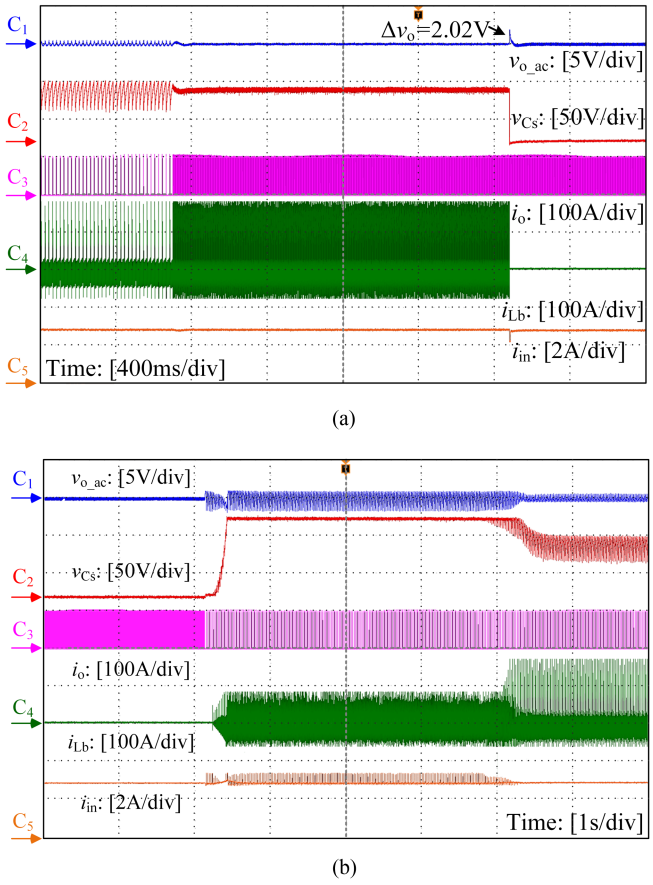

Fig. 18. Experimental waveforms when (a) the PRF increases from 50 Hz to 1.5 kHz and (b) the PRF decreases from 1.5 kHz to 50 Hz.

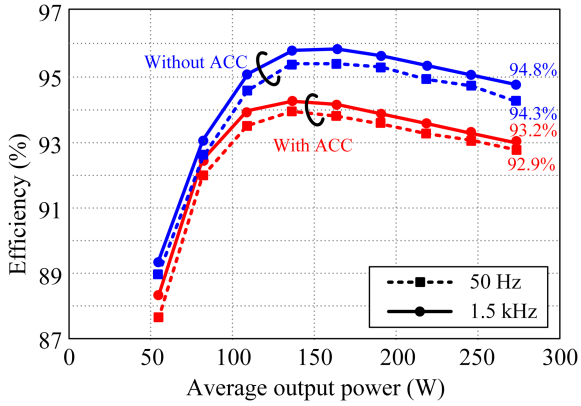

Fig. 19. Measured efficiency curve of the PPS with large capacity storage capacitor, the ACC-based PPS without smart disabling, and the proposed ACC-based PPS with smart disabling.

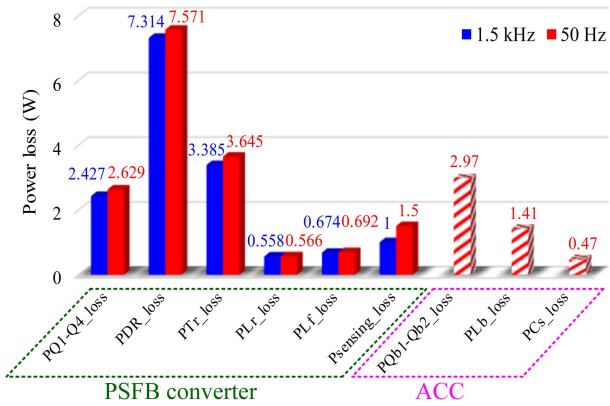

Fig. 20. Loss distribution of the wide PRF range PPS.

In addition, at low PRF, the efficiency of the wide PRF range PPS is lower than the PPS with large capacity storage capacitor. This is because the ACC has been added into the PPS, which significantly reduces the storage capacitance of the PPS and improves the power density of the PPS, but also brings additional loss.

Fig. 20 presents the loss distribution of the wide PRF range PPS with the loss model and the loss calculation method of the PPS given in [20]. As seen, at the lowest PRF (50 Hz), the loss of the PSFB converter is 16.6 W, the loss of the ACC is 4.85 W, and the total loss is 21.45 W. When the PRF is 1.5 kHz, due to the smart disabling control, the ACC is shut down, and the total loss is 15.36 W. As shown in the shaded area in Fig. 20, the loss of ACC is avoided.

The volume and cost of the components in the PPSs are given in Table III. The components of the PSFB converter except the output capacitors in the PPS with large capacity storage capacitor and the ACC-based PPS are identical. In the PPS with large capacity storage capacitor, the output storage capacitance is 214 mF, which can be obtained by Fig. 7. Here, two hundred and fourteen 50 V/1000 μF capacitors (UHD1-H102MHD) are used for C_o. And in the ACC-based PPS, eight 50 V/1000 μF capacitors (UHD1H102MHD) are used for the output capacitor. In ACC, six 100 V/330 μF capacitors (UPW2A331MHD) are used for the storage capacitor. The inductor of the ACC is separated into two inductors connected in series, and two sets of PQ40 ferrite cores are employed. In addition, four MOSFETS (IPB026N10NF2S) are selected for the main switches of the ACC, and two MOSFETS are connected in parallel for each switch. As can be seen, the volume and cost of the ACC-based PPS (162.26 cm^3 and \$75.31) are only 14.47% and 17.64% of the PPS with large capacity storage capacitor (1121.52 cm^3 and \$427.04), respectively. Obviously, the ACC-based PPS can significantly reduce the volume and cost of the PPS.

Table IV gives the comparison of different PPSs. As can be seen, the storage capacitance of the PPS is greatly reduced by adding the active power decoupling circuit. However, most of the existing PPSs based on the active power decoupling circuit are only suitable for low PRF. When the PRF is high, the efficiency of these PPSs still remains at a low level. This article proposes a smart disabling control strategy that can improve the efficiency of the PPS by 1.9% at high PRF. In addition, because the storage capacitance of the PPS based on active power decoupling circuit is too small, the dynamic response characteristics are poor. This article proposes the dynamic response enhancement control strategies without increasing the storage capacitance, which can greatly improve the dynamic response characteristics of the PPS.

TABLE IV
COMPARISON OF DIFFERENT PPSS

Reference		[15]	[17]	[18]	[19]	This Paper
Active Power Decoupling Topology		Two-stage	ACC-based	ACC-based	ACC-based	ACC-based
Active Power Decoupling Control		Dual-loop control with voltage feedforward control	Dual-loop control	Hybrid decoupling control	Current mode control	Dual-loop control with smart disabling and dynamic response enhancement
Pulsed Power		2 kW	2 kW	2.25 kW	784 W	2.8 kW
PRF		150-300 Hz	150-300 Hz	1.6-1.8 Hz	100-300 Hz	50-2000 Hz
Storage Capacitance		3.3 mF	1.5 mF	3 mF	1.5 mF	1.95 mF
Full-Load Efficiency	Low PRF	90.1%	87.3%	92.7%	N/A	92.8%
	High PRF	90.6%	87.6%	92.7%	N/A	94.7%
Undershoot/Overshoot During Load Transients		1.3V /1.5 V	2.6 V/2.5 V	N/A	6.8 V/9.8V	0.34 V/1.22 V

VI. CONCLUSION

This article proposes a wide PRF range PPS based on the ACC. By increasing the voltage ripple of the storage capacitor in the ACC, the storage capacitance can be significantly reduced. This article analyzes the unbalanced charges when the pulse current comes and vanishes and provides a design method for the wide PRF range PPS to minimize the output capacitance and the storage capacitance. Meanwhile, for saving the extra losses brought by the ACC, a smart disabling control strategy is proposed to shut down the ACC at high PRF, and the corresponding control circuit is given. Moreover, the dynamic response enhancement control strategies are proposed, including the output current feedforward control and output voltage limiting control. Finally, the experimental results are provided to validate the correctness and effectiveness of the proposed wide PRF range PPS and the control strategies.

REFERENCES

[1] X. Yue, W. Wan, B. Ning, and L. Jin, "An active phased array radar in China," *Nature Astron.*, vol. 6, no. 5, May 2022, Art. no. 619.

[2] R. D. Palmer et al., "Horus—A fully digital polarimetric phased array radar for next-generation weather observations," *IEEE Trans. Radar Syst.*, vol. 1, pp. 96–117, May 2023.

[3] V. Venkatesh, K. Orzel, and S. Frasier, "Demonstration of a spaced-antenna weather radar using an X-band active phased-array," *IEEE Geosci. Remote Sens. Lett.*, vol. 19, no. 10, Jan. 2022, Art. no. 3509805.

[4] A. Hussain, U. Anjum, B. A. Channa, W. Afzal, I. Hussain, and I. Mir, "Displaced phase center antenna processing for airborne phased array radar," in *Proc. Int. Bhurban Conf. Appl. Sci. Tech.*, 2021, pp. 988–992.

[5] M. Maddegalla, A. A. Bazil Raj, and G. S. Rao, "Beam steering and control algorithm for 5-18 GHz transmit/receive module based active planar array," in *Proc. Int. Conf. Syst., Computation, Automat., Net.*, 2020, pp. 1–6.

[6] W. Zhang, Z. Ye, K. Wei, and Y. Jiang, "Analysis of the operating characteristics of the integrated power system under the action of pulse load," in *Proc. Int. Conf. Data Sci, Comput. Appl.*, 2022, pp. 1131–1136.

[7] C. Zhang et al., "Conjunction of triboelectric nanogenerator with induction coils as wireless power sources and self-powered wireless sensors," *Nature Commun.*, vol. 11, no. 1, Jan. 2020, Art. no. 58.

[8] A. C. Mondini, F. Guzzetti, K. Chang, O. Monserrat, T. R. Martha, and A. Manconi, "Landslide failures detection and mapping using synthetic aperture radar: Past, present and future," *Earth-Sci. Rev.*, vol. 216, no. 1, pp. 1–33, May 2021.

[9] S. Rathod, K. Sreenivasulu, K. S. Beenamole, and K. P. Ray, "Evolutionary trends in transmit receive module for active phased array radars," *Defense Sci. J.*, vol. 68, no. 6, pp. 553–559, Nov. 2018.

[10] S. T. Meraj et al., "A filter less improved control scheme for active/reactive energy management in fuel cell integrated grid system with harmonic reduction ability," *Appl. Energy*, vol. 312, no. 1, pp. 1–17, Apr. 2022.

[11] L. Zhou, W. Yi, and Y. Chen, "Additional synchronous torque coordinated control for approximate-capacity diesel-storage supply system with low-frequency pulsed load," *IEEE Trans. Ind. Electron.*, vol. 70, no. 7, pp. 6919–6930, Jul. 2023.

[12] F. Yang, Y. Jia, X. Y, and H. Wu, "Second-order ripple power suppression for single-phase ac-dc power systems with reduced power conversion stage," *IEEE Trans. Transp. Electrif.*, vol. 10, no. 2, pp. 2965–2973, Jun. 2024.

[13] M. M. Mardani, M. H. Khooban, A. Masoudian, and T. Dragičević, "Model predictive control of dc–dc converters to mitigate the effects of pulsed power loads in naval dc microgrids," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5676–5685, Jul. 2019.

[14] P. J. Palanas, K. Yu, Y. Zeng, and X. Xie, "Analysis and design of a novel *LLC* CCPS for repetitive pulsed power applications," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 14004–14016, Nov. 2023.

[15] X. Gao, H. Wu, S. Gao, Z. Zhang, and Y. Xing, "A two-stage pulsed power supply for low dc voltage and low frequency pulsed current loads," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2298–2309, Feb. 2021.

[16] Z. Yuan and H. Xu, "Pulse power supply with faster response and low ripple current using inductive storage and interleaving technology," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 1, pp. 54–62, Mar. 2020.

[17] X. Huang, X. Ruan, F. Du, F. Liu, and L. Zhang, "A pulsed power supply adopting active capacitor converter for low-voltage and low-frequency pulsed loads," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9219–9230, Nov. 2018.

[18] P. Yang et al., "Hybrid decoupling controlled active power compensator for the ultralow- frequency pulse load with reversed power application," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 6, pp. 5774–5784, Dec. 2023.

[19] X. Chen, P. Yang, Y. Peng, M. Wang, F. Hu, and J. Xu, "Output voltage drop and input current ripple suppression for the pulse load power supply using virtual multiple quasi-notch-filters impedance," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9552–9565, Aug. 2023.

[20] Y. Xu, X. Ruan, and X. Huang, "Comparison of low pulse-repetitive-frequency pulsed power supplies with extremely small storage capacitor," *IEEE Trans. Ind. Electron.*, vol. 70, no. 11, pp. 11194–11204, Nov. 2023.

[21] S. K. Rao and K. Bauman, "Design of buck type switched-mode power supplies using non-ideal components," in *Proc. IEEE Power Electron. Specialists Conf.*, 1975, pp. 126–137.

[22] A. I. Pressman, K. Billings, and T. Morey, *Switching Power Supply Design*, 2nd ed. New York, NY, USA: McGraw-Hill, 2009.

[23] X. Ruan, *Soft-Switching PWM Full-Bridge Converters: Topologies, Control, and Design*. Hoboken, NJ, USA: Wiley, Apr. 2014.

[24] G. D. Capua, S. A. Shirsavar, M. A. Hallworth, and N. Femia, "An enhanced model for small-signal analysis of the phase-shifted full- bridge converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1567–1576, Mar. 2015.

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