A Temperature-Dependent Analytical Transient Model of SiC MOSFET in Half-Bridge Circuits

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***Abstract*—In this article, a temperature-dependent transient model of silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) is proposed. The switching transient of the SiC MOSFET is divided into four phases. In each phase, the operations of the MOSFET and its body diode are analyzed and the corresponding equivalent circuits are obtained. The analysis identifies that the $C_{gd} \times dV_{ds}/dt$ and $L_s \times dI_d/dt$ induced negative feedback mechanisms, excess charge extraction in the N-base of SiC MOSFET body diode and dynamic transfer characteristics at switching transient are pivotal physical characteristics. The dependence of junction temperature T_{J1} of low-side MOSFET and junction temperature T_{J2} of high-side MOSFET on the switching behavior of SiC MOSFET is also analyzed and included in the proposed model. Based on the improved understanding of the switching behavior, an analytical model of SiC MOSFET is derived. The analytically derived switching waveforms and switching losses are compared to the test data and good agreement is obtained.**

***Index Terms*—Analytical model, metal-oxide-semiconductor field-effect transistor (MOSFET), silicon carbide (SiC), switching characteristics, temperature-dependent modeling.**

I. Introduction

THANKS to the superior material properties of silicon carbide (SiC) semiconductors, SiC metal-oxide-semiconductor field-effect transistor (MOSFETs) can operate under very high-frequency and high-temperature conditions. The merits make the device a promising candidate for next-generation power electronic systems. However, the wide utilization of SiC MOSFETs also poses various issues in the power converter design. One major issue is accurate estimation of power losses. At high-frequency power applications, the switching losses dominate the conversion efficiency [1]. The power losses generate heat, which also determines the heat-sink design. The final performance of the converter design is thereby mainly determined by the power losses, which makes the power loss estimation pivotal for converter design. The other issue is related to electromagnetic interference (EMI). The SiC MOSFETs have a fast switching speed, which gives rise to a high drain-source voltage slope ($dV_{\rm ds}/dt$) and drain current slope (dI_d/dt) during the switching transient. The high $dV_{\rm ds}/dt$ and dI_d/dt of SiC MOSFETs generate severe EMI noise, which can jeopardize converter operation [2]. To estimate the EMI, an accurate SiC MOSFET model is required.

The currently available SiC MOSFET models have four kinds: behavior models, analytical models, physics-based models, and numerical models. The behavior models mathematically fit characteristics of SiC MOSFET without reflecting any circuit and device operations [3]. The analytical models yield expressions of the switching characteristics through circuit and device equations based on Kirchhoff's current and voltage laws (KCL and KVL) of the commutation circuit, input, and output characteristics of the devices [4], [5], [6], [7]. Based on semiconductor physics, the physics-based models use physical equations of SiC MOSFET to describe the devices' characteristics [8], [9]. The numerical models [10] use finite element method-based simulation tools to model the SiC MOSFETs. Detailed semiconductor parameters and the cell structure of the SiC MOSFET are required to establish the model.

The behavior models provide fast simulation, but have poor accuracy. The physics-based models and numerical models are very accurate. Nonetheless, challenges with parameter extraction and slow simulation speeds hinder their application. Compared to these models, the analytical model can provide a relatively fast simulation with reasonable accuracy [4], [5], [6]. The parameter extraction is also relatively easy and can be mainly based on datasheet [4]. These merits make the analytical models a good choice for SiC MOSFET modeling.

However, the previous research on analytical modeling of SiC MOSFETs also has certain drawbacks [4], [5], [6], [7]. First, to derive an analytical model, many crucial device operations, such as the bipolar operation of the body diode and feedback actions of stray inductances and capacitances, are often neglected. Second, due to the high $V_{\rm ds}$ applied on the device, dynamic transfer characteristics during switching transients differ from the static transfer characteristics [11]. The static transfer characteristics are thereby not adequate to be used in the SiC MOSFET modeling. Finally, temperature dependence on the switching behavior of SiC MOSFET is often neglected, which leads to some errors [7]. To achieve an improved accuracy, the temperature dependence of SiC MOSFET and its body diode should be analyzed and the strongly temperature-dependent transient characteristics should be considered.

Received 29 May 2024; revised 3 September 2024; accepted 29 September 2024. Date of publication 9 October 2024; date of current version 12 December 2024. This work was supported by the CLEAN-Power (Compatibility and Low electromagnetic Emission Advancements for Next generation Power electronic systems) Project at the Department of Energy, Aalborg University, Aalborg, Denmark, funded by Independent Research Fund Denmark (DFF). Recommended for publication by Associate Editor M. Nawaz. *(Corresponding author: Peng Xue.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3476337.

Digital Object Identifier 10.1109/TPEL.2024.3476337

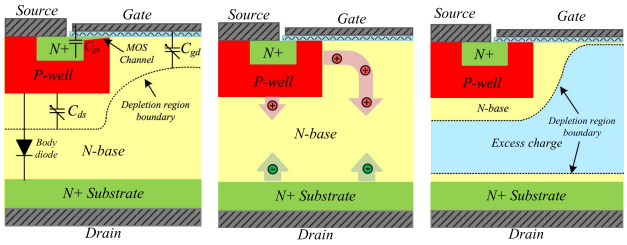

Fig. 1. SiC MOSFET and its body diode: (a) Cell structure and stray capacitances of SiC MOSFET. (b) Forward conduction of body diode. (c) Excess charge extraction of body diode.

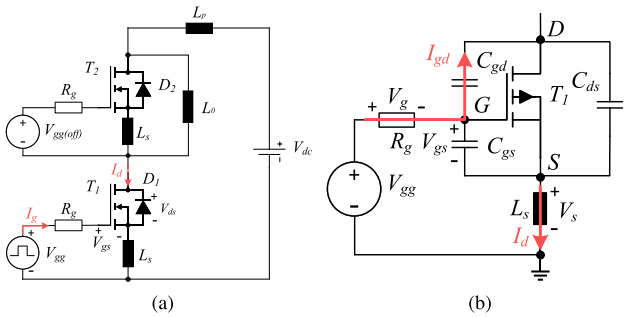

Fig. 2. (a) Half-bridge test circuit. (b) $C_{\rm gd} \times dV_{\rm ds}/dt$ and $L_s \times dI_d/dt$ induced negative feedback mechanisms of SiC MOSFETs.

In this article, to develop a complete analytical model of SiC MOSFETs, the switching transient is segmented into four distinct phases and the device's operation in each phase is analyzed. The analyses unveil pivotal device characteristics that needed to be included in the SiC MOSFET modeling. Based on the improved understanding, the analytical expressions of $V_{\rm ds}$ and I_d at each phase are derived. In addition, the temperature dependence on the switching behavior of SiC MOSFETs is experimentally identified, and temperature-dependent models for pivotal parameters are included. In the end, double pulse test is performed to validate the proposed SiC MOSFET model.

II. Switching Behavior of SiC MOSFET

Fig. 1(a) shows elementary cell structure of a SiC MOSFET and its body diode. The gate-source stray capacitance $C_{\rm gs}$, which originates from the overlap of the N+ source and gate, is voltage-independent. The drain-source and gate-drain stray capacitances $C_{\rm ds}$ and $C_{\rm gd}$ are generated by the depletion region, and thereby depend on $V_{\rm ds}$.

In the SiC MOSFET, the P-well, N-base, and N+ substrate form a body diode, as shown in Fig. 1(a). When the MOSFET is reverse biased, the P-well/N-base junction and N-base/ N+ substrate junction are forward biased, which causes the hole injection at the P-well/N-base junction and electron injection at the N-base/N+ substrate junction, as shown in Fig. 1(b). With a high density of minority carriers built up in the N-base, the body diode can operate like a bipolar *p–i–n* diode [12].

Fig. 2(a) shows the SiC MOSFET-based half-bridge circuit. In the circuit, L_0 is the load inductor. $V_{\rm dc}$ is the dc-bus voltage. $V_{\rm gg}$ is the gate drive voltage at low side, whereas $V_{\rm gg(off)}$ is the high-side OFF-state gate voltage. L_s is the common source stray inductance. L_p is the power loop stray inductance. $R_g = R_{\rm gi} + R_{\rm ge} + R_{\rm gd}$ is the total gate resistance, which includes the internal gate stray resistance $R_{\rm gi}$, external gate resistance $R_{\rm ge}$, and gate driver resistance $R_{\rm gd}$. T_1 and D_1 are the low-side MOSFET and its body diode. T_2 and D_2 are the high-side MOSFET and its body diode. T_1 is the active switch. T_2 is in OFF-state and its body diode D_2 is used as a freewheeling diode. In Fig. 2(a), the gate loop inductance is neglected because the gate loop inductance only affects the turn-ON/OFFdelay time and has no impact on the switching behavior [13], [14].

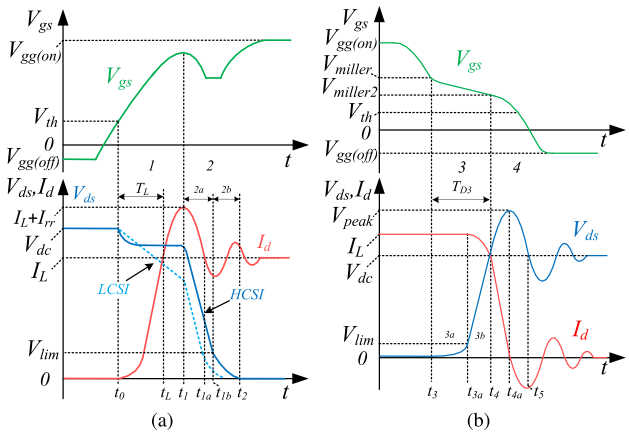

Fig. 3. (a) Turn-ON waveforms and (b) Turn-OFF waveforms of SiC MOSFETs.

A. Turn-ON Behavior

Fig. 3(a) shows the turn-ON transient of SiC MOSFET, which is divided into phases 1 and 2. The equivalent circuits are given in Fig. 4(a)–(c). In the circuits, T_1 is replaced as its stray capacitances and MOS channel current $I_{\rm ch}$. Load current I_L is constant at switching transient and thereby represented as a current source. The two phases are given as follows:

Phase 1 [t_0–t_1] [see Fig. 4(a)]: Phase 1 starts when the gate-souse voltage $V_{\rm gs}$ surpasses its threshold voltage $V_{\rm th}$. In phase 1, $I_{\rm ch}$ starts to increase, which supports the drain current I_d to increase. The dI_d/dt generates voltage on inductances L_p and L_s, which cause the reduction of $V_{\rm ds}$, as shown in Fig. 3(a).

Fig. 2(b) shows L_s induces a negative feedback mechanism in phase 1. The high dI_d/dt generates a positive voltage V_s on the L_s, which counteracts the $V_{\rm gs}$ and slows down its turn-ON. The slowdown of the $V_{\rm gs}$ in return hinders the dI_d/dt to increase. A negative feedback mechanism is thereby achieved.

Due to the negative feedback, the turn-ON in phase 1 greatly depends on L_s. Fig. 3(a) shows the waveforms when the device has high common source inductance (HCSI) and low common source inductance (LCSI) used. For the SiC MOSFETs using common source configuration, the terminal and bond wires in the source generate an HCSI ranging from a few to tens of nanohenries [15]. The HCSI induces very strong negative feedback, which hinders the dI_d/dt from increasing. In the end, a constant dI_d/dt is achieved and a voltage plateau of $V_{\rm ds}$ is generated, as shown in Fig. 3(a). Some new package forms, such as TO-247-4, TO-263-7, and TTOLL, have an additional

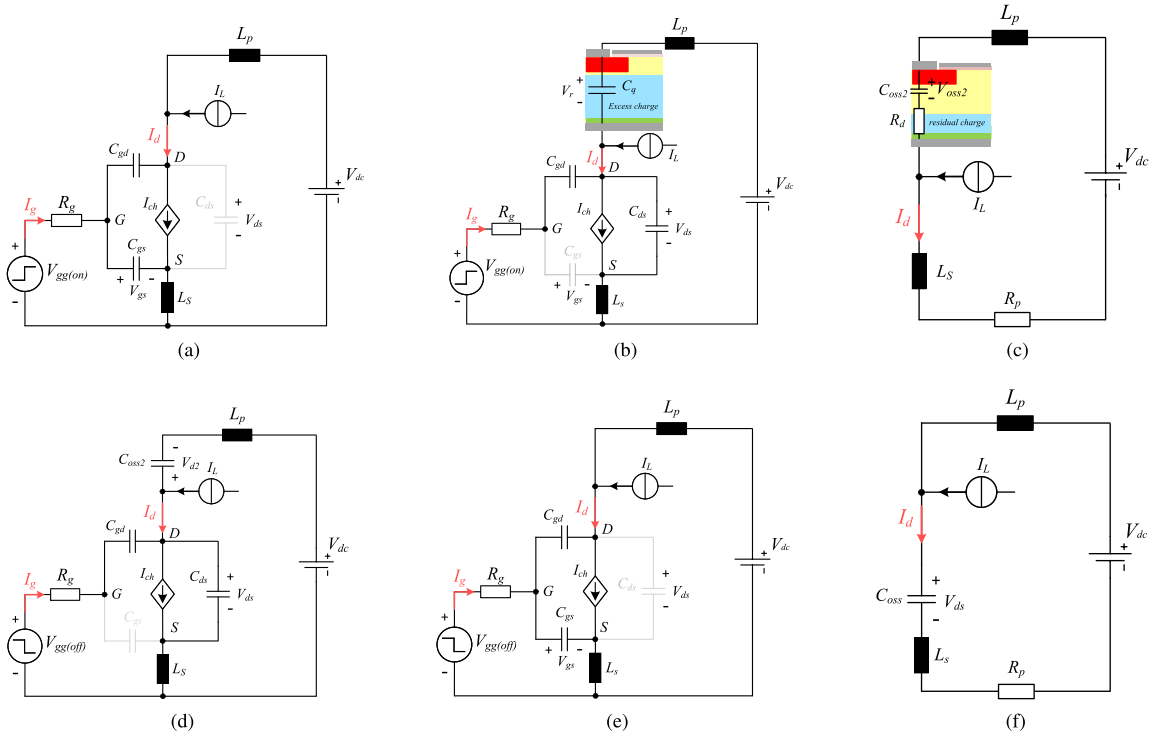

Fig. 4. The equivalent circuit of (a) Phase 1. (b) Phase 2 when T_1 operates in saturation region. (c) The end of phase 2 when T_1 operates in ohmic region. (d) Phase 3. (e) Phase 4 when $I_{\rm ch} > 0$. (f) The end of phase 4 when $I_{\rm ch} = 0$.

Kelvin source terminal. With the Kelvin source utilized, the L_s can be reduced to a level of a few hundred picohenries and the LCSI condition is achieved. Due to the small L_s, the negative feedback mechanism becomes very weak. The dI_d/dt thereby continuously increases, which causes a continuous reduction of $V_{\rm ds}$, as shown in Fig. 3(a).

At the end of this phase, I_d surpasses the load current I_L. The high-side body diode D_2 starts to conduct reverse current. However, since the N-base of SiC MOSFET is not depleted, D_2 can not support high reverse voltage in this phase [12]. Phase 1 ends when I_d reaches $I_L + I_{\rm rr}$, where $I_{\rm rr}$ is the peak reverse recovery current, which can be expressed by

$$I_{\rm rr} = \sqrt{\frac{2Q_{\rm rr} dI_d/dt|_{t=t_L}}{1+S}} \tag{1}$$

where $dI_d/dt|_{t=t_L}$ is the drain current slope when $I_d = I_L$ at $t = t_L$, as shown in Fig. 3(a). $Q_{\rm rr}$ is the reverse recovery charge. S is the softness factor of the body diode.

Phase 2 [t_1–t_2] [see Fig. 4(b) and (c)]: Phase 2 initiates when I_d reaches $I_L + I_{\rm rr}$. In this phase, the depletion region is formed in the P-well/N-base junction and N-base/ N+ substrate junction of D_2, as shown in Fig. 1(c). As a result, D_2 is able to support reverse voltage V_r [12], as shown in Fig. 4(b). With the increase of V_r, the depletion region extends, which extracts the excess charge in the N-base, as shown in Fig. 1(c). The charge extraction generates a capacitive current to support the reverse current of D_2. In Fig. 4(b), a capacitance C_q is used to represent the equivalent capacitance of D_2 in this phase, which consists of the capacitance generated by charge extraction and the output stray capacitance of the T_2. $C_q dV_r/dt$ thereby represents the capacitive current generated on D_2.

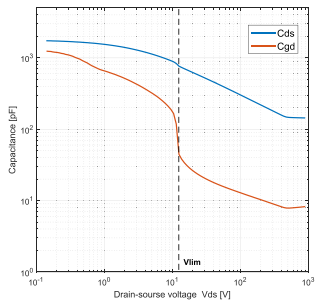

Fig. 5. *C–V* curve of the SiC MOSFET.

In phase 2, $V_{\rm ds}$ abruptly reduces. The high $dV_{\rm ds}/dt$ induces a displacement current $I_{\rm gd}$ on the gate-drain stray capacitance $C_{\rm gd}$. As shown in Fig. 2(b), $I_{\rm gd}$ generates voltage V_g on R_g, which hinders the $V_{\rm gs}$ to turn ON. This in return causes the reduction of $dV_{\rm ds}/dt$. A negative feedback action is thereby achieved to slow down the $dV_{\rm ds}/dt$.

In Fig. 3(a), phases 2a ($t_1 < t \le t_{1b}$) and 2b ($t_{1b} < t \le t_2$) are defined based on the voltage $V_{\rm lim}$ ($V_{\rm ds} = V_{\rm lim}$ at t_{1b}). In phase 2b, the $V_{\rm ds}$ drops below the $V_{\rm lim}$ and $dV_{\rm ds}/dt$ greatly reduces to a much lower level than that in phase 2a. The reduction is mainly due to the abrupt increase in the stray capacitances $C_{\rm gd}$, which cause stronger $C_{\rm gd} dV_{\rm ds}/dt$ induced feedback action to slow down the $dV_{\rm ds}/dt$. As shown in Fig. 5, the stray capacitances $C_{\rm gd}$ and $C_{\rm ds}$ have abrupt reduction when $V_{\rm ds}$ is higher than $V_{\rm lim}$. Due to a large stray capacitance generated by an ion-implantation-induced layer at the JFET region [8], [16], the $C_{\rm gd}$ and $C_{\rm ds}$ have a large value when $V_{\rm ds} < V_{\rm lim}$. When $V_{\rm ds} > V_{\rm lim}$, the depletion

region in N-base covers ion implantation layer. The $C_{\rm gd}$ and $C_{\rm ds}$ thereby greatly reduce [16].

In phase 2, the reverse current of D_2 snaps back to zero. Correspondingly, I_d snaps back from its peak value $I_L + I_{\rm rr}$ and reaches the load current I_L at $t = t_{1a}$, as shown in Fig. 3(a). Due to the high current slope of the snapback current, current oscillation is excited in the stage when $t > t_{1a}$. In this stage, T_1 completely turns ON and the equivalent circuit that excites the oscillation is presented in Fig. 4(c). In the circuit, R_p is power loop ac resistance generated by skin effect and radiation energy dissipation of the power loop circuit [17]. During the oscillatory transient, the residual charge in the N-base of the body diode acts as a damper for the oscillation [18], which gives rise to a damping resistance R_d, as shown in Fig. 4(c). The *RLC* resonance in the circuit generates oscillation of I_d.

B. Turn-OFF Behavior

Fig. 3(b) shows the turn-OFF transient of the SiC MOSFETs, which is divided into phases 3 and 4. Their equivalent circuits are given in Fig. 4(d)–(f). The two phases are given as follows:

Phase 3 [t_3–t_4] [see Fig. 4(d)]: When $V_{\rm gs}$ drops to the Miller voltage $V_{\rm miller}$, which can just support I_L, phase 3 starts. In this phase, the MOS channel current is not able to support I_L. To compensate the MOS channel current reduction, $V_{\rm ds}$ thereby has to increase to generate the displacement current on the output capacitance of T_1. The $C_{\rm gd} \times dV_{\rm ds}/dt$ induced negative feedback action presented in Fig. 2(b) also occurs, which slows down the turn-OFF $dV_{\rm ds}/dt$. In Fig. 3(b), the phases 3a ($t_3 < t \leq t_{3a}$) and 3b ($t_{3a} < t \leq t_4$) are defined by $V_{\rm lim}$. When $V_{\rm ds}$ rises above the $V_{\rm lim}$, the $dV_{\rm ds}/dt$ greatly increases due to the abruptly reduced $C_{\rm gd}$.

The increase of $V_{\rm ds}$ causes the reduction in the voltage of the high-side MOSFET T_2, which generates a displacement current on its output capacitance $C_{\rm oss2}$. In phase 3a, the displacement current is negligible due to the low $dV_{\rm ds}/dt$. In phase 3b, the high $dV_{\rm ds}/dt$ generates a much larger displacement current on $C_{\rm oss2}$, which gives rise to the reduction of I_d, as shown in Fig. 3(b).

Phase 4 [t_4–t_5] [see Fig. 4(e) and (f)]: When the $V_{\rm ds}$ reaches $V_{\rm dc}$ at t_4, phase 4 starts. In this phase, the diode current can divert from T_1 to D_2, I_d thereby quickly reduces. The gate voltage quickly turns OFF, which causes an abrupt reduction of MOS channel current $I_{\rm ch}$. Fig. 4(e) shows the equivalent circuit in this phase when $I_{\rm ch} > 0$. At the end of this phase, $I_{\rm ch} = 0$ and the equivalent circuit is presented in Fig. 4(f). The resonance in the circuit generates turn-OFF oscillation of I_d and $V_{\rm ds}$, which is dampened by the power loop ac resistance R_p.

III. Pivotal Physical Characteristics

Based on the analysis in Section II, some pivotal physical characteristics are discussed as follows.

A. Effective Stray Capacitance of SiC MOSFETs

The stray capacitances are vital for the switching behavior of SiC MOSFETs. The stray capacitances $C_{\rm gd}$ and $C_{\rm ds}$ of the SiC MOSFET are voltage-dependent and change abruptly near $V_{\rm lim}$, as shown in Fig. 5. To linearize the stray capacitances, the charge equivalent effective capacitance can be utilized [7]. As shown in Fig. 6, effective capacitances C_1 (When $V_{\rm ds} \leq V_{\rm lim}$) and C_2 (When $V_{\rm ds} > V_{\rm lim}$) are defined as follows:

$$C_1 = \frac{1}{V_{\rm lim}} \int_0^{V_{\rm lim}} C(v)dv = \frac{Q_1}{V_{\rm lim}} \tag{2}$$

$$C_2 = \frac{1}{V_0 - V_{\rm lim}} \int_{V_{\rm lim}}^{V_0} C(v)dv = \frac{Q_2}{V_0 - V_{\rm lim}}. \tag{3}$$

As shown in Fig. 6, Q_1 and Q_2 are obtained by integrating the *C–V* curve from 0V to $V_{\rm lim}$ and from $V_{\rm lim}$ to V_0, respectively. V_0 is the OFF-state drain-source voltage of the SiC MOSFET. With (2) and (3) utilized, the effective stray capacitances $C_{\rm gd}$ and $C_{\rm ds}$ can be expressed as follows:

$$\begin{cases} C_{\rm gd(ds)} = C_{\rm gd1(ds1)}, & V_{\rm ds} \leq V_{\rm lim} \\ C_{\rm gd2(ds2)}, & V_{\rm ds} > V_{\rm lim} \end{cases}. \tag{4}$$

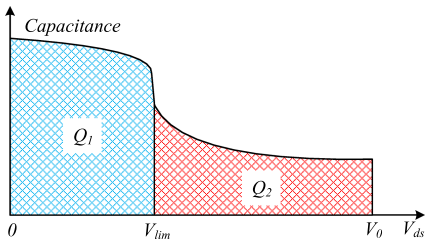

Fig. 6. Charges Q_1 and Q_2 integrated from *C–V* curve.

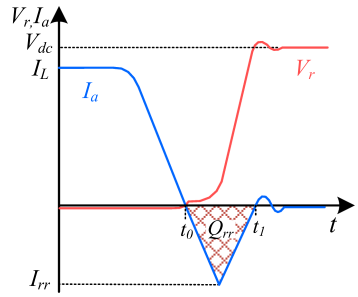

Fig. 7. Reverse recovery waveforms of SiC MOSFET body diode.

B. Effective Capacitance of Body Diode

In phase 2, the voltage-dependent capacitance C_q is used to reflect the excess charge extraction behavior. Fig. 7 shows the reverse recovery waveforms of the body diode. At reverse recovery transient, the diode reverse voltage V_r increases from 0 V to $V_{\rm dc}$, which generates the capacitive current $C_q dV_r/dt$ to support diode current, then

$$\int_0^{V_{\rm dc}} C_q(V)dV_r = Q_b \tag{5}$$

where Q_b is the equivalent charge of the diode, which contains the excess charge stored in the N-base and the capacitive charge stored in the output capacitance of T_2. If turn-ON is fast, all the excess charge in the N-base sweep out to support reverse

recovery and $Q_b \approx Q_{\rm rr}$ can be assumed to extract Q_b. $Q_{\rm rr}$ is the reverse recovery charge defined in Fig. 7. Based on (5), C_q is obtained by

$$C_q = \frac{Q_b}{V_{\rm dc}}. \tag{6}$$

The Q_b greatly depends on the load current I_L. Since Q_b is mainly supported by excess charge stored in the N-base, Q_b can be approximately expressed as [18]

$$Q_b \approx qAW_B\overline{p} \tag{7}$$

where A is die area. W_B is N-base width. $\overline{p}$ is average excess carrier density. Noting the excess carrier density p depends on I_L and can be expressed as [18] follows:

$$p = \frac{K}{2h_p}\left(\sqrt{1+\frac{4bh_pI_L}{(1+b)qAK^2}}-1\right) \approx \frac{1}{h_p}\sqrt{\frac{bh_pI_L}{(1+b)qA}} \tag{8}$$

where h_p is recombination parameter. $b = \mu_n/\mu_p$. μ_n and μ_p are electron and hole mobilities, respectively. Based on (8) and (9) is obtained

$$\overline{p} \propto \sqrt{I_L}. \tag{9}$$

Suppose the Q_{b0} is the excess charge at load current I_{L0}. Utilizing (7) and (9), the Q_b at I_L is obtained by the following:

$$Q_b = Q_{b0}\left(\frac{I_L}{I_{L0}}\right)^a \tag{10}$$

where $a = 0.5$ is default value. The equivalent capacitance C_d of high-side SiC MOSFET body diode can thereby be expressed by the following:

$$\begin{cases} C_d = C_q, & \text{in phase 2} \\ C_{\rm oss2}, & \text{in phase 3} \end{cases} \tag{11}$$

where $C_{\rm oss2} = C_{\rm gd2} + C_{\rm ds2}$. $C_{\rm gd2}$ and $C_{\rm ds2}$ are the effective capacitance of T_2 when $V_{\rm ds} > V_{\rm lim}$.

Since $Q_{\rm rr}$ is mainly supported by Q_b, the $Q_{\rm rr}$ at I_L can be obtained according to (10)

$$Q_{\rm rr} \approx Q_{\rm rr0}\left(\frac{I_L}{I_{L0}}\right)^a \tag{12}$$

where $Q_{\rm rr0}$ is the reverse recovery charge extracted at I_{L0}.

C. $C_{gd} \times dV_{ds}/dt$ and $L_s \times dI_d/dt$ Induced Negative Feedback

Fig. 8(a) summarizes the $C_{\rm gd} \times dV_{\rm ds}/dt$ induced feedback mechanism presented in Fig. 2(b). The $dV_{\rm ds}/dt$ induces a displacement current $I_{\rm gd}$ on $C_{\rm gd}$, which generates voltage V_g to counteract $V_{\rm gs}$. The $V_{\rm gs}$ in return controls $dV_{\rm ds}/dt$ and a feedback mechanism is thereby achieved. In phases 1–3, the negative feedback mechanism can significantly slow down the switching speed and thereby need to be considered.

The $L_s \times dI_d/dt$ induced negative feedback mechanisms are summarized in Fig. 8(b). The dI_d/dt generates a voltage V_s on the L_s, which counteracts the $V_{\rm gs}$ and hider the gate to turn ON/OFF. The $V_{\rm gs}$ in return controls the dI_d/dt and a negative feedback action is achieved. The feedback action significantly slows down the switching speed in phases 1, 3, and 4 and should be considered. In phase 1, $L_s \times dI_d/dt$ induced feedback mechanisms at HCSI and LCSI conditions have a huge impact on the $V_{\rm ds}$ and should be considered.

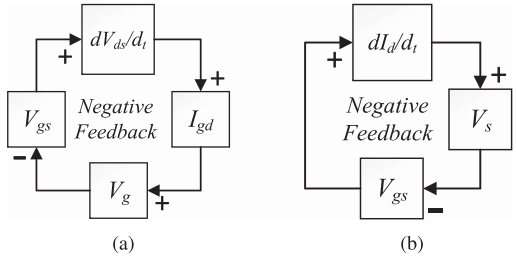

Fig. 8. (a) $C_{\rm gd} \times dV_{\rm ds}/dt$ and (b) $L_s \times dI_d/dt$ induced negative feedback mechanisms.

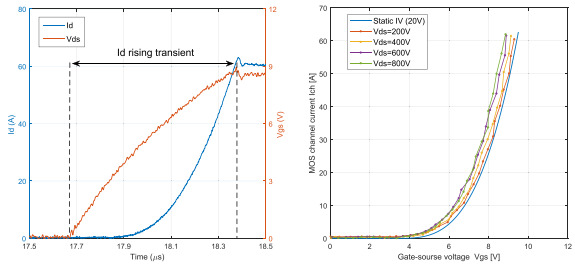

Fig. 9. (a) Turn-ON waveforms of SiC MOSFET C3M0040120K using $R_g = 250\,\Omega$ and (b) transfer characteristics of C3M0040120K extracted at switching and static conditions.

D. Dynamic Transfer Characteristics at Switching Transient

At switching transient, a high $V_{\rm ds}$ is applied. The dynamic transfer characteristics at switching transient are thereby different from at static data (using a low $V_{\rm ds}$) provided in the datasheet [11]. The dynamic transfer characteristics are extracted from turn-ON waveforms of I_d and $V_{\rm gs}$ [19] with a large R_g, which minimize the $V_{\rm ds}$ reduction during the current rising transient and suppress oscillation.

Fig. 9(a) shows the I_d and $V_{\rm gs}$ turn-ON waveforms of SiC MOSFET C3M0040120K. By plotting the $V_{\rm gs} - I_d$ data during the I_d rising transient, the dynamic transfer characteristics can be obtained. Fig. 9(b) compares the dynamic transfer characteristics of SiC MOSFET C3M0040120K under various $V_{\rm ds}$ and static I–V curves measured at $V_{\rm ds} = 20$V. It can be noticed that transfer characteristics of SiC MOSFET depend on $V_{\rm ds}$. Due to the drain-induced barrier lowering (DIBL) effect, the gate threshold voltage slightly reduces at switching transient. When higher $V_{\rm ds}$ is applied, the transconductance increases due to the short-channel effect [20]. During the switching transient, the SiC MOSFET mainly operates in saturation region. The channel current $I_{\rm ch}$ is expressed as [21] follows:

$$I_{\rm ch} = \frac{K_p}{2}(V_{\rm gs} - V_{\rm th})^2(1 + \lambda V_{\rm ds}) \tag{13}$$

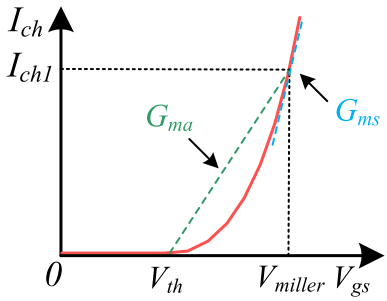

Fig. 10. Transconductance of SiC MOSFET.

where K_p is transconductance coefficient. λ is short-channel coefficient. The square function of $V_{\rm gs}$ in (13) makes analytical modelling infeasible. The (13) is thereby modified as follows:

$$I_{\rm ch} = G_m(V_{\rm gs} - V_{\rm th}) \tag{14}$$

where the transconductance G_m is a function of $I_{\rm ch}$ and $V_{\rm ds}$.

To linearize the G_m, the average transconductance $G_{\rm ma}$ and small-signal transconductance $G_{\rm ms}$ can be utilized [4]. As shown in Fig. 10, suppose the Miller voltage of $I_{\rm ch1}$ is $V_{\rm miller}$, the corresponding average transconductance $G_{\rm ma}$ for $I_{\rm ch} \in [0, I_{\rm ch1}]$ and small-signal transconductance $G_{\rm ms}$ at $I_{\rm ch} = I_{\rm ch1}$ can be calculated using (13)

$$G_{\rm ma} = \frac{I_{\rm ch1}}{V_{\rm miller} - V_{\rm th}} = \sqrt{\frac{I_{\rm ch1} K_p (1 + \lambda V_{\rm ds})}{2}} \tag{15}$$

$$G_{\rm ms} = \frac{dI_{\rm ch}}{dV_{\rm gs}}\Big|_{I_{\rm ch}=I_{\rm ch1}} = \sqrt{2 I_{\rm ch1} K_p (1 + \lambda V_{\rm ds})}. \tag{16}$$

Using (15) and (16), the transconductance in phases 1–4 can be obtained. In phase 1, the $V_{\rm ds}$ clamps near $V_{\rm dc}$ whereas the $I_{\rm ch}$ increases from zero to $I_L + I_{\rm rr}$. With $I_{\rm rr}$ neglected, the average transconductance with $I_{ch} \in [0, I_L]$ can be used in this phase. Using (15) with $V_{\rm ds} = V_{\rm dc}$ and $I_{\rm ch1} = I_L$, the transconductance $G_{\rm ma1}$ in phase 1 is expressed as follows:

$$G_{\rm ma1} = \sqrt{\frac{I_L K_p (1 + \lambda V_{\rm dc})}{2}}. \tag{17}$$

In phase 2, the $V_{\rm ds}$ drops from $V_{\rm dc}$ to ON-state voltage whereas the I_d snaps from $I_L + I_{\rm rr}$ to I_L. With $I_{\rm rr}$ and on-state voltage neglected, the small-signal transconductance $G_{\rm ms2}$ is utilized in phase 2, which is calculated by using (16) with $V_{\rm ds} = V_{\rm dc}/2$ and $I_{\rm ch1} = I_L$

$$G_{\rm ms2} = \sqrt{2 I_L K_p (1 + \lambda V_{\rm dc}/2)}. \tag{18}$$

In phase 3, $V_{\rm ds}$ increase from ON-state voltage to $V_{\rm dc}$ while I_d clamps near I_L. Therefore, (18) also valid in this phase.

In phase 4, I_d turns OFF, which causes the reduction of transconductance. On the other hand, the overshoot of $V_{\rm ds}$ gives rise to an increased transconductance. The small-signal transconductance at $V_{\rm ds} = V_{\rm dc}$ and $I_{\rm ch1} = I_L$ is thereby a good approximation of the transconductance in this phase [22]. The small-signal transconductance $G_{\rm ms4}$ in phase 4 is thereby calculated using (16) with $V_{\rm ds} = V_{\rm dc}$ and $I_{\rm ch1} = I_L$.

$$G_{\rm ms4} = \sqrt{2 I_L K_p (1 + \lambda V_{\rm dc})}. \tag{19}$$

IV. Analytical Model of Switching Transient

In this section, the analytical model of SiC MOSFET is derived. Details of the model are presented as follows.

A. Phase 1

Fig. 4(a) shows the equivalent circuit in phase 1. In the circuit, the gate current I_g can be expressed as follows:

$$I_g = (C_{\rm gs} + C_{\rm gd}) \frac{dV_{\rm gs}}{dt} - C_{\rm gd} \frac{dV_{\rm ds}}{dt}. \tag{20}$$

Using KVL in the gate loop of the circuit, (21) is obtained.

$$V_{\rm gg(on)} = R_g I_g + V_{\rm gs} + L_s \frac{dI_d}{dt}. \tag{21}$$

In phase 1, I_d is mainly supported by $I_{\rm ch}$. Neglecting the $dV_{\rm ds}/dt$ induced displacement current, the following is obtained

$$I_d = G_m(V_{\rm gs} - V_{\rm th}). \tag{22}$$

Using KVL in the power loop of the circuit, the following is obtained

$$V_{\rm dc} = V_{\rm ds} + (L_s + L_p) \frac{dI_d}{dt}. \tag{23}$$

Combining (20)–(23), the following is obtained:

$$\alpha_1 \frac{d^2 I_d}{dt^2} + \beta_1 \frac{dI_d}{dt} + I_d = G_{\rm ma1}(V_{\rm gg(on)} - V_{\rm th}) \tag{24}$$

where $\alpha_1 = (L_s + L_p) R_g C_{\rm gd} G_m$ and $\beta_1 = R_g(C_{\rm gd} + C_{\rm gs}) + L_s G_m$. Equation (24) is solved with following initial conditions:

$$I_d(t = t_0) = 0 \tag{25}$$

$$\frac{dI_d}{dt}\bigg|_{t=t_0} = 0. \tag{26}$$

The solution of (24) depends on the relationship between L_s and its threshold value $L_{S(\rm th)}$, which is defined as follows:

$$L_{S(\rm th)} = \frac{2\sqrt{R_g C_{\rm gd}(G_{\rm ma1} L_p - R_g C_{\rm gs})} - R_g(C_{\rm gs} - C_{\rm gd2})}{G_m}. \tag{27}$$

When $L_s > L_{S(\rm th)}$, the solution of (24) is as follows:

$$I_d = (V_{\rm gg(on)} - V_{\rm th}) \left(\frac{G_m \tau_1}{\tau_0 - \tau_1} e^{\tau_0 (t - t_0)} + \frac{G_m \tau_0}{\tau_1 - \tau_0} e^{\tau_1 (t - t_0)} \right) + G_m (V_{\rm gg(on)} - V_{\rm th}) \tag{28}$$

where the coefficient $\tau_0 = (-\beta_1 + \sqrt{\beta_1^2 - 4\alpha_1})/2\alpha_1$. The coefficient $\tau_1 = (-\beta_1 - \sqrt{\beta_1^2 - 4\alpha_1})/2\alpha_1$.

The dI_d/dt can thereby be obtained as follows:

$$\frac{dI_d}{dt} = (V_{\rm gg(on)} - V_{\rm th}) \left(\frac{G_m \tau_0 \tau_1}{\tau_0 - \tau_1} e^{\tau_0 (t - t_0)} + \frac{G_m \tau_0 \tau_1}{\tau_1 - \tau_0} e^{\tau_1 (t - t_0)} \right) \tag{29}$$

When $L_s < L_{S(\text{th})}$, the solution of (24) is as follows:

$$I_d = e^{\tau_a(t-t_0)}\left(\frac{\tau_a}{\omega}\sin(\omega(t-t_0)) - \cos(\omega(t-t_0))\right) \times G_m(V_{\text{gg(on)}} - V_{\text{th}}) + G_m(V_{\text{gg(on)}} - V_{\text{th}}) \quad (30)$$

where $\tau_a = -\beta_1/2\alpha_1$, and $\omega = \sqrt{4\alpha_1 - \beta_1^2}/2\alpha_1$.

The dI_d/dt can thereby be calculated by the following:

$$\frac{dI_d}{dt} = e^{\tau_a t} G_m \left(\frac{\omega^2+\tau_a^2}{\omega}\right)(V_{\text{gg(on)}} - V_{\text{th}})\sin(\omega(t-t_0)). \quad (31)$$

In phase 1, $C_{\text{gd}} = C_{\text{gd2}}$ and $G_m = G_{\text{ma1}}$. The V_{ds} under HCSI and LCSI conditions are given as follows.

1) HCSI Condition: With HCSI, V_{ds} clamped at a plateau due to the $L_s dI_d/dt$ induced negative feedback. With $L_s dI_d/dt$ included in (21), V_{ds} can be expressed as follows:

$$V_{\text{ds}} = (L_p + L_s)\frac{dI_d}{dt} \quad (32)$$

where dI_d/dt is obtained using (29) or (31).

2) LCSI Condition: With LCSI, dV_{ds}/dt is expressed as follows:

$$\frac{dV_{ds}}{dt} = -\frac{(L_p + L_s)\left.\frac{dI_d}{dt}\right|_{t=t_L}}{T_L}. \quad (33)$$

As shown in Fig. 3(a), t_L is the time when $I_d = I_L$, the duration $T_L = t_L - t_0$. t_L is obtained by using (28) or (30) with $I_d = I_L$. $dI_d/dt|_{t=t_L}$ is obtained using (29) or (31).

B. Phase 2

In this phase, the D_2 starts to support the reverse voltage V_r. The increased V_r generates capacitive current on C_q, then

$$I_L = I_d - C_q\frac{dV_r}{dt} = I_d + C_q\frac{dV_{\text{ds}}}{dt} \quad (34)$$

Since increase of V_r causes reduction of V_{ds}, $dV_{\text{ds}}/dt \approx -dV_r/dt$ is assumed in (34). As shown in Fig. 4(b), I_d is as follows:

$$I_d = G_m(V_{\text{gs}} - V_{\text{th}}) + (C_{\text{gd}} + C_{\text{ds}})\frac{dV_{\text{ds}}}{dt}. \quad (35)$$

With high dV_{ds}/dt, the gate current I_g is mainly supported by $C_{\text{gd}}dV_{\text{ds}}/dt$ induced displacement current in this phase. I_g is thereby expressed as follows:

$$I_g = -C_{\text{gd}}\frac{dV_{\text{ds}}}{dt}. \quad (36)$$

Combing (21) and (34)–(36), the following is obtained

$$\alpha_2\frac{d^2V_{\text{ds}}}{dt^2} + \beta_2\frac{dV_{\text{ds}}}{dt} = I_L - G_m(V_{\text{gg(on)}} - V_{\text{th}}) \quad (37)$$

where $\alpha_2 = G_m L_s C_q$ and $\beta_2 = C_{ds} + C_q + C_{\text{gd}}(1 + R_g G_m)$. Equation (37) is solved in phases 2a and 2b, which is given as follows.

1) Phase 2a: In phase 2a, the initial conditions are as follows:

$$V_{\text{ds}}(t = t_1) = V_1 \quad (38)$$

$$\left.\frac{dV_{\text{ds}}}{dt}\right|_{t=t_1} = S_1. \quad (39)$$

The V_1 and S_1 can be obtained by (32) or (33), respectively. The solution of (37) then can be obtained as follows:

$$V_{\text{ds}} = \frac{S_1\beta_2 + G_m(V_{\text{gg(on)}} - V_{\text{th}}) - I_L}{\beta_2\tau_2}e^{\tau_2(t-t_1)} - \frac{S_1}{\tau_2} + (I_L - G_m(V_{\text{gg(on)}} - V_{\text{th}}))\left(\frac{t-t_1}{\beta_2} + \frac{1}{\beta_2\tau_2}\right) + V_1 \quad (40)$$

where $\tau_2 = -\beta_2/\alpha_2$. The dV_{ds}/dt is thereby obtained as follows:

$$\frac{dV_{\text{ds}}}{dt} = \frac{I_L - G_m(V_{\text{gg(on)}} - V_{\text{th}})}{\beta_2}(1 - e^{\tau_2(t-t_1)}) + S_1 e^{\tau_2(t-t_1)}. \quad (41)$$

In (40) and (41), C_q reflects the impact of charge extraction on the high-side body diode. $C_{\text{gd}}R_g G_m$ reflects the $C_{\text{gd}}dV_{\text{ds}}/dt$ induced feedback mechanism. In phase 2a, $G_m = G_{\text{ms2}}$, $C_{ds} = C_{\text{ds2}}$, and $C_{\text{gd}} = C_{\text{gd2}}$ are utilized.

2) Phase 2b: In phase 2b, the initial conditions are as follows:

$$V_{\text{ds}}(t = t_{1b}) = V_{\text{lim}} \quad (42)$$

$$\left.\frac{dV_{\text{ds}}}{dt}\right|_{t=t_{1b}} = S_2 \quad (43)$$

where the S_2 can be obtained by (41).

The solution (37) in phase 2b is thereby be obtained by the following:

$$V_{\text{ds}} = \frac{S_2\beta_2 + G_m(V_{\text{gg(on)}} - V_{\text{th}}) - I_L}{\beta_2\tau_2}e^{\tau_2(t-t_{1b})} - \frac{S_2}{\tau_2} + (I_L - G_m(V_{\text{gg(on)}} - V_{\text{th}}))\left(\frac{t-t_{1b}}{\beta_2} + \frac{1}{\beta_2\tau_2}\right) + V_{\text{lim}}. \quad (44)$$

The dV_{ds}/dt is expressed as follows:

$$\frac{dV_{\text{ds}}}{dt} = \frac{I_L - G_m(V_{\text{gg(on)}} - V_{\text{th}})}{\beta_2}(1 - e^{\tau_2(t-t_{1b})}) + S_2 e^{\tau_2(t-t_{1b})}. \quad (45)$$

In phase 2b, $G_m = G_{\text{ms2}}$, $C_{ds} = C_{\text{ds1}}$, and $C_{\text{gd}} = C_{\text{gd1}}$.

3) Current Snapback and Oscillation: In phase 2, when $t_1 < t \le t_{1a}$, I_d snaps back to I_L due to the diode reverse recovery, which generates current oscillation. The snapback dI_d/dt is

$$\frac{dI_d}{dt} = -\frac{1}{S}\left.\frac{dI_d}{dt}\right|_{t=t_L}. \quad (46)$$

As shown in Fig. 3(a), when $t > t_{1a}$, the current oscillation occurs. The oscillation is excited by the circuit in Fig. 4(c). Based on the circuit, (47) and (48) are obtained as follows.

$$I_d = C_{\text{oss2}}\frac{dV_{\text{oss2}}}{dt} + I_L \quad (47)$$

$$V_{\text{dc}} = V_{\text{oss2}} + (L_p + L_s)\frac{dI_d}{dt} + I_d(R_p + R_d). \quad (48)$$

Combining (47) and (48), the following is obtained

$$\alpha_r\frac{d^2I_d}{dt^2} + \beta_r\frac{dI_d}{dt} + I_d = I_L \quad (49)$$

where $\alpha_r = C_{\text{oss2}}(L_p + L_s)$, $\beta_r = C_{\text{oss2}}(R_p + R_d)$. At oscillatory transient, the output capacitance C_{oss2} is obtained at $V_{\text{ds}} = V_{\text{DC}}$. The initial conditions for (49) at t_{1a} are as follows:

$$I_d(t = t_{1a}) = I_L \tag{50}$$

$$\frac{dI_d}{dt}(t = t_{1a}) = A_r. \tag{51}$$

The expression of I_d when $t > t_{1a}$ is thereby obtained as follows:

$$I_d = \mathrm{e}^{\xi_r}\frac{A_r}{w_r}\sin(w_r(t - t_{1a})) + I_L \tag{52}$$

where $w_r = \sqrt{4\alpha_r - \beta_r^2}/2\alpha_r$ and $\xi_r = -\beta_r/2\alpha_r$.

C. Phase 3

As shown in Fig. 4(d), in phase 3, (34) is valid with C_Q replaced as C_{oss2}

$$I_L = I_d + C_{\text{oss2}}\frac{dV_{\text{ds}}}{dt}. \tag{53}$$

Using KVL in the gate loop of the circuit, (54) is obtained

$$V_{\text{gg(off)}} = R_g I_g + V_{\text{gs}} + L_s\frac{dI_d}{dt}. \tag{54}$$

The I_d can be expressed as follows:

$$I_d = I_L + G_m(V_{\text{gs}} - V_{\text{miller}}) + (C_{\text{gd}} + C_{\text{ds}})\frac{dV_{\text{ds}}}{dt} \tag{55}$$

where V_{miller} is the miller voltage for the load current I_L. Combining (36) and (53)–(55), the following is obtained

$$\alpha_3\frac{d^2V_{\text{ds}}}{dt^2} + \beta_3\frac{dV_{\text{ds}}}{dt} = G_m(V_{\text{miller}} - V_{\text{gg(off)}}) \tag{56}$$

where $\alpha_3 = G_m L_s C_{\text{oss2}}$ and $\beta_3 = C_{ds} + C_{\text{oss2}} + C_{\text{gd}}(1 + R_g G_m)$. Equation (56) is solved in phases 3a and 3b.

1) Phase 3a: In phase 3a, the initial conditions are as follows:

$$V_{\text{ds}}(t = t_3) = 0 \tag{57}$$

$$\left.\frac{dV_{\text{ds}}}{dt}\right|_{t=t_3} = 0. \tag{58}$$

The solution of (56) in phase 3a is as follows:

$$V_{\text{ds}} = \frac{G_m(V_{\text{gg(off)}} - V_{\text{miller}})}{\beta_3\tau_3}e^{\tau_3(t-t_3)} + G_m(V_{\text{miller}} - V_{\text{gg(off)}})\left(\frac{t - t_3}{\beta_3} + \frac{1}{\beta_3\tau_3}\right) \tag{59}$$

where $\tau_3 = -\beta_3/\alpha_3$. The dV_{ds}/dt is thereby obtained as follows:

$$\frac{dV_{\text{ds}}}{dt} = \frac{G_m(V_{\text{miller}} - V_{\text{gg(off)}})}{\beta_3}(1 - e^{\tau_3(t-t_3)}). \tag{60}$$

In phase 3a, $G_m = G_{\text{ms2}}$, $C_{ds} = C_{\text{ds1}}$, $C_{\text{gd}} = C_{\text{gd1}}$ and $C_{\text{oss2}} = C_{\text{gd2}} + C_{\text{ds2}}$ are utilized. With a low dV_{ds}/dt and a small capacitance C_{oss2}, the displacement current on C_{oss2} is very small and $I_d = I_L$ is assumed in phase 3a.

2) Phase 3b: In phase 3b, the initial condition of (56) is

$$V_{\text{ds}}(t = t_{3a}) = V_{\text{lim}} \tag{61}$$

$$\left.\frac{dV_{\text{ds}}}{dt}\right|_{t=t_{3a}} = S_3. \tag{62}$$

S_3 is obtained from (60). The solution of (56) in phase 3b is

$$V_{\text{ds}} = \frac{\beta_3 S_3 + G_m(V_{\text{gg(off)}} - V_{\text{miller}})}{\beta_3\tau_3}e^{\tau_3(t-t_{3a})} + V_{\text{lim}} + G_m(V_{\text{miller}} - V_{\text{gg(off)}})\left(\frac{t - t_{3a}}{\beta_3} + \frac{1}{\beta_3\tau_3}\right) - \frac{S_3}{\tau_3} \tag{63}$$

The dV_{ds}/dt is obtained as

$$\frac{dV_{\text{ds}}}{dt} = \frac{G_m(V_{\text{miller}} - V_{\text{gg(off)}})}{\beta_3}(1 - e^{\tau_3(t-t_{3a})}) + S_3 e^{\tau_3(t-t_{3a})}. \tag{64}$$

In phase 3b, $G_m = G_{\text{ms2}}$, $C_{ds} = C_{\text{ds2}}$, $C_{\text{gd}} = C_{\text{gd2}}$ and $C_{\text{oss2}} = C_{\text{gd1}} + C_{\text{ds1}}$ are utilized.

In phase 3b, the high dV_{ds}/dt generates displacement current on the high-side MOSFET, which causes the drain current reduction. The dI_d/dt in this phase 3b is obtained by the following:

$$\frac{I_d}{dt} = -\frac{C_{\text{oss2}}(V_{\text{lim}})\left.\frac{dV_{\text{ds}}}{dt}\right|_{t_4}}{T_{D3}} \tag{65}$$

where T_{D3} is the duration of phase 4, as shown in Fig. 3(b). The T_{D3} and $dV_{\text{ds}}/dt|_{t_4}$ are obtained from (63) and (64). $C_{\text{oss2}}(V_{\text{lim}})$ is the output capacitance of high-side MOSFET at V_{lim}. At the end of phase 3, the diode has to support a few to tens of volts due to the voltage on the L_p. The C_{oss2} at t_4 thereby approximately equal to $C_{\text{oss2}}(V_{\text{lim}})$.

D. Phase 4

The equivalent circuit in phase 4 is shown in Fig. 4(e). In phase 4, dV_{ds}/dt greatly reduces, the $C_{\text{gd}} \times dV_{\text{ds}}/dt$ induced feedback is neglected. I_g is thereby expressed as follows:

$$I_g = (C_{\text{gs}} + C_{\text{gd}})\frac{dV_{\text{gs}}}{dt}. \tag{66}$$

Since I_d is mainly supported by MOS channel current, then

$$I_d = G_m(V_{\text{gs}} - V_{\text{th}}). \tag{67}$$

Combining (54), (66), and (67), the following can be obtained

$$\beta_1\frac{dI_d}{dt} + I_d = G_m(V_{\text{gg(off)}} - V_{\text{th}}). \tag{68}$$

Solve the equation (68) with following initial conditions:

$$I_d(t = t_4) = I_{d4} = G_m(V_{\text{miller2}} - V_{\text{th}}) \tag{69}$$

where I_{d4} is I_d at $t = t_4$ and V_{miller2} is the Miller voltage of I_{d4}, as shown in Fig. 3(b). The solution of (68) is as follows:

$$I_d = G_m(V_{\text{miller2}} - V_{\text{gg(off)}})e^{-\frac{t-t_4}{\beta_1}} + G_m(V_{\text{gg(off)}} - V_{\text{th}}). \tag{70}$$

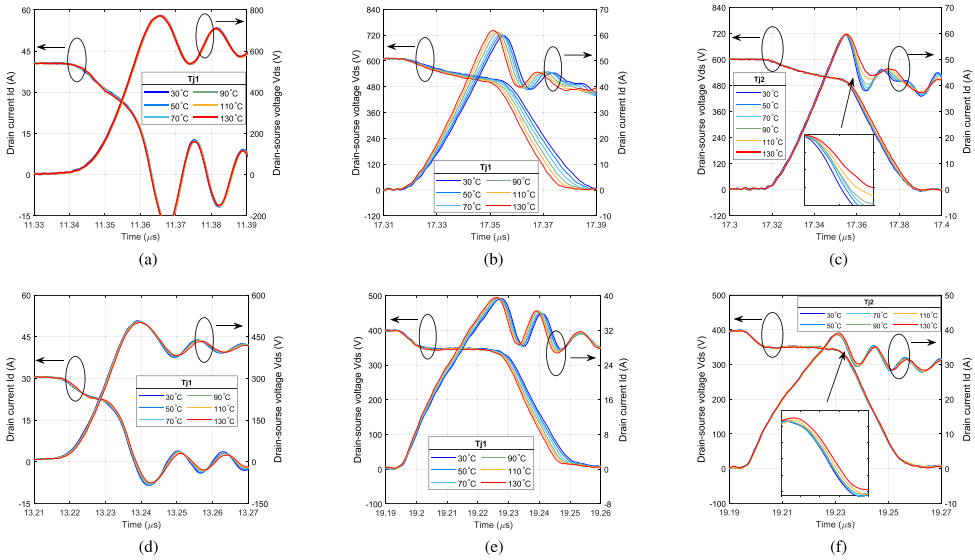

Fig. 11. Comparison of (a) Turn-OFF waveforms of C3M0040120K when T_{J1} varies while $T_{J2} = 30°$C. (b) Turn-ON waveforms of C3M0040120K when T_{J1} varies while $T_{J2} = 30°$C, (c) Turn-ON waveforms of C3M0040120K varies when T_{J2} varies while $T_{J1} = 30°$C. (d) Turn-OFF waveforms of C3M0045065D when T_{J1} varies while $T_{J2} = 30°$C. (e) Turn-ON waveform of C3M0045065D when T_{J1} varies while $T_{J2} = 30°$C, (f) Turn-ON waveforms of C3M0045065D when T_{J2} varies while $T_{J1} = 30°$C.

The dI_d/dt can thereby be expressed as follows:

$$\frac{dI_d}{dt} = -\frac{G_m(V_{\text{miller2}} - V_{\text{gg(off)}})}{\beta_1} e^{-\frac{t-t_4}{\beta_1}} \tag{71}$$

where $G_m = G_{\text{ms4}}$, $C_{\text{ds}} = C_{\text{ds2}}$, $C_{\text{gd}} = C_{\text{gd2}}$ are used.

1) Oscillation of V_{ds} and I_d: The V_{ds} overshoot and oscillation in the end of phase 4 is excited by the circuit shown in Fig. 4(f). Based on Fig. 4(f), the following are obtained

$$I_d = (C_{\text{gd}} + C_{\text{ds}})\frac{dV_{\text{ds}}}{dt} \tag{72}$$

$$V_{\text{dc}} = V_{\text{ds}} + (L_p + L_s)\frac{dI_d}{dt} + I_d R_p. \tag{73}$$

Combining (72) and (73), then

$$\alpha_4 \frac{d^2 V_{\text{ds}}}{dt^2} + \beta_4 \frac{dV_{\text{ds}}}{dt} + V_{\text{ds}} = V_{\text{dc}} \tag{74}$$

where $\alpha_4 = (C_{\text{gd}} + C_{\text{ds}})(L_p + L_s)$ and $\beta_4 = (C_{\text{gd}} + C_{\text{ds}})R_p$. Equation (74) is solved with the following initial conditions:

$$V_{\text{ds}}(t = t_4) = V_{\text{dc}} \tag{75}$$

$$V_{\text{ds}}\big|_{\text{peak}} = V_{\text{peak}}. \tag{76}$$

The peak overshoot voltage $V_{\text{peak}} = -(L_p + L_s)dI_d/dt|_{\text{min}}$. $dI_d/dt|_{\text{min}}$ is the minimum dI_d/dt in phase 4, which can be calculated by (77) according to (71)

$$\left.\frac{dI_d}{dt}\right|_{\text{min}} = -\frac{G_m(V_{\text{miller2}} - V_{\text{gg(off)}})}{\tau_b}. \tag{77}$$

The solution of (74) is

$$V_{\text{ds}} = \text{e}^{\xi_e(t-t_4)} V_{\text{peak}} \sin(\omega_e(t - t_4)) + V_{\text{dc}} \tag{78}$$

where $\omega_e = \sqrt{4\alpha_4 - \beta_4^2}/2\alpha_6$ and $\xi_e = -\beta_4/2\alpha_4$. During the oscillatory transient, C_{ds} and C_{gd} are obtained at V_{dc}.

The oscillation of I_d can be obtained also using circuit presented in Fig. 4(f). Combing (72) and (73), the following can be obtained

$$\alpha_4 \frac{d^2 I_d}{dt^2} + \beta_4 \frac{dI_d}{dt} + I_D = 0. \tag{79}$$

The initial conditions

$$I_D(t = t_{4a}) = 0 \tag{80}$$

$$\frac{dI_D}{dt}(t = t_{4a}) = A_s \tag{81}$$

where A_s can be obtained by (71). The solution of (79) is

$$I_D = \text{e}^{\xi_e t}\frac{A_s}{w_e}\sin(w_e(t - t_{4a})). \tag{82}$$

V. Temperature-Dependency of SiC MOSFET

A. Temperature-Dependent Switching Behavior

To identify the temperature dependence of SiC MOSFET, double pulse test is performed with junction temperature T_{J1} of low-side MOSFET T_1 and junction temperature T_{J2} of high-side MOSFET T_2 heated to various values. Fig. 11 shows the test results using various T_{J1} and T_{J2}. The switching starting time is aligned (the switching delay due to variation of temperature is removed) for comparison. Fig. 12 shows the double-pulse test fixture utilized. An electrical heater is attached to the device under test to heat T_{J1} and T_{J2} to a preset temperature. The heater is integrated with a thermocouple, which is used to monitor the junction temperature.

Fig. 11(a) and (d) compares the experimental turn-OFF waveforms of C3M0040120K and C3M0045065D when $T_{J2} = 30°$C, while T_{J1} varies from 30 to 130°C. It can be noticed that T_{J1} does not significantly affect the turn-OFF behavior of SiC MOSFET. As shown in Fig. 11(b) and (e), the turn-ON

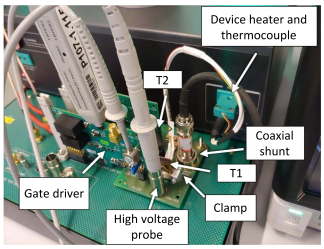

Fig. 12. Double-pulse test platform.

waveforms of C3M0040120K and C3M0045065D shows that turn-ON dI_d/dt and dV_{ds}/dt significantly increases when higher T_{J1} are used.

To identify the T_{J1} and T_{J2} dependence on the switching behavior, a simplified expression of dI_d/dt and dV_{ds}/dt should be derived. The simplified expression of turn-ON dI_d/dt is obtained by neglecting the $C_{gd}dV_{ds}/dt$ term in (20) and combing (20)–(22), then

$$\left.\frac{dI_d}{dt}\right|_{on} \approx \frac{G_m(V_{gg(on)} - V_{th}) - I_L/2}{\beta_1}. \tag{83}$$

Taking the derivation of (83) with respective to T_{J1}

$$\left.\frac{dI_d^2}{dtdT}\right|_{on} = \frac{a_1\dfrac{dG_m}{dT} + b_1\dfrac{dV_{th}}{dT}}{\beta_1^2} \tag{84}$$

where $a_1 = R_G(C_{gs}+C_{gd})(V_{gg(on)}-V_{th}) + I_L L_s/2$ and $b_1 = -G_m\beta_1$. To derive a simplified expression of turn-ON dV_{ds}/dt, the $L_s dI_d/dt$ in (21) is neglected. Combing (34)–(36) and multiplying by -1, turn-ON dV_{ds}/dt is obtained as

$$\left.\frac{dV_{ds}}{dt}\right|_{on} \approx \frac{G_m(V_{GG(on)} - V_{th}) - I_L}{\beta_2}. \tag{85}$$

Take the derivation of (85) with respect to T_{J1}, then

$$\left.\frac{dV_{ds}^2}{dtdT}\right|_{on} = \frac{a_2\dfrac{dG_m}{dT} + b_2\dfrac{dV_{th}}{dT}}{\beta_2^2} \tag{86}$$

where $a_2 = (C_{ds} + C_q + C_{gd})(V_{gg(on)} - V_{th}) + I_L R_g C_{gd}$. $b_2 = -G_m\beta_2$. Combining (54), (66), and (67) and multiplying by -1, the turn-OFF dI_d/dt can be approximately obtained by

$$\left.\frac{dI_d}{dt}\right|_{off} \approx \frac{G_m(V_{th} - V_{gg(off)}) + I_L/2}{\beta_1}. \tag{87}$$

Take the derivation of (87) with respect to T_{J1}

$$\left.\frac{dI_d^2}{dtdT}\right|_{off} = \frac{a_3\dfrac{dG_m}{dT} + b_3\dfrac{dV_{th}}{dT}}{\beta_1^2} \tag{88}$$

where $\alpha_3 = R_g(C_{gs} + C_{gd})(V_{th} - V_{gg(off)}) - L_s I_L/2$ and $b_3 = G_m\beta_1$. With $L_s dI_d/dt$ in (54) neglected, the (89) for turn-OFF dV_{ds}/dt is obtained using (36) and (53)–(55).

$$\left.\frac{dV_{ds}}{dt}\right|_{off} = \frac{G_m(V_{th} - V_{gg(off)}) + I_L}{\beta_3}. \tag{89}$$

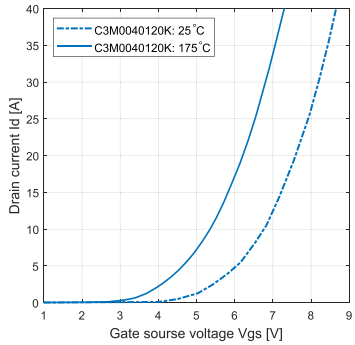

Fig. 13. *IV* curves of the C3M0040120K at 25°C and 175°C ($V_{ds} = 20\,V$).

Take derivative of (89) with respect to T_{J1}, then

$$\left.\frac{dV_{ds}^2}{dtdT}\right|_{off} \approx \frac{a_4\dfrac{dG_m}{dT} + b_4\dfrac{dV_{th}}{dT}}{\beta_3^2} \tag{90}$$

where $a_4 = (C_{ds} + C_{oss2} + C_{gd})(V_{th} - V_{gg(off)}) - I_L R_g C_{gd}$. $b_4 = \beta_3 G_m$. Fig. 13 shows temperature-dependent transfer characteristics of the SiC MOSFET C3M0040120K. With the increase of temperature, V_{th} decreases since the MOS channel becomes easier to invert due to bandgap narrowing [23], [24]. The V_{th} of SiC MOSFETs thereby has a negative temperature coefficient (NTC). For SiC MOSFETs, a higher temperature induce higher channel mobility [25], which can give rise to increased transconductance and positive temperature coefficient (PTC) can be achieved [26].

In (84) and (86), a_1 and a_2 are positive while b_1 and b_2 are negative. With a PTC for G_m and a NTC for V_{th}, the impacts of dG_m/dT and dV_{th}/dT thereby add up, which induces significant temperature dependence of turn-ON dI_d/dt and dV_{ds}/dt. Since a_3 and a_4 are much smaller than b_3 and b_4, the turn-OFFdI_d/dt and dV_{ds}/dt is mainly determined by dV_{th}/dT. Moreover, the a_3 and a_4 can be negative. In this case, the impacts of dG_m/dT and dV_{th}/dT can even contract with each other. The temperature dependence of turn-OFF dI_d/dt and dV_{ds}/dt is thereby very weak and can be neglected.

Fig. 11(c) and (f) shows the experimental turn-ON waveforms of C3M0040120K and C3M0045065D when the T_{J2} varies from 30 to 130°C while $T_{J1} = 30$°C. With the increases of T_{J2}, the excess charge in the N-base of T_2 increases. This generates larger Q_{rr}, which induces softer reverse recovery and higher reverse current peak for their body diodes. Therefore, with the increase of T_{J2}, the slope of snapback current reduces and peak current increases.

B. Temperature-Dependent Models

To model the temperature dependence, the temperature-dependent model of various parameters should be included. The T_{J1} dependent transconductance coefficient is

$$K_p(T_{J1}) = K_{p0}\left(\frac{T_{J1}}{300}\right)^c \tag{91}$$

where c is the temperature coefficient. K_{p0} is the transconductance coefficient at 300 K. The T_{J1} dependent model of V_{th} is

given as follows:

$$V_{\text{th}}(T_{J1}) = V_{\text{th0}} + T_{kp}(T_{J1} - 300) \tag{92}$$

where T_{kp} is temperature coefficient. V_{th0} is threshold voltage at 300 K. T_{J2} dependent model of Q_{rr} is obtained as

$$Q_{\text{rr}}(T_{J2}) = Q_{\text{rr0}} \left(\frac{T_{J2}}{300}\right)^{k} \tag{93}$$

where k is temperature coefficient. Q_{rr0} is reverse recovery charge at 300 K. T_{J2} dependent model of softness factor S is

$$S(T_{J2}) = S_0 \left(\frac{T_{J2}}{300}\right)^{e} \tag{94}$$

where e is the temperature coefficient. S_0 is S at 300 K.

VI. Parameter Extraction

The stray capacitances C_{gd1}, C_{gd2}, C_{ds1}, C_{ds2} and the voltage V_{lim} are extracted from *C–V* curves based on the definition presented in Fig. 6. K_p and λ are estimated from the *I–V* curves of the DUTs [11], [27]. V_{th} can be extracted using dynamic transfer curves presented in Fig. 9(a) or approximately estimated using the gate charge curve *I–V* curves provided in the datasheet [4]. The internal gate resistances R_{gi} and $R_{g(\text{int})}$ can be obtained from the device datasheet or measured using a device analyzer. The reverse recovery charge Q_{rr} can be extracted from reverse recovery waveforms or obtained from the datasheet. The softness factor S can be measured from reverse recovery waveforms or estimated using the following:

$$S = \frac{t_{\text{rr}}^2}{2Q_{\text{rr}}} \frac{dI_F}{dt} - 1 \tag{95}$$

where dI_F/dt is the current slop used to obtain Q_{rr}. t_{rr} is reverse recovery time. The capacitance C_q can be estimated by (6). The coefficients T_{kp}, c, k, and e can be extracted using (91)–(94). The typical values of common source inductance L_s for various device packages are presented in [4], [15], and [28]. L_s can also be extracted from the method presented in [27] or obtained form the Spice model provided by the manufacturer. The power loop inductance L_p can be estimated using turn-OFF dI/dt and overshoot voltage [27]. The ac resistances R_d and R_p can be estimated by fitting the switching oscillation waveforms. Using the approach proposed in [29] and [27], a parameter optimization can be performed to improve the accuracy of the parameters.

VII. Experimental Validation

To validate the proposed model, a 1200 V/60 A SiC MOSFET C3M0040120K, 650 V/39 A SiC MOSFET IMZA65R048M1H, 650 V/40 A SiC MOSFET C3M0045065D, and 650 V/39 A SiC MOSFET IMW65R048M1H are used. Utilizing TO-247-3 package, the C3M0045065D has $L_S = 3.5\,\text{nH}$ and IMW65R048M1H has $L_S = 2\,\text{nH}$. The devices thereby have HCSI. Utilizing TO-247-4 package with a Kelvin source terminal, the C3M0040120K has $L_S = 200\,\text{pH}$ and IMZA65R048M1H has $L_S = 100\,\text{pH}$. LCSI conditions are achieved for the devices.

Fig. 12 shows the double-pulse test fixture. Its equivalent schematic circuit is shown in Fig. 2(a). In the test, the gate drive voltage V_{gg} of T_1 is switched at 18V/-4V. A coaxial shunt resistor SSDN-414-01 is used to monitor the drain current I_d. A high voltage probe 10076C is used to measure the drain-source voltage V_{ds}. In this section, the analytically derived switching waveforms and switching losses are compared with the experimental data to validate the proposed model.

A. Transient Characteristics at Room Temperature

1) LCSI Condition: Figs. 14(a)–(d) and 15(a)–(d) compare the experimental and analytical derived turn-ON and turn-OFFwaveforms at room temperature for C3M0040120K and MZA65R048M1H, respectively. The experimental data align with the analytically derived switching waveforms. Since the C3M0040120K and MZA65R048M1H have LCSI, the $L_s \times dI_d/dt$ induced negative feedback action is very weak, which causes continuous reduction of V_{ds} at phase 1 of turn-ON transient. In Fig. 14(a)–(d), the phenomenon is captured by the proposed model, which validates that the proposed model can accurately predict V_{ds} for SiC MOSFETs with LCSI.

2) HCSI Condition: The experimental and analytical derived turn-ON and turn-OFF waveforms of C3M0045065D and IMW65R048M1H are compared in Figs. 14(e)–(f) and 15(e)–(f). The comparison shows the analytically derived waveforms agree with the test data.

As shown in Fig. 14(e)–(f), a plateau of V_{ds} is generated in phase 1 of turn-ON waveforms. The C3M0045065D and IMW65R048M1H have a few nanohenries of L_S and HCSI is obtained. With HCSI, the $L_s \times dI_d/dt$ induces a very strong negative feedback action, which induces a constant dI_d/dt to generate the V_{ds} plateau. In Fig. 14(e)–(f), the V_{ds} plateau predicted by the proposed model matches with the test data, which validates that the proposed model can make accurate predictions under the HCSI condition.

The high dI/dt and dV/dt of SiC MOSFETs excite severe switching oscillations, as shown in Figs. 14 and 15. To make the analytical model feasible, simplified equivalent circuits are presented in Fig. 4(c) and (f) are used to model the oscillation. However, since some physical operations like nonlinear capacitances and excess carrier dynamics in N-base are not included, the simulated oscillations still show minor errors.

B. Temperature-Dependent Turn-ON Waveforms

To validate the temperature-dependent model, the turn-ON waveforms the various temperatures are obtained. Fig. 16(a) and (b) compares the analytical and experimental turn-ON waveforms of C3M0040120K when T_{J1} is 90°C and 130°C while $T_{J2} = 30°\text{C}$. Fig. 16(c) compares the analytical and experimental turn-ON waveforms of C3M0045065D when $T_{J1} = 130°\text{C}$ while $T_{J2} = 30°\text{C}$. With the temperature-dependent model of G_m and V_{th} included, the T_{J1} dependence on turn-ON behavior is captured by the proposed model.

Fig. 16(d) compares the analytical and experimental turn-ON waveforms of C3M0040120K when T_{J2} is 130°C while $T_{J1} = 30°\text{C}$. Due to the temperature-dependent model of Q_{rr} and S, the impact of T_{J2} is captured by the proposed model.

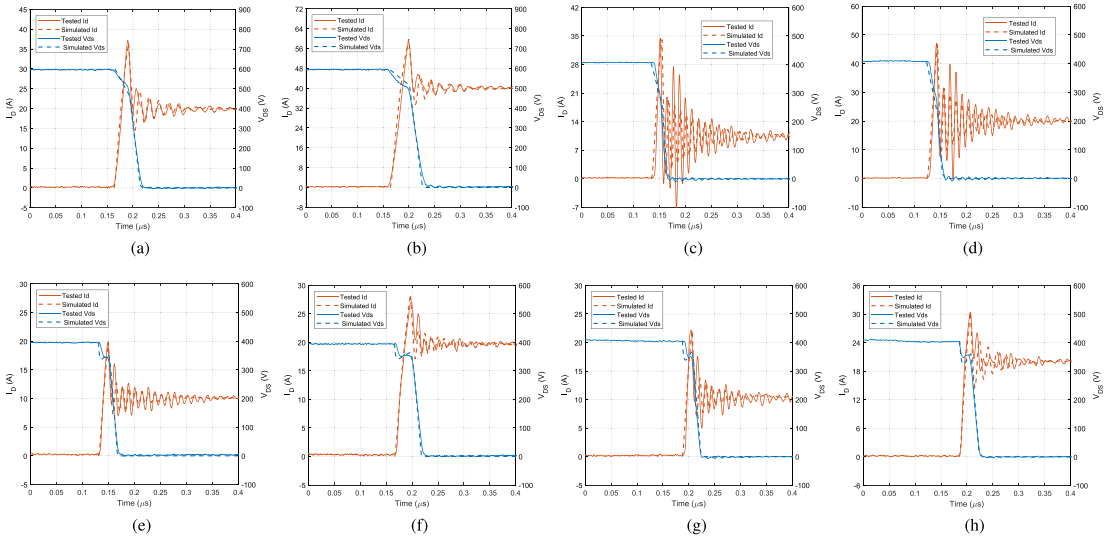

Fig. 14. Experimental and analytical turn-ON waveforms at room temperature with $R_{ge} = 10\,\Omega$: (a) C3M0040120K at 600 V/20 A, (b) C3M0040120K at 600 V/40 A, (c) IMZA65R048M1H at 400 V/10 A, (d) IMZA65R048M1H at 400 V/20 A. (e) C3M0045065D at 400 V/10 A, (f) C3M0045065D at 400 V/20 A, (g) IMW65R048M1H at 400 V/10 A, and (h) IMW65R048M1H at 400 V/20 A.

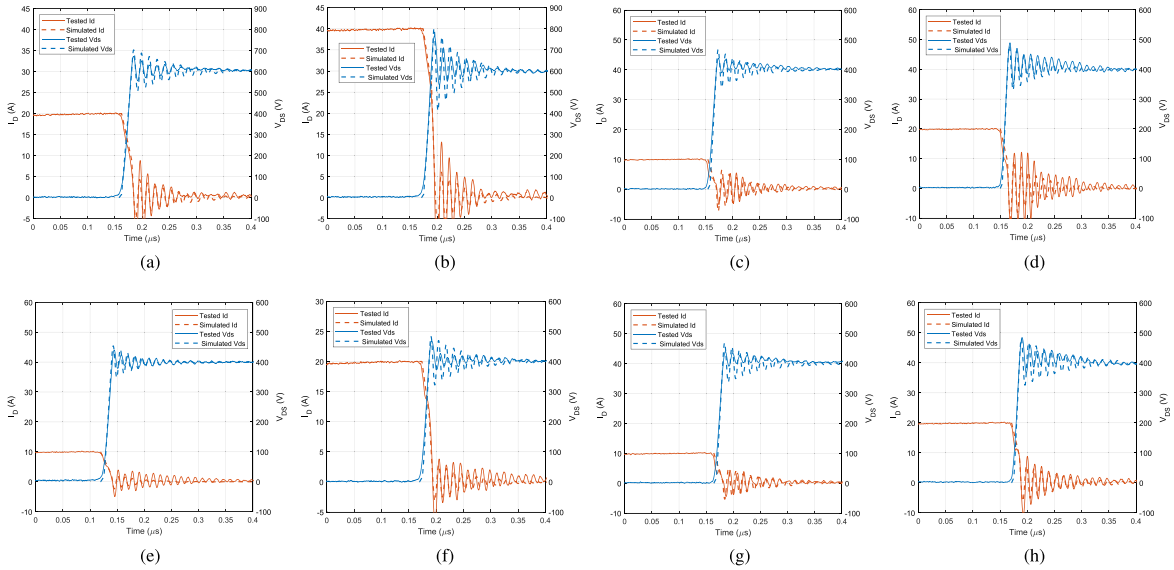

Fig. 15. Experimental and analytical derived turn-OFF waveforms at room temperature with $R_{ge} = 10\,\Omega$: (a) C3M0040120K at 600 V/20 A, (b) C3M0040120K at 600 V/40 A, (c) IMZA65R048M1H at 400 V/10 A, (d) IMZA65R048M1H at 400 V/20 A, (e) C3M0045065D at 400 V/10 A, (f) C3M0045065D at 400 V/20 A, (g) IMW65R048M1H at 400 V/10 A, and (h) IMW65R048M1H at 400 V/20 A.

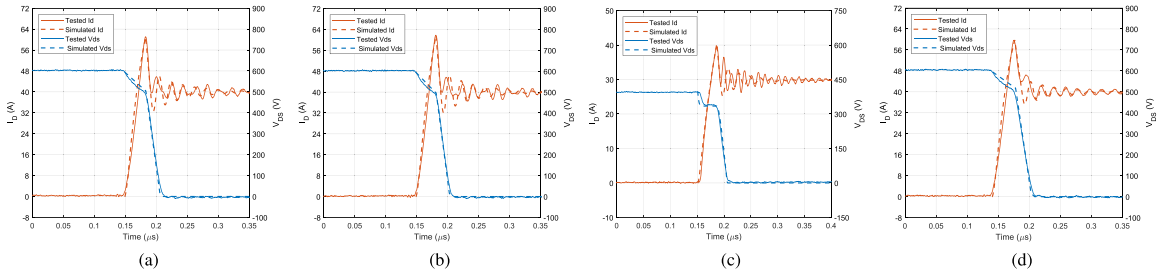

Fig. 16. Experimental and analytical derived turn-ON waveforms: (a) C3M0040120K at 600 V/40 A with $T_{J1} = 90°\text{C}$ and $T_{J2} = 30°\text{C}$, (b) C3M0040120K at 600 V/40 A with $T_{J1} = 130°\text{C}$ and $T_{J2} = 30°\text{C}$, (c) C3M0045065D at 400 V/30 A with $T_{J1} = 130°\text{C}$ and $T_{J2} = 30°\text{C}$, and (d) C3M0040120K at 600 V/40 A with $T_{J2} = 130°\text{C}$ and $T_{J1} = 30°\text{C}$.

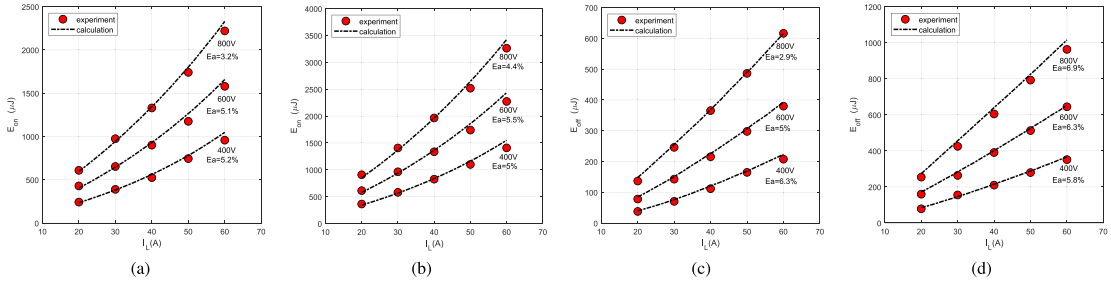

Fig. 17. Comparison of experimental and analytically calculated switching losses of C3M0040120K at room temperature using 400, 600, and 800 V. (a) Turn-ON losses using $R_{ge} = 10\,\Omega$. (b) Turn-ON losses using $R_{ge} = 20\,\Omega$. (c) Turn-OFF losses using $R_{ge} = 10\,\Omega$. (d) Turn-OFF losses using $R_{ge} = 20\,\Omega$.

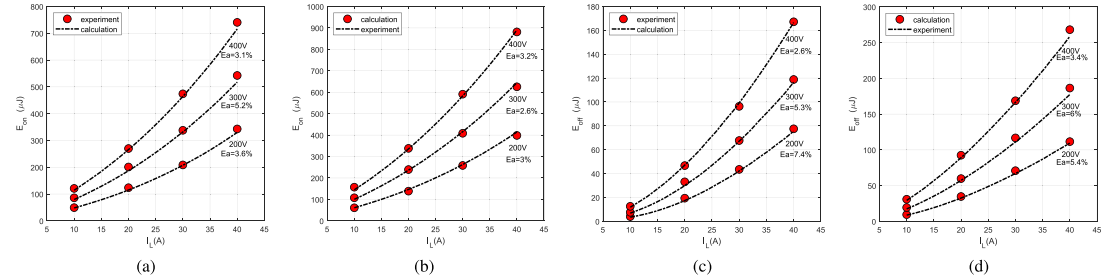

Fig. 18. Comparison of experimental and analytically calculated switching losses of C3M0045065D at room temperature using 200, 300, and 400 V. (a) Turn-ON losses using $R_{ge} = 10\,\Omega$. (b) Turn-ON losses using $R_{ge} = 20\,\Omega$. (c) Turn-OFF losses using $R_{ge} = 10\,\Omega$. (d) Turn-OFF losses using $R_{ge} = 20\,\Omega$.

C. Comparison on Turn-ON and Turn-OFF Losses

The experimental and analytically derived turn-ON losses E_{on} and turn-OFFlosses E_{off} are obtained by the time integration on $V_{ds} \times I_d$ at switching transients. The error E of E_{on} and E_{off} is obtained using the following:

$$E = \frac{|\text{Proposed model} - \text{Experimental data}|}{\text{Experimental data}}. \quad (96)$$

Fig. 17 shows the comparison of experimental and analytically derived turn-ON and turn-OFFlosses of C3M0040120K using various V_{dc} (400, 600, and 800 V), I_L (20, 30, 40, 50, and 60 A) and R_{ge} (10 Ω and 20 Ω). Under each test condition, the average error $E_a = \overline{E}$ is calculated. The average error E_a of the turn-ON losses is within 5.5%. For the turn-OFF losses, the E_a is below 6.9%. In Fig. 18, the turn-ON and turn-OFFlosses of C3M0045065D using various V_{dc} (200, 300, and 400 V) and I_L (10, 20, 30, and 40 A) and R_{ge} (10 Ω and 20 Ω) are obtained analytically and experimentally. The average error E_a is below 5.2% for turn-ON losses and 7.4% for turn-OFFlosses. The switching loss comparison presented in Figs. 17 and 18 demonstrate that the proposed model accurately predict turn-OFF and turn-ON losses of the SiC MOSFET under HCSI and LSCI conditions.

Since the turn-ON behavior depends on junction temperature T_{J1} and T_{J2}. The turn-ON losses E_{on} depends on T_{J1} and T_{J2}. Fig. 19 compares the experimental and analytically calculated E_{on} of C3M0040120K at 600 V/40 A using various T_{J1} and T_{J2}. The average error of the T_{J1} and T_{J2} dependent E_{on} are 0.6% and 1.5% and the proposed model accurately estimates the temperature-dependent E_{on}.

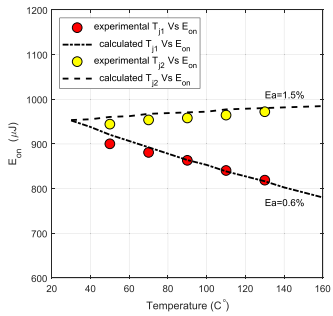

Fig. 19. Comparison of experimental and analytically calculated T_{J1} dependent E_{on} and T_{J2} dependent E_{on} of C3M0040120K at 600 V/40 A.

VIII. Conclusion

In this article, an analytical model is proposed for SiC MOSFET. During the switching transient, the $C_{gd} \times dV_{ds}/dt$ and $L_s \times dI_d/dt$ induced negative feedback mechanisms greatly slow down the switching process. Due to the bipolar nature of the SiC MOSFET body diode, the excess charge extraction of the high-side body diode greatly affects the turn-ON behavior of the MOSFETs. The voltage-dependent stray capacitances and the dynamic transfer characteristics are also critical for the switching characteristics. These pivotal characteristics are included in the model to derive a complete analytical model.

The junction temperatures T_{J1} of low-side MOSFET and T_{J2} of high-side MOSFET have significant impact on the turn-ON behavior. The temperature-dependent models of the transconductance, V_{th}, Qrr, and S are thereby proposed to describe the temperature dependence. In the end, comparison of the analytically derived

and experimental data show that the proposed model can make accurate predictions on the temperature-dependent switching behavior and switching losses of SiC MOSFET.

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