A Multilevel Self-Driving Gate Driver of SiC MOSFET for Crosstalk Suppression Considering Common-Source Inductance

Kaiyuan Hu, Ming Yang, *Senior Member, IEEE*, and Xinmei Zhang

***Abstract*—Compared with conventional silicon-based devices, silicon carbide MOSFET exhibits superior characteristics. However, the high dv/dt caused by high switching speed makes it more susceptible to crosstalk spikes caused by Miller capacitance and common-source inductance, increasing the risk of false-triggering of power device. The mathematical models of most existing methods only consider the Miller capacitance, and adopt the negative turn-OFF voltage method, which increases the negative gate–source voltage stress of the device and shortens service life. This article proposes a mathematical model of crosstalk voltage that takes into account both Miller capacitance and common-source inductance, and a multilevel self-driving gate driver is introduced to mitigate positive and negative crosstalk voltages. This approach employs resistor–capacitor–diode and resistor–MOSFET configurations to establish the multilevel negative turn-OFF voltage and low-impedance branch to suppress positive and negative crosstalk voltages. Incorporating an extra resistor forms a self-driving path for multilevel turn-OFF voltage, mitigating the negative gate–source voltage stress. The circuit comprises several passive components that can be integrated into the driver IC, eliminating the need for additional negative voltage sources and control signals. The effectiveness of the proposed method is demonstrated through a double-pulse test based on SCT3022AL.**

***Index Terms*—Crosstalk suppression, gate driver, self-driving, silicon carbide (SiC).**

I. Introduction

WIDE bandgap devices, exemplified by silicon carbide (SiC), demonstrate superior performance to conventional silicon (Si)-based devices in several aspects, including electron mobility, bandgap width, breakdown field strength, maximum junction temperature, and thermal conductivity [1], [2], [3], [4], [5], [6], [7], [8]. The exceptionally rapid switching speed substantially diminishes switching loss, shorten dead time, and facilitates extensive deployment in high-frequency, high-voltage, and high-power density applications [9], [10], [11], [12].

Nevertheless, the high-speed switching characteristic, while reducing switching loss, also engender several detrimental effects. Prominent among these is the issue of crosstalk in a phase-leg configuration. During rapid turn-ON and turn-OFF transients, high dv/dt and di/dt are coupled to the gate–source of the device through parasitic capacitances and inductances, represented by Miller capacitance and common-source inductance, respectively, as shown in Fig. 1. Excessive positive voltage peak may cause the gate–source voltage to surpass the threshold voltage, elevating the likelihood of device false-triggering and consequent additional switching loss, while excessive negative

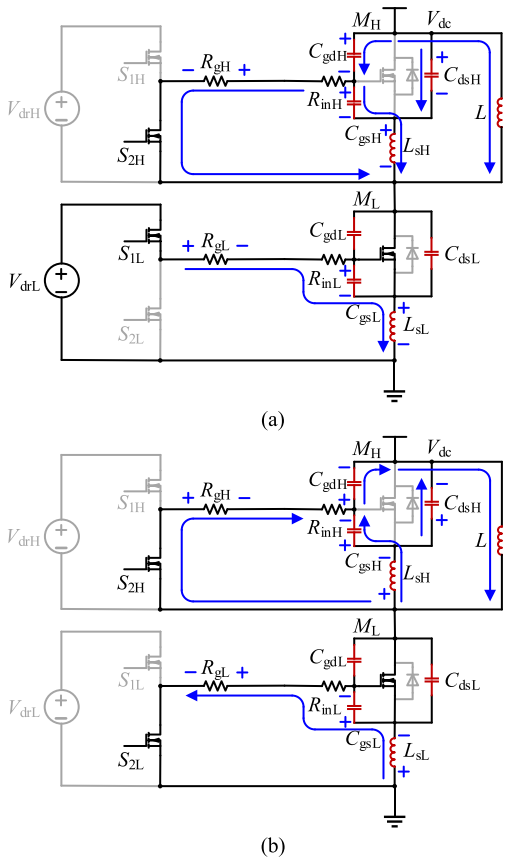

Fig. 1. Mechanism causing crosstalk interference. (a) Turn-ON transient of M_L. (b) Turn-OFF transient of M_L.

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crosstalk voltage can cause the gate–source voltage to below the minimum negative allowable voltage, potentially leading to device damage. The lower threshold voltage and higher minimum negative allowable voltage of SiC MOSFET exacerbate the issue of crosstalk.

Existing crosstalk suppression methods primarily include reducing dv/dt and di/dt, incorporating additional low-impedance path for crosstalk current and utilizing negative turn-OFF voltage. The initial approach is often realized by increasing the gate resistance to decelerate the switching process. This method can fundamentally suppress crosstalk, but unavoidably increase switching loss, and the larger gate resistance may increase the crosstalk voltage in some cases. Although some active gate drive circuits currently mitigate crosstalk while minimizing switching loss, increase cost, volume and complexity [13].

The subsequent method commonly employs additional a large parallel gate–source capacitor or clamping circuit to provide a low-impedance path for the crosstalk current. To avoid extra loss due to reduced switching speed, the additional capacitor is connected in series with transistor [14], [15] or MOSFET [16], and the operational spectrum of the auxiliary capacitor is controlled through the additional switching device. Nevertheless, most methods necessitate extra control signals to regulate the working state, which increases control complexity. Zhang et al. [17] propose an auxiliary circuit composed of additional transistors and a diode to actively modulate the gate voltage and loop impedance during different switching transients. Li et al. [18] propose an auxiliary gate driver based on a negative voltage transistor, utilizing the voltage drop across the gate resistor caused by crosstalk current to control the operating time of the transistor, eliminating the impact of the additional capacitor on the switching transient without necessitating extra control signals.

The tertiary approach customarily achieves negative turn-OFF voltage by adding an additional negative power supply [19] or RCD level-shifting circuit [20]. Employing an additional negative power supply is the most straightforward method, but it lacks flexibility in adjusting the negative voltage value and increases cost and volume. Although negative turn-OFF voltage permits the establishment of a safe negative voltage value for the turn-OFF voltage, thereby preventing the positive crosstalk spike from attaining the threshold voltage, it significantly elevates the likelihood of negative gate overvoltage breakdown caused by the negative crosstalk spike. Therefore, negative turn-OFF voltage is often combined with negative crosstalk suppression circuit. [16] adopts RCD level-shifting circuit to generate negative gate–source voltage and a passive triggered transistor with a series-connected capacitor to suppress the negative voltage spike. On the other hand, due to the thin gate oxide layer of SiC MOSFET, excessive negative voltage stress can shorten the lifespan of the gate oxide and cause threshold voltage drift [21], thereby diminishing device reliability. The current solution mainly uses multilevel driving, where a short-duration large negative gate–source voltage is applied to suppress positive crosstalk spike, followed by clamping the gate voltage to 0 V or a smaller negative voltage using auxiliary circuits to alleviate negative voltage stress and provide negative crosstalk protection. However, this requires additional driver circuits and control signals, greatly increasing cost and complexity. Zhang et al. [22] propose a multilevel gate driver based on magnetic coupling to ensure that the gate voltage operates within a safe range during both positive and negative crosstalk spikes.

Different from the above three methods, Shao et al. [23] proposed a negative feedback active gate drive circuit by introducing an auxiliary PMOSFET to construct a negative feedback control mechanism. Through the negative feedback mechanism, the proposed driving circuit can automatically attenuate the positive and negative crosstalk voltage spikes.

However, the majority of existing SiC MOSFET crosstalk mitigation techniques primarily focus on the crosstalk caused by the Miller capacitance, neglecting the impact of the common-source inductance. A definitive mathematical model elucidating the influence of both the common source inductance and the Miller capacitance on the positive and negative crosstalk spikes is lacking, and the interaction between the low impedance loop and the common-source inductance remains undetermined. Consequently, this paper introduces a comprehensive mathematical model for crosstalk voltage that encompasses the effects of both the Miller capacitance and the common source inductance. Based on this model, a multilevel self-driving gate driver for SiC MOSFET is proposed to suppress both positive and negative crosstalk voltages. The driving circuit establishes negative gate–source voltage through an RCD divider, and collaborates with an R-NMOS-PMOS low-impedance branch to mitigate positive crosstalk voltage. Moreover, to alleviate negative voltage stress, the RC driving circuit leverages the gate–source parasitic capacitance of the PMOS, adjusting the resistor value to set the self-driving time and clamp the gate–source voltage at a specified level. As per the proposed mathematical model, the low-impedance circuit determines the appropriate impedance value necessary for crosstalk voltage suppression. This approach eliminates the requirement for additional control signals and power supplies, rendering it amenable to integration into drive IC.

The rest of this article is organized as follows. Section II introduces the structure and operation modes of the proposed circuit. Section III analyzes the switching transient process, elucidating methodologies for parameter design. Section IV presents a series of experimental results to validate the effectiveness of the proposed method. Finally, Section V concludes this article.

II. Proposed Multilevel Self-Driving Gate Driver Topology and Operation Modes

A. Proposed Multilevel Self-Driving Gate Driver Topology

Crosstalk refers to the positive and negative voltage spikes that occur at the gate–source of the synchronous freewheeling device during switching transient of the control device. During the switching process, the drain–source voltage of the synchronous freewheeling device rises and falls rapidly, leading to the charging and discharging of the parasitic capacitor. As a result, positive and negative voltage spikes are induced across the gate resistance and common-source inductance. Once the

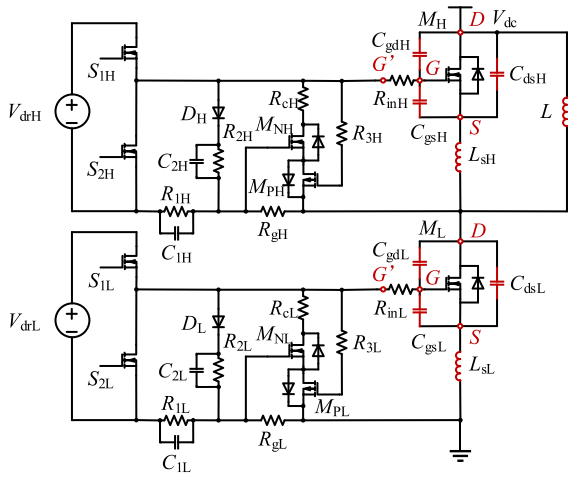

Fig. 2. Topology of the proposed multilevel self-driving gate driver.

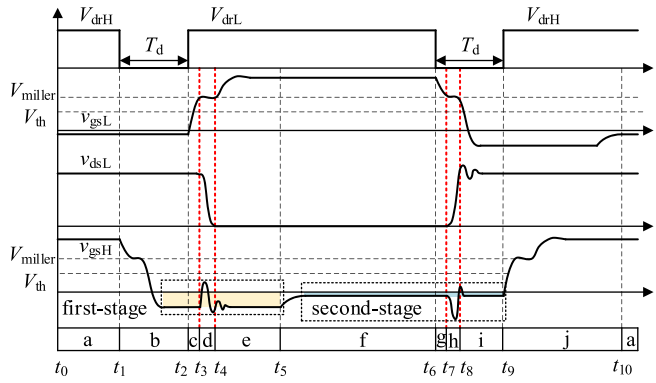

Fig. 3. Operation scheme of the proposed multilevel self-driving gate driver.

positive crosstalk voltage spike exceeds the threshold voltage, the device may be turned on by mistake, thereby elevating the switching loss. Conversely, if the negative crosstalk voltage spike falls below the minimum negative allowable gate voltage, device damage may ensue.

Fig. 1 shows a SiC MOSFET double-pulse test circuit based on a conventional gate driver configuration. M_L is the control device, while M_H is the synchronous freewheeling device. R_{in}, C_{gd}, C_{gs}, C_{ds} and L_s are the gate input resistance, Miller capacitance, gate–source capacitance, drain–source capacitance and common-source inductance of the device, respectively. Additionally, R_g and L are the gate resistance and load inductance.

This article introduces a multilevel self-driven grid drive circuit designed to mitigate crosstalk, as shown in Fig. 2. Since the internal parasitic inductance of the device is very small, in order to simplify the analysis, this article ignores the influence of the internal parasitic inductance and only considers the gate input resistance R_{in} and the external common source parasitic inductance L_S. The G', D, and S terminals set in Fig. 2 are the gate, drain, and source voltage measurement points of the actual MOSFET $M_{H/L}$ in the experiment, respectively. And the theoretical analysis part refers to the actual gate G, drain D and source S of SiC MOSFET. The diodes in parallel to the MOSFETs M_N and M_P are the body diodes of the MOSFETs. The first-stage turn-OFF voltage is generated by the voltage divider composed of R_1, C_1, R_2, C_2, and D, and the NMOSFET M_N turn-ON is controlled by the voltage drop generated by the positive crosstalk current on R_g. The R_c–M_N–D_{MP} low-impedance path composed of R_c, NMOSFET M_N and the body diode D_{MP} of PMOSFET M_P collectively suppresses the positive crosstalk voltage. Furthermore, an RC self-driving circuit composed of R_3 and the gate–source parasitic capacitance C_{gsP} of PMOSFET M_P controls the modify time of the turn-OFF voltage by adjusting the resistance value of R_3. By selecting an appropriate PMOSFET M_P, the second-stage turn-OFF voltage is set near the threshold voltage V_{thP} of PMOSFET M_P. Negative crosstalk voltage is counteracted by a R_c–D_{MN}–M_P low-impedance path that includes R_c, the body diode D_{MN} of NMOSFET M_N and PMOSFET M_P. Select a suitable R_c resistance value to offset the opposite effect of L_s.

B. Operation Modes of the Proposed Gate Driver

The operation principle of the proposed drive circuit can be divided into ten modes, the schematic waveforms within a single switching cycle are shown in Fig. 3. V_{drH} and V_{drL} are the driving signals of the synchronous freewheeling device and the control device, respectively. T_d represents the dead time. V_{dsL} and V_{gsL} are the drain–source and gate–source voltage waveforms of the control device, respectively. V_{gsH} is the gate–source voltage waveform of the synchronous freewheeling device. Since each duty cycle is extremely short, the negative turn-OFF voltage of each stage is assumed to be constant. The equivalent circuit in each mode is demonstrated in Fig. 4. The operation modes of the device are as follows.

Mode a (t_{10}–t_0–t_1): The equivalent circuit is shown in Fig. 4(a). The synchronous freewheeling MOSFET M_H is in conducting, diode D_H is forward biased. The load inductance current flows reversely through M_H, the crosstalk suppression branch is cut off. Meanwhile, both the control MOSFET M_L and diode D_L remain off, and the R_{cL}–D_{MNL}–M_{PL} low-impedance branch is in the preconduction state and clamps the v_{gsL} at the second-stage turn-OFF voltage.

Mode b (t_1–t_2): The equivalent circuit is shown in Fig. 4(b). At t_1, the driving voltage V_{drH} becomes lower, the synchronous freewheeling MOSFET M_H is turned OFF, diode D_H is reverse biased, capacitor C_{2H} discharges through R_{2H}, and C_{1H} functions as a negative voltage source to accelerate the turn-OFF process of M_H, so that v_{gsH} stabilizes at the first-stage turn-OFF voltage, and the gate–source parasitic capacitance C_{gsPH} of PMOSFET M_{PH} begins to discharge continuously through the RC self-driving branch. The load inductance current cannot pass through the control MOSFET M_L, and the body diode of M_H provides a flow path. The drain–source voltages of the two MOSFETs remain unaltered, signifying that M_L experiences no crosstalk interference.

Mode c (t_2–t_3): The equivalent circuit is shown in Fig. 4(c). At t_2, the driving voltage V_{drL} becomes higher, turning ON M_L while M_H remains OFF, diode D_L is forward biased, and

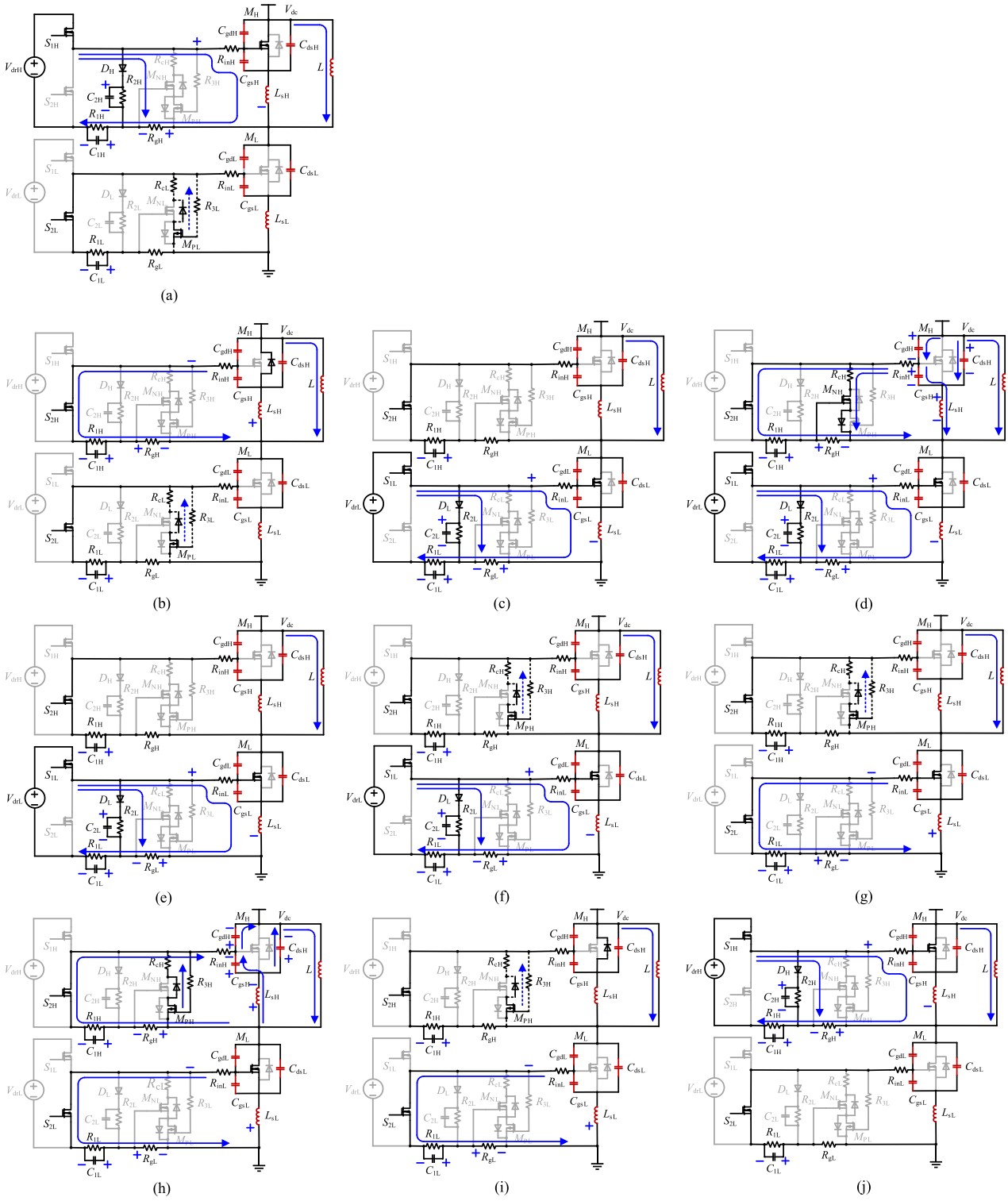

Fig. 4. Equivalent circuit in each mode. (a) Mode a (t_{10}-t_0-t_1). (b) Mode b (t_1-t_2). (c) Mode c (t_2-t_3). (d) Mode d (t_3-t_4). (e) Mode e (t_4-t_5). (f) Mode f (t_5-t_6). (g) Mode g (t_6-t_7). (h) Mode h (t_7-t_8). (i) Mode i (t_8-t_9). (j) Mode j (t_9-t_{10}).

capacitor C_{1L}, C_{2L}, and C_{gsL} are charged, respectively. During this mode, neither of the crosstalk suppression branches are operational.

Mode d (t_3–t_4): The equivalent circuit is shown in Fig. 4(d). At t_3, v_{gsL} reaches the Miller platform, causing v_{dsL} to rapidly decrease from the bus voltage to zero, and v_{dsH} to rise from zero to the bus voltage, accompanied by voltage overshoot and oscillation. The load inductor current begins to flow through L and M_L, and rises rapidly. The high dv/dt couples with the C_{gdH} of M_H to generate a positive crosstalk current that flows

through R_{gH}, and the voltage drop across R_{gH} serves as the control signal of NMOSFET M_{NH}, providing a R_{cH}–M_{NH}–D_{MPH} low-impedance branch to mitigate the positive voltage spike on v_{gsH}, which is subtracted from the positive voltage drop on L_{sH} to obtain the crosstalk voltage spike at the gate–source. Therefore, the voltage spike generated by di/dt coupling with L_{sH} is equivalent to a negative voltage spike at the gate–source.

Mode e (t_4–t_5): The equivalent circuit is shown in Fig. 4(e). Similar to mode c, the control MOSFET M_L conduction, diode D_L forward bias. the synchronous freewheeling MOSFET M_H remains OFF, and the first-stage turn-OFF voltage after positive crosstalk remains nearly constant, and the gate–source parasitic capacitance C_{gsPH} of PMOSFET M_{PH} continues to discharge through the RC self-driving branch.

Mode f (t_5–t_6): The equivalent circuit is shown in Fig. 4(f). The control MOSFET M_L conduction, diode D_L is forward biased, capacitor C_{1H} continuously discharges the gate–source parasitic capacitance C_{gsPH} of PMOSFET M_{PH} through the RC self-driving circuit, reducing the gate–source voltage of PMOSFET M_{PH} to the threshold voltage. This enables the R_{cH}–D_{MNH}–M_{PH} low-impedance branch to conduct. The charges stored in C_{gsH} and C_{1H} are quickly consumed through the branch resistance, causing the gate–source voltage of PMOSFET M_{PH} and SiC MOSFET to rise to near the threshold voltage V_{thP} of PMOSFET M_P. And PMOSFET M_{PH} is turned OFF, maintains the preconduction state, and clamps the gate–source voltage of both near the threshold voltage V_{thP} of PMOSFET M_P, i.e., the second-stage turn-OFF voltage. The relationship between the duration of the discharge process t_{sd}, the turn-OFF time t_{off} and the dead time T_d is

$$t_{off} < T_d < t_{sd}. \tag{1}$$

Mode g (t_6–t_7): The equivalent circuit is shown in Fig. 4(g). At t_6, the driving voltage V_{drL} becomes lower, and the control MOSFET M_L starts to turn OFF, similar to the previously described turn-OFF process of M_H. The R_{cH}–D_{MNH}–M_{PH} low-impedance branch remains the preconduction state and the v_{gsH} is clamped at the second-stage turn-OFF voltage.

Mode h (t_7–t_8): The equivalent circuit is shown in Fig. 4(h). At t_7, v_{gsL} reached the Miller platform, and v_{dsL} rises rapidly while v_{dsH} decreased rapidly. The load inductor current begins to flow through the body diode of M_H and L, rising quickly. High dv/dt coupled with C_{gdH} of the synchronous freewheeling MOSFET M_H generates negative crosstalk current, which flows through R_{gH}, and the resulting negative voltage spike. The negative voltage spike across R_{gH} and the negative voltage v_{C1H} across C_{1H} act together on both ends of the $R_{3H}C_{gsPH}$ branch, further reducing the gate–source voltage v_{gsPH} of PMOSFET M_{PH}, which near the threshold voltage. Therefore, the gate–source voltage of PMOSFET M_{PH} is significantly lower than the threshold voltage V_{thP}, and PMOSFET M_{PH} is turned ON. Then the R_{cH}–D_{MNH}–M_{PH} low-impedance branch is turned on, providing a low-impedance path for the negative crosstalk current. The high di/dt coupled with L_{sH} leads to a negative voltage spike, which is equivalent to a positive voltage spike at the gate–source and opposites to the effect of C_{gdH} on crosstalk.

Mode i (t_8–t_9): The equivalent circuit is shown in Fig. 4(i). Similar to mode g, the control MOSFET M_L is turned OFF and diode D_L is reverse biased. The synchronous freewheeling MOSFET M_H remains OFF, and the R_{cH}–D_{MNH}–M_{PH} low-impedance branch still maintains the pre-conduction state after negative crosstalk, with the second-stage turn-OFF voltage remaining nearly unchanged.

Mode j (t_9–t_{10}): The equivalent circuit is shown in Fig. 4(j). At t_9, the driving voltage V_{drH} becomes high, and the synchronous freewheeling MOSFET M_H turn-ON process mirrors that of M_L previously. With the control MOSFET M_L OFF, the load inductor current cannot pass through the M_L, and M_H provides a flow path. The v_{ds} of the two MOSFETs does not change, and no crosstalk occurs in M_L.

According to the above analysis, the crosstalk problem is primarily affected by both C_{gd} and L_s, and the two effects are completely opposite. The proposed topology can generate a stable two-stage negative turn-OFF voltage, using a low-impedance branch to mitigate the impact of C_{gd} on the crosstalk voltage. Additionally, selecting an appropriate clamping resistor R_c can utilize the crosstalk current generated by C_{gd} to offset partial impact of L_s.

III. Transient Analysis and Parameters Design of Proposed Gate Driver

A. Analysis of Turn-Off Transient

When the synchronous freewheeling MOSFET M_H is turned OFF, M_L remains OFF, the current path of the inductor switches from M_H to its body diode. C_1 acts as a negative power source to accelerate the turn-OFF, diode D is reverse biased, and the crosstalk suppression branch is nonoperational. The equivalent circuit is shown in Fig. 5(a).

According to Kirchhoff's law, the relationship between voltage and current can be obtained as follows:

$$\begin{cases} v_1 = (R_g + R_{in})\left(\frac{v_1}{R_1} + C_1\frac{dv_1}{dt}\right) + v_{gs} \\ \frac{v_1}{R_1} + C_1\frac{dv_1}{dt} + C_{gs}\frac{dv_{gs}}{dt} = 0. \end{cases} \tag{2}$$

The initial voltages of C_{gs}, and C_1 are defined as $v_{gs\_off}(0\_)$, and $v_{1\_off}(0\_)$, respectively. According to the Laplace transform of (2), v_{gs} can be obtained as follows:

$$v_{gs}(s) = \frac{\frac{(R_{in}+R_g)G_{i\_off}+1}{(R_{in}+R_g)C_{gs}s+1}C_{gs}v_{gs\_off}(0\_) + C_1 v_{1\_off}(0\_)}{G_{i\_off}} \tag{3}$$

$$G_{i\_off} = (R_{in}+R_g)C_1C_{gs}s^2 + \left(\frac{R_{in}+R_g+R_1}{R_1}C_{gs} + C_1\right)s + \frac{1}{R_1}. \tag{4}$$

The time domain expression of v_{gs} obtained by inverse Laplace transformation is

$$v_{gs}(t) = \frac{(A_{1f}+A_{2f}T_{1f})e^{-\frac{t}{T_{1f}}} - (A_{1f}+A_{2f}T_{2f})e^{-\frac{t}{T_{2f}}}}{T_{1f}-T_{2f}} \tag{5}$$

where $A_{1f} = R_1C_1[v_{1\_off}(0\_) - v_{gs\_off}(0\_)]$, $A_{2f} = v_{gs\_off}(0\_)$, $T_{1f} = [T_{3f} + (T_{3f}^2 - 4T_{4f}^2)^{1/2}]/2$, $T_{2f} = [T_{3f} - (T_{3f}^2 -$

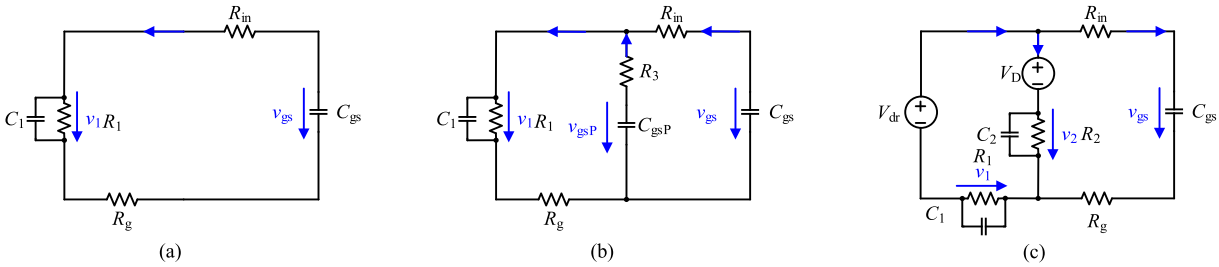

Fig. 5. Equivalent circuits of proposed gate driver. (a) Turn-OFF transient. (b) Self-driving process. (c) Turn-ON transient.

$4T_{4f}^2)^{1/2}]/2$, $T_{3f} = R_1(C_{gs} + C_1) + (R_{in} + R_g)C_{gs}$, $T_{4f} = [(R_{in} + R_g)R_1C_1C_{gs}]^{1/2}$.

According to (5), the final values of v_{gs} and v_1 tend to zero. Therefore, the parameter design principle that the time constant of the R_1-C_1 branch should be large enough to maintain a stable negative voltage level over a control cycle.

B. Analysis of Self-Driving Process

In order to reduce the negative voltage stress without adding extra control signals and voltage sources, a self-driving circuit is proposed, and the equivalent circuit is shown in Fig. 5(b). After the device is turned OFF, capacitor C_1 continuously discharges the gate–source capacitor of PMOSET M_P through the loop resistance until the gate–source voltage of PMOSFET M_P drops below the threshold voltage V_{thP}. PMOSFET M_P then turns on and clamps the turn-OFF voltage at V_{thP} to achieve multilevel turn-OFF.

According to Kirchhoff law, the relationship between voltage and current can be obtained as follows:

$$\begin{cases} v_1 = v_{gs} + R_g\left(C_{gs\mathbf{P}}\frac{dv_{gs\mathbf{P}}}{dt} + C_{gs}\frac{dv_{gs}}{dt}\right) + R_{\mathbf{in}}C_{gs}\frac{dv_{gs}}{dt} \\ v_{gs} + R_{\mathbf{in}}C_{gs}\frac{dv_{gs}}{dt} = v_{gs\mathbf{P}} + R_3C_{gs\mathbf{P}}\frac{dv_{gs\mathbf{P}}}{dt}. \end{cases} \tag{6}$$

The gate–source voltage v_{gsP} of PMOSFET M_P can be calculated as follows:

$$v_{gsP}(t) = \frac{A_{\mathbf{sd1}}e^{-\frac{t}{T_{\mathbf{sd1}}}} + A_{\mathbf{sd2}}e^{-\frac{t}{T_{\mathbf{sd2}}}}}{B_{\mathbf{sd2}}} \tag{7}$$

where $A_{sd1} = B_{sd1}R_{in}v_{1\_off}(0\_) - v_{gsP\_off}(0\_)C_{gsP}{}^2R_3(1 + R_g)(R_g + R_{in} + R_gR_{in}) + C_{gsP}R_gR_{in}(B_{sd1}v_{gsP\_off}(0\_) - v_{1\_off}(0\_)) + C_{gsP}R_3(B_{sd1}R_gv_{gsP\_off}(0\_) + B_{sd1}R_{in}v_{gsP\_off}(0\_) - 2R_gv_{1\_off}(0\_) - R_{in}v_{1\_off}(0\_)) + C_{gs}\{R_{in} + v_{gsP\_off}(0\_)C_{gsP}R_{in}{}^2(R_g + R_3) + C_{gsP}R_g{}^2(R_3 + R_{in})(v_{gsP\_off}(0\_) - 2v_{gs\_off}(0\_)) + R_gR_{in}[v_{1\_off}(0\_) + 2C_{gsP}R_3(v_{gsP\_off}(0\_) - v_{gs\_off}(0\_))]\}$, $A_{sd2} = B_{sd1}R_{in}v_{1\_off}(0\_) + v_{gsP\_off}(0\_)C_{gsP}{}^2R_3(1 + R_g)(R_g + R_{in} + R_gR_{in}) + C_{gsP}R_gR_{in}(B_{sd1}v_{gsP\_off}(0\_) + v_{1\_off}(0\_)) + C_{gsP}R_3(B_{sd1}R_gv_{gsP\_off}(0\_) + B_{sd1}R_{in}v_{gsP\_off}(0\_) + 2R_gv_{1\_off}(0\_) + v_{1\_off}(0\_)) - C_{gs}\{v_{gsP\_off}(0\_)C_{gsP}R_{in}{}^2(R_g + R_3) + C_{gsP}R_g{}^2R_3(v_{gsP\_off}(0\_) - 2v_{gs\_off}(0\_)) + R_{in}[R_g(v_{1\_off}(0\_) + 2C_{gsP}R_3v_{gsP\_off}(0\_)) - 2C_{gsP}R_3v_{gs\_off}(0\_)) + C_{gsP}R_g{}^2(v_{gsP\_off}(0\_) - 2v_{gs\_off}(0\_)) - 1]\}$, $T_{sd1} = 2C_{gs}C_{gsP}(1 + R_3)(R_g + R_{in})/[C_{gs}R_g + C_{gsP}(R_g + R_3) + C_{gs}R_{in} + B_{sd1}]$, $T_{sd2} = 2C_{gs}C_{gsP}(1 + R_3)(R_g + R_{in})/[C_{gs}R_g + C_{gsP}(R_g + R_3) + C_{gs}R_{in} - B_{sd1}]$, $B_{sd1} = \{C_{gsP}{}^2(R_g + R_3)^2 + C_{gs}{}^2(R_g + R_{in})^2 - 2C_{gs}C_{gsP}[R_g(R_{in} - R_g) + R_3(R_g + R_{in})]\}^{1/2}$, $B_{sd2} = 2C_{gsP}(1 + R_3)(R_g + R_{in})\{[C_{gsP}(R_g + R_3) + C_{gs}(R_g + R_{in})]^2 - 4C_{gs}C_{gsP}(1 + R_3)(R_g + R_{in})\}^{1/2}$. Therefore, the self-driving time t_{sd} can be approximated as follows:

$$t_{sd} \approx T_{\mathbf{sd2}}\ln\frac{A_{\mathbf{sd2}}}{V_{thP}B_{\mathbf{sd2}}}. \tag{8}$$

According to (1) and (8), while leaving a time margin for positive crosstalk, select appropriate R_3 to set t_{sd}.

C. Analysis of Turn-on Transient

The control MOSFET M_L remains in OFF-state when the synchronous freewheeling MOSFET M_H is turned ON, M_H can be equivalent to the capacitor C_{gs}. Diode D is forward biased, which is regarded as a voltage source V_D. The crosstalk suppression branch is nonoperational, and the gate inductance is ignored. The equivalent circuit is shown in Fig. 5(c).

According to Kirchhoff's law, the relationship between voltage and current can be obtained as follows:

$$\begin{cases} \frac{v_1}{R_1} + C_1\frac{dv_1}{dt} + \frac{v_2}{R_2} + C_2\frac{dv_2}{dt} + C_{gs}\frac{dv_{gs}}{dt} = 0 \\ V_{dr} + v_1 = V_D + v_2 \\ V_D + v_2 = v_{gs} + (R_{in} + R_g)C_{gs}\frac{dv_{gs}}{dt}. \end{cases} \tag{9}$$

Similar to the previous turn-OFF transient analysis, v_{gs} can be expressed as follows:

$$v_{gs}(t) = \frac{(A_{1r} + A_{2\mathbf{r}}T_{\mathbf{1r}})e^{-\frac{t}{T_{\mathbf{1r}}}} - (A_{\mathbf{1r}} + A_{\mathbf{2r}}T_{\mathbf{2r}})e^{-\frac{t}{T_{\mathbf{2r}}}}}{(R_1 + R_2)(T_{\mathbf{1r}} - T_{\mathbf{2r}})} + \frac{R_1V_D + R_2V_{dr}}{R_1 + R_2} \tag{10}$$

where $A_{1r} = R_1R_2\{C_1V_{dr} + C_2[V_D + v_{2\_on}(0\_) - V_{thP}]\}$, $A_{2r} = R_1(V_{thP} - V_D) + R_2(V_{thP} - V_{dr})$, $T_{1r} = [T_{3r} + (T_{3r}{}^2 - 4T_{4r}{}^2)^{1/2}]/2$, $T_{2r} = [T_{3r} - (T_{3r}{}^2 - 4T_{4r}{}^2)^{1/2}]/2$, $T_{3r} = R_1R_2(C_{gs} + C_1 + C_2)/(R_1 + R_2) + (R_{in} + R_g)C_{gs}$, $T_{4r} = [(R_{in} + R_g)(C_1 + C_2)R_1R_2C_{gs}/(R_1 + R_2)]^{1/2}$.

According to (10), the final values of C_{gs}, C_1, and C_2 terminal voltages in ON-state are approximately calculated separately as follows:

$$v_{gs\_off}(0\_) = v_{gsP\_off}(0\_) = v_{gs\_on}(DT_s) \approx \frac{R_1V_D + R_2V_{dr}}{R_1 + R_2} \tag{11}$$

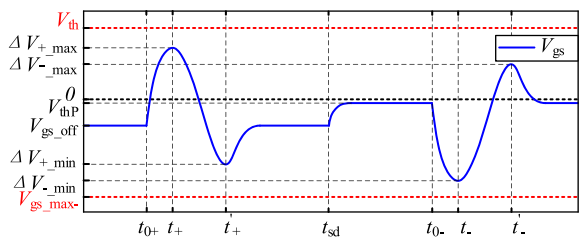

Fig. 6. Crosstalk spikes of gate–source voltage during switching transients.

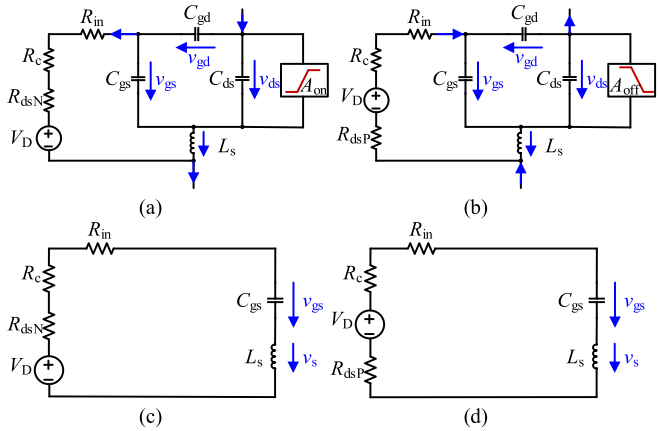

Fig. 7. Equivalent circuits of proposed gate driver. (a) Turn-ON transient. (b) Turn-OFF transient. (c) After turn-ON transient. (d) After turn-OFF transient.

$$v_{1\_\mathrm{off}}(0_-) = v_{1\_\mathrm{on}}(DT_\mathrm{s}) \approx -\frac{R_1(V_\mathrm{dr}-V_\mathrm{D})}{R_1+R_2} \tag{12}$$

$$v_{2\_\mathrm{on}}(DT_\mathrm{s}) \approx \frac{R_2(V_\mathrm{dr}-V_\mathrm{D})}{R_1+R_2}. \tag{13}$$

Since R_2 and C_2 form the RC circuit during the turn-OFF transient, according to (13), the initial value of v_2 during the turn-ON transient is expressed as follows:

$$v_{2\_\mathrm{on}}(0_-) = \frac{R_2(V_\mathrm{dr}-V_\mathrm{D})}{R_1+R_2} e^{-\frac{(1-D)T_\mathrm{s}}{R_2C_2}}. \tag{14}$$

D. Operation Principle and Parameter Design of the Proposed Crosstalk Voltage Suppression Circuit

To mitigate the crosstalk spikes caused by the high switching speed of SiC MOSFET, it is essential to confine the gate–source voltage spikes between the minimum negative allowable gate voltage $V_{\mathrm{gs\_min-}}$ and the threshold voltage V_th, as shown in Fig. 6. The proposed crosstalk suppression circuit provides an additional low-impedance path for both positive and negative crosstalk currents during the switching transients, which effectively suppresses the crosstalk voltage spikes. Fig. 7(a) depicts the equivalent circuit during turn-ON transient.

According to Kirchhoff's law, the principle of crosstalk spike suppression during turn-ON transient can be expressed as follows:

$$\begin{cases} v_\mathrm{ds} = v_\mathrm{gs} + v_\mathrm{gd} \\ \frac{dv_\mathrm{ds}}{dt} = A_\mathrm{on} \\ V_\mathrm{D} + (R_\mathrm{in}+R_\mathrm{c}+R_\mathrm{dsN})\left(C_\mathrm{gd}\frac{dv_\mathrm{gd}}{dt} - C_\mathrm{gs}\frac{dv_\mathrm{gs}}{dt}\right) = v_\mathrm{gs} \\ +L_\mathrm{s}\frac{d}{dt}\left(C_\mathrm{ds}\frac{dv_\mathrm{ds}}{dt} + C_\mathrm{gs}\frac{dv_\mathrm{gs}}{dt}\right) \end{cases} \tag{15}$$

where V_D is the diode conduction voltage drop, R_dsN is the drain–source ON-state resistance of NMOSFET M_N, and A_on is the slew rate of turn-ON transient. And the turn-ON transient gate–source voltage spike ΔV_+ can be obtained as follows:

$$\Delta V_+ = -R_+C_\mathrm{gd}A_\mathrm{on} - V_\mathrm{D} + \frac{1}{2T_+}\left(c_+e^{-a_+t} + d_+e^{-b_+t}\right) \tag{16}$$

where $a_+ = (R_+C_\mathrm{iss} + T_+)/(2L_\mathrm{s}C_\mathrm{gs})$, $b_+ = (R_+C_\mathrm{iss} - T_+)/(2L_\mathrm{s}C_\mathrm{gs})$, $c_+ = R_+C_\mathrm{gd}A_\mathrm{on}T_+ + V_\mathrm{D}T_+ + 2L_\mathrm{s}C_\mathrm{ds}A_\mathrm{on} - R_+{}^2C_\mathrm{iss}C_\mathrm{gd}A_\mathrm{on} - R_+C_\mathrm{iss}V_\mathrm{D}$, $d_+ = R_+C_\mathrm{gd}A_\mathrm{on}T_+ + V_\mathrm{D}T_+ - 2L_\mathrm{s}C_\mathrm{ds}A_\mathrm{on} + R_+{}^2C_\mathrm{iss}C_\mathrm{gd}A_\mathrm{on} + R_+C_\mathrm{iss}V_\mathrm{D}$, $T_+ = (R_+{}^2C_\mathrm{iss}{}^2 - 4L_\mathrm{s}C_\mathrm{gs})^{1/2}$, $R_+ = R_\mathrm{in} + R_\mathrm{c} + R_\mathrm{dsN}$.

According to (16), ΔV_+ first increases and then decreases with the turn-ON transient duration, and has a maximum value. The time t_+ when ΔV_+ is maximum value can be calculated as follows:

$$t_+ = \frac{L_\mathrm{s}C_\mathrm{gs}}{T_+}\ln\frac{(T_+ + R_+C_\mathrm{iss})c_+}{(T_+ - R_+C_\mathrm{iss})d_+}. \tag{17}$$

After the drain–source voltage no longer change, the change of the gate–source voltage is only determined by the initial state and parameters, as shown in Fig. 7(c). In this case, the gate–source voltage spike $\Delta V'_+$ can be expressed as follows:

$$\Delta V'_+ = -R_+C_\mathrm{gd}A_\mathrm{on} - V_\mathrm{D} + \frac{1}{2T_+}\left(c_+\mathrm{e}^{-\frac{a_+V_\mathrm{dc}}{A_\mathrm{on}}} + d_+\mathrm{e}^{-\frac{b_+V_\mathrm{dc}}{A_\mathrm{on}}}\right) + \frac{V_{0+}\left(\mathrm{e}^{-a'_+t} - \mathrm{e}^{-b'_+t}\right)}{\sqrt{R_+^2C_\mathrm{gs}^2 - 4L_\mathrm{s}C_\mathrm{gs}}} \tag{18}$$

where $V_{0+} = -(R_+C_\mathrm{gd} + L_\mathrm{s}C_\mathrm{ds})A_\mathrm{on} - 2V_\mathrm{D} + [(1 + L_\mathrm{s}a_+)c_+\mathrm{e}^{-a+V\mathrm{dc}/A\mathrm{on}} + (1+L_\mathrm{s}b_+)d_+\mathrm{e}^{-b+V\mathrm{dc}/A\mathrm{on}}]/(2T_+)$, $a'_+ = [R_+C_\mathrm{gs} + (R_+{}^2C_\mathrm{gs}{}^2 - 4L_\mathrm{s}\,C_\mathrm{gs})^{1/2}]/(2L_\mathrm{s}C_\mathrm{gs})$, $b'_+ = [R_+C_\mathrm{gs} - (R_+{}^2C_\mathrm{gs}{}^2 - 4L_\mathrm{s}C_\mathrm{gs})^{1/2}]/(2L_\mathrm{s}C_\mathrm{gs})$.

According to (18), $\Delta V'_+$ has only one extreme value, and whether it is the maximum or minimum value is determined by V_{0+}. The time t'_+ when $\Delta V'_+$ is the extreme value can be calculated as follows:

$$t'_+ = \frac{L_\mathrm{s}C_\mathrm{gs}}{\sqrt{R_+^2C_\mathrm{gs}^2 - 4L_\mathrm{s}C_\mathrm{gs}}}\ln\frac{R_+C_\mathrm{gs} + \sqrt{R_+^2C_\mathrm{gs}^2 - 4L_\mathrm{s}C_\mathrm{gs}}}{R_+C_\mathrm{gs} - \sqrt{R_+^2C_\mathrm{gs}^2 - 4L_\mathrm{s}C_\mathrm{gs}}}. \tag{19}$$

From the above analysis, it can be seen that the positive crosstalk spike during the turn-ON transient is determined by the turn-ON transient duration $V_\mathrm{dc}/A_\mathrm{on}$. When $V_\mathrm{dc}/A_\mathrm{on}$ is less than t_+, the maximum positive crosstalk spike $\Delta V_{+\_\mathrm{max}}$ appears at $V_\mathrm{dc}/A_\mathrm{on}$, and vice versa at t_+. The maximum positive crosstalk

spike during the turn-ON transient can be obtained as follows:

$$\Delta V_{+\_\max} = \begin{cases} -R_+C_{\rm gd}A_{\rm on} - V_{\rm D} + \frac{1}{2T_+}\left(c_+ e^{-\frac{a_+V_{\rm dc}}{A_{\rm on}}} + d_+ e^{-\frac{b_+V_{\rm dc}}{A_{\rm on}}}\right), \\ \qquad\qquad \text{if} \quad 0 \le \frac{V_{\rm dc}}{A_{\rm on}} < t_+, \\ -R_+C_{\rm gd}A_{\rm on} - V_{\rm D} + \frac{1}{2T_+}\left(c_+ e^{-a_+t_+} + d_+ e^{-b_+t_+}\right), \\ \qquad\qquad \text{if} \quad \frac{V_{\rm dc}}{A_{\rm on}} \ge t_+. \end{cases} \tag{20}$$

According to (18), the negative crosstalk spike is determined by V_{0+}. When V_{0+} is less than zero, $\Delta V'_+$ first decreases and then increases, and the minimum negative crosstalk spike $\Delta V_{+\_\min}$ appears at t'_+, vice versa at the initial time. The minimum negative crosstalk spike is obtained as follows:

$$\Delta V_{+\_\min} = \begin{cases} -R_+C_{\rm gd}A_{\rm on} - V_{\rm D} + \frac{1}{2T_+}\left(c_+ e^{-\frac{a_+V_{\rm dc}}{A_{\rm on}}} + d_+ e^{-\frac{b_+V_{\rm dc}}{A_{\rm on}}}\right) \\ \quad + \frac{V_{0+}\left(e^{-a'_+t'_+} - e^{-b'_+t'_+}\right)}{\sqrt{R_+^2C_{\rm gs}^2 - 4L_sC_{\rm gs}}}, \qquad \text{if} \quad V_{0+} < 0, \\ -R_+C_{\rm gd}A_{\rm on} - V_{\rm D} + \frac{1}{2T_+}\left(c_+ e^{-\frac{a_+V_{\rm dc}}{A_{\rm on}}} + d_+ e^{-\frac{b_+V_{\rm dc}}{A_{\rm on}}}\right), \\ \qquad\qquad \text{if} \quad V_{0+} \ge 0. \end{cases} \tag{21}$$

Similarly, the equivalent circuit during turn-OFF transient is shown in Fig. 7(b). When $V_{\rm dc}/A_{\rm off}$ is less than t_-, the minimum negative crosstalk spike $\Delta V_{-\_\min}$ appears at $V_{\rm dc}/A_{\rm off}$, vice versa at t_-, and $\Delta V_{-\_\min}$ can be expressed as follows:

$$\Delta V_{-\_\min} = \begin{cases} R_-C_{\rm gd}A_{off} + V_{\rm D} + \frac{1}{2T_-}\left(c_- e^{\frac{a_-V_{\rm dc}}{A_{off}}} + d_- e^{\frac{b_-V_{\rm dc}}{A_{off}}}\right), \\ \qquad\qquad \text{if} \quad 0 \le \frac{V_{\rm dc}}{A_{off}} < t_-, \\ R_-C_{\rm gd}A_{off} + V_{\rm D} + \frac{1}{2T_-}\left(c_- e^{-a_-t_-} + d_- e^{-b_-t_-}\right), \\ \qquad\qquad \frac{V_{\rm dc}}{A_{off}} \ge t_- \end{cases} \tag{22}$$

where $a_- = (R_-C_{\rm iss} + T_-)/(2L_sC_{\rm gs})$, $b_- = (R_-C_{\rm iss} - T_-)/(2L_sC_{\rm gs})$, $c_- = -R_-C_{\rm gd}A_{\rm off}T_- - V_{\rm D}T_- - 2L_sC_{\rm ds}A_{\rm off} + R_-^2C_{\rm iss}C_{\rm gd}A_{\rm off} + R_-C_{\rm iss}V_{\rm D}$, $d_- = -R_-C_{\rm gd}A_{\rm off}T_- - V_{\rm D}T_- + 2L_sC_{\rm ds}A_{\rm off} - R_-^2C_{\rm iss}C_{\rm gd}A_{\rm off} - R_-C_{\rm iss}V_{\rm D}$, $T_- = (R_-^2C_{\rm iss}{}^2 - 4L_sC_{\rm gs})^{1/2}$, $R_- = R_{\rm in} + R_{\rm c} + R_{\rm dsP}$, $t_- = (L_sC_{\rm gs}/T_-)\ln[(T_-c_- + R_-C_{\rm iss}c_-)/(T_-d_- - R_-C_{\rm iss}d_-)]$, $R_{\rm dsP}$ is the drain–source ON-state resistance of PMOSFET $M_{\rm P}$, and $A_{\rm off}$ is the slew rate of turn-OFF transient.

Similar to the turn-ON transient, the gate–source voltage is only determined by the initial state and parameters after the turn-OFF transient, as shown in Fig. 7(d). The positive crosstalk spike is determined by V_{0-}. When V_{0-} exceed zero, the maximum positive crosstalk spike $\Delta V_{-\_\max}$ appears at t'_-, vice versa at the initial time, and $\Delta V_{-\_\max}$ can be expressed as follows:

$$\Delta V_{-\_\max} = \begin{cases} R_-C_{\rm gd}A_{off} + V_{\rm D} + \frac{1}{2T_-}\left(c_- e^{\frac{a_-V_{\rm dc}}{A_{off}}} + d_- e^{\frac{b_-V_{\rm dc}}{A_{off}}}\right), \\ \qquad\qquad \text{if} \quad V_{0-} < 0, \\ R_-C_{\rm gd}A_{off} + V_{\rm D} + \frac{1}{2T_-}\left(c_- e^{\frac{a_-V_{\rm dc}}{A_{off}}} + d_- e^{\frac{b_-V_{\rm dc}}{A_{off}}}\right) \\ \quad + \frac{V_{0-}\left(e^{-a'_-t'_-} - e^{-b'_-t'_-}\right)}{\sqrt{R_-^2C_{\rm gs}^2 - 4L_sC_{\rm gs}}}, \qquad \text{if} \quad V_{0-} \ge 0 \end{cases} \tag{23}$$

where $V_{0-} = (R_-C_{\rm gd} + L_sC_{\rm ds})A_{\rm off} + 2V_{\rm D} + [(1 + L_sa_-)c_-e^{a\text{-}V{\rm dc}/A{\rm off}} + (1+L_sb_-)d_-e^{b\text{-}V{\rm dc}/A{\rm off}}]/(2T_-)$, $a'_- = [R_-C_{\rm gs} + (R_-^2C_{\rm gs}{}^2 - 4L_s\ C_{\rm gs})^{1/2}]/\ (2L_sC_{\rm gs})$, $b'_- = [R_-C_{\rm gs} - (R_-^2C_{\rm gs}{}^2 - 4L_sC_{\rm gs})^{1/2}]/(2L_sC_{\rm gs})$, $t'_- = L_sC_{\rm gs}\ln\{[R_-C_{\rm gs} + (R_-^2C_{\rm gs}{}^2 - 4L_sC_{\rm gs})^{1/2}]/[R_-C_{\rm gs} - (R_-^2C_{\rm gs}{}^2 - 4L_s\ C_{\rm gs})^{1/2}]\}/(R_-^2C_{\rm gs}{}^2 - 4L_s\ C_{\rm gs})^{1/2}$.

TABLE I
BASIC PARAMETERS OF SIC MOSFET

Symbol	Descriptions	Values
$C_{\rm iss}$	Input capacitance(pF)	2208
$C_{\rm gs}$	Capacitance(pF)	2156
$C_{\rm gd}$	Capacitance(pF)	52
$C_{\rm ds}$	Capacitance(pF)	66
$R_{\rm in}$	Gate input resistance(Ω)	5
$V_{\rm th}$	Gate threshold voltage(V)	2.7
$V_{\rm gs\_min-}$	Minimum negative allowable gate voltage(V)	-4

Based on (20), (21), (22), and (23), it is clear that the bus voltage, switching slew rate, Miller capacitance, and common-source inductance are key factors affecting the crosstalk voltage. To eliminate the risk of false-triggering, it is necessary to confine the crosstalk voltage spikes within a safe range through the low-impedance path. Therefore, the following requirements must be met

$$\begin{cases} V_{\rm gs\_off} + \Delta V_{+\_\max} < V_{\rm th} \\ V_{\rm gs\_off} + \Delta V_{+\_\min} > V_{gs\_\max -} \\ V_{\rm thP} + \Delta V_{-\_\min} > V_{gs\_\max -} \\ V_{\rm thP} + \Delta V_{-\_\max} < V_{\rm th}. \end{cases} \tag{24}$$

The switching loss $E_{\rm sw}$ of the proposed circuit in each period can be calculated as follows:

$$\begin{aligned} E_{\rm sw} = {} & \frac{1}{2}V_{\rm dc}^2 I_{\rm L}\left\{\frac{R_{\rm G}C_{\rm gd}}{V_{\rm dr} - V_{\rm miller}} + \frac{2g_{\rm m}R_{\rm G}C_{\rm gd} + C_{\rm oss}}{2g_{\rm m}V_{\rm miller}}\left[1 + \right.\right. \\ & \left.\left.\frac{L_{loop}\left(g_{\rm m}V_{\rm th} + 0.5I_{\rm L}\right)}{V_{\rm dc}\left(g_{\rm m}L_{\rm s} + R_{\rm G}C_{\rm iss}\right)}\right]^2\right\} \\ & + \frac{1}{2}V_{\rm dc}I_{\rm L}^2\left[\frac{g_{\rm m}L_{\rm s} + R_{\rm G}C_{\rm iss}}{g_{\rm m}\left(V_{\rm dr} - V_{\rm th}\right) - 0.5I_{\rm L}} + \frac{g_{\rm m}L_{\rm s} + R_{\rm G}C_{\rm iss}}{g_{\rm m}V_{\rm th} + 0.5I_{\rm L}}\right] \\ & + V_{\rm dc}\left(Q_{\rm rr} + I_{\rm L}\sqrt{\frac{Q_{\rm rr}\left(g_{\rm m}L_{\rm s} + R_{\rm G}C_{\rm iss}\right)}{g_{\rm m}\left(V_{\rm dr} - V_{\rm th}\right) - 0.5I_{\rm L}}}\right) \end{aligned} \tag{25}$$

where the equivalent gate drive resistance $R_{\rm G} = R_{\rm g} + R_{\rm in} + 1/(wC_1)$, input capacitance $C_{\rm iss} = C_{\rm gd} + C_{\rm gs}$, output capacitance $C_{\rm oss} = C_{\rm gd} + C_{\rm ds}$, $g_{\rm m}$ is transconductance, $L_{\rm loop}$ is total power loop inductance, and $Q_{\rm rr}$ is reverse recovery charge.

The SCT3022AL is taken as an example, with its fundamental parameters delineated in Table I. Based on (12) and the targeted

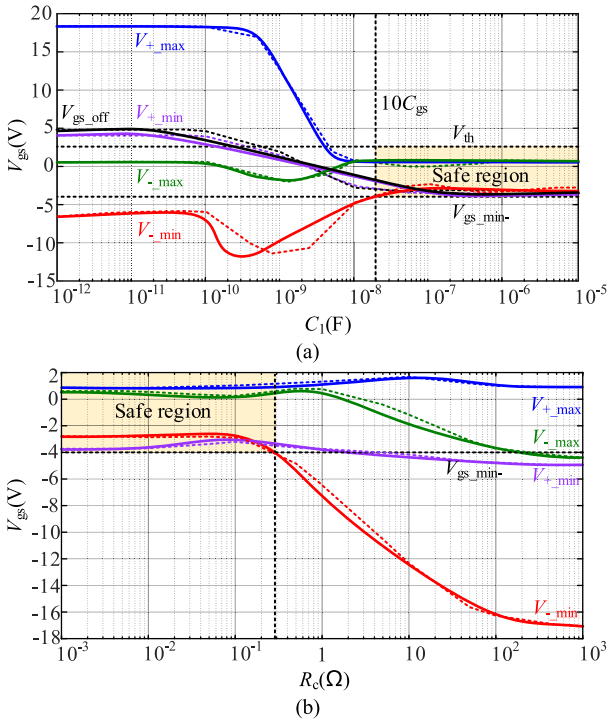

Fig. 8. Effect of C_1 and R_c on the gate–source voltage. (a) Effect of C_1 on the gate–source voltage. (b) Effect of R_c on the gate–source voltage.

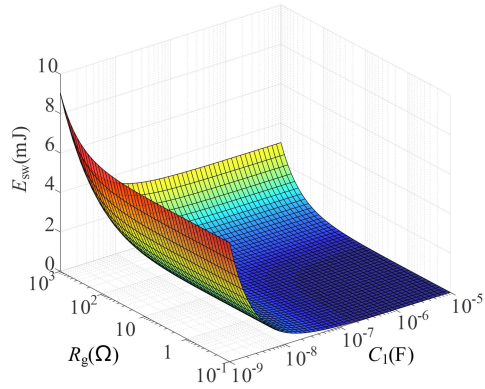

Fig. 9. Effect of C_1 and R_g on the switching loss.

TABLE II
COMPARISON OF DIFFERENT CROSSTALK SUPPRESSION DRIVING CIRCUITS

	Turn-ON process		Turn-OFF process		
	Positive spike/ Negative spike(V)	Turn-ON loss(μJ)	Positive spike/ Negative spike(V)	Turn-OFF loss(	Power supply/ Control signal
Propsoed	0.41/−3.46	239	0.71/−3.27	151	1/1
[17]	1.6/−4.7	321	1.11/−13.95	191	2/2
[18]	−0.85/−5.12	289	−1.15/−5.42	115	2/1
[20]	1.55/−4.79	304	−1.82/−16.89	188	1/1

turn-OFF voltage, resistor R_1 is configured to 20 kΩ, resistor R_2 to 100 kΩ, and capacitor C_2 to 470 nF. Based on (20), (21), (22), (23), and (24), the effect of capacitor C_1 and resistor R_c on the gate–source voltage can be obtained, as shown in Fig. 8. Fig. 8(a) shows the effect of C_1 on V_{gs_off}, V_{+_max}, V_{+_min}, V_{-_max}, and V_{-_min}, where the solid lines are the theoretical results and the dotted lines are the simulation results. From the above analysis, it is inferred that the safety region should lie between V_{gs_min-} and V_{th}. Furthermore, to provide a stable negative off voltage while avoiding affecting the switching speed, the value of C_1 should be significantly larger than that of C_{gs}, specifically, $C_1 > 10C_{gs}$. Consequently, the safe region for C_1 can be determined from the shaded area in Fig. 8(a). Incorporating a safety margin, C_1 is set as 2.2 μF in this article.

Fig. 8(b) demonstrates the effect of R_c on V_{+_max}, V_{+_min}, V_{-_max}, and V_{-_min}, where the solid lines are the theoretical results and the dotted lines are the simulation results. Since the crosstalk current flows in the same direction in the low-impedance path and the common-source inductor L_s, the voltages of the two have the same positive and negative sign. The crosstalk voltage on the gate–source of the SiC MOSFET is approximately equal to the voltage across the low-impedance path minus the voltage across the common-source inductor L_s. Therefore, the effect of the low-impedance branch on the crosstalk voltage is opposite to that of the common-source inductor L_s. When the lower device is turned ON and OFF, R_c in the low impedance branch causes positive crosstalk spike and negative crosstalk spike to the gate–source voltage v_{gs}, respectively, while the common source inductance L_s is completely opposite. According to (20), (21), (22), and (23), setting a suitable R_c value can partially offset the effect of the common source inductance L_s on the crosstalk voltage. It can be observed that when R_c is near 100 mΩ counterbalances the crosstalk voltage spike induced by the Miller capacitor on R_c against the voltage drop caused by common-source inductance. The positive and negative crosstalk spikes caused by common-source inductance are significantly mitigated, aligning with prior analytical results. Considering the interplay among R_c, Miller capacitance, and common-source inductance, the R_c is set to 100 mΩ. According to (25), a decrease in C_1 coupled with an increase in R_g results in elevated equivalent gate drive resistance, which in turn augments the switching loss E_{sw}, as shown in Fig. 9. Therefore, when setting C_1 and R_g, it is also necessary to consider the impact of both on the switching loss. Integrating the aforementioned analysis, R_g is chosen to be 10 Ω.

E. Simulation Comparison of the Proposed Crosstalk Suppression Circuit and Other Crosstalk Suppression Circuits

Fig. 10 shows the simulation results of the switching waveforms and crosstalk voltages of different crosstalk suppression circuits. Table II shows the comparison of crosstalk spikes, losses, power supplies, and control signals of different circuits. The quantitative comparison between the proposed circuit and [17], [18], [20] shows that the positive and negative crosstalk voltage spikes of the proposed circuit are always within the allowable range of the device, and the crosstalk peak amplitude is significantly smaller than that of other circuits, which effectively suppresses the crosstalk phenomenon. In terms of switching loss, the proposed circuit is superior to other circuits, and the added

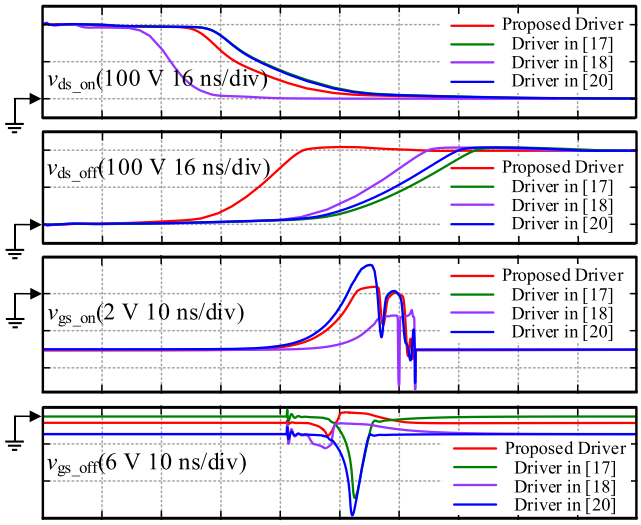

Fig. 10. Switching waveforms and crosstalk waveforms of different crosstalk suppression driving circuits.

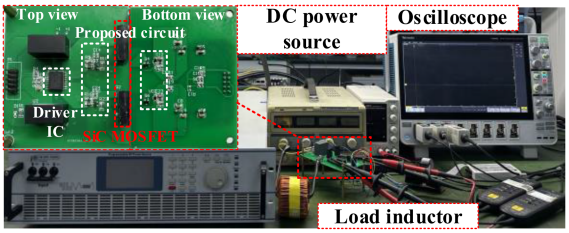

Fig. 11. Double-pulse test platform.

crosstalk suppression structure has little effect on the switching process. Moreover, compared with papers [17] and [18], the proposed circuit does not use additional power supply and control signal, which reduces the cost, volume, and logic signal control complexity of the drive circuit. The proposed circuit can effectively eliminate the crosstalk phenomenon caused by high dv/dt, and is easy to integrate into the driver IC.

IV. Experiment Results

To demonstrate the effectiveness of the proposed multilevel self-driving gate drive circuit in mitigating crosstalk voltage, a double-pulse test platform as shown in Fig. 11 is established, with component parameters listed in Table III. SiC MOSFET used is ROHM SCT3022AL, and the load inductance is 100 μH. The upper MOSFET functions for synchronous freewheeling, while the lower MOSFET is used to control the operational state of the half-bridge circuit.

To substantiate the effectiveness of the proposed crosstalk suppression gate drive circuit, double-pulse test waveforms for both the proposed gate drive circuit and the conventional negative turn-OFF voltage gate drive circuit are given, including gate–source voltage v_{gs_H}, v_{gs_L}, drain–source voltage v_{ds_L}, and drain–source current i_{ds_L}, as shown in Fig. 12. The conventional negative turn-OFF voltage gate drive circuit is different

TABLE III
Parameters of Proposed Crosstalk Suppression Circuit

Symbol	Descriptions	Values
Driver IC	Isolated dual-channel gate driver	UCC21521
M_N	N-channel power MOSFET	IRLML2502
M_P	P-channel power MOSFET	IRLML6401
D	Diode	1N5819HW
V_{dc}	Bus voltage(V)	200
R_1	Resistance(kΩ)	20
R_2	Resistance(kΩ)	100
R_3	Auxiliary resistance(Ω)	750
R_c	Auxiliary resistance(mΩ)	100
R_g	Gate resistance(Ω)	10
C_1	Capacitance(μF)	2.2
C_2	Capacitance(nF)	470
C_{gsP}	Capacitance(pF)	705

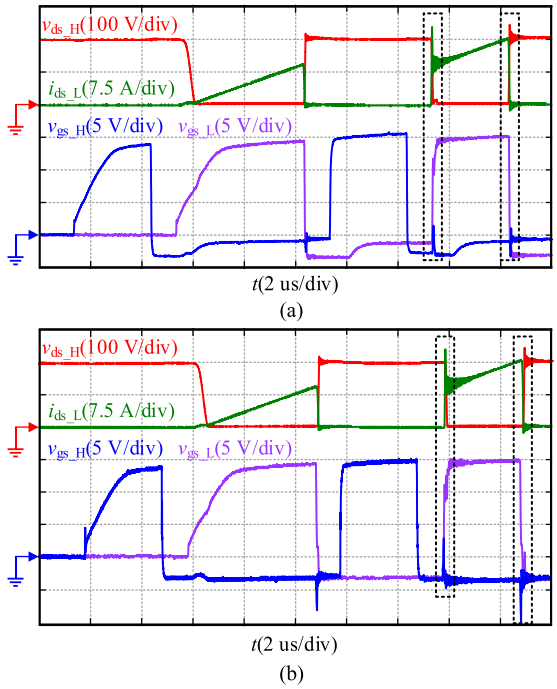

Fig. 12. Waveforms of the double-pulse test. (a) Proposed circuit. (b) Conventional circuit with constant −3 V turn-OFF voltage.

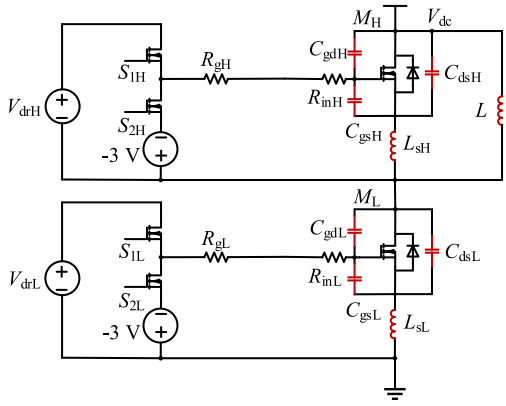

Fig. 13. Conventional circuit with constant −3 V turn-OFF voltage.

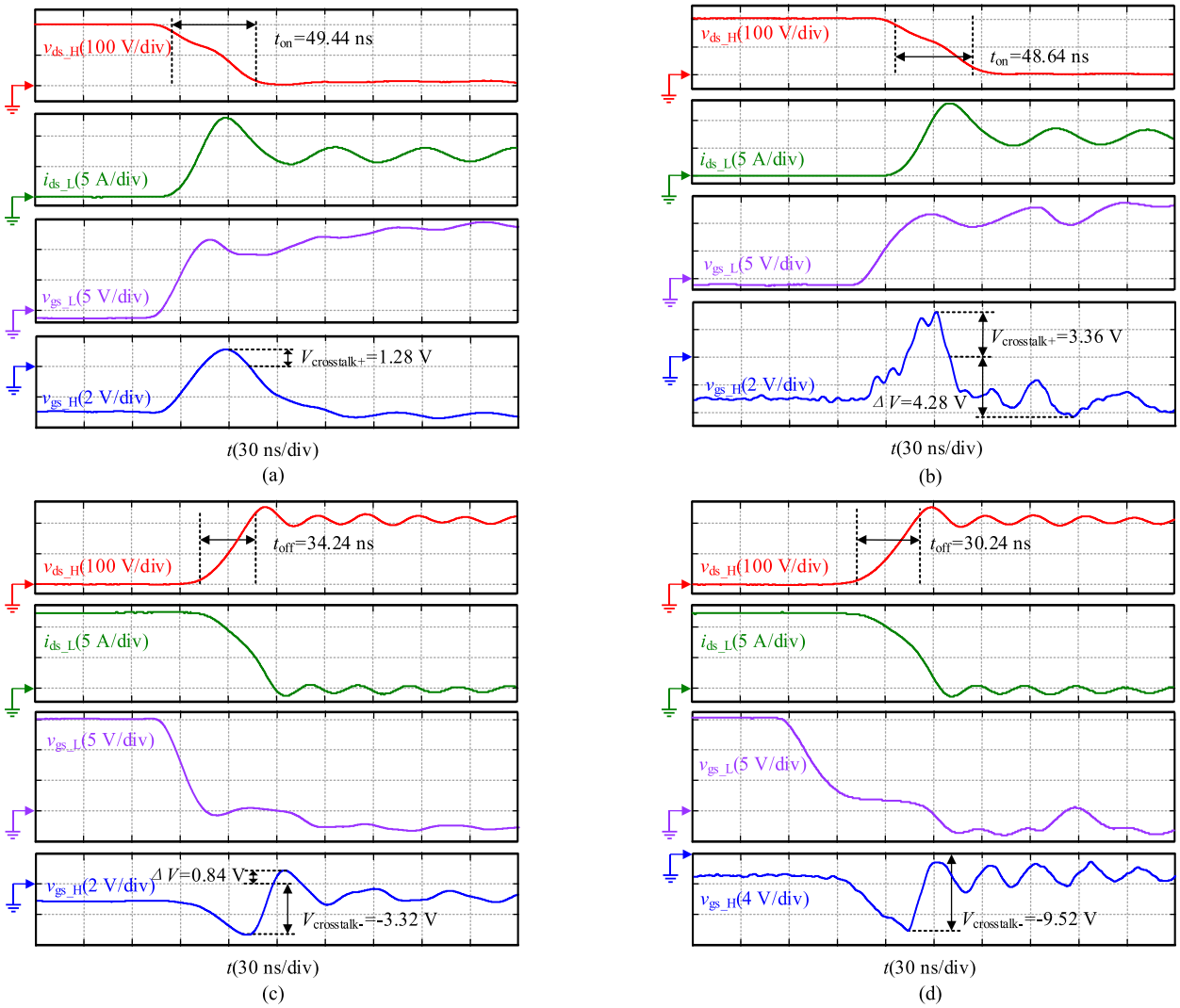

Fig. 14. Waveform enlargement of the double-pulse test. (a) Turn-ON transient of proposed circuit. (b) Turn-ON transient of conventional circuit. (c) Turn-OFF transient of proposed circuit. (d) Turn-OFF transient of conventional circuit.

from the traditional gate drive circuit with a turn-OFF voltage of 0 V, which uses an extra power supply with a turn-OFF voltage of −3 V to suppress the positive crosstalk spike, as shown in Fig. 13. In the double-pulse test, the control device M_L has two pulses of durations 5 and 3 μs, respectively, whereas M_H requires two 3 μs pulses to generate a stable negative turn-OFF voltage through precharging of C_1 and C_2, without extra negative power source. The negative turn-OFF voltage v_{g_off} is −3 V, the dead time T_d is 1 μs, and the self-driving time t_{sd} is set to 2 μs ($R_3 = 750\ \Omega$). During the M_L turn-ON and turn-OFF transients, the gate–source voltage of M_H appears obvious crosstalk phenomenon.

The suppression effect of the crosstalk suppression circuit on the positive and negative crosstalk voltage during the switching transients is shown in Fig. 14. It can be observed that both conventional method and proposed method provide a −3 V turn-OFF voltage. During the turn-ON transient of the control device M_L, the turn-ON time of conventional method is 48.64 ns, with the positive crosstalk voltage peak reaching 3.36 V, surpassing the threshold voltage of 2.7 V. Despite the device not being triggered, there remains a substantial risk of false-triggering. The negative crosstalk voltage peak reaching −4.28 V, marginally below the minimum negative allowable gate voltage of the device of −4 V. The R_{cH}–M_{NH}–D_{MPH} low-impedance branch of the crosstalk suppression circuit can significantly diminishes the crosstalk voltage peak caused by the turn-ON process. For the proposed crosstalk suppression circuit, the turn-ON time is 49.44 ns, with the positive crosstalk voltage peak at 1.28 V, which is 61.9% lower than the conventional method and well below the threshold voltage, without any significant negative crosstalk spike. Compared to the conventional method, the proposed circuit ensures that the gate–source voltage v_{gs_H} remains within a safe range during turn-ON transient, reducing the risk of false-triggering while having minimal impact on the ON-speed, and the ON-time is only increased by 0.8 ns. Similar to the turn-ON transient, the conventional method provides a −3 V turn-OFF voltage during turn-OFF transient of the control device M_L, while the proposed circuit clamps turn-OFF voltage at −1.2 V. The turn-OFF time of the conventional method is 30.24 ns, with the negative crosstalk

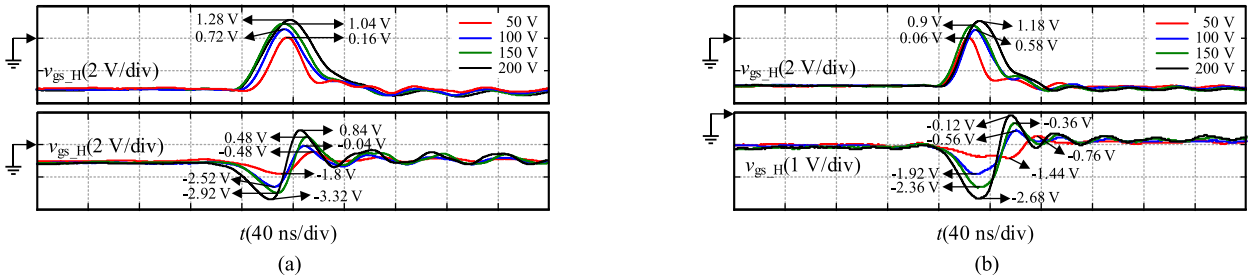

Fig. 15. Crosstalk voltage waveforms of the v_{gs} of the upper device when the lower device is turned ON and OFF under different working conditions. (a) Different bus voltages at 15 A. (b) Different bus voltages at 7.5 A.

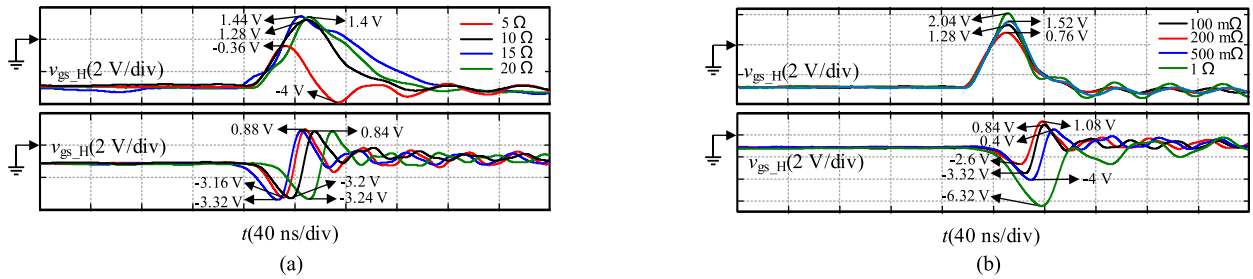

Fig. 16. Crosstalk voltage waveforms of the v_{gs} of the upper device when the lower device is turned ON and OFF under different parameters. (a) Gate drive resistance R_g. (b) Auxiliary resistance R_c.

voltage peak reaching −9.52 V, far exceeding the minimum negative allowable gate voltage of −4 V. Although the power device is not damaged immediately, the long-term overvoltage operation poses a serious threat to the lifespan and reliability of the device. The R_{cH}–D_{MNH}–M_{PH} low-impedance branch of the crosstalk suppression circuit can significantly inhibit the voltage peak caused by the turn-OFF process. For the proposed crosstalk suppression circuit, the turn-OFF time is 34.24 ns, and the turn-OFF time is increased by 4 ns. The negative crosstalk voltage peak is −3.32 V, which is 65.13% lower than that of the conventional method. The positive crosstalk spike is 0.84 V, which is much lower than the threshold voltage, ensuring that the gate–source voltage v_{gs_H} remains within a safe range during the turn-OFF transient, significantly reducing the risk of false-triggering and negative voltage stress while having little influence on the turn-OFF speed. The proposed method solves the crosstalk problem of power devices during switching transients without additional negative power supply and control signals.

From the above analysis, it can be seen that the crosstalk voltage spike of proposed scheme is influenced by the bus voltage and load inductor current. Fig. 15 shows the impact of different voltages/currents on crosstalk voltage. It can be observed that as the bus voltage gradually increases from 50 to 200 V, the positive crosstalk voltage of the synchronous freewheeling device M_H increases and the negative crosstalk voltage decreases. Conversely, when the load inductor current is reduced from 15 to 7.5 A, there is a marginal reduction in the crosstalk voltage during the turn-ON transient. However, during the turn-OFF transient, the positive crosstalk voltage significantly diminishes, and the negative crosstalk voltage elevates. The positive and negative crosstalk voltages always remain within the safe region, demonstrating the efficacy of the proposed scheme in mitigating crosstalk voltage spikes under different working conditions.

The gate drive resistance is a double-edged sword for suppressing the crosstalk voltage. While increasing the gate resistance can reduce dv/dt, the crosstalk current may generate a greater voltage drop on the resistance, leading to an increase in the crosstalk spike initially, as shown in Fig. 16(a). The positive crosstalk voltage spike at the turn-ON transient increases at first with the increase of the gate drive resistance until the gate drive resistance reaches a critical point between 15 and 20 Ω, beyond which it begins to diminish. Because the low-impedance circuit is in the pre-conduction state when M_L is turned OFF, the influence of the gate resistance on the crosstalk voltage is weakened, so the change of gate resistance has little influence on the crosstalk voltage when M_L is turned OFF. As shown in Fig. 16(b), as the auxiliary resistance R_c increases from 100 mΩ to 1 Ω, the positive crosstalk spike V_{+_max} first decreases and then increases, whereas the positive crosstalk spike V_{-_max} and negative crosstalk spike V_{-_min} exhibit an opposite trend, and V_{+_min} is negligible. This is consistent with the above analysis, which proves the correctness of the analysis.

Table IV shows a comparison of switching loss between proposed method and conventional method under different conditions. Observations indicate as drain–source voltage V_{ds} and drain circuit I_d increase, the turn-ON and turn-OFF losses for both methods incrementally rise, and the proposed method is slightly better than the conventional method. Therefore, the proposed

TABLE IV
COMPARISON OF SWITCHING LOSS BETWEEN THE PROPOSED METHOD AND CONVENTIONAL METHOD UNDER DIFFERENT CONDITIONS

	V_{ds}(V)	50		100		150		200	
	I_d(A)	$E_{on}(\mu J)$	$E_{off}(\mu J)$	$E_{on}(\mu J)$	$E_{off}(\mu J)$	$E_{on}(\mu J)$	$E_{off}(\mu J)$	$E_{on}(\mu J)$	$E_{off}(\mu J)$
Conventional method	5	4.679	2.982	14.711	8.031	23.682	12.905	37.365	16.913
	7.5	7.911	5.053	19.528	12.135	33.005	19.901	48.028	27.514
	10	11.807	8.901	24.991	17.379	44.215	28.023	65.723	40.021
	15	18.072	15.134	39.875	28.121	65.141	46.504	98.456	66.011
Proposed method	5	3.983	2.115	12.261	5.852	22.143	9.230	35.704	12.091
	7.5	7.023	4.101	16.971	9.215	30.013	12.956	46.018	18.931
	10	10.022	6.175	22.017	12.535	41.891	19.711	60.404	26.552
	15	16.302	11.397	33.446	20.715	62.593	30.941	92.108	43.232

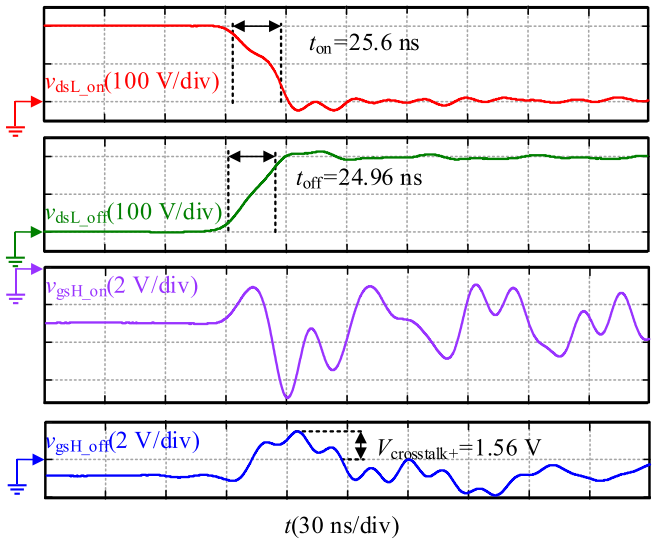

Fig. 17. Switching waveforms and crosstalk waveforms of planar SiC MOSFET.

crosstalk suppression circuit has little effect on the switching loss. These results corroborate the analysis in this article, thereby validating the efficacy of the proposed method.

Since SCT3022AL is a trench SiC MOSFET, in order to verify the effectiveness of the proposed method for different types of SiC MOSFETs, this article adds a comparative experiment with planar SiC MOSFET C3M0015065D under the same experimental conditions, as shown in Fig. 17. According to the data sheet, the minimum allowable negative voltage of C3M0015065D is −8 V, and the threshold voltage is 2.3 V. It can be seen that the switching speed is faster because the internal gate resistance of C3M0015065D is 1.5 Ω, which is less than 5 Ω of SCT3022AL. Although the crosstalk spike suppression effect caused by the common-source inductance of C3M0015065D is worse than that of SCT3022AL and there is obvious oscillation phenomenon, the positive and negative crosstalk voltage spikes of the method proposed are within the safe allowable range, verifying the effectiveness of the method proposed for planar SiC MOSFET.

V. CONCLUSION

This article presents a multilevel self-driving crosstalk suppression circuit based on SiC MOSFET and alongside a comprehensive mathematical model for crosstalk voltage that incorporates both Miller capacitance and common-source inductance. The circuit employs resistors, NMOS, and PMOS to establish a low impedance path for both positive and negative crosstalk currents. According to the proposed model, setting a appropriate resistance value effectively mitigates the impact of Miller capacitance and common-source inductance on crosstalk voltage. Moreover, a voltage divider is utilized to generate the first-stage turn-OFF voltage, which aids in suppressing the positive crosstalk voltage spike. The low-impedance branch is preconducted through the RC branch, and the turn-OFF voltage is clamped at the second-stage turn-OFF voltage to alleviate negative voltage stress and minimize the negative crosstalk spike. The NMOS and PMOS of the low impedance branch are controlled by R_g and the RC branch, respectively, without additional control signals. The method proposed herein relies solely on passive devices, thereby facilitating the integration of the crosstalk suppression circuit into the driver IC. In comparison to the conventional method, this approach effectively mitigates both positive and negative crosstalk voltages, with minimal impact on switching transient duration and switching loss. Experimental results demonstrate that the proposed method is effective for both trench and planar SiC MOSFETs. However, under different operating conditions, the proposed circuit cannot adaptively adjust the multilevel negative turn-OFF voltage, self-driving time and resistance value of the low-impedance branch. To address this limitation, the relevant resistors can be replaced with digital rheostats, and the resistance values can be adaptively adjusted to suit different operating conditions through additional control signals. Other passive devices can be integrated into the driver IC, which is the direction of future improvement.

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