A Four Switch Common Ground-Based Single Phase Current-Fed Boost Inverter

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***Abstract*—Single-stage boost inverters are gaining more attention in photovoltaic (PV) applications. These inverters utilize a shoot-through state to deliver power at the rated voltage. However, most of them require at least five controlled active switches and more than two passive reactive elements in the intermediate network. Also, the absence of galvanic isolation introduces a high-frequency common mode voltage, leading to a circulating current. To address these limitations, a compact four-switch common ground-based single-phase current-fed boost inverter is proposed in this article. It utilizes four controlled active switches, two diodes, one inductor, and one capacitor. The common ground configuration of the inverter effectively eliminates the circulating current. The utilization of a single capacitor in the intermediate network, as well as the symmetrical operation of the inverter for both half cycles of ac output, reduces the dc offset. Further, the continuous input current and step-up nature of the inverter make it appropriate for PV applications. The design, operational modes, pulse width modulation control strategy, and closed-loop control of the proposed inverter are presented. The steady-state and dynamic analyses are validated using MATLAB Simulink, while the thermal and power loss analyses are performed by PLECS software. Finally, the simulation results and performance of the inverter are verified with experimental results.**

***Index Terms*—Boost inverter, common ground (CG), current-fed switched inverter (CFSI), grid-connected photovoltaic (PV) inverter.**

I. INTRODUCTION

THE penetration of sustainable energy sources is enhancing significantly day-by-day. Amidst all the green sustainable energy sources, photovoltaic (PV) energy is indeed a pivotal and increasingly prominent source in the global energy landscape [1]. The traditional voltage source inverter (VSI) used for PV systems acts as a buck converter. Therefore, in the conventional PV system, either a dc–dc boost converter is employed before the VSI, or a line-frequency transformer is utilized after the VSI for power transfer at the rated voltage. However, cascading the step-up converter into the VSI increases the number of stages. On the other side, a line-frequency transformer expands the overall dimensions and weight of the system. To overcome these difficulties, impedance source inverters (ISIs) emerge as a prominent solution for low and medium-power applications [2].

ISI offers single-stage dc–ac power conversion with inherent boost functionality, achieved through the utilization of the shoot-through (ST) state to transform the input dc voltage to the preferred output ac voltage. The ISI, such as the Z source inverter (ZSI) [3] and quasi-Z source inverter (Q-ZSI) [4], employs a unique impedance network coupled between the input dc power supply and output ac load (or) grid, facilitating the boost operation of the inverter. The input current of the ZSI is discontinuous, and Q-ZSI is continuous in nature. However, the higher count of passive reactive elements increases the size and cost of these inverters. The enhanced voltage gain ISIs are discussed in [5], [6], and [7]. These inverters improve the voltage gain by utilizing more than two passive reactive elements. To reduce the number of impedance elements, a switched boost inverter (SBI) [8] and a current-fed switched inverter (CFSI) [9] are presented. These inverters retain all the benefits of ZSI and Q-ZSI, with two passive reactive elements, while adding one extra active switch in the intermediate impedance network. The additional controlled active switch in the intermediate network of these inverters and their derivatives may cause additional losses and increase the cost of the inverter. In [10], a single-stage SBI with four switch configurations is discussed. The inverter exhibits all the merits of ZSI and Q-ZSI. In addition, it requires only four controlled active switches, and the dc offset is minimized by utilizing the additional filter capacitor. However, the voltage gain of the inverter is limited.

Furthermore, due to the lack of galvanic isolation for the above-discussed inverters (ZSI, Q-ZSI, SBI, etc.) and their derivatives, the switching characteristics of the inverter induce a high-frequency common mode voltage (CMV) over the parasitic capacitance (C_{PV}) of the PV panel [11]. This CMV results in a circulating current (i_{LK}) flowing through the circuit. Consequently, harmonics may be injected into the grid, electromagnetic compatibility may deteriorate, and the lifespan of PV systems may be reduced. As per the standard and recommendations, the amplitude of the circulating current should not exceed 30 mA, and according to the NEC 690 standards, proper grounding is required for the grid-tied PV inverter [12]. Also, as per the IEEE 1547 and IEC 61727 standards, the maximum allowed dc offset current injection into the grid should be less than 0.5%. Considering the above-mentioned standards,

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PV-integrated inverters, such as H6 and H10 are discussed in [13] and [14], where the amplitude of circulating current is reduced to 45 and 11.3 mA, respectively. In [15] and [16], common ground (CG)-based step-down inverters are discussed, where the CG completely eliminates the circulating current. However, the step-down nature of the above-mentioned inverters [13], [14], [15], [16] necessitates an extra converter stage to boost the input voltage, which may limit its applications.

The CG-based ISIs are discussed in [17], [18], [19], and [20]. However, these inverters utilize more than two passive reactive elements, which may increase the size and cost of the inverter prototype. In [21] and [22], CG-based boost inverters with reduced reactive elements and controlled active switches are discussed. However, the input current is discontinuous in nature. A single-phase, single-stage boost inverter with a four-switch configuration for PV applications is discussed in [23]. However, it utilizes four passive-reactive elements. A four-switch θ-type PV grid-connected inverter is discussed in [24]. The focus of this literature is power frequency harmonic ripple reduction, where the boost function of the inverter has not been explored much. In addition, the bipolar pulse width modulation (PWM) control technique and unsymmetrical operation of these inverters [23], [24] lead to the dc offset and the injection of harmonics into the grid. In [25], a CG-based single-stage nonisolated boost inverter is discussed. However, the overall elements of the inverter and discontinuous mode operation may limit its applications. In [26], a CG-based five-switch boost inverter is discussed. The inverter employs just two impedance elements and eliminates the dc offset by operating symmetrically during both the positive and negative half cycles. Nevertheless, this comes with the tradeoff of needing an extra active switch and associated gate driver.

Considering the aforementioned limitations, a compact four-switch CG-based single-phase current-fed boost inverter is proposed in this article. The major characteristics of the proposed inverter include the following.

1) It requires only four controlled active switches, one inductor, and one capacitor.
2) The CG nature of the inverter eliminates the circulating current.
3) It can boost the input dc voltage to supply the power at the rated voltage by utilizing the intermediate impedance network.
4) The improved voltage gain allows the inverter to function with a reduced duty ratio and a higher modulation index. Consequently, the voltage across the inverter elements is minimized.
5) The symmetrical operation and the utilization of a single capacitor in the intermediate network eliminate the injection of dc offset current into the grid.

The proposed inverter's continuous input current, single-stage power conversion, and above-mentioned potentials make it suitable for applications, such as PV systems.

II. OPERATIONAL DESCRIPTION

Fig. 1 depicts the proposed CG-based single-phase current-fed boost inverter. It comprised one inductor, one capacitor, two diodes (D_0, D_{10}), and a set of four active switches (S_W, S_1–S_3). The impedance LC network is utilized to boost the input dc voltage. The input inductor L ensures a continuous input current, while the capacitor C provides voltage with two polarities for the grid. The ground of the input dc terminal is connected to the output ac grid neutral terminal, which eliminates the circulating current. The working operation is described in three intervals. Interval-I addresses the active state's positive and negative half cycles, whereas the zero state discourses interval-II. Finally, the interval-III is an energy-boosting state, and this state provides a unique boost feature to the inverter.

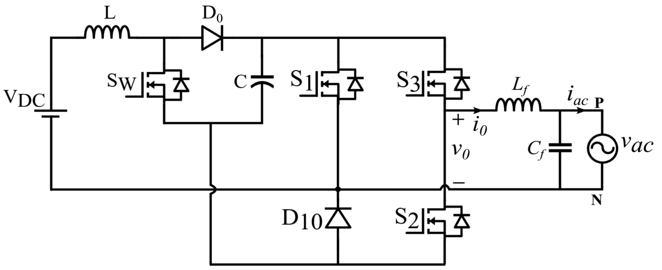
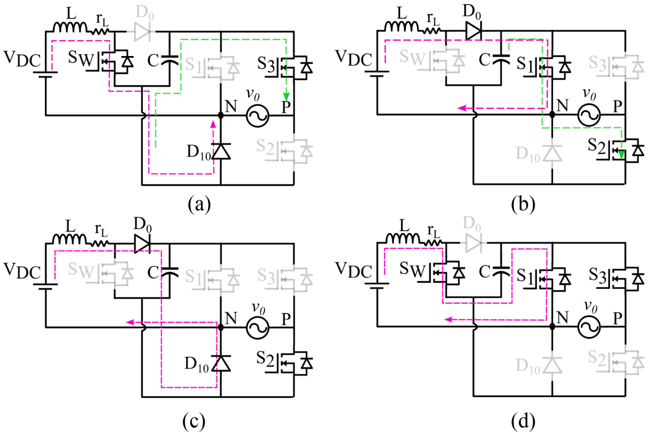


Fig. 1. Schematic diagram of the four-switch CG-based current-fed boost inverter.



(a) (b) (c) (d)

Fig. 2. Equivalent circuit for the different operating intervals. (a) Interval-I. (b) Interval-I. (c) Interval-II. (d) Interval-III.

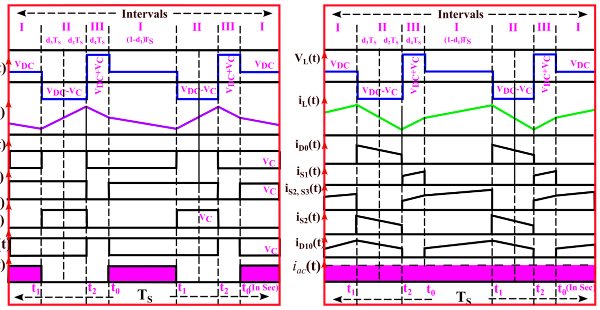
A. Operational Principles

1) Interval-I [t_0–t_1]: During the positive half cycle of this active state, the switches S_W and S_3 are switched ON, while the switches S_1 and S_2 are switched OFF. As a result, the diode D_0 is reverse-biased, while the diode D_{10} is forward-biased. Here, the inductor L builds energy from the dc source while the capacitor C delivers power to the load, as shown in Fig. 2(a). It can be noted that the inverter is operating in boost mode. As a result, the input current is greater than the load current, leading to the forward-biasing of diode D_{10}. Consequently, the load current flows through switch S_3 and diode D_{10}. During this interval $(1-d_1)T_S$, the voltage across the inductor V_L, current through the capacitor i_C, and output voltage v_0 can be expressed as

$$V_L = V_{\text{dc}} - i_L r_L \tag{1}$$

$$i_C = -i_0 \tag{2}$$

$$v_0 = +V_C \tag{3}$$



(a) (b)

Fig. 3. Operating behavior of inverter elements in a switching period. (a) Voltage waveforms. (b) Current waveforms.

where i_0 is the inverter output current, V_C is the capacitor voltage, and r_L is the internal resistance of the inductor. Fig. 3 displays the ideal steady-state waveforms for the interval $[t_0\text{–}t_1]$, depicting the voltage and current behavior of the semiconductor switches and impedance elements. During the negative half cycle, the switches S_1 and S_2 are switched ON, while the switches S_W and S_3 are switched OFF. Consequently, the diode D_0 is forward-biased, and the diode D_{10} is reverse-biased. Similar to the positive half cycle, the dc power supply magnetizes the inductor while the capacitor delivers power to the load, as shown in Fig. 2(b). During this interval $(1-d_1)T_S$, the V_L, i_C, and v_0 are expressed as

$$V_L = V_{\text{dc}} - i_L r_L \tag{4}$$

$$i_C = -i_0 \tag{5}$$

$$v_0 = -V_C. \tag{6}$$

From the expressions (1), (2), (4), and (5), it can be observed that the inverter operates symmetrically in both half cycles (excluding the parasitic drops of the switches). Therefore, the ideal steady-state waveforms of the voltage and current stress remain the same as in the positive half cycle.

2) Interval-II [t_1–t_2]: During this zero state, the switch S_2 is switched ON, while the switches S_W, S_1 and S_3 are switched OFF. As a result, both the diodes are forward-biased. During this interval $[t_1\text{–}t_2]$, the capacitor is charged by the dc supply and inductor, while the load freewheels through S_2 and D_{10}, as depicted in Fig. 2(c). During this interval $(d_2 + d_3)T_S$, the output voltage is zero, while the V_L and i_C are given in the following:

$$V_L = V_{\text{dc}} - V_C - i_L r_L \tag{7}$$

$$i_C = i_L. \tag{8}$$

3) Interval-III [t_2–t_0]: During this energy boosting state, the switches S_W, S_1, and S_3 are switched ON, while the switch S_2 is switchedOFF. As a result, the diodes are reverse-biased. During this interval $[t_2\text{–}t_0]$, the dc power supply and capacitor energize the inductor while the load freewheels through the switches S_1 and S_3, as depicted in Fig. 2(d). During this interval $d_4 T_S$, the output voltage is zero, while the V_L and i_C are given as follows:

$$V_L = V_{\text{dc}} + V_C - i_L r_L \tag{9}$$

$$i_C = -i_L. \tag{10}$$

The operational waveforms of the V_L, i_L, V_C, and corresponding switching pulse for intervals II and III can be observed from Fig. 3. The operating status of the switches for various intervals is provided in Table I.

TABLE I
SWITCH STATUS FOR DIFFERENT OPERATING INTERVALS

Intervals	ON elements	OFF elements	Output
I (+ve half)	S_W, S_3, D_{10}	S_1, S_2, D_0	$+v_{\text{ac}}$
I (−ve half)	S_1, S_2, D_0	S_W, S_3, D_{10}	$-v_{\text{ac}}$
II	$S_2, , D_0, D_{10}$	S_W, S_1, S_3	0
III	S_W, S_1, S_3	S_2, D_0, D_{10}	0

B. Steady-State Analysis

In the steady-state condition, utilizing the volt–second balance principle for the inductor and the charge balance for the capacitor over one switching cycle (T_S) results in

$$\begin{aligned}(V_{\text{dc}} - i_L r_L)(1-d_1) &+ (V_{\text{dc}} - V_C - i_L r_L)(d_2 + d_3)\\ &+ (V_{\text{dc}} + V_C - i_L r_L)d_4 = 0\end{aligned} \tag{11}$$

$$-i_0(1-d_1) + i_L(d_2 + d_3) - i_L d_4 = 0 \tag{12}$$

where $d_1 T_S$ is the sum of zero state and energy boosting state, $d_1 T_S = (d_2 + d_3 + d_4)T_S$, and $d_3 T_S = d_4 T_S$. The $d_3 T_S$ and $(1-d_1)T_S$ periods vary sinusoidally with respect to time, while the duty ratio d_2 is constant. From (11), and (12), the V_C and i_L can be derived as

$$V_C = \frac{V_{\text{dc}} - i_L r_L}{d_2} \tag{13}$$

$$i_L = i_0 \frac{(1-d_1)}{d_2}. \tag{14}$$

Considering the average output power of the inverter as P_0 and by substituting (14) in (13), the voltage boost factor (B) and voltage gain (G) is

$$B = \frac{V_C}{V_{\text{dc}}} = \frac{1}{d_2\left(1 + \frac{(1-d_1) r_L i_0^2}{P_0 d_2^2}\right)} \tag{15}$$

$$G = \frac{v_{\text{ac}}}{V_{\text{dc}}} = mB = \frac{m}{d_2\left(1 + \frac{(1-d_1) r_L i_0^2}{P_0 d_2^2}\right)} \tag{16}$$

where m is the modulation index and v_{ac} is the output ac voltage. From (16), it has been identified that the voltage gain is the function of the internal resistance of the inductor (r_L) and load power (P_0). Neglecting the power loss linked with the r_L, the capacitor voltage is

$$V_C = \frac{V_{\text{dc}}}{d_2} = BV_{\text{dc}}. \tag{17}$$

Fig. 4 shows the plot between G, m, and d_2 by neglecting the r_L. From the plot, it can be observed that for the same voltage gain, there are multiple operating points as a function of the modulation index and duty ratio. Hence, to achieve the required voltage gain, the modulation index and duty ratio are optimally selected, leading to reduced power loss and improved efficiency. To make sure that the duty ratio does not overlap with the modulation index, the following constraint (18) should

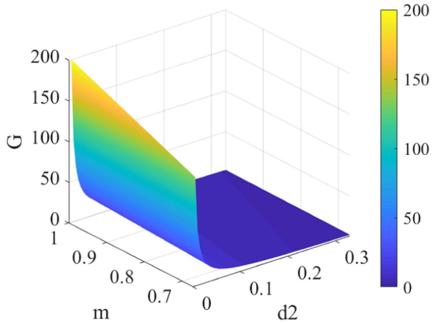


Fig. 4. Correlative plot between modulation index (m), duty ratio (d_2), and voltage gain (G).

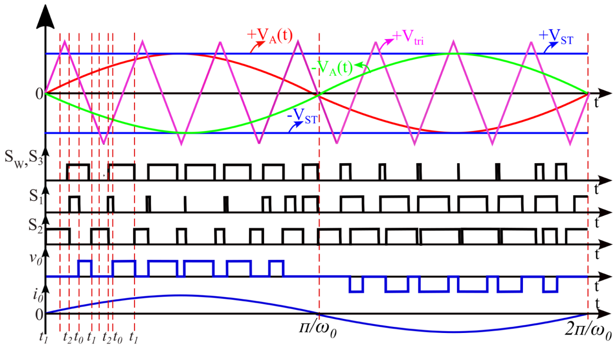


Fig. 5. PWM control technique and switching pulses for the inverter.

be satisfied:

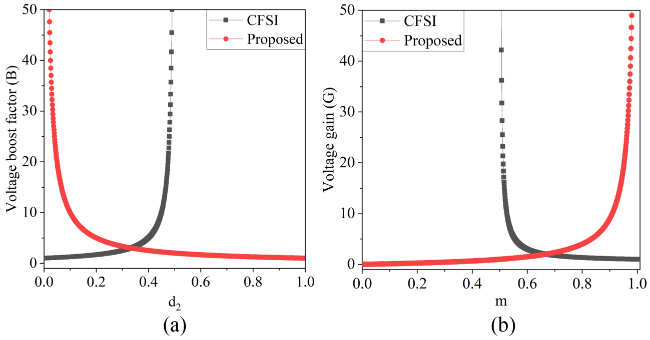
$$d_2 + m = 1. \tag{18}$$

The mean duty ratio of the active state, computed as explained in [6], is obtained as

$$d_1 = \frac{T_0(\theta)}{T_S} = d_2 + d_3 + d_4 = 1 - \frac{2m}{\pi}. \tag{19}$$

C. PWM Control Technique

The unipolar PWM control technique is utilized to generate the switching pulse for the proposed inverter. It effectively eliminates the center band harmonics and reduces the filter requirement. To produce the switching pulse, the high-frequency triangular carrier signal is compared with the two modulating signals phase shifted by 180° (V_A(t) and $-V_A$(t)), along with two constant amplitude signals (V_{ST} and $-V_{\mathrm{ST}}$), as shown in Fig. 5. Using the constraints (16) and (18), the amplitude of the modulating signals and constant signals are selected. The switching pulse for interval-I is created by comparing the triangular signal with two modulating signals. During $d_2 T_S$ period, the PWM pulses are developed by comparing the triangular signal with $\pm V_{\mathrm{ST}}$, while in $d_3 T_S$ period, the PWM signals are developed when the triangular signal falls between the modulating signal and the constant amplitude signal. Here, the $d_2 T_S$ and $d_3 T_S$ are combined as interval-II, as shown in Fig. 5 and the other $d_4 T_S$ is considered as interval-III to lessen the current ripple and improve the voltage gain.



(a) (b)

Fig. 6. Comparison of the conventional CFSI and proposed inverter. (a) Boost factor (B) versus duty ratio (d_2). (b) Voltage gain (G) versus modulation index (m).

TABLE II
VOLTAGE AND CURRENT STRESSES

Parameter	Peak voltage	Parameter	Peak current
V_C	$\frac{1}{d_2}V_{\mathrm{dc}}$	i_L,I_{SW}, I_{D_0}	$\frac{(1-d_1)}{d_2}i_0$
$V_{\mathrm{SW}}, V_{S1}, V_{S2}$	$\frac{1}{d_2}V_{\mathrm{dc}}$	I_{S2}, I_{S3}	i_0
V_{S3}, V_{D10}, V_{D0}	$\frac{1}{d_2}V_{\mathrm{dc}}$	I_{S1}, I_{D10}	$(\frac{(1-d_1)}{d_2}+1)i_0$

A comparative plot has been drawn between conventional CFSI [9] and the proposed inverter in terms of boost factor (B) and voltage gain (G), as displayed in Fig. 6. From Fig. 6(a) and (b), it is evident that the inverter operates at a lower duty ratio and higher modulation index, which reduces the capacitor voltage demand. Consequently, the switch voltage stress gets minimized.

D. Intermediate Parameter Selection

1) Semiconductor Device Selection: The selection of active switches and a power diode primarily relies on the maximum voltage stress and the maximum current flowing through them. From Table II, it can be noticed that the stress experienced by the switches does not exceed their rated output voltage, highlighting the advantage of the inverter.

2) Impedance Parameter Selection: The inductor and capacitor are chosen based on the allowable peak-to-peak ripple. The inductor current can be written in terms of load power (P_0) as

$$i_L = \frac{P_0}{V_{\mathrm{dc}}}. \tag{20}$$

The ripple in the capacitor voltage (ΔV_C) and the ripple in the inductor current (ΔI_L) can be obtained from (7) and (8), respectively, as given in the following:

$$\Delta V_C = \frac{i_L}{C}(d_2 + d_3)T_S \tag{21}$$

$$\Delta i_L = \frac{V_{\mathrm{dc}} - V_C}{L}(d_2 + d_3)T_S. \tag{22}$$

The normalized peak-to-peak ripple in inductor current and capacitor voltage is given as

$$\Delta i_{Ln} = \frac{\Delta i_L}{i_L}, \Delta V_{Cn} = \frac{\Delta V_C}{V_C}. \tag{23}$$

Using (20), (22), and (23), the inductance (L) can be attained as

$$L = \frac{V_{\text{dc}}^2 (1 - \frac{1}{d_2})(d_2 + d_3)}{\Delta i_{\text{Ln}} P_0 f_s (1 - d_1)} \tag{24}$$

where f_s is the switching frequency. Using (20), (21), and (23), the expression for the capacitance (C) can be attained as

$$C = \frac{P_0 d_2 (1 - d_1)(d_2 + d_3)}{\Delta V_{Cn} V_{\text{dc}}^2 f_s}. \tag{25}$$

E. LC Filter Design

In order to mitigate significant voltage and current harmonics, a second-order *LC* low-pass filter is designed. The design mainly focuses on achieving a unity gain at 50 Hz while attenuating the higher frequency components effectively. In general, the cutoff frequency is set slightly higher than the fundamental frequency and lower than the switching frequency. In general, the cutoff frequency (ω_c) can be calculated using filter impedance elements as

$$\omega_c = \frac{1}{\sqrt{L_f C_f}}. \tag{26}$$

Another consideration when selecting components for the second-order low-pass filter is the quality factor (Q-factor) or damping ratio. In *LC* filter design for inverters, the Q-factor is a crucial parameter that indicates the performance and efficiency of the filter. Hence, selecting the appropriate filter impedance elements (L_f, C_f) is crucial to achieving the desired cutoff frequency (ω_c) and Q-factor. From the proposed inverter, the voltage across the filter inductor (v_{L_f}) can be expressed as

$$v_{L_f} = v_0 - v_{\text{ac}}. \tag{27}$$

Considering the acceptable load current ripple, which is 10% of the load current, the filter inductor can be formulated as

$$L_f = \frac{d_2 (1 - d_1)^2 v_0^2}{0.4 P_0 f_s}. \tag{28}$$

In the same way, the filter capacitor (C_f) can be determined as

$$C_f = \left(\frac{10}{2\pi f_s}\right)^2 \frac{1}{L_f}. \tag{29}$$

III. CMV ANALYSIS

The switching between different operating states of the inverter causes high-frequency CMV. The CG of the proposed inverter connects the input to the output ac load or grid, as shown in Fig. 7. It was found in [11] that the differential mode voltage also affects the circulating current along with the CMV. Hence, the simplified expression of total CMV v_{CM} and circulating current i_{LK} are given as

$$v_{\text{CM}} = \frac{v_{\text{ac}}}{2} \tag{30}$$

$$i_{\text{LK}} = C_{\text{PV}} \frac{dv_{\text{CM}}}{dt}. \tag{31}$$

The overall CMV v_{CM} in (30) is immune to any high-frequency component. Due to this, the circulating current passes through the parasitic capacitance (C_{PV}) is nullified, as in (31).

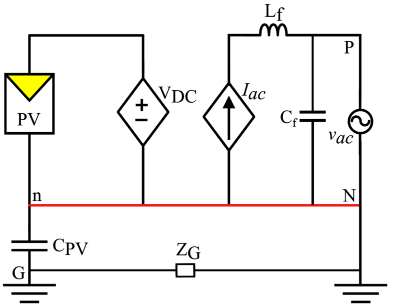
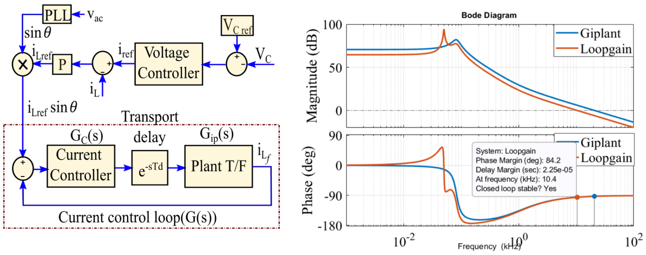


Fig. 7. Equivalent single line schematic of proposed inverter.



(a) (b)

Fig. 8. (a) Control strategy of the proposed inverter. (b) Bode plot of the plant transfer function $G_{\text{iplant}}(s)$, and loop gain $G(s)$.

This zero-circulating current may improve a PV panel's life span and satisfy safety standards.

IV. INVERTER MODELING AND CONTROLLER DESIGN

The overall control block diagram of the proposed inverter, shown in Fig. 8(a), adopted from [27]. The current control loop $G(s)$ consists of the PR controller $G_C(s)$, transport delay, and plant transfer function $G_{\text{iplant}}(s)$ of the proposed inverter.

A. Inverter Modeling

The small-signal model of the inverter is derived using the state–space average technique. The state variables of the inverter include intermediate inductor current i_L, filter inductor current i_{L_f}, intermediate capacitor voltage v_C, and filter capacitor voltage v_{C_f}. The state–space expressions of the three operating intervals, specifically the active state $(1 - d_1)T_S$, zero state $(d_2 + d_3)T_S$, and the energy-boosting state $d_4 T_S$ are formulated as

$$\begin{bmatrix} \dot{i}_L \\ \dot{i}_{L_f} \\ \dot{v}_C \\ \dot{v}_{C_f} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_f} & -\frac{1}{L_f} \\ 0 & -\frac{1}{C} & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{RC_f} \end{bmatrix} \begin{bmatrix} i_L \\ i_{L_f} \\ v_C \\ v_{C_f} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{\text{dc}} \tag{32}$$

$$\begin{bmatrix} \dot{i}_L \\ \dot{i}_{L_f} \\ \dot{v}_C \\ \dot{v}_{C_f} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_f} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{RC_f} \end{bmatrix} \begin{bmatrix} i_L \\ i_{L_f} \\ v_C \\ v_{C_f} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{\text{dc}} \tag{33}$$

$$\begin{bmatrix} \dot{i}_L \\ \dot{i}_{L_f} \\ \dot{v}_C \\ \dot{v}_{C_f} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 & \frac{1}{L} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_f} \\ -\frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{RC_f} \end{bmatrix} \begin{bmatrix} i_L \\ i_{L_f} \\ v_C \\ v_{C_f} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{\mathrm{dc}}. \tag{34}$$

Perturbations of state variables and duty cycle are given as

$$\left.\begin{aligned} i_L = I_L + \hat{i_L}, i_{L_f} = I_{L_f} + \hat{i_{L_f}}, d_2 = D_2 + \hat{d_2} \\ v_C = V_C + \hat{v_C}, v_{C_f} = V_{C_f} + \hat{v_{C_f}}, v_{\mathrm{dc}} = V_{\mathrm{dc}} + \hat{v_{\mathrm{dc}}} \end{aligned}\right\} \tag{35}$$

where $I_L, I_{L_f}, V_C, V_{C_f}$, and D_2 are dc quantities of intermediate and filter inductor currents (i_L and i_{L_f}), intermediate and filter capacitor voltages (v_C and v_{C_f}), and duty ratio d_2, respectively. Similarly, $\hat{i_L}$, $\hat{i_{L_f}}$, $\hat{d_2}$, $\hat{v_C}$, $\hat{v_{\mathrm{dc}}}$, and $\hat{v_{C_f}}$ are the perturbations. Using the small signal perturbations around the steady-state operating point while neglecting the second-order terms, the equivalent state–space expression can be given as

$$\begin{bmatrix} \dot{i}_L \\ \dot{i}_{L_f} \\ \dot{v}_C \\ \dot{v}_{C_f} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 & -\frac{d_2}{L} & 0 \\ 0 & 0 & \frac{(1-d_1)}{L_f} & -\frac{1}{L_f} \\ \frac{d_2}{C} & -\frac{(1-d_1)}{C} & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{RC_f} \end{bmatrix} \begin{bmatrix} \hat{i_L} \\ \hat{i_{L_f}} \\ \hat{v_C} \\ \hat{v_{C_f}} \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v_{\mathrm{dc}}} + \begin{bmatrix} -\frac{V_C}{L} \\ -\frac{V_C}{L_f} \\ -\frac{i_L + i_{L_f}}{2} \\ 0 \end{bmatrix} \hat{d}_2 \tag{36}$$

where $\hat{d}_2(s)$ is the control variable, $\hat{V}_{\mathrm{dc}}(s)$ is the disturbance variable. By applying the Laplace transform to the above-mentioned equation and simplifying it, the expression for the intermediate inductor current and capacitor voltage, as well as the filter inductor current and capacitor voltage, are obtained as follows:

$$\left.\begin{aligned} s\hat{i}_L(s) &= -\tfrac{r_L}{L}\hat{i}_L - \tfrac{d_2}{L}\hat{V}_C + \tfrac{1}{L}\hat{V}_{\mathrm{dc}} - \tfrac{V_C}{L}\hat{d}_2 \\ s\hat{V}_C(s) &= \tfrac{d_2}{C}\hat{i}_L - \tfrac{(1-d_1)}{C}\hat{i}_{L_f} + \tfrac{(i_L+i_{L_f})}{L}\hat{d}_2 \\ s\hat{i}_{L_f}(s) &= \tfrac{(1-d_1)}{L_f}\hat{V}_C - \tfrac{1}{L_f}\hat{V}_{Cf} - \tfrac{V_C}{L_f}\hat{d}_2 \\ s\hat{V}_{C_f}(s) &= \tfrac{1}{C_f}\hat{i}_{L_f} - \tfrac{1}{C_f R}\hat{v}_{C_f} \end{aligned}\right\} \tag{37}$$

Neglecting the internal resistance of the inductor and input voltage perturbations, the plant transfer function $G_{ip}(s)$ is formulated as

$$G_{\mathrm{iplant}}(s) = \left.\frac{\widehat{i}_{L_f(s)}}{\hat{d}_S(s)}\right|_{\widehat{v}_{\mathrm{dc}}(s)=0} = \frac{a_0 s^3 + s^2 a_1 + s a_2 + a_3}{b_0 s^4 + b_1 s^3 + b_2 s^2 + b_3 s + b_4}. \tag{38}$$

The $G_{\mathrm{iplant}}(s)$ is utilized in the design of the controller. The detailed mathematical expressions of the variables $a_0 - a_3$, and $b_0 - b_4$ are presented in the Appendix.

B. Controller Design

Fig. 8(a) shows the closed-loop block diagram for the proposed boost inverter. Here, the current controller is designed to follow the sinusoidal current reference at the grid frequency, aiming for minimal steady-state error and distortion. This is achieved by ensuring a high loop gain in the low-frequency region of the frequency response. The proportional resonant (PR) controller, as described by the transfer function in (39), is tuned to achieve the current loop stability so that the inverter system can follow the grid frequency under different operating conditions

$$G_C(s) = k_p \left(1 + \frac{k_i 2\omega_r s}{s^2 + \omega_r s + \omega_n^2}\right) \tag{39}$$

where k_p and k_i are the proportional and integral gains, and ω_n and ω_r are the grid frequency and resonant cutoff frequency in rad/sec. The parameters of the PR controller have been designed using [27]. The obtained control parameters are $k_p = 0.06$, $k_i = 80$, $\omega_r = 10$ rad/s, and $\omega_n = 314.159$ rad/s. The bode plot of the plant transfer function $G_{\mathrm{iplant}}(s)$, and loop transfer function $G(s)$ are plotted, as shown in Fig. 8(b). This plot indicates a gain margin of inf., phase margin of $84.4°$ at a gain cross over the frequency of 10.4 kHz. These stability margins of the current controller evidently indicate the closed-loop stability and its robustness against the system's uncertainties. During the discontinuous mode of operation, the controller parameters need small adjustments to ensure the stable operation of the inverter.

V. COMPARATIVE ANALYSIS

A detailed comparative study with respect to the other contemporary inverters is presented in Table III. The inverters presented in [13] and [14] are developed to maintain the circulating current within acceptable limits, as defined by the NEC 690 standards. However, these inverters function as step-down inverters, necessitating an additional stage for boosting the input voltage prior to grid connection. The CG-based boost inverters reported in [17], [18], [19], [20], [21], and [22] can enhance the input dc voltage while maintaining the CG. However, compared to the proposed inverter, the inverters presented in [17], [18], [19], and [20] necessitate more impedance parameters. The inverters [17], [18], [19] consist of more semiconductor devices in conducting state, and the inverters [17], [18] encounter twice the rated output voltage across the switches. The input current of the inverters [21], [22] is discontinuous in nature. The unsymmetrical operation of the inverter [23], in both half cycles, injects dc offset current into the grid. In addition, it utilizes the bipolar PWM control technique, which increases the harmonics. Meanwhile, the proposed inverter achieves symmetrical operation through a unipolar PWM control technique and operates in continuous conduction mode, effectively reducing both dc offset and current harmonics. Although the voltage gain of the inverter [25] is computed under continuous conduction mode, the higher number of overall elements and discontinuous input current limit its application. The inverter presented in [26] achieves symmetrical operation by employing a unipolar PWM control technique. However, these inverters require five controlled active switches and associated gate drivers, whereas the proposed inverter utilizes only four controlled active switches.

Furthermore, to emphasize the merits of the proposed inverter, a comparative analysis of the proposed inverter with the recent contemporary four-switch inverters is conducted, as given in Table IV. It includes the number of elements, input current, switching frequency, dc offset, Fourier series expression of output voltage, the inductor current ripple, capacitor voltage ripple, and leakage current. The inverters presented

TABLE III
PERFORMANCE COMPARISON WITH GRID-CONNECTED INVERTERS

Inverters	Power elements				Input current	Boost factor	Voltage stress	Current stress	Total conducting switches and diodes	Circulating current	PWM control	Independent gate driver	DC offset	Reactive power capability
	L	C	S	D_0										
Ref. [13]	0	0	6	2	Disc.	NA	v_0	i_{peak}	3	45 mA	Unipolar	4	NA	NA
Ref. [14]	0	0	10	0	Disc.	NA	v_0	i_{peak}	5	11.7 mA	Unipolar	5	NA	NA
Ref. [17]	2	4	4	3	Cont.	$\frac{1}{(1-2d_2)}$	$2v_0$	$(1-d_2)Bi_{\text{peak}}$	4	≈ 0	Unipolar	3	Yes	Yes
Ref. [18]	1	2	6	3	Disc.	$\frac{2(1-d_2)}{(1-3d_2)}$	$2v_0$	$(1-d_2)Bi_{\text{peak}}$	4	≈ 0	Unipolar	4	Yes	Yes
Ref. [19]	2	3	4	2	Cont.	$\frac{1}{(1-2d_2)}$	v_0	$(1-d_2)Bi_{\text{peak}}$	4	≈ 0	Unipolar	3	Yes	Yes
Ref. [20]	2	2	3	1	Cont.	$\frac{(1-2d_2)}{d_2(1-d_2)}$	$2v_0$	$(1-d_2)Bi_{\text{peak}}$	2	≈ 0	Unipolar	3	Yes	Yes
Ref. [21]	1	1	5	1	Disc.	$\frac{(1-d_2)}{d_2}$	v_0	$(1-d_2)Bi_{\text{peak}}$	3	≈ 0	Unipolar	3	No	Yes
Ref. [22]	1	1	6	1	Disc.	$\frac{d_2}{(1-d_2)}$	$v_0 + V\text{dc}$	$\frac{2}{(1+d_2)}i_{\text{peak}}$	4	≈ 0	Modified bipolar	5	Yes	Yes
Ref. [23]	2	2	4	0	Cont.	$\frac{(2d_2-1)}{d_2(1-d_2)}$	$\frac{1}{(1-d_2)}v\,\text{dc}$	$\frac{1}{(1-d_2)}i_{\text{peak}}$	2	≈ 0	Bipolar	2	Yes	Yes
Ref. [25]	1	2	3	3	Disc.	$\frac{1}{(1-d_2)}$	v_0	$(1-d_2)Bi_{\text{peak}}$	3	≈ 0	Unipolar	3	Yes	Yes
Ref. [26]	1	1	5	1	Cont.	$\frac{1}{d_2}$	v_0	$(1-d_2)Bi_{\text{peak}}$	3	≈ 0	Unipolar	4	No	Yes
Proposed	1	1	4	2	Cont.	$\frac{1}{d_2}$	v_0	$(1-d_2)Bi_{\text{peak}}$	3	≈ 0	Unipolar	3	No	Yes

L: Inductor, C: Capacitor, S: Switch, D_0: Diode, Disc.: Discontinuous, Cont.: Continuous, d_2: Duty ratio, i_{peak} : Peak load current, NA: Not Applicable, NR: Not Reported.

TABLE IV
PERFORMANCE COMPARISON WITH LOW SWITCH COUNT BOOST INVERTERS

Ref	Power elements and devices					Input current	Switching frequency (kHz)	Switch type	Dc offset	Charging and discharging Operation	Fourier expression of the output voltage waveform	Inductor current ripple	Capacitor voltage ripple	Active Switches in conduction	Leakage current
	L	C	S	D_0	Total										
Proposed	1	1	4	2	8	Cont.	10	Si	No	Symmetrical	$v_0(t) = \sum_{n=1,3,5}^{N} \frac{4V_C}{n\pi}\sin(n\omega t)$	Low	Low	2	≈ 0
Ref. [29]	2	2	4	0	8	Cont.	10	Si	No	Symmetrical	$v_0(t) = \sum_{n=1,3,5}^{N} \frac{4V_C}{n\pi}\sin(n\omega t)$	Low	Low	2	Exists
Ref. [24]	1	2	4	0	7	Cont.	20	Si	Yes	Unsymmetrical	$v_0(t) = \frac{V_{\text{offset}}}{2} + \sum_{n=1,3,5}^{N}\left(\frac{4V_{C1}}{n\pi} - \frac{2V_{\text{offset}}}{n\pi}\right)\sin(n\omega t)$	High	High	2	≈ 0
Ref. [25]	1	2	3	3	9	Disc.	20	SiC	Yes	Unsymmetrical	$v_0(t) = \frac{V_{C1}-V_{C2}}{2} + \sum_{n=1,3,5}^{N}\left(\frac{2V_{C1}}{n\pi} + \frac{2V_{C2}}{n\pi}\right)\sin(n\omega t)$	High	High	2	≈ 0
Ref. [30]	1	1	6	0	8	Cont.	NR	GaN	No	Symmetrical	$v_0(t) = \sum_{n=1,3,5}^{N} \frac{4V_C}{n\pi}\sin(n\omega t)$	Low	Low	3	≈ 0
Ref. [31]	2	0	7	2	11	Disc.	40	SiC	Yes	Unsymmetrical	$v_0(t) = \frac{V_{L1}-V_{L2}}{2} + \sum_{n=1,3,5}^{N}\left(\frac{2V_{L1}}{n\pi} + \frac{2V_{L2}}{n\pi}\right)\sin(n\omega t)$	High	High	5	Exists
Ref. [28]	1	2	4	0	7	Cont.	20	Si	Yes	Unsymmetrical	$v_0(t) = \frac{V_{\text{offset}}}{2} + \sum_{n=1,3,5}^{N}\left(\frac{4V_{C1}}{n\pi} - \frac{2V_{\text{offset}}}{n\pi}\right)\sin(n\omega t)$	High	High	2	≈ 0
Ref. [32]	1	1	4	2	8	Disc.	20	Si	Yes	Symmetrical	$v_0(t) = \sum_{n=1,3,5}^{N} \frac{4V_0}{n\pi}\sin(n\omega t)$	High	High	3	≈ 0

Si: Silicon switches, SiC: Silicon Carbide switches, GaN: Gallium Nitride switches, NR: Not Reported.

in [25], [31], and [32] operated in discontinuous conduction mode, which leads to complex maximum power point tracking (MPPT). In addition, the inverter [32] utilizes two dc power supplies to realize the inverter. Otherwise, extra capacitors and one dc source are required. The unsymmetrical charging and discharging of the capacitors during the positive and negative half cycles of the active state in the inverter [25] results in offset voltage (V_{offset}) and increased peak-to-peak capacitor voltage ripple. Although the inverter discussed in [29] consists of four active switches and is operated symmetrically, it requires four intermediate impedance elements, which increases the overall inverter size. The dc offset of the inverters has been expressed in a Fourier series. From the Fourier series analysis, it can be observed that the inverters [24], [25], [31], and [32] contain dc offset voltage. As per the IEEE 1547 and IEC 61727 standards, the maximum allowed dc offset current injection into the grid should be less than 0.5%. Due to the dc offset, the peak-to-peak ripple in the capacitor voltage is greater, which leads to an increase in the size of the intermediate impedance elements. However, the proposed inverter maintains the continuous input current and is symmetrically operated for both half cycles. As a result, the dc offset in the proposed inverter is mitigated. From the above-mentioned distinctive comparisons, it is evident that the proposed inverter exhibits benefits, such as continuous input current, fewer switches, high voltage gain, less voltage stress, zero dc offset, and zero circulating current by employing only four active switches, two diodes, one inductor, and one capacitor.

TABLE V
PARAMETERS USED FOR THE SIMULATION AND EXPERIMENTAL ANALYSIS

Parameter	Specification (or) part no.
Input dc voltage (V_{dc})	40 V
Output ac voltage (v_{ac}), $Frequency(f)$	110 V (rms), 50 Hz
Inductor (L)	2 mH
Capacitor (C)	$1000\ \mu F/400V$
Carrier frequency (f_s)	10 kHz
MOSFET	SIHG25N40D-GE3
Diode	U30D30C
LC filter (L_f, C_f)	5 mH, 10 μF
RL Load	400 W

VI. RESULTS AND DISCUSSION

A. *Simulation Results and Analysis*

The performance of the proposed inverter employing a unipolar PWM control technique has been analyzed with MATLAB Simulink in grid-connected mode. The simulated results are cross-validated with the help of a real-time OPAL-RT (OP-4510) simulator. Using (24) and (25), the inductor and capacitor have been designed for 5% and 1% of peak-to-peak ripple, respectively. In order to eliminate switching frequency ripples and achieve a smooth output voltage and current, the filter inductor and capacitor were designed based on (28) and (29). The specifications used for the simulation are given in Table V.

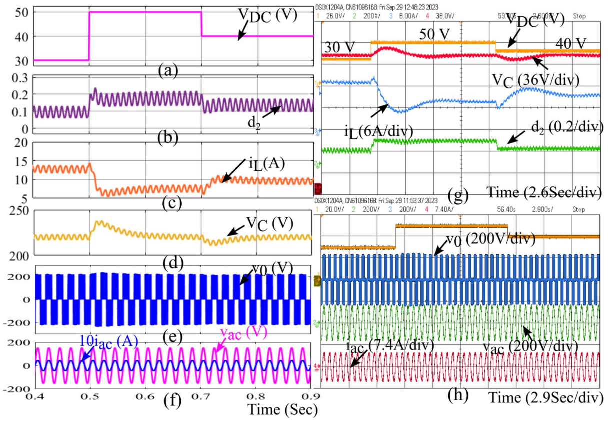


Fig. 9. Step response of the inverter for the grid-connected mode. (a)–(f) MATLAB simulation results. (g) and (h) OPAL-RT results.

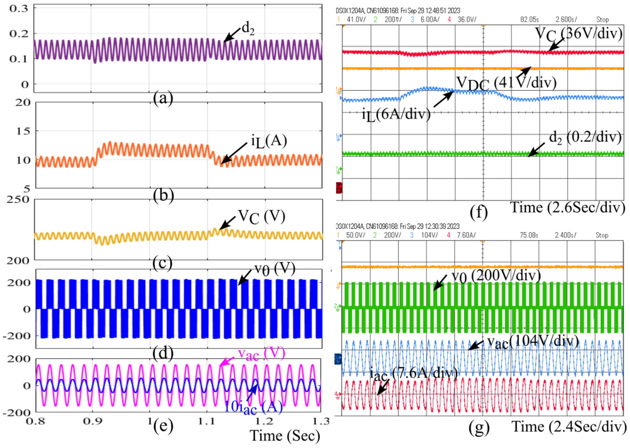


Fig. 10. Transient response of the inverter for the load change in the grid-connected mode. (a)–(e) Simulation results. (f) and (g) OPAL-RT results.

A dual-loop control system with a voltage controller in the outer loop and a proportional (P) controller in the inner loop is utilized. Here, the voltage controller generates a reference current by assessing the capacitor voltage, while the P controller compares this reference current with the inductor current to determine and produce the regulated reference current. Meanwhile, the PR controller is utilized to inject active power at the unity power factor (PF).

The inverter's dynamic behavior in response to a step change in input voltage is shown in Fig. 9. Fig. 9(a) illustrates that the input voltage variation initially starts from 30 to 50 V and then settles at 40 V. In Fig. 9(b), it has been noticed that the controller effectively regulates the duty ratio (d_2) starting from 0.1363 to 0.2272 and then settles at 0.1818, ensuring a stable capacitor voltage of 220 V. It can be inferred from Fig. 9(c) and (d) that the inductor current changes from 14 to 9 A and then settles at 11 A, while the capacitor maintains a stable output voltage of 220 V. Fig. 9(e) shows a stable two-level output voltage $\pm$ 220 V in response to a sudden change in the input voltage. Conversely, the PR controller regulates the duty ratio to maintain the grid voltage and current constant, as depicted in Fig. 9(f).

Further, the real-time simulator OPAL-RT (OP-4510) has been utilized to verify the simulation results, and the outcomes are shown in Fig. 9(g) and (h), respectively. Fig. 9(g) illustrates the controlled behavior of the duty ratio and transient response of the inductor current and capacitor voltage, while Fig. 9(h) displays the two-level output voltage alongside the grid voltage and current. It is evident from the figures that the controller effectively aligns the grid current in phase with the grid voltage, leading to the proper injection of active power. It can be observed that, despite variations in the input voltage, no notable differences are observed in the grid voltage and current. The THD of the grid voltage and grid current are found to be 1.64% and 1.56%, respectively, with zero dc offset current.

Furthermore, a dynamic analysis was carried out to verify the controller's performance under a change in power injection to the grid. In order to vary the amount of power injected into the grid, the grid current reference is varied from 4.8 to 5.8 A and then settles at 5 A, and the simulation results are shown in Fig. 10. According to the law of conservation of energy, the change in power injected into the grid leads to a variation in the input power, resulting in a fluctuation in the inductor current at a constant supply voltage. Due to the change in inductor current reference from 4.8 to 5.8 A, there is a slight increase in duty ratio, which then decreases while the inductor current reference is reduced to 5 A, as shown in Fig. 10(a). Due to this transition in duty ratio, a slight deviation in capacitor voltage is observed during dynamic conditions. The dynamic behavior of the inductor current and capacitor voltage has been shown in Fig. 10(b) and (c), respectively. Fig. 10(d) and (e) clearly demonstrates that the grid voltage remains consistent despite the change in the grid current. Fig. 10(f) and (g) shows the OPAL-RT results for the same case. Both results validate the active power injection at the unity PF. The performance of the inverter is verified under varying input voltage and load current in order to emulate the change in temperature and irradiation of the PV system with MPPT control.

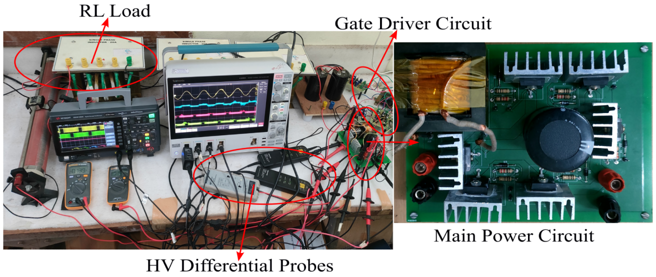


Fig. 11. Photograph of the experimental setup.

B. Experimental Results

A 400 W laboratory prototype has been developed to verify the feasibility of the proposed inverter, as illustrated in Fig. 11. The prototype was tested with a 60 V input dc voltage and a 110 V (rms) output ac voltage, and the remaining parameters are considered the same, as given in Table V. Based on the specified input and output voltages, the duty ratio and modulation index are calculated within the given constraints (16) and (18). The obtained values are 0.2783 and 0.7216, respectively. The active

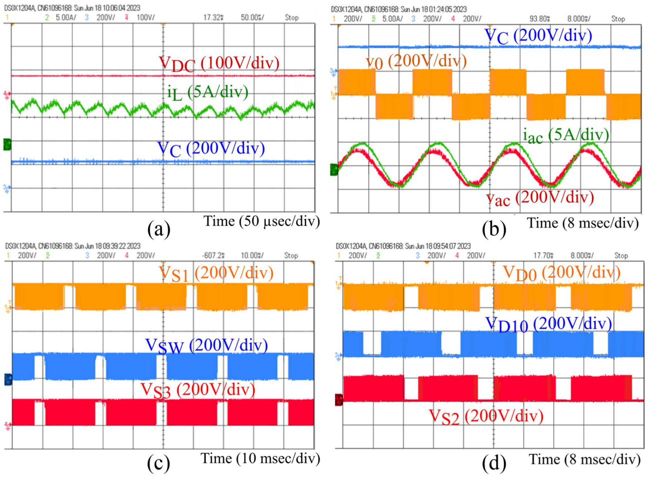


Fig. 12. Experimental results for 60 V input dc voltage. (a) Input voltage (V_{dc}), inductor current (i_L), capacitor voltage (V_C). (b) Output voltage with and without filter (v_0, v_{ac}), and output current (i_{ac}). (c) Switch voltage (V_{SW}, V_{S1}, V_{S3}). (d) Diode and switch voltages (V_{D0}, V_{S2}, V_{D10}).

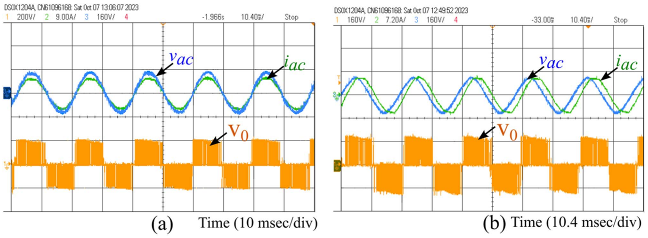


Fig. 13. Experimental results at different PF conditions. (a) Unity. (b) 0.7PF.

switch PWM control signals have been generated using the reconfigurable Xilinx Spartan-6 XC6SLX4 board. The steady-state experimental outcomes for the rated load condition are displayed in Fig. 12. Fig. 12(a) shows that the average inductor current and capacitor voltages are 7 A and 211 V, respectively, closely aligning with the theoretical values. Thereby, the peak amplitude of the two-level output voltage is also 211 V, as shown in Fig. 12(b). The filtered output voltage and output current are also shown in Fig. 12(b). Fig. 12(c) and (d) illustrates the voltage stress across the semiconductor devices. It is evident from the figure that the maximum voltage stress experienced by the switches does not exceed the rated output voltage. The slight deviation is due to the nonidealities of the inverter elements. By choosing optimal snubber elements for the proposed inverter, the switching transients and switching losses can be reduced. Finally, the proposed inverter has been tested under different load PF conditions, as depicted in Fig. 13. Experimental findings for the unity PF condition have been shown in Fig. 13(a), while Fig. 13(b) shows a 0.7 lagging PF condition. This indicates the ability of the inverter to meet the reactive power requirement of the load or grid.

C. Loss Analysis

A detailed analysis of the power loss has been carried out using the PLECS simulation software. For better insights, the inverter specifications are retained the same for the power loss analysis. A constant room temperature of 25 °C has been evaluated, and a heat sink has been applied uniformly to the inverter for thermal analysis. The junction temperature of the switches and diode under steady-state operating conditions has been shown in Fig. 14(a). The total power loss in the switches has been computed in PLECS based on the device specifications. The overall power loss of the switches has been shown in Fig. 14(b). Finally, the overall efficiency of the inverter at different load conditions has been shown in Fig. 14(c). The efficiency of the proposed inverter at the rated load is estimated to be 96.4%.

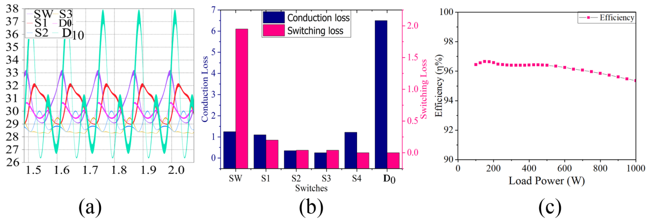


Fig. 14. Power loss and efficiency of the proposed inverter. (a) Thermal loss profile of the switches. (b) Switching and conduction loss profile of the switches. (c) Efficiency versus load power.

VII. CONCLUSION

This article discussed a four-switch CG-based single-phase current-fed boost inverter. It employs only four controlled active switches, one inductor, and one capacitor. The CG in the proposed inverter evicts the circulating current, and the increased voltage gain enables the inverter to function with a lower duty ratio and higher modulation index. Consequently, the voltage stress on the inverter elements is reduced, leading to a reduction in overall power losses. The results reveal that the input current is continuous, which is a merit for a PV-connected system. In addition, the symmetrical operation and utilization of a single dc capacitor in the inverter throughout both half cycles eliminate the injection of dc offset current into the grid. To emphasize the advantages of the proposed inverter, its features are compared with those of the recently reported grid-tied inverters. The dynamic response of the inverter in grid-connected mode has been validated with the OPAL-RT simulator. The thermal and power loss analyses have been carried out using PLECS simulation software. Finally, the analysis of the 400 W experimental prototype proves the viability of the proposed inverter.

APPENDIX

$$a_0 = -V_c LCC_f^2 L_f R,\ a_1 = LL_f C_f^2 R(1-d_1)(i_L + i_{L_f}) - LCL_f C_f,\ a_2 = L(1-d_1)(i_L + i_{L_f}) - L_f C_f^2 R V_C + V_C d_2^2 L_f C_f^2 R,\ a_3 = V_C(1 + d_2^2 L_f C_f)\ b_0 = L_f^2 C_f^2 LCR,\ b_1 = L_f^2 C_f LC,\ b_2 = L_f^2 C_f^2 R d_2^2 + (1-d_1)^2 L_f C_f^2 LR + L_f C_f LRC,\ b_3 = L_f C_f L(1-d_1)^2,\ b_4 = L_f^2 C_f d_2^2 + L_f C_f R d_2^2.$$

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