A Control to Address Issues of Synchronization and Voltage Rise in Grid Integrated Solar Photovoltaic-Battery Storage System

Gaurav Modi, *Member, IEEE*, and Bhim Singh, *Fellow, IEEE*

***Abstract*—This work presents a second-order generalized integrator (SOGI)-adaptive complex filter (ACF) based control with variable power mode to address synchronization and voltage rise issues in a grid integrated solar photovoltaic battery storage system. SOGI-ACF method is a fourth-order filter that resolves synchronization and power quality (PQ) issues by obtaining positive sequence components (PSCs) of unbalanced/distorted grid voltages. It has an excellent dynamic response with inherent dc offset, negative sequence rejection capabilities, and better harmonic rejection than other fourth-order generalized integrator-based filters. This algorithm is also used to acquire the load current's PSCs, incorporating multifunctional capability into system. In addition, the system provides grid support by restraining voltage rise at the point of common coupling during high solar photovoltaic array penetration into ac grid, according to the IEEE std 1547 limit. To provide grid support, the control strategy operates the system in variable power operating modes, depending upon system constraints, and accordingly regulates active and reactive powers of ac grid. Experimental results reveal restrain in voltage rise during peak generation and PQ improvement under unbalanced/ distorted grid voltage and load current conditions.**

***Index Terms*—Distorted-unbalanced voltage, overvoltage, solar photovoltaic system (SPV), synchronization, weak grid.**

ABBREVIATIONS

ACF	Adaptive complex filter.
BDDC	Bidirectional dc–dc converter.
BS	Battery storage.
BTC	Boost converter.
CDSC	Cascaded delay signal cancellation.
C-SOGI	Cascaded second-order generalized integrator.
GSPV	Grid integrated solar photovoltaic.
LV	Low voltage.
MAF	Moving average filter.
MPP	Maximum power point.
MPPT	Maximum power point tracking.
PCC	Point of common coupling.
PI	Proportional integral.
PLL	Phase locked loop.
PQ	Power quality.
PR	Proportional-resonant.
PSCs	Positive sequence components.
QT1-PLL	Quasi-type-1 phase-locked loop.
RET	Renewable energy technology.
SOGI	Second-order generalized integrator.
SPV	Solar photovoltaic.
UPF	Unity power factor.
VSC	Voltage source converter.
i_{Sa}, i_{Sb}, i_{Sc}	AC grid currents.
i_{La}, i_{Lb}, i_{Lc}	Load currents.
$i_{\mathrm{VSC}a}$, $i_{\mathrm{VSC}b}$, $i_{\mathrm{VSC}c}$	VSC currents.
I_B, V_B, $I_{\max}$, SOC, $\mathrm{SOC}_{\max}$	BS current, voltage, allowable maximum current. Charge status and maximum value of SOC.
v_{Sab}, v_{Sbc}, v_{Sca}	PCC line voltages.
v_{Sa}, v_{Sb}, v_{Sc}	PCC phase voltages.
V_{dc}, V_{dcr}	DC link voltage and its reference value.
I_{PV}, V_{PV}, P_{PV}	SPV array current, voltage, and power.
S_{rated}, S_{VSC}	Rated and estimated KVA rating of VSC.
V_{PCC}	Amplitude of PCC's phase voltage.
$V_{\max}$	Maximum allowable limit of V_{PCC}.
P_{STH}	Threshold feed-in grid power.
P_{SR}, Q_{SR}	Reference active and reactive powers for ac grid.
P_{BR}, I_{BR}	Reference BS powers and current.
P_S, P_L, P_{VSC}	Active power of ac grid, load, and VSC.
Q_S, Q_L, Q_{VSC}	Reactive power of ac grid, load, and VSC.

Received 18 June 2024; revised 18 August 2024; accepted 8 September 2024. Date of publication 12 September 2024; date of current version 12 December 2024. This work was supported in part by the Department of Science and Technology, Government of India, under project UKICERI, in part by the Department of Science and Technology, Government of India, under project SERI, and in part by the Department of Science and Technology, Government of India, under SERB National Science Chair Fellowship. Recommended for publication by Associate Editor F. Lin. *(Corresponding author: Gaurav Modi.)*

The authors are with the Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi 110016, India (e-mail: gaurav.modi@ee.iitd.ac.in; bsingh@ee.iitd.ac.in).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3459625.

Digital Object Identifier 10.1109/TPEL.2024.3459625

PV_M	Signal to control the operation of BTC.
I_{BC}	Controlling current parameter to estimate reference BS current.
ΔI_B	Current perturbation factor for I_{BC} estimation.
V_{PVR}	Reference SPV array voltage.
$i_{Sa}{}^*$, $i_{Sb}{}^*$, $i_{Sc}{}^*$	Sinusoidal reference ac grid currents.
$v_{S\alpha 1}{}^+$, $v_{S\beta 1}{}^+$	Estimated fundamental PSCs of PCC's phase voltages.
$i_{L\alpha 1}{}^+$, $i_{L\beta 1}{}^+$	Estimated fundamental PSCs of load current.
$H(s)_{SOGI}$ and $H(s)_{ACF}$	Transfer functions of SOGI and ACF algorithms.
k_1 and k_2	Gains of SOGI and ACF algorithms.
θ_{Se}	Estimated phase error.

I. Introduction

SPV has emerged as a prime RET, with least levelized costs than other RETs [1]. However, compared to conventional power plants and other major RETs such as wind and hydro, its efficiency is low, which is further affected by its nonlinear power-voltage aspect. Therefore, SPV array-based systems are associated with a tracking method, such as hill climbing or incremental and conductance, forcing SPV array to operate at its maximum efficiency [2]. In addition, SPV array is a highly inconsistent energy source due to the strong dependence of its output on solar irradiation. Therefore, to ensure power reliability, SPV systems are interfaced with power lines or associated with BS.

In recent years, a major drop in battery cost is observed. Due to this development, GSPV-BS-based systems have become more popular as they have provided improved control flexibility than GSPV system. Various structural designs are developed for GSPV-BS system in [3]. Here, different power converters for SPV array and BS, sharing a central power converter for power conversion-based design is adopted due to its merits over other structures [4].

However, many obstacles are faced in the integration of SPV system with power lines [5]. This work is concentrated on two issues, which are described as follows.

1) Issue of unsatisfactory PQ performance due to poor synchronization and local load harmonics, causing proliferation of substantial harmonics into power lines.
2) Issue of voltage rise at PCC during high SPV array penetration into ac grid, creating overvoltage challenges in system.

Therefore, limits have been defined by the IEEE std. 1547 [6] for GSPV system, to restrain voltage rise and limit flow of harmonics current in local grid.

A. Issue of Substandard Power Quality Performance

Most loads are designed to reduce power consumption with flexible control. However, these loads are nonlinear, drawing substantial harmonics. These harmonics give rise to unbalanced and distorted voltage issues, especially in LV or distribution grid [7]. When an SPV system is integrated into such a polluted power network, it undergoes substandard power quality performance, generating harmonics currents [8], as conventional algorithms fail to operate satisfactorily [9]. In addition, if these nonlinear local loads are coupled at PCC of GSPV system, its PQ performance is further degraded [10]. Therefore, algorithms are designed to address these issues, where sensed signals are filtered using a superior filter method to remove undesirable harmonics components. These filtered signals are used to govern system's response. However, performance of these designed controls is highly influenced by characteristics of used filter technique, where high attenuation to unwanted harmonics components, fast dynamic response, ease of real-time implementation, and low computation burden are desired attributes.

Some famous techniques are SOGI [11] and signal delay-based methods such as CDSC and MAF methods [12]. SOGI method is one of the simplest techniques reported in the literature, with a small computation burden and ease of execution. Though, it offers little attenuation to dominant 3rd-, 5th-, and 7th-order harmonics and does not offer any dc offset reduction to its quadrature component. Hence, its advanced forms such as C-SOGI method are developed to remove its shortcomings [13], [14]. In contrast, CDSC and MAF methods provide superior attenuation to both low-order and high-order harmonics. However, they have relatively high computation complexity due to requirement of a large number of delays in their operation. In addition, their real-time implementation is somewhat tricky as their delay length depends on input signal frequency and sampling frequency (f_{samp}) [15]. Hence, advanced methods such as extended-CDSC [16] and SOGI-MAF [17] are designed to address issues of large delay length.

This work presents a simple technique to filter sensed signal. In this technique, sensed distorted/ unbalanced signal is first passed through SOGI block, followed by ACF block [18]. Here, SOGI algorithm provides dc offset elimination and limited attenuation to harmonic components. Then, ACF offers further attenuation, enhancing overall harmonics rejection capability and directly estimating signal's PSCs. In addition, in this work, a QT1-PLL structure is adopted to make designed filter frequency adaptive. QT1-PLL is selected over conventional PLL, as it offers high response speed and less complexity [19].

B. Issue of Voltage Rise at Point of Common Coupling

A voltage rise is experienced at PCC due to feed-in power from SPV system to local grid. It is a result of a reverse voltage drop across power lines impedance. If this rise crosses maximum acceptable limit (V_{max}), connected load and system can be damaged due to overvoltage. Therefore, provision is provided in GSPV system, where controller shuts down operation if overvoltage is detected, causing loss of generation [20]. As a result, methods are presented based on active [21] and reactive [22] powers to restrain voltage rise, having their advantages and limitations.

In active power-based methods, feed-in power to grid is limited by derating SPV, causing a drop in system efficiency

and financial loss [21]. In [23], SPV array continues to yield maximum power, and excess generation is delivered to BS to restrict voltage rise. Since BS capacity is limited, there may be a case that BS gets overcharged. Moreover, these methods are based on threshold feed-in grid power (P_{STH}) above which, voltage rise becomes more than $V_{\max}$. However, estimation of P_{STH} is cumbersome as it depends upon network configuration. Tewari et al. [24] have presented, an on-load tap changing (OLTC) transformer and BS-based hybrid method to address limited BS size issue. Moreover, to avoid estimation of P_{STH}, they have used PI regulator to govern BS power according to rise in PCC voltage. However, OLTC increases the system's overall cost. In addition, PI regulator causes issues of saturation and large overshoot in BS power.

In reactive power-based methods, voltage rise is restrained by injecting reactive power into grid, using unutilized capacity of SPV system's power converter [25]. This method has benefits if feeder impedance has a low *R/X* ratio, like in a high-voltage ac grid. However, in a LV grid, such as a distribution grid, feeder has a high value of *R/X* ratio. Hence, a sizable amount of reactive power is required, which is constrained by converter rating [22]. In addition, grid works at a low power factor, causing higher line losses [26]. Therefore, coordinated active and reactive power-controlled method is presented to address these limitations [27].

On summarizing above literature review, it is observed that active power-based method has advantages over reactive power-based methods, especially for a LV or distribution grid, which is considered in this work. However, active power-based methods have their limitation due to limited BS size and other constraints. Therefore, in this work, a variable power mode strategy is presented to address this voltage rise issue. Here, grid's active or reactive power or both are regulated, according to constraints of system, such as BS charge status (*SOC*), allowable maximum BS current ($I_{\max}$), and rating of power converter (S_{rated}). However, priority is given to active power control.

C. Main Contributions and Structure of Paper

This work presents a SOGI-ACF-controlled GSPV-BS system with a variable power mode operation strategy to limit PCC voltage rise and PQ improvement. Presented SOGI-ACF algorithm and designed variable power mode approach have following merits.

1) SOGI-ACF algorithm functions as a 4th-order bandpass filter (BPF), providing superior harmonic rejection and dynamic response compared to C-SOGI method, which also features a 4th-order BPF. Detailed analysis reveals that SOGI-ACF filter offers better attenuation of dominant harmonic components, such as 3rd, 5th, and 7th harmonics, leading to improved harmonic rejection. Dynamic response analysis shows that SOGI-ACF filter exhibits less overshoot in estimated frequency and phase angle during sudden phase angle or frequency changes, as well as lower settling time values and reduced execution time. Another advantage of SOGI-ACF is its avoidance of frequency-dependent delay blocks, like those in MAF and CDSC methods, facilitating easier real-time application. However, SOGI-ACF filter's complexity is higher than C-SOGI method due to complex control gain of ACF [28], which poses challenges for real-time implementation. To address this, modifications using simple trigonometric analysis are made. As a result, SOGI-ACF filter offers superior performance compared to C-SOGI algorithm without added complexity and real-time implementation issues.
2) Compared to existing control strategy, proposed approach activates only when PCC voltage amplitude (V_{PCC}) exceeds maximum allowable limit ($V_{\max}$). When V_{PCC} is below $V_{\max}$, grid operates at a UPF to reduce feeder losses, maintaining grid power factor (pf) at unity. In this mode, grid's active power is regulated according to load demand and SPV array power. If V_{PCC} exceeds $V_{\max}$, priority shifts to active power control, with excess generation diverted to BS to keep V_{PCC} within limit, provided BS constraints are not violated. This prevents power losses in power line and converter due to reactive power injection. To regulate BS power and maintain V_{PCC} within allowable limit, a simple perturbation-based strategy is employed, which does not require P_{STH} estimation and a PI regulator. If BS constraints are violated, both active and reactive powers are adjusted according to system constraints. In this scenario, same perturbation-based strategy is used to control reactive power, eliminating need for a PI regulator. This simplification makes proposed approach more straightforward and effective than existing methods.

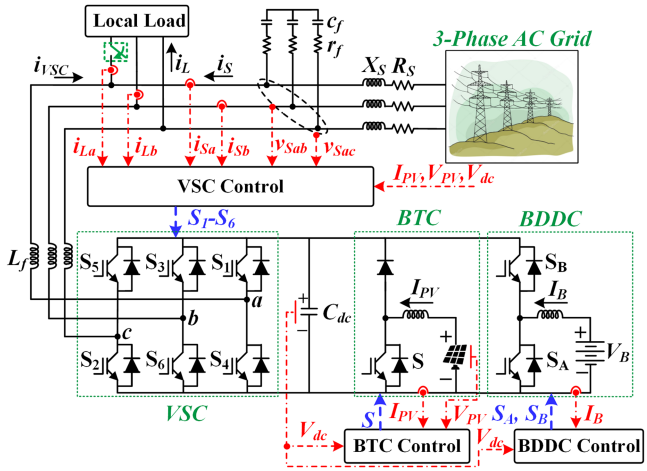

Fig. 1. Layout of GSPV-BS system.

The rest of this article is organized as follows: Section II illustrates structure of GSPV-BS system, while Section III explains control strategy. Section IV analyzes the performance of SOGI-ACF algorithm and compares it with the C-SOGI method. Section V presents test results demonstrating containment of PCC voltage rise during peak generation and improvements in power quality under unbalanced and distorted grid voltage and load current conditions. Finally, Section VI concludes this article and discusses the limitations of presented work.

II. Layout of GSPV-BS System

System layout is illustrated in Fig. 1, where red dotted lines indicate sensed signals. SPV array and BS are connected to dc

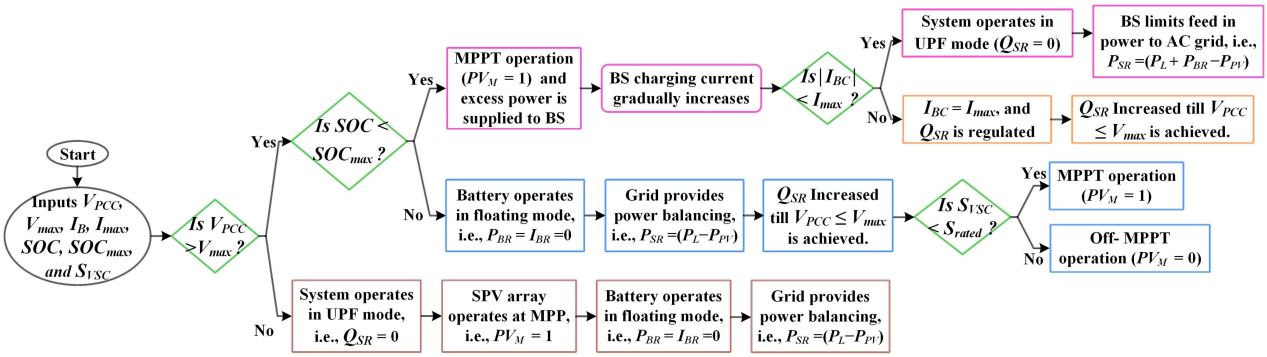

Fig. 2. Flowchart to determine system operating conditions and different control modes.

link ($C_{\rm dc}$) of central power converter (a voltage source converter VSC) through their respective power converters. A major advantage of this configuration is that dc-link voltage ($V_{\rm dc}$) becomes independent of BS voltage (V_B) and SPV array voltage ($V_{\rm PV}$). Hence, an adaptive dc link voltage strategy can be adopted to reduce system's losses [29]. Boost converter (BTC) is responsible for regulating SPV array generation, while BDDC controls $V_{\rm dc}$ at estimated reference value (V_{dcr}). Main VSC administers feed-in active and reactive power to ac grid and regulates BS power to achieve set objectives. A high-pass filter (*rc* filter) is placed before grid voltage sensors to reduce effect of switching ripples on sensed voltage signal. Additionally, a breaker (knife switch) is connected in series with phase "a" load (green dotted line) to analyze system's behavior under single-phase loading or sudden reduction in load demand conditions.

III. Designed Control Strategy

This section explains developed scheme to control power converters of GSPV-BS system. First, designed variable power mode strategy is described, establishing reference powers to control central power converter or VSC. Then, estimation of gating pulses for BTC, BDDC, and VSC is explained.

A. Determination of Reference Powers Using Designed Approach

As discussed, designed approach regulates grid's active or reactive power, or both, according to various system constraints such as *SOC*, $I_{\rm max}$, and $S_{\rm rated}$, to limit voltage rise. Additionally, it controls system's operation only when $V_{\rm PCC} > V_{\rm max}$ is detected. Hence, based on $V_{\rm PCC}$, SOC, $I_{\rm max}$, and $S_{\rm rated}$ values, reference active and reactive powers for grid (P_{SR}, Q_{SR}) are determined. A flowchart is shown in Fig. 2 to identify the system's operating conditions based on these constraints. Here, three cases are defined based on the system's constraints.

1) Case-I: $\rm V_{PCC} < V_{max}$*:* In this case, control strategy does not regulate grid's powers, and system operates like a regular GSPV system, *i.e.,* SPV array works at MPP ($PV_M = 1$), reference BS power or current is zero ($P_{BR} = I_{BR} = 0$), and grid operates at UPF ($Q_S = 0$) [4]. Thus, grid's reference active and reactive powers (P_{SR}, Q_{SR}) are assessed as follows:

$$\underbrace{P_{SR} = P_L - P_{\rm PV}}_{\text{Grid } Provides\ Power\ Balancing}, \underbrace{P_{BR} = I_{BR} = 0}_{\text{Floating } Mode}, \underbrace{\rm P_{PV}{}_M = 1}_{\text{MPP } Operation} \quad (1)$$

$$\underbrace{Q_{SR} = 0}_{\text{UPF } Mode}, \ \& \ \underbrace{Q_{\rm VSC} = Q_L}_{\text{VSC } Compensated\ for\ Load\ Reactive\ Power}. \quad (2)$$

Here, $P_{\rm PV}$ and P_L represent SPV array and load active power, respectively, while $Q_{\rm VSC}$ and Q_L denote VSC and load reactive power. $\rm PV_M$ controls BTC operation: if it is one, MPPT operation is activated; otherwise, off-MPPT operation is used.

2) Case-II: $\rm V_{PCC} > V_{max}$ *&& SOC* $<$ SOC_{max}*:* If $V_{\rm PCC} > V_{\rm max}$ is detected, then controller takes action to restrict $V_{\rm PCC}$ value below $V_{\rm max}$. It first checks BS charge status (*SOC*), and if $\rm SOC < SOC_{max}$ is detected, then surplus generation is delivered to BS. Here, $\rm SOC_{max}$ is upper limit of SOC, set to protect BS from being overcharged.

In these situations, SPV array is operated at MPP ($\rm PV_M = 1$), and excess generation is transferred to the BS. This is achieved by gradually increasing controlling current parameter I_{BC} using a perturbation method until $V_{\rm PCC} \le V_{\rm max}$ is achieved. Expression to determine $I_{\rm BC}$ is given as follows:

$$I_{BC}(k+1) = \left\langle \begin{matrix} I_{BC}(k) + \Delta I_B, & \text{if } V_{\rm PCC} > V_{\rm max} \\ 0, & \text{otherwise} \end{matrix} \right| \begin{matrix} I_{BC}(k) > 0 \\ \Delta I_B > 0 \end{matrix}. \quad (3)$$

Here, ΔI_B is current perturbation, a percentage of $I_{\rm max}$. Using I_{BC}, reference BS power (P_{BR}) is determined, which is used to regulate P_{SR}. However, there can be a situation where I_{BC} exceeds $I_{\rm max}$, violating BS's current constraint. Hence, two sub\cases are formed.

a) When $\rm I_{BC} < I_{max}$*:* In this case, grid operates at UPF and BS regulates P_{SR} until $V_{\rm PCC} \le V_{\rm max}$ is achieved. Thus, P_{SR} and Q_{SR} are calculated as follows:

$$\underbrace{P_{SR} = P_L + P_{BR} - P_{\rm PV}}_{\text{BS } Regulates\ Grid\ Power}, \underbrace{P_{BR} < 0, |P_{BR}| = |V_B \times I_{BC}|}_{\text{BS Charging Power}} \quad (4)$$

$$\underbrace{Q_{SR} = 0}_{\text{UPF } Mode}, \ \& \ \underbrace{Q_{\rm VSC} = Q_L}_{\text{VSC } Compensated\ for\ Load\ Reactive\ Power}. \quad (5)$$

Here, V_B denotes voltage of BS.

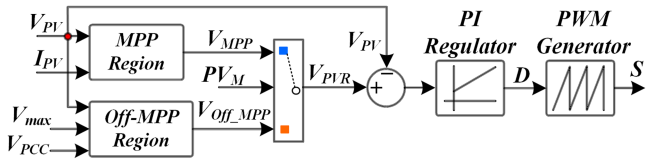

Fig. 3. Control strategy for BTC.

b) When $\mathrm{I_{BC}} > \mathrm{I}_{max}$*:* In this case, the controller limits I_{BC} at $I_{\max}$ to protect BS from overheating, and remaining surplus power is delivered at PCC. Moreover, controller regulates ac grid's reactive power (Q_s) by gradually increasing Q_{SR} until $V_{\mathrm{PCC}} \leq V_{\max}$ is achieved. Here, VSC and load together behave as an inductive load and draw reactive power from AC grid, causing grid to operate at a lagging power factor P_{SR} and Q_{SR} are calculated as follows:

$$\underbrace{P_{SR} = P_L + P_{BR} - P_{\mathrm{PV}}}_{\text{BS } Regulates\ Grid\ Power},\ \underbrace{P_{BR} < 0, |P_{BR}| = |V_B \times I_{\max}|}_{\text{BS } Charging\ Power} \tag{6}$$

$$Q_{SR}(k+1) = \left\langle \begin{matrix} Q_{SR}(k) + \Delta Q_S, & \text{if } V_{\mathrm{PCC}} > V_{\max} \\ 0, & \text{otherwise} \end{matrix} \right| \begin{matrix} Q_{SR}(k) > 0 \\ \Delta Q_S > 0 \end{matrix}. \tag{7}$$

3) Case-III: $\mathrm{V}_{PCC} > \mathrm{V}_{max}$ *&& SOC* $\approx$ *SOC*$_{max}$*:* In this case, excess power cannot be supplied to BS to prevent it from overcharging. Hence, P_{BR} is kept at zero ($P_{BR} = 0$), while Q_{SR} gradually increases until $V_{\mathrm{PCC}} \leq V_{\max}$ is achieved. In this case, P_{SR} and Q_{SR} are calculated as follows:

$$\underbrace{P_{SR} = P_L - P_{\mathrm{PV}}}_{\text{Grid } Provides\ Power\ Balancing},\ \underbrace{P_{BR} = I_{BR} = 0}_{\text{Floating } Mode},\ \underbrace{\mathrm{P}_{PVM} = 1}_{\text{MPP } Operation} \tag{8}$$

$$Q_{SR}(k+1) = \left\langle \begin{matrix} Q_{SR}(k) + \Delta Q_S, & \text{if } V_{\mathrm{PCC}} > V_{\max} \\ 0, & \text{otherwise} \end{matrix} \right| \begin{matrix} Q_{SR}(k) > 0 \\ \Delta Q_S > 0 \end{matrix}. \tag{9}$$

However, there can be a case when required reactive power to maintain $V_{\mathrm{PCC}} \leq V_{\max}$ becomes substantial, causing VSC to become overloaded ($S_{\mathrm{VSC}} > S_{\mathrm{rated}}$). Therefore, two subcases are created to protect VSC from being overloaded.

a) When $\mathrm{S}_{VSC} < \mathrm{S}_{rated}$*:* In this case, system operates in MPP region ($\mathrm{PV}_M = 1$) and generates maximum power.

b) When $\mathrm{S}_{VSC} > \mathrm{S}_{rated}$*:* In this case, SPV array generation is gradually reduced by operating it in off-MPP region ($\mathrm{PV}_M = 0$) until S_{VSC} becomes less than S_{rated} ($S_{\mathrm{VSC}} \leq S_{\mathrm{rated}}$).

B. Estimation of Gating Pulses for BTC (S)

Control scheme to estimate gating pulses for BTC is disclosed in Fig. 3. As discussed, BTC manages SPV array power (P_{PV}) by controlling its voltage (V_{PV}) either at its MPP or in off-MPP region based on PV_M signal status. Hence, reference SPV array voltage (V_{PVR}) is determined based on operating conditions.

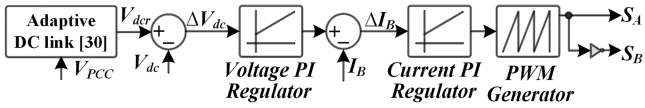

Fig. 4. Control strategy for BDDC.

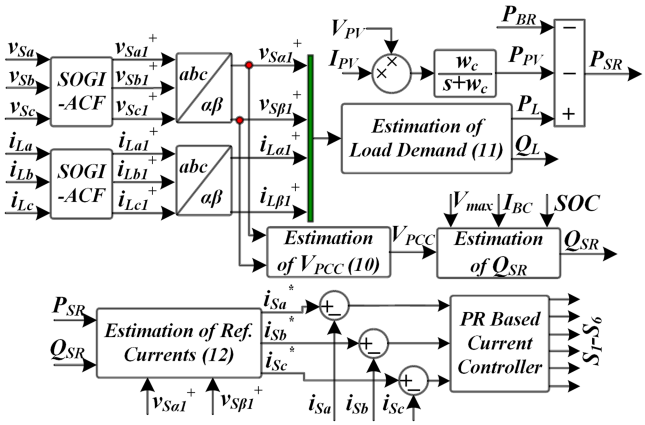

Fig. 5. Control strategy for VSC.

Assessed V_{PVR} and sensed V_{PV} are used to find gating pulses for BTC (S) using a PI regulator and pulsewidth modulation generator, as depicted in Fig. 3.

C. Estimation of Gating Pulses for BDDC ($\mathrm{S_A}$, $\mathrm{S_B}$)

As discussed above, BDDC governs V_{dc} at reference value V_{dcr}, calculated using an adaptive dc link approach for reduced converter losses [29]. Fig. 4 reveals control scheme to estimate switching signals S_A and S_B for BDDC. It is a double-loop control scheme, where outer loop regulates V_{dc} and determines set point for inner loop controller. Meanwhile, inner loop operates as a secondary controller and controls BS current. In [30], controller design and procedure to determine compensator parameters are briefly discussed.

D. Estimation of Gating Pulses for VSC (S_1–S_6)

VSC controls ac grid's active (P_S) and reactive power (Q_S) according to calculated references (P_{SR}, Q_{SR}) in (1)–(9). Additionally, it compensates for local load harmonics. To achieve these objectives, sinusoidal reference currents ($i_{Sa}{}^*$, $i_{Sb}{}^*$, $i_{Sc}{}^*$) are calculated, and gating pulses (S_1–S_6) are generated using an indirect current control approach, as shown in Fig. 5.

Information on V_{PCC}, P_L, and Q_L is required to generate S_1–S_6. Since grid voltages and load currents have harmonics and are unbalanced, estimated V_{PCC}, θ_{PCC}, P_L, and Q_L contain 2kth (k $\in N$) order ripples, deteriorating system's PQ performance. Hence, sensed voltages (v_{Sab}, v_{Sac}) and currents (i_{La}, i_{Lb}) are processed first using SOGI-ACF algorithm, and their PSCs ($v_{S\alpha 1}{}^+$, $v_{S\beta 1}{}^+$) and ($i_{L\alpha 1}{}^+$, $i_{L\beta 1}{}^+$) are determined. From estimated PSCs, V_{PCC}, P_L, and Q_L are calculated as follows:

$$V_{\mathrm{PCC}} = \left| \sqrt{(v_{S\alpha 1}{}^+)^2 + (v_{S\beta 1}{}^+)^2} \right| \tag{10}$$

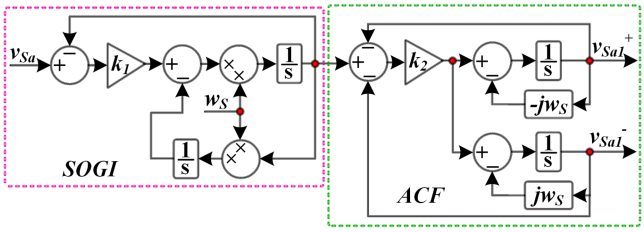

Fig. 6. Structure of SOGI-ACF algorithm.

$$\begin{bmatrix} P_L \\ Q_L \end{bmatrix} = \begin{bmatrix} {v_{S\alpha 1}}^+ & {v_{S\beta 1}}^+ \\ -{v_{S\beta 1}}^+ & {v_{S\alpha 1}}^+ \end{bmatrix} \begin{bmatrix} {i_{L\alpha 1}}^+ \\ {i_{L\beta 1}}^+ \end{bmatrix}. \tag{11}$$

Now, P_{SR}, and Q_{SR} are determined using estimated P_L, Q_L, V_{PCC}, and (1)–(9), followed by estimation of reference currents using inverse Clarke transformation matrix.

$$\begin{bmatrix} {i_{Sa}}^* \\ {i_{Sb}}^* \\ {i_{Sc}}^* \end{bmatrix} = \sqrt{\frac{1}{6}} \begin{bmatrix} 2 & 0 \\ -1 & \sqrt{3} \\ -1 & -\sqrt{3} \end{bmatrix} \begin{bmatrix} {v_{S\alpha 1}}^+ & {v_{S\beta 1}}^+ \\ -{v_{S\beta 1}}^+ & {v_{S\alpha 1}}^+ \end{bmatrix}^{-1} \begin{bmatrix} P_{SR} \\ Q_{SR} \end{bmatrix}. \tag{12}$$

Now, using these estimated currents ${i_{Sa}}^*$, ${i_{Sb}}^*$, ${i_{Sc}}^*$) and sensed ac grid currents (i_{Sa}, i_{Sb}, i_{Sc}), S_1–S_6 are generated. Here, a PR regulator is used to track sensed ac grid currents with estimated reference currents. Guidelines for finding PR regulator parameters are provided in [31].

IV. Analysis of SOGI-ACF Algorithm

This work filters sensed PCC voltage and load currents using introduced SOGI-ACF algorithm. Fig. 6 shows the structure of designed algorithm, where the input signal is first passed through SOGI block, followed by ACF block. Its transfer function *H(s)* is given as follows:

$$H(s) = {v_{Sa1}}^+ / v_{Sa} = H(s)_{\mathrm{SOGI}} \times H(s)_{\mathrm{ACF}}$$

$$H(s)_{\mathrm{SOGI}} = \frac{k_1 w_S s}{s^2 + k_1 w_S s + {w_S}^2}; H(s)_{\mathrm{ACF}} = \frac{k_2 (s + j w_S)}{s^2 + 2k_2 s + {w_S}^2}. \tag{13}$$

Here, $H(s)_{\mathrm{SOGI}}$ and $H(s)_{\mathrm{ACF}}$ are transfer functions of SOGI and ACF algorithms, respectively, and k_1 and k_2 are their gains, controlling their response. w_S is the ac grid voltage frequency, determined using QT1-PLL structure [19]. Fig. 6 shows that complex gain is used in ACF, increasing filter complexity. Therefore, modifications are made to address issue of complex gain. Using trigonometric analysis, terms $-j{v_{Sa1}}^+$ and $j{v_{Sa1}}^-$ can be written as follows:

$$-j{v_{Sa1}}^+ = \frac{({v_{Sa1}}^+ + 2{v_{Sb1}}^+)}{\sqrt{3}}; j{v_{Sa1}}^- = \frac{({v_{Sa1}}^- + 2{v_{Sb1}}^-)}{\sqrt{3}}. \tag{14}$$

Similarly, for phase "b," $-j{v_{Sb1}}^+$ and $j{v_{Sb1}}^-$ can be written as follows:

$$-j{v_{Sb1}}^+ = \frac{-({2v_{Sa1}}^+ + {v_{Sb1}}^+)}{\sqrt{3}};$$
$$j{v_{Sb1}}^- = \frac{-({2v_{Sa1}}^- + {v_{Sb1}}^-)}{\sqrt{3}}. \tag{15}$$

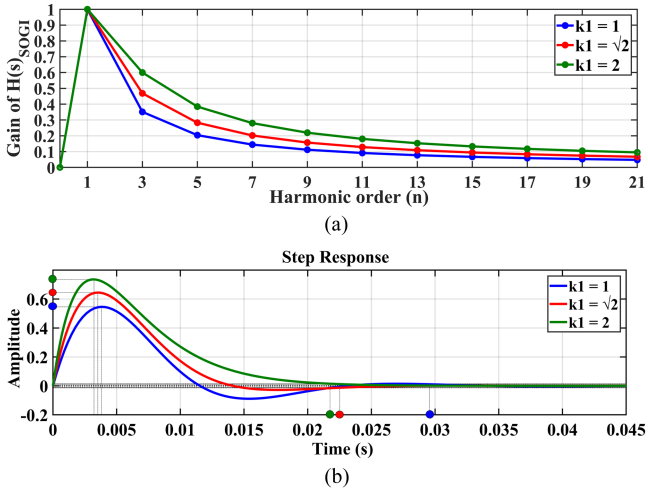

Fig. 7. (a) Plot of $|H(s)_{SOGI}|$ and n (b) step response of SOGI algorithm.

After estimating PSC and NSC of phases "a" and "b," PSC and NSC of phase "c" are directly estimated as follows:

$${v_{Sc1}}^+ = -\left({v_{Sa1}}^+ + {v_{Sb1}}^+\right); {v_{Sc1}}^- = -\left({v_{Sa1}}^- + {v_{Sb1}}^-\right). \tag{16}$$

Thus, designed SOGI-ACF algorithm is applied to only two phases, reducing its complexity [32]. Since transfer functions $H(s)_{\mathrm{SOGI}}$ and $H(s)_{\mathrm{ACF}}$ govern behavior of SOGI-ACF filter, transfer functions of SOGI and ACF are examined first to analyze filtering capability of SOGI-ACF.

A. Analysis of $\mathrm{H(s)}_{SOGI}$ and $\mathrm{Q(s)}_{SOGI}$ and Selection of k_1

Attenuation and phase shift provided by SOGI algorithm to dc offset, fundamental component, and other harmonic components are estimated as follows:

$$|H(s)_{\mathrm{SOGI}}(s = jnw))| = \frac{k_1 w_S (nw)}{\left[\left({w_S}^2 - n^2 w^2\right)^2 + \left(k_1 w_S nw\right)^2\right]^{0.5}} \tag{17}$$

$$\angle H(s)_{\mathrm{SOGI}}(s = jnw) = \frac{\pi}{2} - \tan^{-1}\frac{k_1 nw}{{w_S}^2 - n^2 w^2}. \tag{18}$$

It is observed that for $n = 0$ (dc offset), SOGI provides zero gain, eliminating dc offset entirely from sensed signal. From (17)-(18), it is noted that SOGI provides desirable unity gain and zero phase shift to fundamental component ($n = 1$), when signal frequency matches estimated frequency ($w = w_S$). However, attenuation provided to harmonic components ($n > 1$) depends on k_1. Fig. 7(a) plots curve between $|H(s)_{\mathrm{SOGI}}|$ and n for different values of k_1. Meanwhile, Fig. 7(b) shows step response of SOGI algorithm, revealing required settling time (t_s) for different values of k_1. It is observed that as k_1 increases, harmonic rejection capability of SOGI decreases. In contrast, a lower value of k_1 degrades response speed. Considering both harmonic rejection and response speed, $k_1 = 1.414$ is chosen in this work.

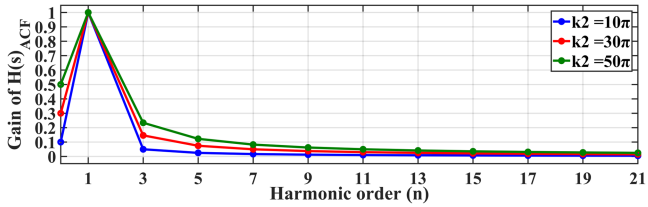

Fig. 8. Plot between $|H(s)_{ACF}|$ and n for different values of k_2.

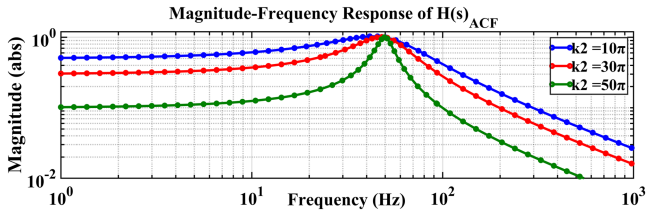

Fig. 9. Magnitude frequency response of ACF for different values of k_2.

B. Analysis of $\mathrm{H(s)}_{ACF}$ and Selection of k_2

In Fig. 7, it can be observed that gain provided by SOGI algorithm to dominant 3rd, 5th, and 7th harmonics is more than 0.2, causing poor harmonic rejection. Therefore, output of SOGI filter is fed to ACF to enhance overall harmonic rejection capability. Attenuation and phase shift provided by it can be estimated by the following expression:

$$|H(s)_{\mathrm{ACF}}(s=jnw))| = \frac{k_2\left(w_S+w\right)}{\left[\left(w_S{}^2-n^2w^2\right)^2+\left(2k_2nw\right)^2\right]^{0.5}} \tag{19}$$

$$\angle H(s)_{\mathrm{ACF}}(s=jnw) = \frac{\pi}{2}-\tan^{-1}\frac{2k_2nw}{w_S{}^2-n^2w^2}. \tag{20}$$

In (19) and (20), it is observed that when $w = w_S$, ACF provides unity gain and zero phase shift to fundamental component. Hence, SOGI-ACF provides unity gain and zero degrees phase shift to fundamental component, which is an essential characteristic of a filter algorithm. For further analysis, curves of $|H(s)_{\mathrm{ACF}}|$ and n and magnitude-frequency response of $H(s)_{\mathrm{ACF}}$ are plotted for different values of k_2, as shown in Figs. 8 and 9. Following points are observed.

1) Filtering capability of ACF reduces as k_2 increases. Moreover, its filtering capability is better than SOGI. However, attenuation provided to 3rd and 5th harmonics is insufficient. Therefore, a cascaded SOGI-ACF filter provides superior harmonic rejection capability.
2) ACF has limited dc offset rejection capability, making it unsuitable when input has dc offset, usually present due to offset in sensing circuitry. Since SOGI algorithm eliminates dc offset from input signal, SOGI-ACF filter's performance is not affected by dc offset.
3) In Fig. 9, it is observed that bandwidth of ACF decreases as k_2 decreases. Therefore, a lower value of k_2 degrades dynamic response. Hence, $k_2 = 50\ \pi$ is selected.

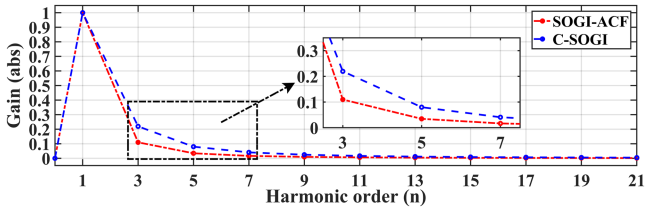

Fig. 10. Comparison of harmonic rejection capability of SOGI-ACF and C-SOGI methods.

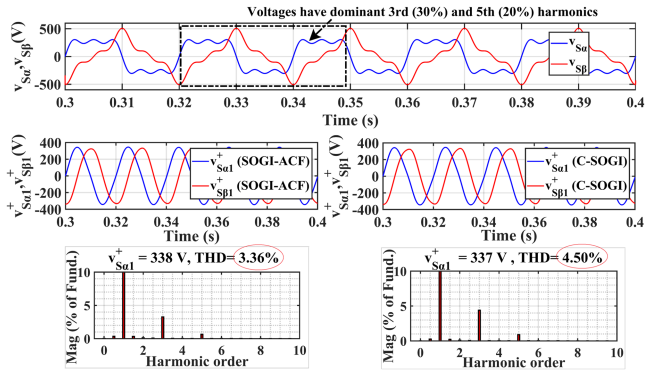

Fig. 11. Obtained PSCs by SOGI-ACF and C-SOGI methods.

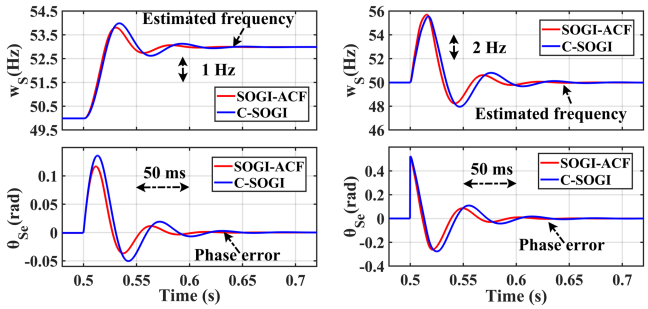

Fig. 12. Dynamic performance of SOGI-ACF and C-SOGI methods under a step change of (a) +3 Hz in grid voltage frequency and (b) +30° in phase angle.

4) $H(s)_{\mathrm{ACF}}$ becomes zero when $s = -jw_S$ is substituted in (13). Therefore, ACF output is free from negative sequence components and directly gives PSC of sensed signal.

C. Comparison of SOGI-ACF and C-SOGI Methods

Fig. 10 reveals attenuation provided by SOGI-ACF and C-SOGI methods to harmonic components. It is observed that presented algorithm offers greater rejection of dominant 3rd, 5th, and 7th harmonics compared to C-SOGI technique, thereby improving performance of GSPV system under distorted grid voltages and load currents. Fig. 11 shows obtained PSCs of distorted grid voltages by SOGI-ACF and C-SOGI algorithms. Obtained PSC and its THD value further validate proposed algorithm's superiority in harmonic rejection capability.

Fig. 12 shows estimated frequency and phase error (θ_{Se}) during a step change of +3 Hz in frequency and +30° in phase

TABLE I
SUMMARY OF SOGI-ACF AND C-SOGI ALGORITHMS PERFORMANCE

Conditions	SOGI-ACF Algorithm	C-SOGI Algorithm
Attenuation Provided to Dominant Harmonics		
3rd Harmonic	89.03%	78.05%
5th Harmonic	96.54%	92.01%
7th Harmonic	98.33%	95.92%
THD Value of obtained PSC	3.36%	4.50%
+3 Hz Frequency Jump		
2% Settling Time	≈ 5 Cycles	≈ 6.7 Cycles
Frequency Overshoot	0.8 Hz (1.6%)	0.98 Hz (1.96%)
Phase Overshoot	6.7°	7.79°
+30° Phase Jump		
2% Settling Time	≈ 5.2 Cycles	≈ 6.8 Cycles
Frequency Overshoot	5.7 Hz	5.6 Hz
Phase Overshoot	15.05° (50.17%)	15.87° (52.90%)
Execution Time	7.95 μs	8.04 μs

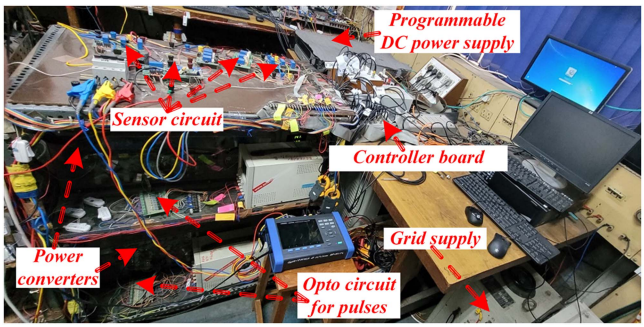

Fig. 13. Developed test bench of GSPV-BS system.

angle. θ_{Se} with designed SOGI-ACF algorithm settles to zero faster than with C-SOGI algorithm. Furthermore, there is less overshoot with developed algorithm in estimated frequency and phase error. Table I provides an analysis of SOGI-ACF and C-SOGI algorithms, including their required execution times for implementation. It is observed that both algorithms have almost same execution time; however, the performance of SOGI-ACF algorithm is superior to C-SOGI filter.

V. TEST PERFORMANCE OF GSPV-BS SYSTEM

To demonstrate and validate the performance of designed SOGI-ACF algorithm and control strategy, it is implemented on a test bench setup of a GSPV-BS system developed for 220 V, 50 Hz ac grid voltage. The built test bench setup is shown in Fig. 13. It is assembled with help of a programmable dc power supply (ETS600X17D-PVF), lead-acid battery bank, IGBT switches-based converter, Hall-Effect-based sensors, and PPC controller board (DS1103). Parameters of battery bank, programmable power supply, and other components used for experimental analysis are stated in Table II.

A. Performance of Designed SOGI-ACF Algorithm

Before inspecting power quality performance and issue of PCC voltage rise, performance of designed SOGI-ACF filter

TABLE II
PARAMETERS OF TEST BENCH SETUP

	Symbol	Values
Local Grid	V_{rated}, V_{PCCr}, w_{Sr}	220 V, 179.63 V, 50 Hz
SPV Array	V_{oc}, I_{sc}	400 V, 14 A
Battery Storage	V_{BN}, CH_B, $SOC_{\max}$, $I_{\max}$	240 V, 42 AH, 90%, 8.4 A, 0.084 A
Power Converter	S_{VSC}	5.5 kVA
DC Link	V_{dc}, C_{dc}	400 V, 1200 μF
Ripple Filter	r_f, c_f	5 Ω, 5 μF
Interfacing Inductor	L_f	2.0 mH
Filter's Gain	k_1, k_2	$\sqrt{2}$, 50π
PR Controller	k_{pr}, k_{ir}	0.5, 5
Perturbation Factors	ΔI_B, ΔQ_S	0.084 A, 5 VAR
Sampling Time	T_{samp}	30 μs

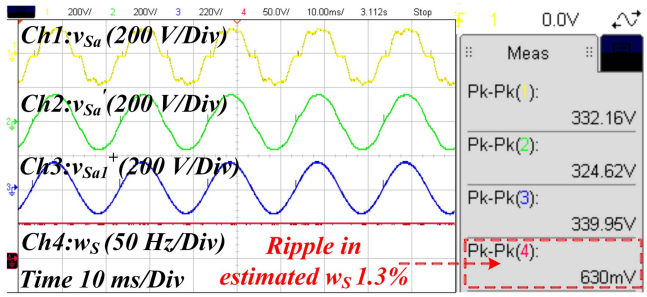

Fig. 14. Internal signals of SOGI-ACF algorithm.

is examined by reviewing its internal signals and THD value of obtained PSC. Fig. 14 shows internal signals of filter for distorted ac grid voltage (v_{Sa}). It is observed that output of filter's first stage ($v_{Sa}{}'$) is distorted, which is anticipated due to limited filtering capability of SOGI. However, output of filter's second stage ($v_{Sa1}{}^+$) is almost sinusoidal and free from distortion. Fig. 14 also reveals estimated grid frequency (w_S). It is observed that estimated w_S is almost constant with a peak-to-peak ripple of 630 mV (1.3%), which is significantly low. Hence, when this filter voltage and frequency are used to control GSPV-BS system, its power quality performance is not expected to be affected.

Fig. 15 demonstrates PSCs of load currents ($i_{L\alpha 1}{}^+$, $i_{L\beta 1}{}^+$) using SOGI-ACF and C-SOGI methods for both balanced and unbalanced loads, with their THD values. It is observed that THD values of obtained PSC from SOGI-ACF algorithm are relatively lower than THD value of obtained PSC from C-SOGI method, confirming superior filtering of SOGI-ACF algorithm.

B. Power Quality Performance of GSPV-BS System Without and With Compensation of Local Load Currents Harmonics

Connected local loads at PCC draw power from the supply. When these loads draw distorted currents, harmonic currents are injected into grid. This results in distorted grid currents, which further exacerbates the harmonic distortion of the already distorted PCC voltages. Fig. 16 illustrates this phenomenon. So, even if GSPV system injects purely sinusoidal currents, overall system's PQ performance remains suboptimal due to harmonic currents from local loads. Fig. 16(a) and (b) clearly demonstrate

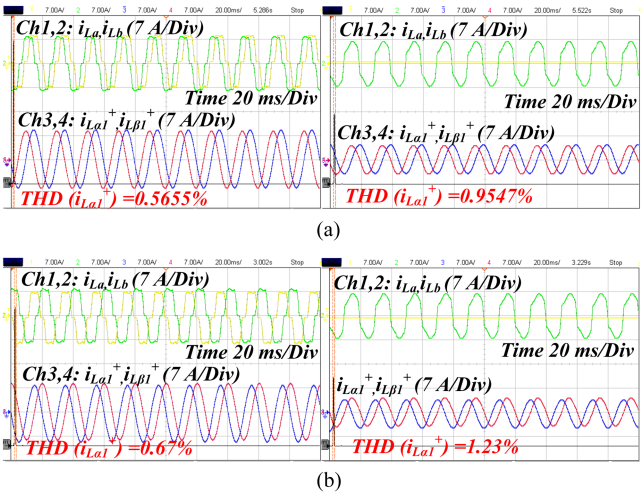

Fig. 15. Obtained PSCs for balanced and unbalanced load currents using (a) SOGI-ACF and (b) C-SOGI algorithms.

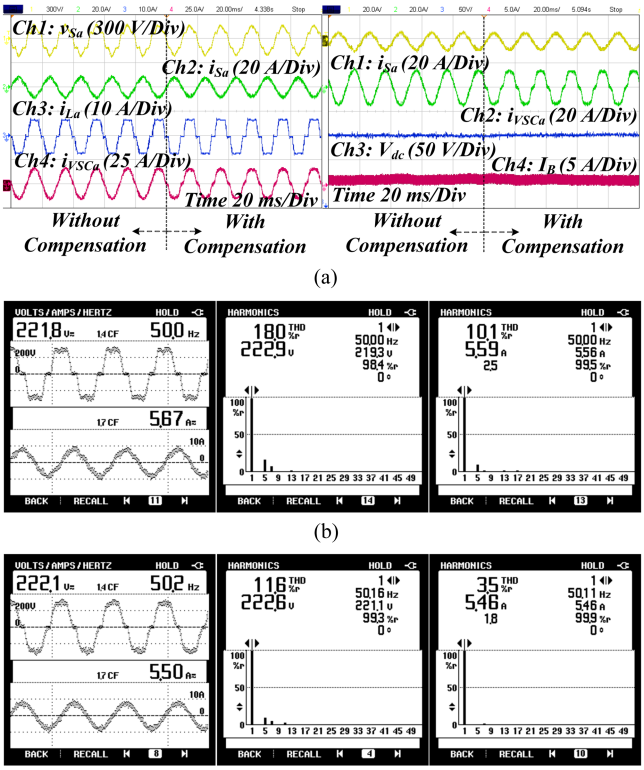

Fig. 16. GSPV-BS system's PQ performance with a balanced load case (a) recorded various waveforms and THD values of local grid voltage-current (b) without and (c) with load's harmonics compensation.

that despite sinusoidal current injection from VSC of GSPV-based system ($i_{\mathrm{VSC}a}$), grid current (i_{Sa}) is distorted with a THD of 10%. Consequently, these distorted grid currents intensify harmonic distortion of PCC voltage (v_{Sa}), increasing THD to 18%.

However, by compensating for harmonic load currents using VSC, these harmonic currents are prevented from flowing into

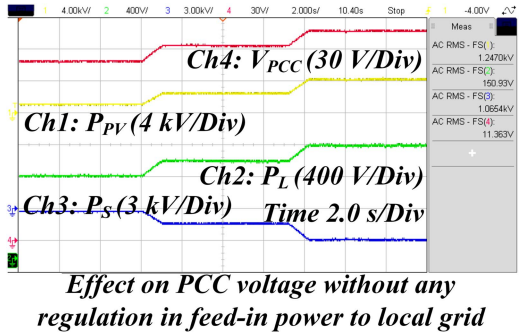

Fig. 17. Effect of high SPV array penetration on GSPV-BS system.

grid. This results in a significantly improved grid current THD of approximately 3.5%. Consequently, harmonic distortion of PCC voltages is reduced to around 11.6%, as confirmed by recorded power analyzer measurements in Fig. 16(c). While this approach introduces harmonic distortion in VSC current ($i_{\mathrm{VSC}a}$), as shown in Fig. 16(a), it does not adversely affect system performance. This is evident from stable dc link voltage (V_{dc}) and BS current (I_B) waveforms in Fig. 16(a) during load compensation, indicating undisturbed system operation.

C. Effect of High SPV Array Penetration on GSPV-BS System

To examine effect of high PV penetration on PCC voltage (V_{PCC}), solar insolation (I_{rr}) value increases from 0.3 to *0.6* kW/m^2 and from 0.6 to 1.0 kW/m^2. Fig. 17 shows recorded results when no regulation is provided for feed-in of active and reactive power to ac grid, i.e., ac grid operates at UPF, and all SPV array power (P_{PV}) is supplied to PCC. These results reveal that V_{PCC} continually rises. An increase of around 30 V is observed from $I_{rr} = 0.3$ kW/m^2 to $I_{rr} = 1.0$ kW/m^2, with V_{PCC} reaching 198 V, approximately 110% of rated value ($V_{\mathrm{PCC}r} = 179.63$ V). Such high voltage levels may damage GSPV-BS system and load; therefore, a maximum permissible rise of 6% above rated value ($V_{\max} = 190.4$ V) is allowed according to IEEE std. 1547 [6]. Hence, regulating grid active and reactive power is needed to protect GSPV-BS system from such situations.

D. Effect of High PV Penetration on V_{PCC} With New Control

Figs. 18–21 illustrate impact of high SPV array penetration on V_{PCC}, when proposed control strategy is implemented. Figs. 18–19 present results for scenarios where BS's state of charge is below its maximum limit (SOC $<$ SOC$_{\max}$). In this condition, system operates according to Case II, and a portion of generated SPV power (P_{PV}) is diverted to BS using control parameter (I_{BC}) as soon as $V_{\mathrm{PCC}} > V_{\max}$ is detected. Moreover, if injected excess power to BS is less than specified maximum limit ($I_B < I_{\max}$), then system operation is controlled by case II(a), and provides UPF operation at ac grid, meaning grid reactive power is maintained at zero despite load reactive power demand.

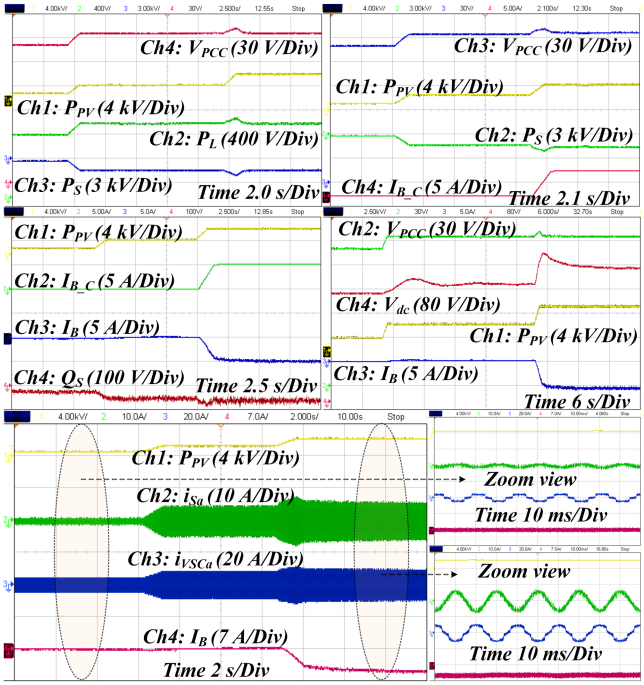

Fig. 18. Performance of GSPV-BS system with developed control strategy when SOC $<$ SOC$_{\max}$ and $V_{\rm PCC} > V_{\max}$ are detected.

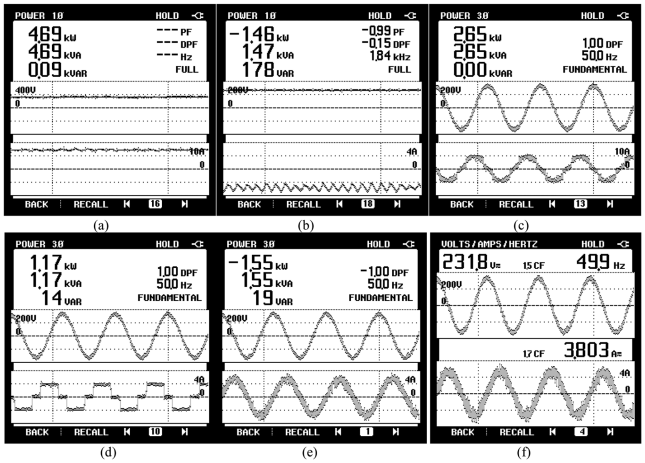

Fig. 19. Recorded power when SOC $<$ SOC$_{max}$ and $V_{\rm PCC} > V_{\max}$ is detected (a) $P_{\rm PV}$, (b) P_B, (c) $P_{\rm VSC}$, (d) P_L, (e) P_S, and (f) ac grid voltage-current waveforms.

Documented test results in Figs. 18 and 19 indicate that I_{BC} initially remains zero and gradually increases as defined by (3) once $V_{\rm PCC} > V_{\max}$ is detected. Here, ΔI_B parameter is set to 1% of $I_{\max}$, with $I_{\max}$ determined by manufacturer's recommended C-rate for BS. By increasing I_{BC}, a portion of $P_{\rm PV}$ is transferred to BS, limiting power injection into ac grid (P_S) to a constant value, as shown by P_S and I_B waveforms. Consequently, $V_{\rm PCC}$ is capped at $V_{\max}$. The steady-state value of I_{BC} is less than $I_{\max}$ (8.4 A). Additionally, power results in Fig. 19 confirm that power supplied to BS remains within the manufacturer's specified limit (2.01 kW). Hence, system operation is controlled by case II(a) and only active power feed-in to ac grid is controlled to maintain

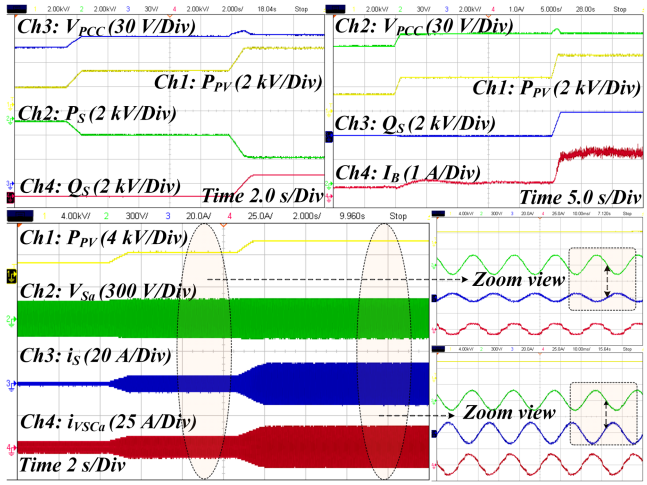

Fig. 20. Performance of GSPV-BS system with new control when BS is charged.

$V_{\rm PCC}$ at $V_{\max}$. Furthermore, system upholds UPF operation on ac grid side. As shown in Figs. 18 and 19, grid reactive power (Q_S) is negligible.

The recorded test results in Fig. 18 also display variations in I_B, V_{dc}, i_{Sa}, and $i_{\rm VSC\,a}$. It is observed that direction of I_{BC} and I_B are opposite, which is expected since BS current is sensed outward, as shown in Fig. 1. In these test results, $V_{\rm dc}$ fluctuates due to the employed adaptive dc link control strategy, resulting in a new steady-state value in response to changes in $V_{\rm PCC}$. With increasing $P_{\rm PV}$, i_{Sa} and $i_{\rm VSC\,a}$ also adjust accordingly. A zoomed-in view of these results shows that ac grid current remains sinusoidal, while VSC current becomes distorted as system compensates for local load's harmonic currents. However, after a certain point, no further changes occur in amplitude of grid and VSC currents with increase in $P_{\rm PV}$, as indicated in Fig. 18. This is due to excess generation being transferred to BS by controlling parameter I_{BC} to cap $V_{\rm PCC}$ at $V_{\max}$.

Figs. 20 and 21 present results for scenarios where BS's state of charge is at its maximum limit (SOC$\approx$SOC$_{\max}$) and $V_{\rm PCC} > V_{\max}$ are detected. Under these conditions, generated solar PV array power cannot be transferred to BS to prevent overcharging. Consequently, system operates according to Case III, and controller regulates Q_S to restrain rise in $V_{\rm PCC}$, while entire SPV array generation is delivered to ac grid. In this case, SPV array operates at its MPP if VSC's apparent power ($S_{\rm VSC}$) remains below its rated value. Otherwise, SPV array generation is curtailed to maintain $S_{\rm VSC}$ within its specified limit.

Documented test results in Figs. 20 and 21 illustrate system performance under these conditions. Initially, system operates at UPF ($Q_S \approx 0$) as $V_{\rm PCC}$ is below $V_{\max}$. However, when $V_{\rm PCC} > V_{\max}$ is detected, controller increases Q_S until $V_{\rm PCC}$ is brought back below $V_{\max}$. In this scenario, VSC injects reactive power into ac grid, causing a lagging power factor. This behavior is evident in zoomed waveforms of ac grid phase voltage (v_{Sa}) and line current (i_{Sa}) in Fig. 20. When $V_{\rm PCC}$ is less than $V_{\max}$, the zero crossings of v_{Sa} and i_{Sa} coincide, indicating UPF operation. Conversely, when $V_{\rm PCC}$ exceeds $V_{\max}$, zero

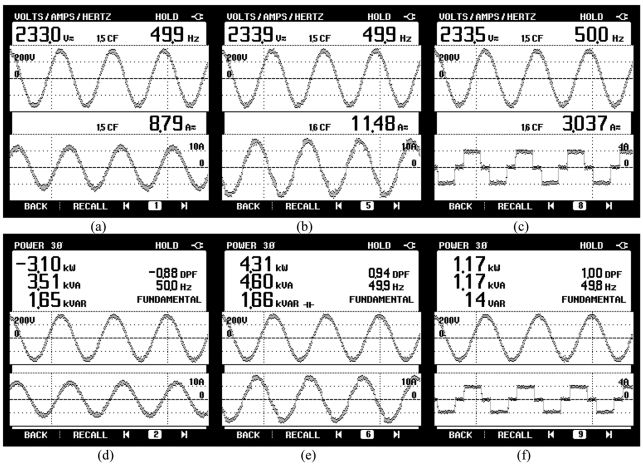

Fig. 21. Power quality analyzed results when SOC $\approx$ $\mathrm{SOC}_{\max}$ and $V_{\mathrm{PCC}} > V_{\max}$ is detected (a) v_{Sab}-i_{Sa}, (b) v_{Sab}-i_{VSCa}, (c) v_{Sab}-i_{La}, (d) P_S, (e) P_{VSC}, and (f) P_L.

crossings do not overlap, and i_{Sa} lags v_{Sa}, signifying reactive power flow from ac grid to PCC. This observation is corroborated by power quality analyzer results in Fig. 21, which include ac grid voltage-current waveform, its various powers. The RMS value of ac grid line voltage is approximately 1.06 times of rated voltage, confirming successful operation of control strategy. Additionally, Fig. 21 shows that VSC's apparent power (S_{VSC}) remains below its rated value (specified in Table II), indicating continued SPV array operation at the MPP. This is supported by SPV array power generation (4.69 kW) in Fig. 19(a) and VSC power (4.31 kW) in Fig. 21(e), although VSC power is lower due to power losses in BTC.

Fig. 20 also illustrates variations in I_B. While I_B is negligible when Q_S is approximately zero, it increases to around 1.6 A when Q_S is raised to limit V_{PCC}. This increase is attributed to higher semiconductor losses due to increased reactive power generation of VSC [33], necessitating additional power from BS to maintain dc link voltage at the set reference value. Consequently, BS supplies power, leading to a positive I_B.

VI. Conclusion

A new SOGI-ACF-based algorithm is established to enhance PQ performance of GSPV-BS system under nonideal ac grid voltage and load current conditions, such as unbalance and distortion. In addition, a variable power mode-based strategy is developed to restrain voltage rise during high SPV array penetration. Following points have been observed.

1) Performance of designed filter algorithm is compared with popular C-SOGI algorithm in terms of harmonic attenuation, dynamic response, and computational complexity. It is observed that SOGI-ACF algorithm performs better. In addition, modifications are made to the designed algorithm to address the complex gain issue in ACF, which reduces its complexity compared to existing ACF-based methods.
2) To validate designed filter performance, both SOGI-ACF and C-SOGI algorithms are implemented on a test bench, and THD of load current's PSC is examined. It is seen that THD value of PSC obtained from SOGI-ACF algorithm is lower.
3) PQ of GSPV-BS system is analyzed with and without local load harmonics compensation. It has been observed that harmonics are induced in ac grid current and PCC voltage without compensation. However, system demonstrates satisfactory PQ with load's harmonics compensation.
4) Effect of high SPV array penetration on PCC voltage is recorded, and it has been observed that without regulation of ac grid's active and/or reactive power, system may experience overvoltage, damaging system and local load.
5) However, with designed control strategy, rise in PCC voltage is restrained to allowable permissible limit defined by IEEE std. 1547. Based on BS charge status and other constraints of GSPV-BS system, it successfully controls ac grid's active or reactive power to restrain V_{PCC} rise. This developed control can also be extended to regulate PCC voltage during peak load demand and low or no SPV generation conditions.
6) In addition, designed control to restrain the rise in V_{PCC} uses a simple perturbation method instead of PI regulators, resulting in a reduction in overall complexity of control structure of GSPV-BS system compared to existing methods.
7) It has been seen that designed variable power mode control strategy controls ac grid's active or reactive power only when $V_{\mathrm{PCC}} > V_{\max}$ is detected. Under normal conditions, it operates system in UPF mode and maintains ac grid power factor at unity, which reduces line losses in ac grid.
8) Proposed control is verified using a simple test bench setup of GSPV-BS system. Its performance on a complex system, where many GSPV-BS systems are connected, is yet to be investigated, which is to be explored in future work.

Acknowledgment

The authors acknowledge DST. GOI India, for supporting under UKICERI, SERI projects, and SERB-NSC fellowship.

References

[1] "Levelized costs of new generation resources in the annual energy outlook 2022?" 2022. [Online]. Available: https://www.eia.gov/outlooks/aeo/pdf/electricity_generation.pdf
[2] X. Li, H. Wen, Y. Hu, Y. Du, and Y. Yang, "A comparative study on photovoltaic MPPT algorithms under EN50530 dynamic test procedure," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4153–4168, Apr. 2021.
[3] J. Wang, K. Sun, C. Xue, T. Liu, and Y. Li, "Multi-port DC-AC converter with differential power processing DC-DC converter and flexible power control for battery ESS integrated PV systems," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4879–4889, May 2022.
[4] G. Modi and B. Singh, "SPV-BES system synchronized to three-phase four-wire AC distribution network," *IEEE Trans. Ind. Appl.*, vol. 57, no. 6, pp. 5667–5676, Nov./Dec. 2021.
[5] R. Panigrahi, S. K. Mishra, S. C. Srivastava, A. K. Srivastava, and N. N. Schulz, "Grid integration of small-scale photovoltaic systems in secondary distribution network—A review," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 3178–3195, May/Jun. 2020.
[6] *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces*, IEEE Std 1547, 2018.

[7] J. Roy, A. K. Jain, and B. Mather, "Impacts of experimentally obtained harmonic spectrums of residential appliances on distribution feeder," in *Proc. IEEE Texas Power Energy Conf.*, 2020, pp. 1–6.
[8] G. Lou, Q. Yang, W. Gu, X. Quan, J. M. Guerrero, and S. Li, "Analysis and design of hybrid harmonic suppression scheme for VSG considering nonlinear loads and distorted grid," *IEEE Trans. Energy Convers.*, vol. 36, no. 4, pp. 3096–3107, Dec. 2021.
[9] B. Liu, F. Zhuo, Y. Zhu, H. Yi, and F. Wang, "A three-phase PLL algorithm based on signal reforming under distorted grid conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5272–5283, Sep. 2015.
[10] G. Modi, B. Singh, and Y. Singh, "Control of solar PV-battery system to limit in PCC voltage rise and for power quality improvement," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 945–950.
[11] J. Xu, H. Qian, Q. Qian, and S. Xie, "Modeling, stability, and design of the single-phase SOGI-based phase-locked loop considering the frequency feedback loop effect," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 987–1002, Jan. 2023.
[12] I. Ullah and M. Ashraf, "Comparison of synchronization techniques under distorted grid conditions," *IEEE Access*, vol. 7, pp. 101345–101354, 2019.
[13] S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki, "Standard SOGI-FLL and its close variants: Precise modeling in LTP framework and determining stability region/robustness metrics," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 409–422, Jan. 2021.
[14] J. Xu, H. Qian, Y. Hu, S. Bian, and S. Xie, "Overview of SOGI-based single-phase phase-locked loops for grid synchronization under complex grid conditions," *IEEE Access*, vol. 9, pp. 39275–39291, 2021.
[15] M. Mellouli, M. Hamouda, J. B. H. Slama, and K. Al-Haddad, "A third-order MAF based QT1-PLL that is robust against harmonically distorted grid voltage with frequency deviation," *IEEE Trans. Energy Convers.*, vol. 36, no. 3, pp. 1600–1613, Sep. 2021.
[16] A. R. Zamani, M. H. Ghaderi, and M. Hamzeh, "Dynamic response and filtering capability improvement of $\alpha\beta$-frame cascaded delayed signal cancellation based PLL," *IEEE Trans. Energy Convers.*, vol. 37, no. 2, pp. 1156–1163, Jun. 2022.
[17] S. Prakash, J. K. Singh, R. K. Behera, and A. Mondal, "A type-3 modified SOGI-PLL with grid disturbance rejection capability for single-phase grid-tied converters," *IEEE Trans. Ind. Appl.*, vol. 57, no. 4, pp. 4242–4252, Jul./Aug. 2021.
[18] P. Zhong, J. Sun, Z. Tian, M. Huang, P. Yu, and X. Zha, "An improved impedance measurement method for grid-connected inverter systems considering the background harmonics and frequency deviation," *IEEE J. Emer. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4236–4247, Aug. 2021.
[19] S. Golestan, F. D. Freijedo, A. Vidal, J. M. Guerrero, and J. Doval-Gandoy, "A quasi-type-1 phase-locked loop structure," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6264–6270, Dec. 2014.
[20] Y. Zhou, H. Li, and L. Liu, "Integrated autonomous voltage regulation and islanding detection for high penetration PV applications," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2826–2841, Jun. 2013.
[21] A. Narang et al., "Dynamic reserve power point tracking in grid-connected photovoltaic power plants," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 5939–5951, May 2023.
[22] A. Amanipoor, M. S. Golsorkhi, N. Bayati, and M. Savaghebi, "V-Iq based control scheme for mitigation of transient overvoltage in distribution feeders with high PV penetration," *IEEE Trans. Sustain. Energy*, vol. 14, no. 1, pp. 283–296, Jan. 2023.
[23] M. Ahmed et al., "Effects of household battery systems on LV residential feeder voltage management," *IEEE Trans. Power Del.*, vol. 37, no. 6, pp. 5325–5336, Dec. 2022.
[24] T. Tewari, A. Mohapatra, and S. Anand, "Coordinated control of OLTC and energy storage for voltage regulation in distribution network with high PV penetration," *IEEE Trans. Sustain. Energy*, vol. 12, no. 1, pp. 262–272, Jan. 2021.
[25] M. Kashif, M. J. Hossain, E. Fernandez, M. S. H. Nizami, S. M. N. Ali, and V. Sharma, "An optimal allocation of reactive power capable end-user devices for grid support," *IEEE Syst. J.*, vol. 15, no. 3, pp. 3249–3260, Sep. 2021.
[26] K. Ndirangu, H. D. Tafti, J. E. Fletcher, and G. Konstantinou, "Impact of grid voltage and grid-supporting functions on efficiency of single-phase photovoltaic inverters," *IEEE J. Photovolt.*, vol. 12, no. 1, pp. 421–428, Jan. 2022.
[27] J. Yang, W. Tushar, T. K. Saha, M. R. Alam, and Y. Li, "Prosumer-driven voltage regulation via coordinated real and reactive power control," *IEEE Trans. Smart Grid*, vol. 13, no. 2, pp. 1441–1452, Mar. 2022.
[28] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Is using a complex control gain in three-phase FLLs reasonable?," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 2480–2484, Mar. 2020.
[29] C. Karasala and S. K. Ganjikunta, "An adaptive DC-link voltage control of a multifunctional SPV grid-connected VSI for switching loss reduction," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12946–12956, Dec. 2022.
[30] A. Ozdemir and Z. Erdem, "Double-loop PI controller design of the DC-DC boost converter with a proposed approach for calculation of the controller parameters," *J. Syst. Control Eng.*, vol. 232, no. 2, pp. 137–148, Feb. 2018.
[31] T. Ye, N. Dai, C.-S. Lam, M.-C. Wong, and J. M. Guerrero, "Analysis, design, and implementation of a quasi-proportional-resonant controller for a multifunctional capacitive-coupling grid-connected inverter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4269–4280, Sep./Oct. 2016.
[32] G. Modi and B. Singh, "A novel multilayer N-LMS adaptive filter based control for synchronization and power quality improvement in grid-tied SPV system," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 9158–9168, Sep. 2023.
[33] K.-N. D. Malamaki and C. S. Demoulias, "Estimation of additional PV converter losses operating under PF $\neq$ 1 based on manufacturer's data at PF = 1," *IEEE Trans. Energy Convers.*, vol. 34, no. 1, pp. 540–553, Mar. 2019.

Gaurav Modi (Member, IEEE) received the B.Tech. degree in energy engineering from the Maulana Azad National Institute of Technology, Bhopal, India, in 2012, the M.Tech. degree in electrical drives and power electronics from the Indian Institute of Technology Roorkee, Roorkee, India, in 2015, and the Ph.D. degree in power electronics, electrical machines, and drives research group from the Institute of Technology Delhi, New Delhi, India, in 2024.

He was a Visiting Researcher with the School of Engineering, Cardiff University, U.K., in 2019. He is currently a Senior Technical Project Engineer with Power Grid Grid Integration Division, Hitachi Energy India Pvt. Ltd., Chennai, India. His research interests include grid-tied/off-grid renewable energy systems, grid synchronization, power quality solutions, custom power devices, and electrical drives.

Bhim Singh (Fellow, IEEE) received the B.E. degree in electrical engineering from the University of Roorkee, Roorkee, India, in 1977, and the M.Tech. degree in power apparatus and systems, and the Ph.D. degree in electrical engineering from IIT Delhi, New Delhi, India, in 1979 and 1983, respectively.

In 1983, he joined the Department of Electrical Engineering, University of Roorkee, as a Lecturer and became a Reader in 1988. In 1990, he joined the Department of Electrical Engineering, IIT Delhi, as an Assistant Professor, where he was also an Associate Professor in 1994 and a Professor in 1997. He was the Head of the Department of Electrical Engineering, IIT Delhi, from 2014 to 2016. He has been the Dean, Academics with IIT Delhi from 2016 to 2019. He has been the JC Bose Fellow of DST, Government of India, from 2015 to 2021. He has been serving as an Emeritus Professor and SERB National Science Chair at IIT Delhi since 2021. He has guided 129 Ph.D. dissertations, and 183 Mater theses. He has 68 granted and 40 filed patents. His research interests include solar PV grid interface systems, microgrids, power quality mitigation, solar PV water pumping, improved power quality ac–dc converters, power electronics, electrical machines, drives, and electric vehicles.