A Closed-Loop Compensated Rogowski Coil Current Sensor for Three-Phase Inverter

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***Abstract*—Accurate current measurement is crucial in power electronic converters to achieve fault protection and current control. Among the various options available, the printed circuit board Rogowski coil current sensor (PCB RCCS) emerges as a strong contender due to its advantages of higher bandwidth, smaller volume, and lower cost. However, the presence of offset voltage and offset current in operational amplifiers (op-amps) greatly limits the measurement accuracy of PCB RCCS, and is greatly affected by the individual differences of op-amps and temperature changes. Traditional error compensation methods lack self-adjusting capabilities, leading to significant limitations in compensation effectiveness. This article proposes a closed-loop error compensation method that can monitor the compensation effect in real-time under actual operating conditions, adjust the compensating signal promptly, and achieve precise compensation of integral errors in PCB RCCS. Moreover, the proposed PCB RCCS is highly integrated into a three-phase inverter, achieving not only reliable short-circuit protection for power devices but also recovering phase current information for successful utilization in system current control.**

***Index Terms*—Current sensor, error compensation, printed circuit board (PCB) Rogowski coil, resettable integrator, three-phase inverter.**

I. Introduction

With the continuous upgrading of power semiconductor devices, power electronic converters have been constantly advancing towards increased intelligent and informational capabilities. The switching current information, as a critical common parameter in power electronic converters for functions such as short-circuit protection, closed-loop control, loss calculation, and lifetime prediction [1], [2], [3], holds significant research value and application prospects.

This article takes the three-phase inverter as an example, as shown in Fig. 1. In traditional control logic [4], the phase current information at the inverter-side inductor node contains power frequency current information and switching ripple current information, which is widely used for current control and harmonic suppression. However, it does not include switching edge information, and therefore, short-circuit protection must be achieved by alternative methods such as desaturation detection, gate charge detection, and parasitic inductance voltage detection. A new method of measuring switching current information at the input and output nodes of the inverter bridge arm has been proposed in [5], which can reduce redundant current sensors and short-circuit protection circuits in the system, and promote the intelligent and informational development of the inverter. The switching current information can not only be used for loss calculation, lifetime prediction and short-circuit protection, but also can be based on the waveform reconstruction principle to reconstruct three phase current information and be used for current control and harmonic suppression [5].

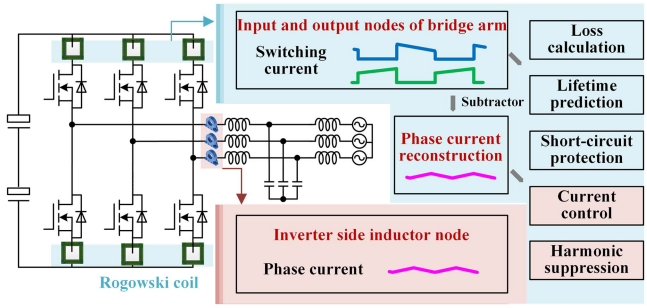

Fig. 1. Structure of three-phase inverter integrated PCB RCCS.

However, traditional current sensing techniques face challenges in terms of bandwidth [6], intrusion [7], and integration to measure switching current information at input and output nodes of the inverter bridge arm. Currently, the main types of current sensors include current transformer, shunt, Hall current sensor, magneto-resistor (MR) current sensor, and Rogowski coil current sensor (RCCS). Current transformer transforms the large primary system current into a small secondary system current, but it suffers from possible flux saturation and size limitations [8]. Shunt uses a tiny resistance in the main circuit to measure the voltage across the resistance, but lacks electrical isolation between input and output, which exists security risks in three-phase inverter control system [9]. Hall current sensor provides magnetic isolation, but its bandwidth is normally less than 1 MHz, which cannot measure the switching edge

Received 1 April 2024; revised 22 July 2024; accepted 5 September 2024. Date of publication 19 September 2024; date of current version 12 December 2024. This work was supported by the National Natural Science Foundation of China under Grant 52377179. Recommended for publication by Associate Editor M. Liserre. *(Corresponding author: Jianlong Kang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3464121.

Digital Object Identifier 10.1109/TPEL.2024.3464121

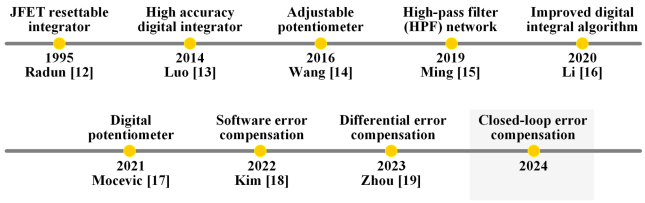

Fig. 2. Timeline of integral processing circuit improvement.

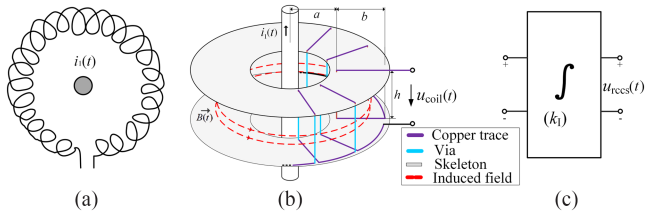

Fig. 3. Sketch of RCCS. (a) Winding coil. (b) PCB Rogowski coil. (c) Integrator.

information [10]. MR current sensor, based on the magnetoresistive effect, indirectly measures the current to be tested by detecting linear variation of resistance with the magnetic field, but its measurement accuracy and bandwidth are limited by hysteresis effect, skin effect, and non-negligible temperature drift [28]. A better alternative is the printed circuit board RCCS (PCB RCCS), which offers bandwidth in the tens of MHz range, as well as low cost, small size, and excellent isolation [5], [11], [14].

The PCB RCCS eliminates the need for a magnetic core, making it suitable for integration into power electronic converters. However, the offset voltage and current of operational amplifiers (op-amps) introduce drift and droop phenomena in active integrators, affecting the measurement accuracy of PCB RCCS. In this article, "accuracy" represents the degree of closeness between the measurement results of the PCB RCCS and the accurate current value, corresponding to the magnitude of the error between them. Many improved methods are constantly proposed to address these issues, as shown in Fig. 2. Resettable integrator was firstly put forward using junction field-effect transistor (JFET) in 1995 but the JFET as a reset switch did not perform ideally [12]. Then, the digital integrator was tried in [13] and [16], but its measurement bandwidth is limited by the sampling rate and algorithms. In addition, a method that uses a high-pass filter after the integrator to reduce the bias error is proposed [15]. However, the low-frequency measurement performance of the PCB RCCS will be further reduced. Meanwhile, potentiometer circuits were applied in [14] and [17] to reduce the offset voltage of op-amps. However, the compensation method relies on the precision of adjustable resistors, and ignores the charge injection effect of the reset switch. A software error compensation scheme reducing errors in programs was also proposed in [18]. However, this method can only compensate for errors at the sampling point, and the bandwidth of PCB RCCS is reduced. A differential compensation scheme was proposed in [19]. Nevertheless, the error signal generated by the main integrator is not the same as the compensating signal generated from the slave integrator due to differences in op-amps, the compensation effect remains challenging. In summary, traditional methods cannot fully achieve accurate adaptive error compensation.

To overcome the challenges of random changing integral errors, a closed-loop error compensation method is proposed for PCB RCCS in this article. This method employs an analog to digital converter (ADC) sampling module to real-time capture integral error information, and utilizes a PI controller to achieve zero-error tracking. Simultaneously, digital compensating information is converted to analog signal through a digital to analog converter (DAC) output module, and a high-speed subtractor is used to compensate for integral errors in the PCB RCCS. This approach can effectively enhance measurement accuracy of PCB RCCS without impacting measurement bandwidth. The rest of this article is organized as follows. Section II describes the basic principle of the PCB RCCS, including the PCB Rogowski coil and the active integrator, the droop and drift phenomena of active integrators are discussed. In Section III, the closed-loop error compensation circuit is analyzed, and its three-stage reset logic, sampling logic, and compensation method are introduced. In addition, the compensation effect is verified when the test current signal is 0. In Section IV, the structure and parameters design of PCB RCCS is introduced first, and a three-phase inverter with integrated PCB RCCS is designed. Moreover, Section V presents the testing results of switching currents, and the short circuit protection and current control are realized successfully by the proposed PCB RCCS. Finally, Section VI concludes this article.

II. Principle of PCB RCCS

This section elaborates on the measurement principle of the PCB RCCS and analyzes its high-frequency characteristics based on the lumped parameter model of the PCB Rogowski coil. Furthermore, this section analyses the performance constraints of the active integrators, revealing the contradiction between the drift phenomenon in ideal integrators and the droop phenomenon in lossy integrators.

A. Basic Structure of PCB RCCS

As shown in Fig. 3, the PCB RCCS is composed of a PCB Rogowski coil and an integrator. The PCB Rogowski coil, which is a hollow coil, is composed of copper traces, vias, and the insulating dielectric skeleton. Based on Faraday's law of electromagnetic induction and Ampere's loop law, the PCB Rogowski coil acts as a differentiator, and its output voltage is proportional to the di/dt, as shown in (1) [20], [21]. The integrator is employed to restore the switching current signal using the output voltage of the PCB Rogowski coil, and the final PCB RCCS output voltage can be expressed as (2). Compared with the winding coil, the PCB Rogowski coil is more unified and easily scales production [22]. Therefore, the PCB Rogowski coil has greater potential for development and application prospects

$$u_{\text{coil}}(t) = -N\frac{d\Phi}{dt} = -\frac{N\mu_0 h}{2\pi}\ln\frac{a+b}{b}\cdot\frac{di_1(t)}{dt} = -M\frac{di_1(t)}{dt} \tag{1}$$

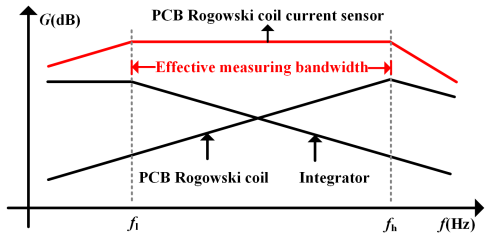

Fig. 4. Amplitude-frequency characteristics of the PCB RCCS.

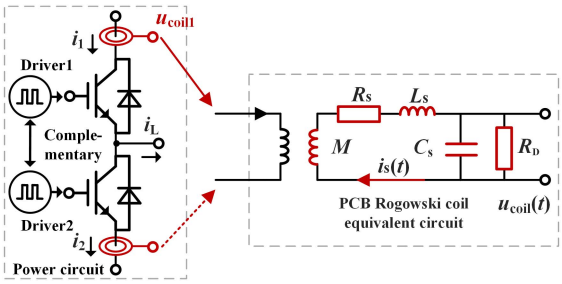

Fig. 5. Equivalent circuit of the PCB Rogowski coil, where L_S is parasitic inductance, R_S is parasitic resistance, C_S is parasitic capacitance, M is mutual inductance, and R_D is damping resistance.

$$u_{\text{rccs}}(t) = -K_I \int \left(-M\frac{di_1(t)}{dt}\right) dt = K_I M \cdot i_1(t) \tag{2}$$

where N is the turns, μ_0 is the air permeability, h is the thickness, a and b are the internal and external diameters of the coil, M is the mutual inductance, K_I is the integral coefficient, and $i_1(t)$ is the measured switching current.

The amplitude-frequency characteristic curve of PCB RCCS is shown in Fig. 4. The PCB Rogowski coil exhibits good differential characteristics at low frequencies but has a high-frequency resonance point due to parasitic inductance and capacitance. The integrator demonstrates effective integration characteristics at high frequencies but has a low-frequency cutoff frequency to mitigate integral drift caused by the offset voltage of op-amps. Therefore, the RCCS can only measure the current signal between the high-frequency resonant frequency of the coil and the low-frequency cutoff frequency of the integrator. However, the measurement results from the PCB RCCS exhibit low-frequency errors and high-frequency noises, which affect the sensor's measurement accuracy.

The PCB Rogowski coil is composed of traces and vias in the printed circuit board. In addition to the equivalent mutual inductance between the coil and measured conductor, there are many parasitic parameters in actual design practice, which make it difficult to determine the characteristics of the coil at high frequency. The lumped parameter model is widely used to explore the high-frequency characteristics of the PCB Rogowski coil further and determine its high-frequency measurement bandwidth.

The equivalent circuit of the PCB Rogowski coil is shown in Fig. 5, where L_S is parasitic inductance, R_S is parasitic resistance, C_S is parasitic capacitance, M is mutual inductance, and R_D is damping resistance in parallel at the output side of the coil. Considering the lumped parameters, the transfer function from the switching current to the output voltage of the PCB Rogowski coil can be described as (3). It does not act as an ideal differential element but rather as a second-order resonant element [24]. The first resonant frequency, generally referred to as the bandwidth of PCB RCCS, can be obtained by (4)

$$\begin{aligned} G_{\text{coil}}(s) &= \frac{u_{\text{coil}}(s)}{i_1(s)} \\ &= \frac{sMR_D}{s^2R_DL_SC_S + s\left(L_S + R_SR_DC_S\right) + \left(R_S + R_D\right)} \end{aligned} \tag{3}$$

$$f_0 = \frac{1}{2\cdot\pi\cdot\sqrt{L_S\cdot C_S}}\cdot\sqrt{\frac{R_D + R_S}{R_D}}. \tag{4}$$

B. Challenge of Integrator Design

Integrators can be categorized into passive integrators, active integrators, and digital integrators. Among these, passive integrators lack integral amplification capability and incur significant phase shifts, and therefore, exhibit poor low-frequency performance. The performance of the digital integrator is limited by the sampling rate and operation period, making it unable to measure high-frequency switching currents. Active integrators, introducing op-amps to achieve integral amplification of input signals, can offer a broader current measurement range and measurement bandwidth.

However, the nonidealities of op-amps are important factors affecting the performance of active integrators, primarily categorized into bandwidth, delay, offset voltage, and offset current aspects. The bandwidth of the op-amps will affect the integrator's high-frequency signal processing capability, manifested by the inability to accurately restore current information during switching edge moments. Therefore, the bandwidth of the op-amps should be at least 10 times the maximum frequency of the input signal in active integrator [29].

Furthermore, the delay of the op-amps will affect the response speed of the integrator, leading to signal processing results distortion or latency. To minimize the impact of op-amps delay on measurement results, the slew rate SR of the op-amps must satisfy the condition, as shown in (5). Here, V_p represents the peak output voltage of the sensor, and t_{edge} is the ON/OFF time of power switch. In this article, an operational amplifier (THS4031) with a bandwidth of 100 MHz and a slew rate of 100 V/μs is selected

$$SR > \frac{V_p}{t_{\text{edge}}}. \tag{5}$$

In addition, the input sides of op-amps may exhibit offset voltage (V_{OS}) and offset currents (I_{B+} and I_{B-}), with an equivalent circuit shown in Fig. 6(a). In ideal integrator circuits, the offset voltage and offset current will cause drift phenomena, which accumulate over time and eventually lead to op-amps saturation, rendering the integrator circuit unable to function properly. Taking the measurement of switching current information as an example, the drift phenomenon introduced by the ideal integrators is illustrated in Fig. 6(b). Therefore, ideal integrators cannot operate normally in practice.

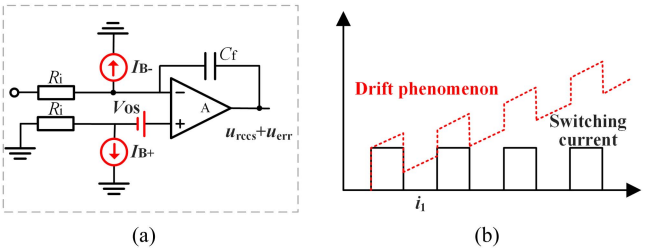

Fig. 6. (a) Ideal integrator. (b) Drift phenomenon.

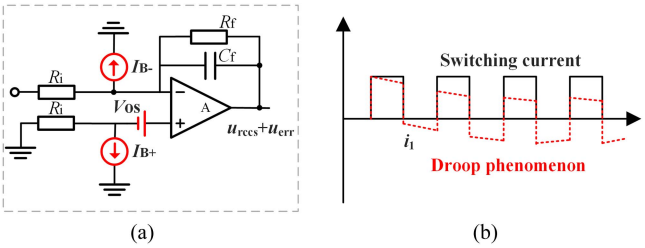

Fig. 7. (a) Lossy integrator. (b) Droop phenomenon.

To suppress the continuous drift phenomenon in the ideal integrators, the lossy integrators introduce a damping resistor in parallel to the integrator capacitor of the ideal integrators. The circuit structure is illustrated in Fig. 7(a). The lossy integrators exhibit no drift phenomenon, but it has low-frequency cutoff frequency, manifested by significant droop phenomenon in the measured current signal from the sensor, as depicted in Fig. 7(b). To sum up, it is difficult to avoid the contradiction between droop and drift phenomena when the switching current needs to be measured continuously.

III. Closed-Loop Error Compensation Scheme

To address the contradiction between drift and droop phenomena in PCB RCCS, the resettable integrator is employed in [14], [18], [19]. However, some non-negligible integral errors still exist in its output results. This section first analyzes the error signal present in the integral phase of the resettable integrator, and proposes a closed-loop error compensation method. This method enables real-time precise tracking and compensation of integral errors and further improves the measurement accuracy of PCB RCCS. The control logic and compensation effectiveness are validated through experiments.

A. Errors Analysis of the Resettable Integrator

The resettable integrator is adopted in this article, as shown in Fig. 8(a). Different from the lossy integrator, the resettable integrator features a reset switch S connected in parallel with the integrator capacitor. When the reset switch S is closed, the resettable integrator enters the reset phase, with the integrator capacitor short-circuited and the output voltage of the integrator maintained at 0. When the reset switch S is opened, the resettable integrator transitions to the integral phase, effectively behaving as an ideal integrator. This design effectively suppresses drift phenomenon and eliminates droop issues by enabling the periodic discharge of accumulated drift charges within the integrator

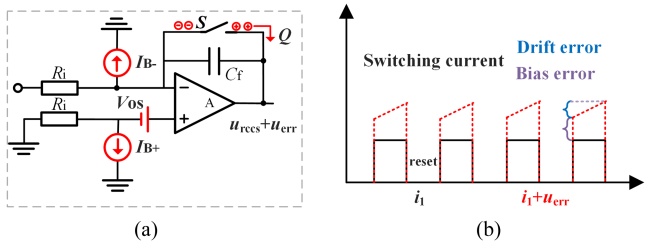

Fig. 8. (a) Resettable integrator. (b) Drift error and bias error.

capacitor. It is particularly suitable for the accurate restoration of switching current information. However, the output of the resettable integrator exhibits noticeable drift error and bias error, especially when the amplitude of the switching current is low, leading to poor measurement accuracy of the sensor.

The errors of the resettable integrator mainly include drift error and bias error, as shown in Fig. 8(b). The drift error is caused by the offset voltage and offset current on the input sides of op-amps, gradually accumulating with increasing integration time, as defined in (6). The bias error is induced by the charge injection effect of the reset switch, which can be equivalently represented as a charge Q flowing from the reset switch, as depicted in Fig. 8(a). At the moment the switch opens, injected charges flow towards the integrator capacitor C_{f} of the resettable integrator, generating a bias error during the integral phase, as defined in (7)

$$u_{\mathrm{drift}} = \frac{R_{\mathrm{i}} \cdot C_{\mathrm{f}} \cdot s + 1}{R_{\mathrm{i}} \cdot C_{\mathrm{f}} \cdot s} \cdot V_{\mathrm{OS}} + \frac{1}{C_{\mathrm{f}} \cdot s}[I_{\mathrm{B-}} - (R_{\mathrm{i}} \cdot C_{\mathrm{f}} \cdot s + 1) \cdot I_{\mathrm{B+}}] \tag{6}$$

$$u_{\mathrm{bias}} = \frac{Q}{C_{\mathrm{f}}}. \tag{7}$$

The autozero technique of the op-amps can reduce the offset voltage and offset current on the input side, thereby minimizing the integrator's drift error. However, the autozero technique often sacrifices the bandwidth of the op-amps, with bandwidth typically less than 10 MHz [26], which cannot meet the basic bandwidth requirements of the active integrator for the PCB RCCS. In addition, the bias error can be reduced by increasing the integrator capacitance of the integrator and reducing injected charge of reset switch. However, under the premise of ensuring the same integration gain, increasing the integrator capacitance means a decrease in input resistance, challenging the op-amps' loading capacity and losses. The decrease in the injected charge of analog switches will also increase their on-resistance and on-time, thereby affecting the discharge performance of the integrator capacitor during the reset phase. Therefore, this article opted for the more balanced performance of the THS4031 op-amp and DG401 analog switch.

B. Improved Integral Scheme

It is inevitable that active integrators will introduce errors in PCB RCCS. Different compensation schemes are applied, but it is difficult to have a good compensation effect. This is because

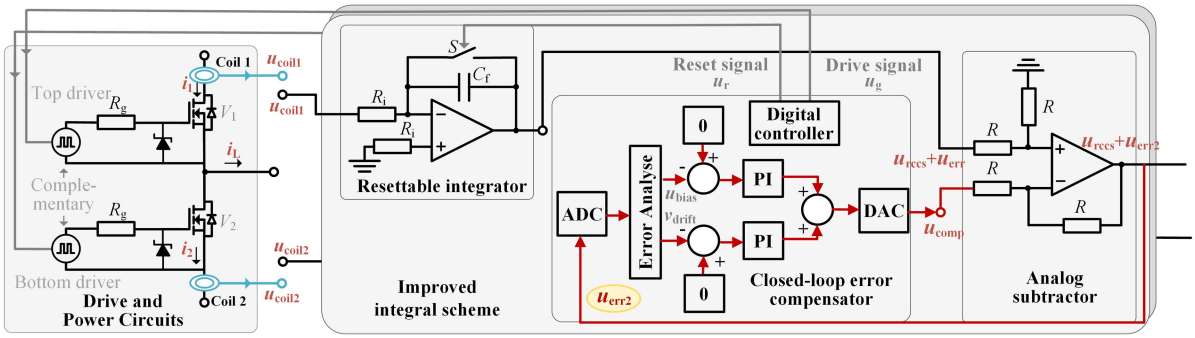

Fig. 9. Topology of the closed-loop error compensation scheme.

most of the methods only offer "open-loop" error compensation [15], [16], [17], [18], [19], while these errors tend to vary greatly across different op-amps and analog switches, even within the same type. In [27], randomly checked 250 op-amp samples and tested the input offset voltage of op-amps. It was found that the difference in input offset voltages among the same batch of op-amps could reach up to 3.2 mV. Additionally, the injected charge Q was also found to vary greatly among analog switches. If the temperature difference is big, the errors in active integrators will be more difficult to predict. Hence, the error compensation scheme for active integrators must have a closed-loop adjustment capability.

A closed-loop error compensation scheme is proposed herein that effectively reduces the integral error of the PCB RCCS without affecting its high-frequency bandwidth. It should be noted that the term "closed-loop" refers to the error loop within the sensor here. As shown in Fig. 9, the compensation circuit can be divided into three parts: 1) resettable integrator, 2) closed-loop error compensator, and 3) analog subtractor. The resettable integrator is connected to the PCB Rogowski coil to restore the switching current information, the results can be represented using u_{rccs}, but its output contains the integral error signal u_{err} of resettable integrator. The closed-loop error compensator is used to generate the reset signal u_{r} driving the reset switch, and the analog compensating signal u_{comp} based on the drive signal u_{g} of power switch. The high-speed subtractor is used to restore accurate switching current information. However, inaccurate compensating signal may introduce compensation deviation u_{err2} into the output results of subtractor.

To achieve closed-loop regulation of integral error, it is necessary to collect compensating deviation signal u_{err2} and control compensating deviation component is 0. The traditional control logic [18], [19] of the resettable integrator is shown in Fig. 10(a) with the compensating signal u_{comp} is 0. It can be observed that the reset signal of integrator u_{r} is the complementary waveform of the switch drive signal u_{g}. In the integral phase, the subtractor output contains both the measured switching current information u_{rccs} and the compensating deviation information u_{err2}. In the reset phase, the subtractor output remains consistently at 0. Therefore, in the traditional control logic, the compensating deviation information u_{err2} cannot be separated from the switching current information u_{rccs}, and the sampled result is not u_{err2} but rather $u_{\mathrm{rccs}}+u_{\mathrm{err2}}$.

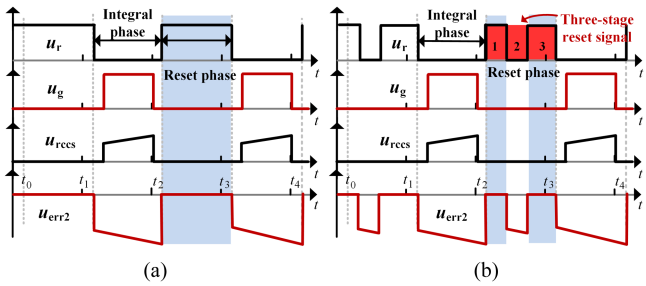

Fig. 10. (a) Traditional control logic. (b) Improved control logic.

The improved control strategy adjusts the logic of the reset signal from a continuous reset signal to a three-stage reset signal without altering the drive signal, as shown in Fig. 10(b). In the first stage, the reset switch is closed, causing the integrator capacitor to discharge and reset the integral error to 0. In the second stage, the reset switch is opened, resulting in integral error. However, as the drive signal u_{g} is low, the restored switching current information u_{rccs} is 0, and the output of the subtractor contains only the compensating deviation information u_{err2}. By controlling the ADC sampling module to sample during the second stage, the u_{err2} and u_{rccs} can be separated. In the third stage, the reset switch closes again, resetting the sensor's integral error to 0, ready for the start of the integral phase.

In addition, since the integral error of the resettable integrator changes with the integration time, and the PI controller can only achieve zero-error tracking for dc quantities, it is not possible to directly achieve closed-loop control of the error signal. This article first separates the error signal into bias error signal u_{bias} introduced by charge injection effect of the reset switch and drift error signal u_{drift} introduced by offset voltage of op-amps, and then constructs two sets of PI controllers for control. The bias error signal u_{bias} remains constant during the integral phase and can be directly controlled using the PI controller, while the drift error signal u_{drift} varies linearly with integral time t and can be represented by drift velocity v_{drift}, which is a dc quantity, as shown in

$$u_{\mathrm{err}} = u_{\mathrm{bias}} + u_{\mathrm{drift}} = u_{\mathrm{bias}} + v_{\mathrm{drift}} \cdot t. \tag{8}$$

The sampling method for the bias error u_{bias} and drift velocity v_{drift} are illustrated in Fig. 11(a). Specifically, sampling is performed only during sampling phase within each switching

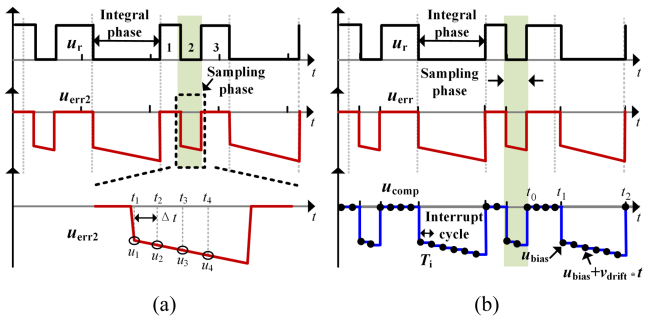

Fig. 11. (a) Sampling method of error signal. (b) Generation method of compensating signal.

cycle. In the sampling phase, four sampling instants are set at t_1, t_2, t_3, and t_4, where the voltage values obtained at these instants are represented as u_1, u_2, u_3, and u_4. It is noted that bias and drift error calculations are updated only when all four sampling instants within the sampling phase are completed. The calculation formulas for the bias error and drift velocity are shown in (9) and (10). A moving average filtering method is employed to calculate the drift velocity to reduce random errors during the sampling process

$$u_{\text{bias}} = u_1 \tag{9}$$

$$v_{\text{drift}} = \left(\frac{u_2 - u_1}{\Delta t} + \frac{u_3 - u_1}{2\Delta t} + \frac{u_4 - u_1}{3\Delta t} \right) /3. \tag{10}$$

To ensure the accuracy of compensation, the compensating signal needs to maintain a high degree of consistency with the error signal in terms of amplitude and time base. In this article, a digital signal processor (DSP) controls the digital-to-analog conversion module DAC to output analog compensating signals, as shown in the control logic in Fig. 11(b). When the integrator is in the reset phase, the compensating signal constantly remains at 0, rises to u_{bias} at the moment the reset switch opens, and gradually increases to $u_{\text{bias}} + v_{\text{drift}} * t$ in the integral phase. It should be noted that the compensating signal u_{comp} generated by the DAC model can only achieve timed updates, and its update rate is controlled by the system interrupt cycle T_{i}. A shorter interrupt period can result in better compensation effects. This section simplifies the compensation program accordingly, enabling interrupt period within 1 μs.

C. Effectiveness of the Closed-Loop Error Compensation

To verify the effectiveness of the closed-loop error compensation scheme, this section first validates its control logic, as shown in Fig. 12. It should be noted that the measured current signal is always 0 at this time. It can be observed that the purple reset signal no longer exhibits continuous reset logic during the reset phase, but instead becomes a three-stage reset signal. During the sampling phase (the second stage), the resettable integrator recommences operation, and the integral errors exist again. By configuring the ADC sampling module to sample only during the sampling phase, the integral error can be isolated from the switching current. The sampling trigger signal is set as shown

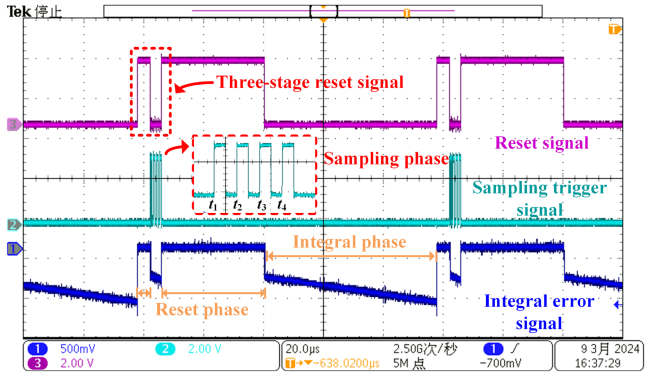

Fig. 12. Improved control logic of resettable integrator.

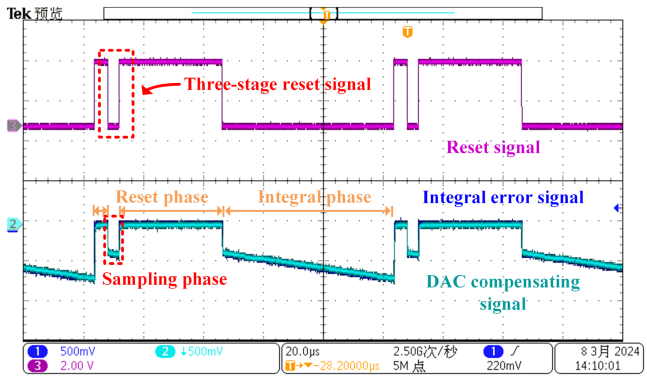

Fig. 13. Effect of error compensation.

in the light blue waveform and the integral error signal is shown in the deep blue waveform. Furthermore, within the sampling phase, four sampling instants, t_1, t_2, t_3, and t_4, are set at 1 μs intervals, and each sampling phase occurs at intervals of one switching cycle. The generated sampling trigger signals follow the same sampling method, as shown in Fig. 11(a), thus allowing for the separation of bias error and drift speed, as indicated by (9) and (10).

Fig. 13 illustrates the compensation effect of the closed-loop error compensation scheme. It can be observed that, whether in the sampling phase or the integral phase, the light blue DAC compensating signal consistently exhibits a high degree of overlap with the deep blue actual integral error signal. Simultaneously, the integral error signal and compensating signal both remain at 0 during the reset phase. This confirms the effectiveness of the closed-loop error compensation scheme.

To verify the real-time tracking capability of the closed-loop error compensation scheme on the integral error signal, this section alters the initial bias and drift component values of the compensating signal to simulate the scenario where the DAC compensating signal tracks the integral error signal during normal operation. The tracking process is depicted in Fig. 14. It can be observed that upon device startup, the bias and drift components of the light blue DAC compensating signal differ significantly from the amplitude of the deep blue integral error signal, resulting in both bias and drift deviation errors in the error compensation outcome. Subsequently, through the fast closed-loop adjustment of the error loop in Fig. 9, the DAC

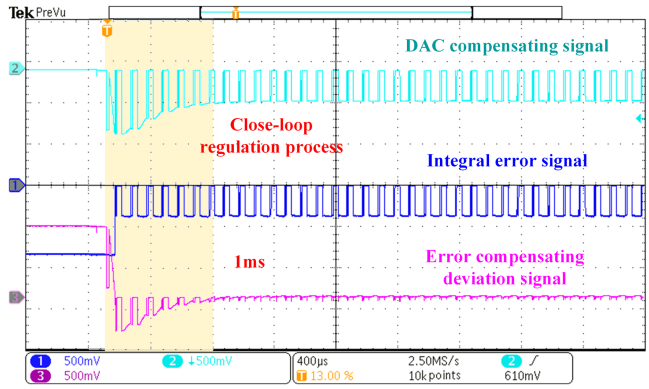

Fig. 14. Closed-loop regulation process of error compensation.

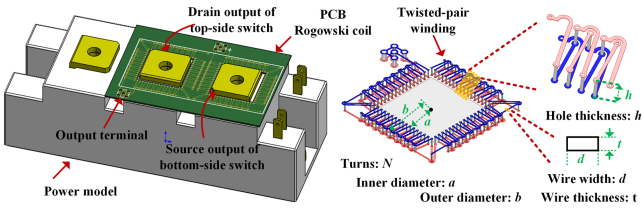

Fig. 15. Geometry structure of PCB Rogowski coil.

compensating signal achieves error correction within 1 ms, demonstrating the real-time adjustment capability of the closed-loop error compensation scheme.

IV. Design of the Hardware Platform

In this section, the parameters and structure of the PCB Rogowski coil current sensor are determined by simulation and test, with a high-frequency bandwidth of 43 MHz and a sensitivity of 0.1 V/A. The sensor's bandwidth is primarily constrained by the coil's high-frequency resonance, while sensitivity requires coordination between the coil and the integrator. In addition, this section successfully integrates the PCB RCCS into a three-phase pulse width modulation (PWM) inverter, and the measured switching current information is utilized for short-circuit protection and current control.

A. Design of PCB RCCS Parameters

The structure of the designed PCB Rogowski coil is shown in Fig. 15. The coil is tightly mounted outside the power module to achieve a better coupling effect, and the drain output terminal of the top-side power switch and source output terminal of the bottom-side power switch are surrounded by coils. In addition, the output terminal of the coil uses microminiature coaxial (MMCX) connectors to ensure superior signal transmission. The geometric parameters of the designed PCB Rogowski coil mainly include turns N, inner diameter a, outer diameter b, hole thickness h, wire width d, and wire thickness t, as shown in Table I.

Meanwhile, there is high electromagnetic noise in the switching process of the power module. Hence, the PCB RCCS needs to have the anti-interference capabilities. This article employs the twisted-pair winding structure [23] in coil, as shown in Fig. 15,

TABLE I
PCB Dimensions of the Coil

Parameter	Symbol	Specification
Number of turns	N	67
Inner diameter	a (mm)	7.5
Outer diameter	b (mm)	10.7
Hole thickness	h (mm)	1.52
Wire thickness	t (OZ)	1
Line width	d (mm)	0.21

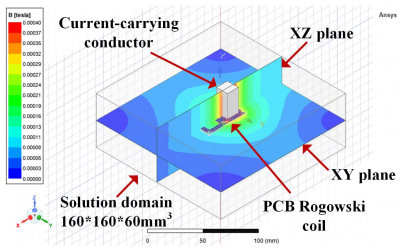

Fig. 16. Magnetic flux density distribution from Maxwell.

TABLE II
Rogowski Coil Parameters: Simulation and Measurement

Parameter	Simulation	Measurement
Mutual inductance M (nH)	8.4	9.3
Parasitic inductance L_S (µH)	0.78	0.736
Parasitic resistance R_S (Ω)	1.43	1.512
Parasitic capacitance C_S (pF)	16.5	19.3
Resonant frequency f_0 (MHz)	44.36	42.2

to reduce the influence of external interference magnetic field. A coaxial structure can reduce the loop area and ground impedance in the signal transmission process and is employed to connect the coil to the integrator.

After the designed PCB Rogowski coil has been drawn in Altium Designer, it can be imported into Ansys Maxwell to analyze parasitic parameters, as shown in Fig. 16. First, an air solution domain of $160\times160\times60$ mm^3 is established, and the PCB Rogowski coil is in the center of the solution domain. The current-carrying conductor is perpendicular to the coil plane and tangent to the upper and lower solution domains. The size of the current to be measured is set to 30 A, the frequency is set to sweep from 10 kHz to 100 kHz, and the eddy current field analysis is carried out on the horizontal XY plane and the vertical XZ plane. The simulation results are shown in Table II.

The simulations can provide preliminary guidance for coil design, but due to the limitations of grid size and modeling accuracy, there are certain errors in the results. The accurate parasitic parameters and frequency characteristic curve of the PCB Rogowski coil can be obtained by vector network analyzer BODE100. In one-port mode, the BODE100 source terminal is directly connected with the output terminal of the coil through the RF coaxial cable and MMCX-BNC coaxial adapter, as shown in Fig. 17(a). Specifically, "RF" denotes the coaxial cable model connecting the coil to the integrator, and "MMCX-BNC" indicates the adapter from MMCX interface (coil) to BNC interface

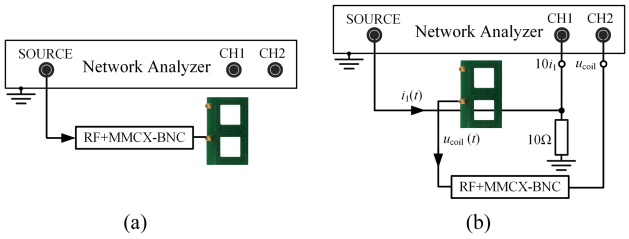

Fig. 17. Frequency response test platform for PCB RCCS. (a) One-port mode. (b) Transfer function mode.

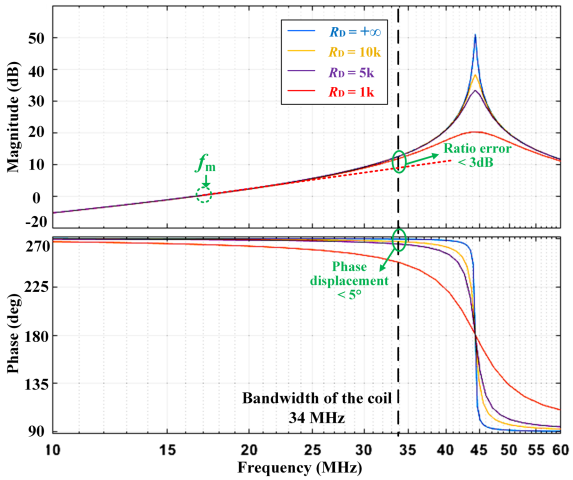

Fig. 18. Frequency response of the PCB Rogowski coil with various damping resistances.

(Bode100). The measured parasitic inductance, resistance, and capacitance of the coil are shown in Table II. Despite some errors between experimental and simulated results due to limitations in simulation modeling and solution network, the simulation can still offer valuable guidance for the design and optimization of coils.

The transfer function of the PCB Rogowski coil can be represented by (3) when using the lumped parameter model. A more precise method involves directly measuring its frequency response curve using the BODE100 transfer function mode, as shown in Fig. 17(b). The sine sweep signal is emitted from the source terminal of the BODE100 and is grounded through a 10 Ω resistor to simulate the current to be measured $i_1(t)$, and the CH1 interface indirectly obtains $i_1(t)$ by sampling the voltage of the 10 Ω resistor. The output end of the coil is connected to CH2 to provide the induced voltage of the coil. BODE100 plots the frequency characteristic curve of the coil and the current-carrying conductor by calculating the ratio of the induced voltage to the measured current.

The frequency characteristic curve of the PCB Rogowski coil can be obtained by (11), as indicated in Fig. 18. Assuming the intersection frequency of the coil frequency response curve with the 0 dB horizontal line is denoted as f_m, the mutual inductance M between the coil and the current-carrying conductor can be expressed, as shown in (12).

In addition, the impact of the damping resistor on the high-frequency characteristics of the coil is illustrated using examples of 1 kΩ, 5 kΩ, 10 kΩ, and $+\infty$ resistors. As the damping resistance R_D decreases, the ratio error of the coil becomes smaller, but the phase error becomes larger. Therefore, the selection of damping resistors needs to balance the ratio error and phase error [24]. A 5 kΩ damping resistance is adopted, and the high-frequency cutoff frequency is regarded as 34 MHz in this article. At this point, the ratio error is less than 3 dB, and the phase error is less than 5°. It is noted that, to mitigate the impact of the integrator circuit on the coil resonance characteristics, a voltage follower is inserted between the coil and the integrator because it is characterized by infinite input impedance and infinitesimal output impedance

$$\frac{U_{\text{coil}}(s)}{i_1(s)} = \frac{10U_{\text{CH2}}(s)}{U_{\text{CH1}}(s)} \tag{11}$$

$$M = \frac{1}{2\pi f_m}. \tag{12}$$

The resettable integrator, during the integral phase, can be equivalently modeled as an ideal integrator, hence, its high-frequency bandwidth primarily depends on the bandwidth of the op-amp. In this article, THS4031 is chosen with a bandwidth of 100 MHz. Moreover, the amplification factor of the integrator depends on the values of the input resistance and integrator capacitor, which need to be coordinated with the mutual inductance of the coil to set the sensor's sensitivity, as shown in (13), where S_{RCCS} is the sensitivity of the sensor, R_i is input resistance, C_f is integrator capacitor. R_i is set to 1 kΩ, the C_f is set to 43 pF here, and the sensitivity of PCB RCCS is ensured to be 0.1 V/A

$$S_{\text{RCCS}} = \frac{M}{R_i \cdot C_f}. \tag{13}$$

To sum up, the bandwidth of the PCB Rogowski coil is limited to 34 MHz due to parasitic inductance and capacitance resonance. The high-frequency bandwidth of the resettable integrator is constrained by the op-amp's bandwidth of 100 MHz. The closed-loop error compensator mitigates integral errors through an analog subtractor, thus, not affecting the sensor's high-frequency bandwidth. The sampling frequency during the sampling phase only affects the precision of error acquisition and compensation. Therefore, the proposed PCB RCCS in this paper has a bandwidth of 34 MHz.

B. Integrated Design of Rogowski Coil and Three-Phase Inverter

The three-phase inverter with integrated PCB Rogowski coil current sensor is illustrated in Fig. 19. The bus capacitor is composed of 5 sets of series-connected capacitors with a voltage rating of 450 V and a capacitance of 220 μF, arranged in parallel to meet the voltage withstand and ripple requirements of the bus. The half-bridge power module utilizes the IGBT FF150R12RT4, with heatsinks mounted on the lower side for cooling facilitated by a fan. The filtering circuit employs an *LCL* third-order filtering circuit, which exhibits superior harmonic suppression capability while maintaining a smaller size and lower cost.

To ensure that the Rogowski coil can effectively capture the magnetic field of the current to be measured, the PCB Rogowski

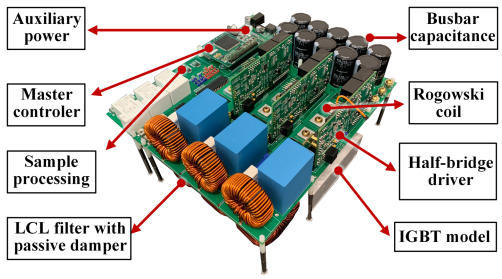

Fig. 19. Three-phase inverter integrated PCB RCCS.

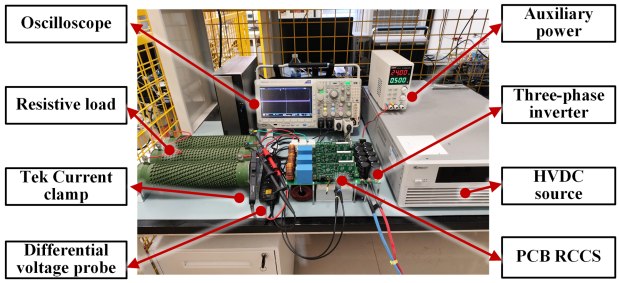

Fig. 20. Test setup with three-phase inverter.

coil is positioned closely to the IGBT module terminals and connected to the designed half-bridge driver board through a coaxial transmission line. Due to their fixed relative positions, the mutual inductance of PCB Rogowski coils exhibits minimal variation in experimental conditions. This section integrates the resettable integration processing circuit, error compensation circuit, short-circuit protection circuit, phase current reconstruction circuit, and drive circuit into the half-bridge driver.

The experimental platform is conducted, as shown in Fig. 20. A 10 Ω three-phase resistor load is applied on the ac side, with a dc voltage of 400 V and auxiliary power of 24 V. Phase current and switching current are compared using the Tek current clamp TCP0030A, while voltage is measured using the Tek THDP0200 differential probe.

The control logic of the three-phase PWM inverter system is depicted in Fig. 21. The outer loop consists of the current loop for the three-phase PWM inverter, where the reconstructed three-phase phase currents are transformed into direct and quadrature axis signals via Park transformation, and the magnitude and phase angle of the output current are controlled by a PI controller to achieve the desired current. Subsequently, the information is converted into duty cycle signals to generate PWM waves that control the three-phase inverter to produce three-phase ac power, which is then transmitted to the load.

The inner loop represents the error loop of the PCB RCCS. The DSP collects the compensating deviation signal from the sensor, analyzes the bias and drift errors, and utilizes PI controllers for closed-loop control to generate real-time self-adjusting error compensating signals. Simultaneously, the measured switching current signal is employed in the short-circuit protection circuit of power devices, ensuring reliable protection of the three-phase system through shutdown drive signals.

V. Experimental Analysis

In this section, the analysis of the switching current measurement effectiveness of the proposed PCB RCCS is conducted under actual operating conditions. Additionally, the short-circuit protection and current control effect based on the PCB RCCS are validated. Experimental results indicate that the proposed PCB RCCS can accurately measure transient and steady switching currents, achieve reliable power switch protection within 1 μs, and demonstrate excellent performance in load transition experiment and harmonic injection experiment.

A. Comparison of the Switching Current Measurement Results

This section analyzes the switching current measurement results of the PCB RCCS in a three-phase PWM inverter, with the test waveform shown in Fig. 22. The experiment is conducted with a 400 V dc busbar voltage, 10 kHz switching frequency, and load resistance. Due to the bandwidth of the commercial current probe TCP0030A being 120 MHz, its measurement results can be used as a reference. It can be observed that the measurement results of the proposed PCB RCCS closely match those of the commercial current probe within one switching cycle, as shown in Fig. 22, showing no significant bias error or drift error. This validates the excellent effectiveness of the proposed closed-loop error compensation scheme. It should be noted that due to the reverse recovery process of the free-wheeling diode, there is a significant current overshoot in the measured IGBT switching current. Fig. 22 also presents details of the turn-ON and turn-OFF current transient. The proposed PCB RCCS performs well in measuring current at the edge of switching transition, confirming the outstanding high-frequency measurement performance of the current sensor. Additionally, the sensitivity of the proposed PCB RCCS is 0.1 V/A, consistent with the parameter design in Section IV, as shown in (13).

The switching current waveform data within one power frequency cycle saved in the oscilloscope is imported into MATLAB for spectral analysis, enabling further testing of the measurement capabilities of the proposed PCB RCCS at multiple frequencies. The frequency distribution of the measurement results is shown in Fig. 23 between the commercial current clamp and the proposed PCB RCCS. It can be observed that the switching current information contains not only low-frequency current data but also higher frequency harmonic current information at the switching frequency and above. Within 10 times the switching frequency range (100 kHz), the proposed PCB RCCS achieves a measurement accuracy comparable to the commercial current clamp, while offering significant advantages in terms of size, cost, and integrability.

B. Verification of Protection and Control Effects

In this section, the proposed PCB RCCS is first applied to system short-circuit protection, achieving fast and reliable protection of power switches. The effectiveness of the short-circuit protection is shown in Fig. 24. It can be observed that the proposed PCB RCCS accurately measures the short-circuit current, matching the results obtained from the commercial

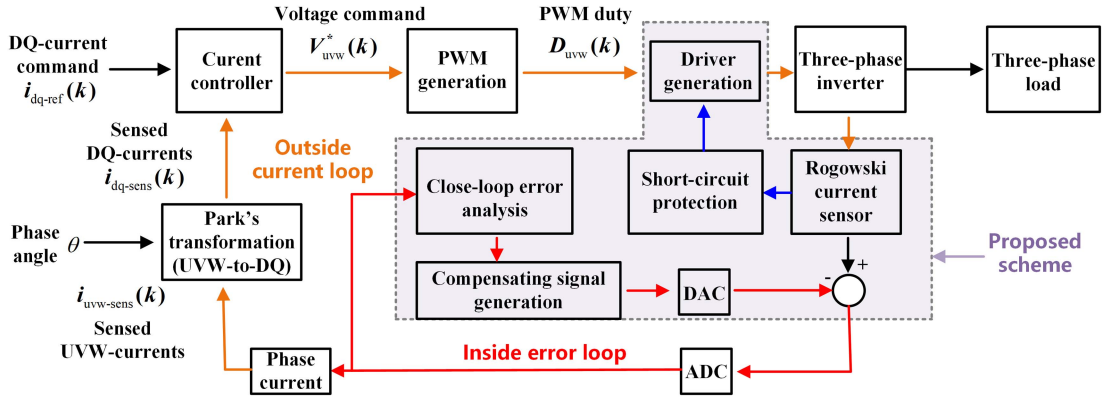

Fig. 21. Control strategy for current control of three-phase inverter with proposed PCB RCCS.

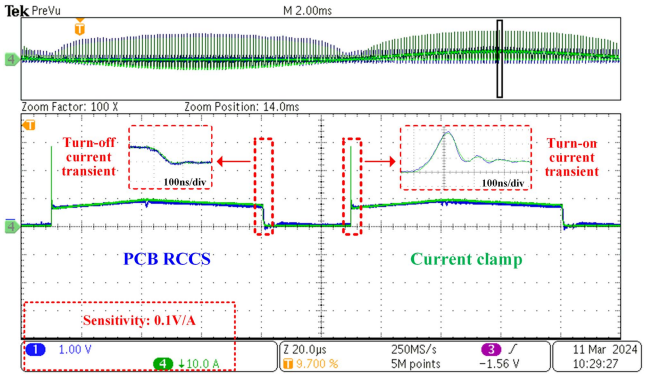

Fig. 22. Comparison between the current clamp and PCB RCCS.

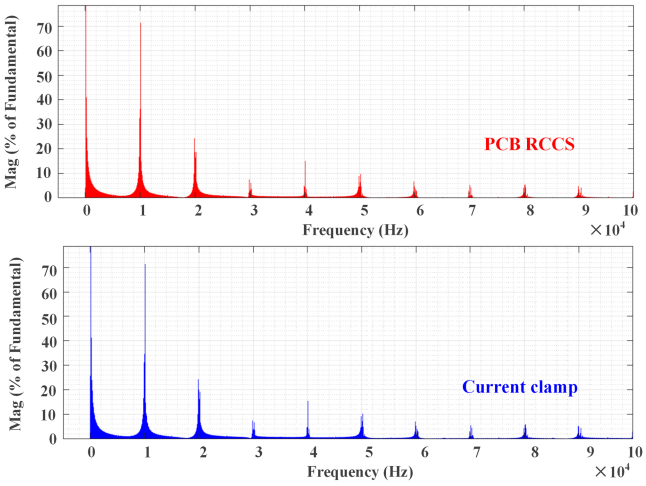

Fig. 23. Frequency distribution of measured current by MATLAB.

current clamp. Following the occurrence of a short-circuit fault, the short-circuit current reaches the set protection threshold of 70 A after 400 ns. The designed short-circuit protection circuit successfully ensures the reliable protection of the device within 750 ns. Furthermore, to reduce the voltage overshoot peaks generated during protection, thus avoiding device overvoltage damage, a soft turn-OFF protection circuit is incorporated into the short-circuit protection circuit in this section [25]. By reducing

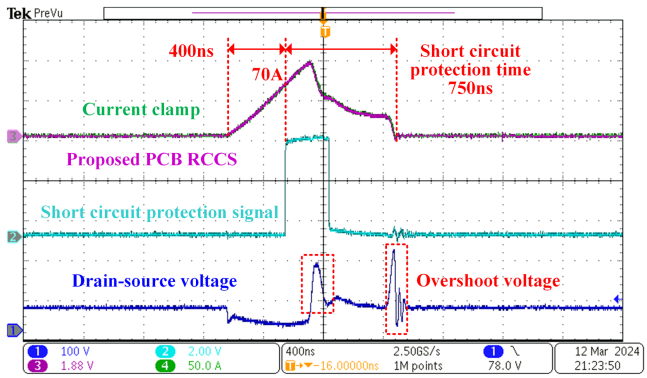

Fig. 24. Short-circuit protection based on PCB RCCS.

the drive voltage to decrease the rate of current decay, the voltage overshoot is divided into two stages for release, further enhancing the reliability of power switches. It should be noted that the insertion of a two-stage soft turn-OFF protection circuit results in an extended protection duration. However, the protection time can be adjusted according to practical needs using an *RC* delay circuit. The chosen 750 ns protection time in this article ensures device reliable protection while effectively reducing overshoot in the drain-source voltage.

In addition, based on the waveform reconstruction principle [5], this section utilizes the upper and lower switching current signals to reconstruct the phase current information. The principle is illustrated in Fig. 1, and the reconstructed phase current waveforms are shown in Fig. 25. It can be observed that the reconstructed phase current waveforms exhibit a high degree of consistency in terms of amplitude and phase with the measured waveforms, and the switching ripples can also be accurately reconstructed. Furthermore, after simple low-pass filtering, accurate load-side current information can be obtained for system current control, enabling the replacement of traditional Hall current sensors.

The closed-loop current control experiment is conducted to test the effect of taking PCB RCCS for control. Fig. 26 shows the results of the load transient test. The controlled direct-axis current changes from 0 A to 1 A and changes from 1 A to 5 A. Direct-axis current information is outputted through DAC,

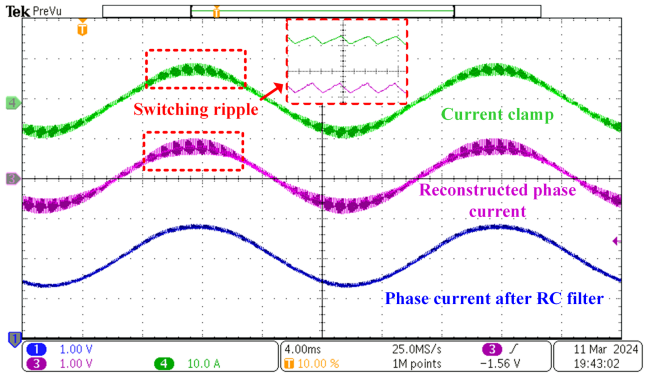

Fig. 25. Phase current waveform reconstruction effect.

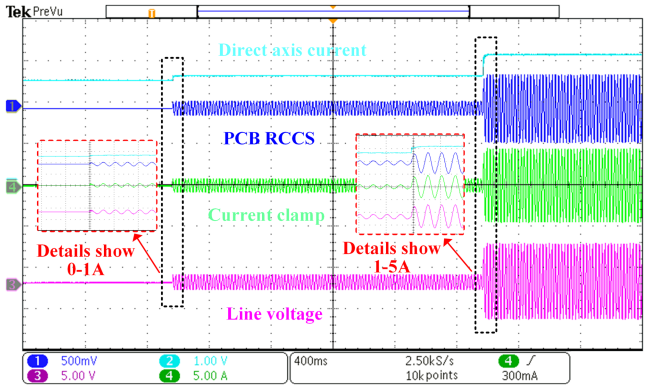

Fig. 26. Load jumping from 0 A to 1 A and from 1 A to 5 A.

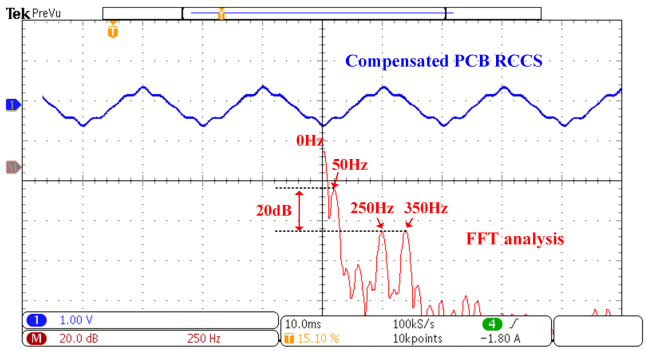

Fig. 27. Measurement of third, fifth, and seventh harmonic.

and line voltage is measured by voltage probe THDP0200. It is obvious that the control of closed-loop using PCB RCCS is stable and accurate. The edge of load jumping is also smooth, which verifies the performance of PCB RCCS in the current closed-loop control.

The power frequency of the above experiments is 50 Hz. To verify the performance of measuring current low-frequency harmonics, 0.1 times the third, fifth, and seventh harmonic are injected in modulation. The measured waveform and fast Fourier transform results are shown in Fig. 27. It can be observed that the amplitudes at frequencies of 0 Hz, 50 Hz, 250 Hz, and 350 Hz component is significant. Especially, the 0 Hz component in results is caused by 1.5 V bias voltage to be sampled by DSP, and the third harmonic (150 Hz) is canceled out in three-phase

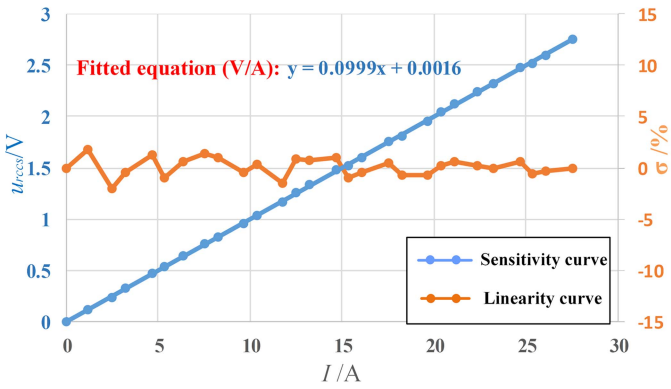

Fig. 28. Result of sensitivity and linearity of PCB RCCS.

inverter system. The amplitude of the fundamental wave differs from fifth and seventh harmonic (250 Hz, 350 Hz) by 20 dB meaning that the multiple difference between them is 0.1 times. The experimental results aligned with the established settings in control program, thereby substantiating the performance of the designed PCB RCCS.

The test of sensitivity and linearity is conducted, as shown in Fig. 28. The I, u_{rccs} is the effective value of phase current signal measured by current clamp and proposed PCB RCCS, and the σ is the linearity, as shown in (14). The experimental result (0.0999) closely matches the targeted sensitivity (0.1) outlined by the design, thus confirming the reasonability and accuracy of the above design procedures. In addition, it can be observed that the linearity σ of the proposed PCB RCCS decreases with increasing measured current, and is consistently confined to within 3%, demonstrating the performance of the designed PCB RCCS

$$\sigma = \frac{u_{\mathrm{rccs}} - 0.1 \cdot I}{0.1 \cdot I} \cdot 100\%. \tag{14}$$

VI. Conclusion

This article proposed a PCB RCCS integrated into the three-phase PWM inverter, with a closed-loop error compensation method based on ensuring the sensor's measurement bandwidth. Compared to traditional error compensation methods, this method can automatically collect compensation deviation signal during actual operation and adjust compensating signal in real time, offering advantages such as high compensation accuracy, short response time, and strong adaptability. Moreover, this article modified the traditional reset signal to a three-stage reset signal achieving the separation of compensation deviation information from restored switching current information.

In addition, by employing a combined approach of Ansys simulation and Bode100 testing, the parasitic parameters and resonant frequency of the coil are evaluated. Concurrently, the performance of resettable integrator is analyzed to guide effective device selection. Results demonstrate that the proposed PCB RCCS achieves a high-frequency bandwidth of 34 MHz with a sensitivity of 0.1 V/A. Additionally, a closed-loop error compensation circuit is designed to reduce integral errors in

sensors, and short-circuit protection and closed-loop control of a three-phase inverter are achieved through a two-stage soft turn-OFF method and waveform reconstruction method. Experimental results indicate that the proposed PCB RCCS can accurately measure the switching current information of IGBTs and exhibit excellent performance in hard-switching short-circuit experiment, load step experiment, low-frequency harmonic injection experiment, and linearity testing. Additionally, the three-phase inverter platform developed in this article can serve as a valuable reference for the high integration of PCB RCCS. Further research is required to focus on developing even more low parasitic parameter structures of PCB Rogowski coil to meet the demands of higher bandwidth measurements, as wide band-gap devices continue to advance.

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