A 96.3% Efficient, 6mV$_{pp}$ Line Transient Response Time-Based Boost Converter With Feedback-PID for AMOLED Displays

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***Abstract*—In this article, a time-based boost converter with line feedforward for active matrix organic light emitting diode displays is presented. The time-based control features a novel feedback-proportional–integral–derivative (F-PID) structure, which enables to implement a line feedforward compensation with negligible impact on the controller area occupation. Moreover, the differential VCO employed in the proposed F-PID has a much larger gain compared with that of a conventional time-based PID structure, providing a considerable reduction in the output voltage offset related to the frequency mismatch. A 900 mA prototype converter with 2.3–4.8 V input and 5 V output voltage, fabricated in a 180 nm BCD process, shows an up to 6× reduction in the line transient response when compared with a peak-current-mode boost converter for the same application. The die area is 4.1 mm^2, while the controller occupies only 0.21 mm^2, which is almost 30% smaller compared with other published and commercially available products.**

***Index Terms*—Boost converter, fast response, feed-forward, feedback-proportional–integral–derivative (F-PID), high efficiency, time-based control.**

I. Introduction

ACTIVE matrix organic light emitting diode (AMOLED) displays are being broadly used in portable devices owing to their high resolution, low power consumption, and low cost [1], [2]. Fig. 1 shows the power management system and the typical two thin-film transistors (TFT) and one storage capacitor pixel-level driving circuit of an AMOLED display [3], [4], [5]. The driving TFT operates as a current source and converts the data voltage stored on the storage capacitor (CST) to the amount of current required to produce a given luminance. The data voltage is set by an appropriate circuit and applied to the source of the switching TFT. The whole driver requires a pair of bipolar voltage supplies, V_P and V_N and an auxiliary voltage supply, AV_{DD} [4]. Those voltage supply rails can be generated by single inductor multiple outputs (SIMO) converters [6], [7], [8] or by power management integrated circuits (PMIC) [9], [10], which incorporate a buck–boost and two boost converters. The architecture choice is mainly restricted by the maximum load current required by the target application. Indeed, SIMO converters are substantially limited by the right-half-plane (RHP) zero [6], which is related to the large conversion ratio. In recent years, SIMO converters were proposed [7], [8] to improve the power density of AMOLED power supplies, employing hybrid topologies. However, the use of flying capacitors and additional switches can enhance the power density at the cost of reduced efficiency, making those solutions less suitable for portable applications. Thus, for applications, such as smartphones and small tablets, a preferable approach is to use a PMIC with two separate boost converters and one buck–boost converter. The positive supply rail, V_P, is the most critical one, since any voltage variation on this rail changes the gate–source voltage of the TFT current source, notably affecting the display quality [5]. As sketched in Fig. 1, large voltage disturbances occur on the power distribution bus upon sudden current requests from other

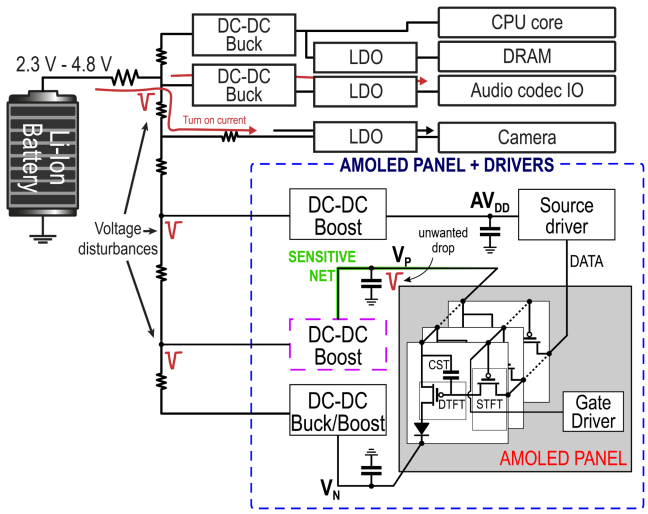

Fig. 1. Block diagram of the power management architecture for a portable device. AMOLED panel subsystem is shown in the dashed box.

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loads. If not properly compensated, these voltage variations could cause disturbances on V_P, resulting in screen flickering. Therefore, a tightly regulated boost converter with fast line transient response is required in high-quality AMOLED displays. Moreover, low quiescent current and high conversion efficiency are essential to avoid thermal management issues and to extend the battery runtime.

Time-based signal processing [6], [11], [12], [13], [14], [15] proved to be a valuable control approach for applications requiring reduced area occupation and power consumption, as the power-hungry error-amplifier and the pulsewidth modulator (PWM) are removed. Coding the information in the time interval between events is a promising strategy to avoid constraints related to the limited headroom in scaled technology nodes. Time-based control, indeed, employs CMOS-level signals, as for digital control, but without introducing any quantization. Unfortunately, the closed-loop bandwidth of boost converters operating in continuous conduction mode (CCM) is limited by the RHP zero in their *control-output* transfer function [16], [17], resulting in poor line transient response.

With PWM current-mode (CM) control [16], [18], the bandwidth limitation caused by the RHP zero remains unchanged in CCM operation. However, CM control has an inherent input voltage feedforward characteristic [19], [20], leading to an improved open-loop dc and dynamic line regulation. On the downside, robust and precise inductor current sensing is needed in CM controllers. OFF-chip current sensing [21] is ruled out in applications requiring a minimum number of external passive components. ON-chip current sensors monitor the switch current as an approximation of the inductor current. They are typically half-wave sensors that only track the current of the switch during a single PWM phase, whereas they are reset during the opposite phase. This poses challenging bandwidth and a settling time requirements to the current sensing amplifiers, leading to a stringent tradeoff between accuracy and power consumption [22], [23]. ON-chip indirect current sensing techniques have been proposed in combination with time-based control [12] resulting, however, in poor load regulation.

A more effective strategy to achieve a good line response combines voltage-mode feedback and input-voltage feedforward control. Feedforward control is accomplished by sampling the converter input voltage and using this signal to control the duty cycle [24], [25], [26], [27], providing the main part of voltage regulation. Negative feedback is used to clean up only the imperfections of the feedforward control. Unfortunately, the well-known feedforward techniques exploited in voltage-based analog controllers rely on the presence of the PWM [24], [25], [26], which is not available in time-based controllers. A straightforward extension of the technique reported in [25] to the time-based realm has been introduced in [14]. Nevertheless, this solution requires additional voltage-controlled delay-lines (VCDLs) having a linear voltage-to-delay characteristic over the whole input voltage range, leading to extra area occupation and increased power consumption.

To overcome the abovementioned issues, in this article, we present a time-based boost converter with a novel proportional–integral–derivative (PID) control architecture referred to as feedback PID (F-PID). The F-PID has two distinct advantages over the standard time-based PID (T-PID): 1) It provides an alternative path for the feedforward signal that avoids using additional wide-range linear VCDLs, thus substantially reducing both controller area occupation and power consumption; 2) it allows to strongly reduce the impact of the frequency mismatch between the voltage-controlled oscillators (VCOs), resulting in a lower offset on the output voltage [28].

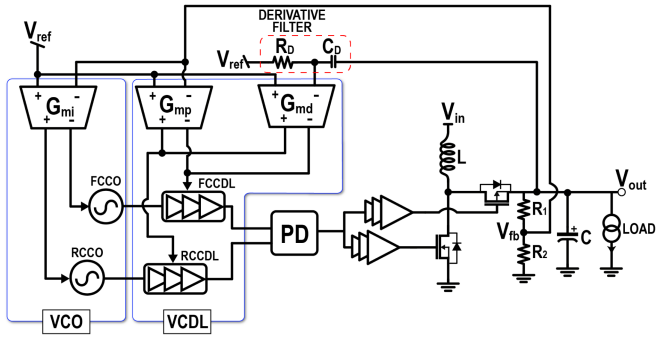


Fig. 2. Block diagram of a boost converter with time-based PID compensator.

The proposed technique demonstrates an up to 6× reduction in the line transient response and a 30% reduction in the controller area, with respect to other published and commercially available boost converters for the same application.

The rest of this article is organized as follows. Section II provides an overview of the time-based control in dc–dc converters and introduces the small signal model of the boost converter in CCM. In Section III, the proposed F-PID compensator is described, and the feedforward transfer function is carried out. Section IV illustrates the transistor-level implementation of the main building blocks. Measurement results for the prototype boost converters are presented in Section V. Finally, Section VI concludes this article.

II. Boost Converter With Time-Based PID Control

The block diagram of a boost converter with time-based PWM control is shown in Fig. 2.

A. Time-Based PID Compensator

The T-PID compensator is composed of two main subblocks: a VCO and a VCDL. The VCO is implemented by combining a differential transconductor and two current-controlled-oscillators (CCOs), namely, FCCO and RCCO. The input to the transconductor is the error voltage, $v_e(t) = v_{\text{out}}(t)/N - V_{\text{ref}}$, where $1/N = R_2/(R_1 + R_2)$ is the scaling factor given by the voltage divider at the converter output, and V_{ref} the reference voltage. The VCO acts as a voltage-to-phase integrator with transfer function, $G_{\text{I}}(s)$, given by

$$G_{\text{I}}(s) = \frac{\tilde{\Phi}_{\text{vco}}(s)}{\tilde{v}_e(s)} = \frac{G_{mi} \cdot K_{\text{CCO}}}{s} \tag{1}$$

where $\tilde{\Phi}_{\text{vco}}$ and $\tilde{v}_e$ are the small-signal ac phase difference between the two CCO outputs and the small-signal ac error

voltage, respectively, and G_{mi} is the integral transconductance. The differential architecture is basically meant to prevent the steady-state switching frequency of the CCOs from changing with the output voltage [11].

The proportional transfer function is obtained with the VCDL subblock, implemented by combining a differential transconductor and two current-controlled delay lines (CCDLs), namely, reference current-controlled delay line (RCCDL) and feedback current-controlled delay line (FCCDL). The VCDL takes the VCO differential output signal as an input, adding to it a delay proportional to the applied differential control current. This current is generated by the transconductor, G_{mp}, and it is proportional to error voltage v_e, leading to a voltage-to-phase transfer function given by

$$G_{\rm P}(s) = \frac{\tilde{\Phi}_{\rm vcdl}(s)}{\tilde{v}_e(s)} = G_{mp} \cdot K_{\rm CCDL}\ . \tag{2}$$

The derivative transfer function can be implemented both in time-domain [29] or in the voltage domain [11] (as shown in Fig. 2) with a simple high-pass filter (HPF). The filtered voltage is then converted into a differential current signal via the transconductor G_{md}, and injected in the same CCDLs used for the proportional gain. The derivative transfer function can be written as follows:

$$G_{\rm D}(s) = \frac{\tilde{\Phi}_{\rm vcdl}(s)}{\tilde{v}_{\rm out}(s)} = \frac{\frac{s}{\omega_{\rm D}}}{1+\frac{s}{\omega_{\rm D}}} \cdot G_{md} \cdot K_{\rm CCDL} \tag{3}$$

where $\omega_{\rm D} = 1/(C_{\rm D}R_{\rm D})$ is the angular frequency of the pole in the derivative path. The outputs of the two CCDLs are then used to generate the PWM signal by means of a phase-detector (PD). Different from the PWM generator used in the digital and voltage-mode control, this component is a simple digital gate with negligible impact on power consumption and area occupation.

B. Boost Converter Small-Signal Transfer Functions

The state-space averaged model [16] for a boost converter operating in CCM predicts a small-signal *duty-cycle-to-output* transfer function given by

$$G_{\rm od}(s) = G_{\rm od}(0)\frac{\left(1-\frac{s}{\omega_{z,rhp}}\right)\left(1+\frac{s}{\omega_{z,lhp}}\right)}{\left(\frac{s^2}{\omega_0^2}+\frac{s\cdot 2\zeta}{\omega_0}+1\right)} \tag{4}$$

where

$$G_{\rm od}(0) = \frac{V_{\rm out}}{D'} \cdot \frac{(RD'^2 - r)}{(RD'^2 + r)} \tag{5a}$$

$$D' = 1 - D = \frac{V_{\rm in}}{V_{\rm out}} \cdot \eta \tag{5b}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \cdot \sqrt{\frac{RD'^2 + r}{R}} \tag{5c}$$

$$Q = \frac{\sqrt{LC \cdot (R + r_{\rm C}) \cdot (RD'^2 + r)}}{C(r(R + r_{\rm C}) + RD'^2 r_{\rm C}) + L} \tag{5d}$$

$$\omega_{z,\rm lhp} = \frac{1}{C \cdot r_{\rm C}} \tag{5e}$$

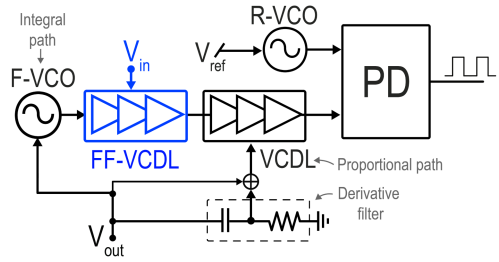


Fig. 3. Straightforward implementation of line feedforward in a T-PID compensator, exploiting an additional CCDL.

$$\omega_{z,\rm rhp} = \frac{(RD'^2 - r)}{L}. \tag{5f}$$

In the above equations, R is the load resistor, D is the duty-cycle of the converter, ω_0 is the angular frequency of the *LC* filter with quality factor Q, $r_{\rm C}$ is the capacitor series resistance, η is the converter efficiency, and $r = r_{\rm L} + R_{\rm ON,HS} \cdot D + R_{\rm ON,LS} \cdot (1 - D)$ is an equivalent average resistance [30] including the parasitic resistances of the inductor, $r_{\rm L}$ and of the power MOSFETs, $R_{\rm ON,HS}$ and $R_{\rm ON,LS}$. The open-loop *line-to-output* transfer function, $G_{\rm ol,OL}$, which describes the boost converter response to a variation of the input voltage is given by

$$G_{\rm ol}(s) = \frac{1}{D'}\frac{RD'^2}{(RD'^2 + r)} \cdot \frac{\left(1+\frac{s}{\omega_{z,\rm lhp}}\right)}{\left(\frac{s^2}{\omega_0^2}+\frac{s}{\omega_0 Q}+1\right)}. \tag{6}$$

To the purpose of this work, the left-half-plane zero, $\omega_{z,\rm lhp}$ will be neglected, assuming its angular frequency being much higher than the loop crossover frequency. This is a reasonable assumption if multilayer ceramic capacitors are used, being their equivalent series resistance in the order of a few mΩ.

III. Time-Based F-PID With Line Feedforward

As shown in Fig. 2, time-based control eliminates the PWM, relying on a simple PD with fixed gain $G_{\rm PD} = 1/2\pi$ [11]. As a consequence, the feedforward compensation technique typically adopted in analog controllers [25] cannot be applied to time-based controllers to improve the converter line transient response. The straightforward extension of [25] to a time-based controller, introduced in [14], is depicted in Fig. 3. The input voltage forces the delay of the feedforward VCDL (FF-VCDL) resulting in an additional phase-shift at the PD input equal to

$$\Phi_{\rm FF}(t) = 2\pi \cdot (1 - v_{\rm in}(t)/V_{\rm out}). \tag{7}$$

However, the effective duty-cycle

$$d(t) = 1 - v_{\rm in}(t)/V_{\rm out} \cdot \eta \tag{8}$$

at which the boost is operating shows a dependence on the converter's efficiency, η, that cannot be estimated. Thus, the feedforward phase-shift, $\Phi_{\rm FF}$, only allows for a coarse correction of the duty-cycle based on the input voltage. This approximation gives rise to a small phase-shift estimation error

$$\Phi_e(t) = 2\pi \cdot d(t) - \Phi_{\rm FF}(t) = 2\pi(1-\eta) \cdot v_{\rm in}(t)/V_{\rm out} \tag{9}$$

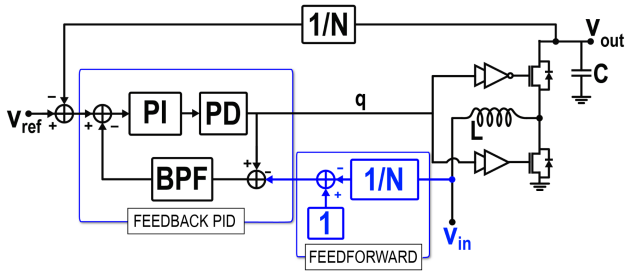


Fig. 4. Block diagram of the proposed boost converter with F-PID and line feedforward compensation.

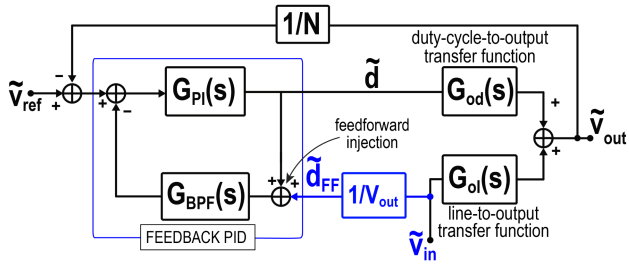


Fig. 5. Small-signal averaged model of the proposed F-PID with line feedforward compensation.

which is adjusted by the control loop by adding a phase contribution, $\Phi_{\text{PID}} = \Phi_\epsilon$, at the PD input. The overall phase-shift at the PD input, Φ_{PD} is therefore given by a dominant feedforward and a minor feedback contribution

$$\Phi_{\text{PD}}(t) = \Phi_{\text{FF}}(t) + \Phi_{\text{PID}}(t) = 2\pi \cdot (1 - v_{\text{in}}(t)/V_{\text{out}} \cdot \eta). \tag{10}$$

This solution, however, requires the additional FF-VCDL to be linear over the whole input voltage range, at the cost of extra area occupation and power consumption.

Fig. 4 shows the block diagram of an alternative implementation of a PID controller, referred to as F-PID in the following. The F-PID controller has been specifically devised to provide an alternative line feedforward path, which turns out to be particularly useful in a time-based architecture.

The forward block is a proportional–integral (PI) filter with transfer function $G_{\text{PI}}(s)$, namely

$$G_{\text{PI}}(s) = \frac{K_{\text{I}}}{s}\left(1 + \frac{s}{\omega_{\text{PI}}}\right) \tag{11}$$

where the gain of the PD has been incorporated into the integral factor, K_{I}. The feedback block is a band-pass filter (BPF) with transfer function

$$G_{\text{BPF}}(s) = \frac{sK_{\text{B}}}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)} \tag{12}$$

having a gain $K_{\text{B}} = K_0/\omega_1$ and two poles having angular frequencies ω_1 and ω_2. This controller configuration, assuming $K_{\text{I}} \cdot K_{\text{B}} \gg 1$, is equivalent to a PID with transfer function $G_{\text{F-PID}}$ equal to

$$G_{\text{F-PID}}(s) = \frac{G_{\text{PI}}(s)}{1 + G_{\text{PI}}(s)G_{\text{BPF}}(s)} \simeq \frac{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)}{s \cdot K_{\text{B}}\left(1 + \frac{s}{\omega_{\text{P}}}\right)} \tag{13}$$

where the zero of the PI compensator cancels with the pole generated by the interaction between the BPF and the PI itself, and the high-frequency pole angular frequency, ω_{P} is given by

$$\omega_{\text{P}} = \frac{K_{\text{I}}K_{\text{B}} \cdot \omega_1\omega_2}{\omega_{\text{PI}}}. \tag{14}$$

The small signal average model of a boost converter with time-domain F-PID controller and line feedforward is shown in Fig. 5. The feedforward signal $\tilde{d}_{\text{FF}} = -\tilde{v}_{\text{in}}/V_{\text{out}}$, induced by an input voltage variation $\tilde{v}_{\text{in}}$, is injected at the BPF input. The transfer function from the feedforward injection point to the PD output, $G_{\text{FF}}(s)$, is

$$G_{\text{FF}}(s) = -\frac{G_{\text{BPF}}(s) \cdot G_{\text{PI}}(s)}{1 + G_{\text{PI}}(s) \cdot G_{\text{BPF}}(s)} \tag{15}$$

which shows a unity gain and a high frequency pole at ω_{P}. Therefore, the system is able to correct the duty-cycle also in the presence of fast variations of v_{in}.

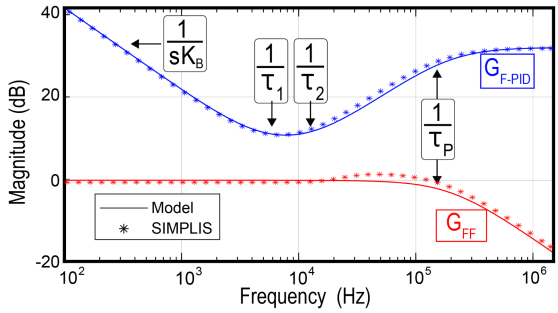


Fig. 6. Theoretical (solid) and simulated (*) magnitude Bode plot of the F-PID transfer function, $G_{\text{F-PID}}(s)$ and feedforward transfer function, $G_{\text{FF}}(s)$.

TABLE I
SYSTEM PARAMETERS

Parameter	Value
V_{in} [V]	2.3–4.8
V_{out} [V]	5
I_{load} [A]	0–0.8
f_{sw} [MHz]	1.5
L, C [μH, μF]	2.2, 44
r, r_c [$m\Omega$]	78, 2
K_{P}	28
K_{I} [rad/s]	$2.2 \cdot 10^6$
K_{B} [rad/s]$^{-1}$	$8 \cdot 10^{-6}$
ω_1 [rad/s]	$3.8 \cdot 10^4$
ω_2 [rad/s]	$9.4 \cdot 10^4$

Fig. 6 shows the Bode diagrams of the transfer functions $G_{\text{F-PID}}(s)$ and $G_{\text{FF}}(s)$ derived from the small-signal model, compared to those simulated by using SIMetrix/SIMPLIS ac analysis. The Bode plots are in excellent agreement, which proves the accuracy of the small-signal model derivation. From now on, all the theoretical analyses and simulations will be performed by using the system parameters reported in Table I, with an input voltage $V_{\text{in}} = 3.5$ V and a load current $I_{\text{load}} = 500$ mA.

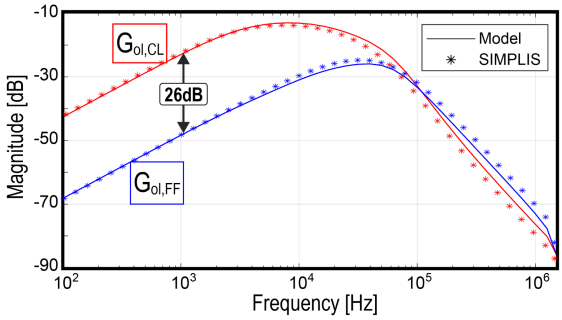


Fig. 7. Theoretical (solid) and simulated (*) magnitude Bode plot of the closed-loop line-to-output transfer functions, with ($G_{\text{ol}_{\text{FF-CL}}}(s)$) and without ($G_{\text{ol}_{\text{CL}}}(s)$) feedforward compensation.

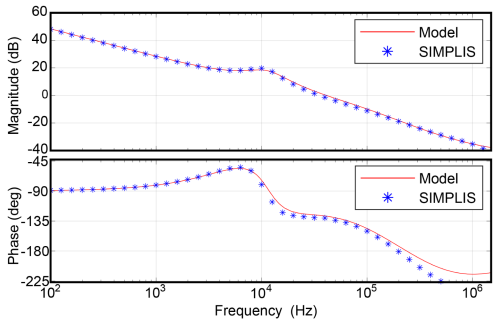


Fig. 8. Theoretical (solid) and simulated (*) magnitude Bode plot of the boost converter control loop $T(s)$.

More details on the derivation of system parameters are given in Section IV.

The closed-loop line-to-output transfer function of the time-based boost converter with the proposed F-PID with line feedforward, $G_{\text{ol}_{\text{FF-CL}}}(s)$, can be computed by solving the following system:

$$\begin{cases} \tilde{v}_{\text{out}} = \tilde{v}_{\text{in}} \cdot G_{\text{ol}}(s) + \tilde{d} \cdot G_{\text{od}}(s) \\ \tilde{v}_e = -\frac{\tilde{v}_{\text{out}}}{N} - \tilde{d} \cdot G_{\text{BPF}}(s) - \frac{\tilde{v}_{\text{in}}}{V_{\text{out}}} \cdot G_{\text{BPF}}(s) \\ \tilde{d} = \tilde{v}_e \cdot G_{\text{PI}}(s) \end{cases} \tag{16}$$

leading to

$$G_{\text{ol}_{\text{FF-CL}}}(s) = \frac{G_{\text{ol}}(s) + G_{\text{FF}}(s) \cdot G_{\text{od}}(s)/V_{\text{out}}}{1 + T(s)} \tag{17}$$

where $T(s)$ is the loop gain

$$T(s) = \frac{G_{\text{F-PID}}(s) \cdot G_{\text{od}}(s)}{N}. \tag{18}$$

Fig. 6 shows that $G_{\text{FF}}(s) \simeq -1$ for frequencies up to $1/\tau_{\text{P}}$, i.e., well beyond the loop crossover frequency. We can therefore approximate (17) as follows:

$$G_{\text{ol}_{\text{FF-CL}}}(s) \simeq \frac{G_{\text{ol}}(s) - G_{\text{od}}(s)/V_{\text{out}}}{1 + T(s)} \tag{19}$$

which can be easily compared with the closed-loop line-to-output transfer functions without feedforward, given by

$$G_{\text{ol}_{\text{CL}}}(s) = \frac{G_{\text{ol}}(s)}{1 + T(s)}. \tag{20}$$

It is worth noting that the numerator of (19) that is, the open-loop line-to-output transfer function is identical to that obtained in [27] with a feedforward PWM. This proves that the proposed F-PID is able to extend the feedforward PWM concept reported in [25] to the time-based domain.

Fig. 7 shows the magnitude Bode plots of the transfer functions $G_{\text{ol}_{\text{FF-CL}}}(s)$ and $G_{\text{ol}_{\text{CL}}}(s)$ derived from the small-signal model, compared with SIMPLIS ac simulations.

Fig. 8 shows the theoretical and simulated Bode diagrams of the magnitude and phase of the loop gain $T(s)$. In both Figs. 7 and 8, SIMPLIS ac simulations are in excellent agreement with the theoretical results.

Fig. 9 shows the schematic diagram of the boost converter equipped with time-based F-PID compensator and line feedforward circuit. In this system, the integrator is designed by cascading a transconductor denoted as G_{mi} with a pair of CCO, namely, RCCO and FCCO. Similarly, the proportional path includes another transconductor, G_{mp}, combined with a couple of current-controlled delay lines, RCCDL and FCCDL, in a cascade configuration [13]. The BPF is split into an HPF and a low-pass filter (LPF). The HPF incorporates the feedforward injection circuit. Cascade to the HPF, a LPF is realized using a resistor, R_{LPF}, and a capacitor, C_{LPF} in parallel. Finally, the BPF drives two transconductors (TCs), $G_{m\text{Fi}}$ and $G_{m\text{Fp}}$, whose output currents are added to the control currents of the CCOs and CCDLs, respectively. The combined HPF and feedforward circuit block produces a current i_{LPF}, given by the difference between the currents i_{S0} and i_{D} flowing through the switch S_0 and the MOSFET M_0, respectively. The current $i_{\text{S}_0}(\text{t})$ is generated by modulating a reference current, I_{REF}, via the PD output, $q(t)$, by means of the switch S_0, resulting in $i_{S_0}(t) = q(t) \cdot I_{\text{REF}}$. Being $d(t) =< q(t) >_{\text{T}_s}$, where T_s is the switching period, a small-signal perturbation, $\tilde{d}$, applied to the duty-cycle would result in a small-signal current $\tilde{i}_{S_0} = \tilde{d} \cdot I_{\text{REF}}$. The current $i_{\text{D}}(t)$ is the mirrored version of the output current of the transconductor $G_{m\text{D}}$, which is driven by the difference between the voltage $v_{\text{C}}(t)$ across the integration capacitor C_{INT} and the input voltage $v_{in}(t)$, scaled by a resistive divider with gain $1/N$.

Therefore

$$i_D(t) = G_{m\text{D}} \cdot \left(v_{\text{C}}(t) - \frac{v_{\text{in}}(t)}{N} \right). \tag{21}$$

A swift change in the input voltage v_{in} produces a variation in the current i_{D} equal to $\tilde{i}_{\text{D}} = -G_{m\text{D}} \cdot \frac{\tilde{v}_{\text{in}}}{N}$, leading to an unbalance in the charge injected in the LPF. The voltage that builds up on the LPF produces a variation in the current of the TCs in the feedback path, $G_{m\text{Fi}}$ and $G_{m\text{Fp}}$. In turn, this current forces the CCOs and the CCDLs to produce a phase-shift at the PD input, proportional to the duty-cycle resulting from the new operating conditions. Due to the nonideal efficiency of the converter ($\eta < 1$), the phase-shift produced by the feedforward gives rise to a nonzero average current i_{LPF}, which results in a residual error on the regulated output voltage. Thanks to the presence of the integrator in feedback (HPF), the voltage on the capacitor C_{INT}

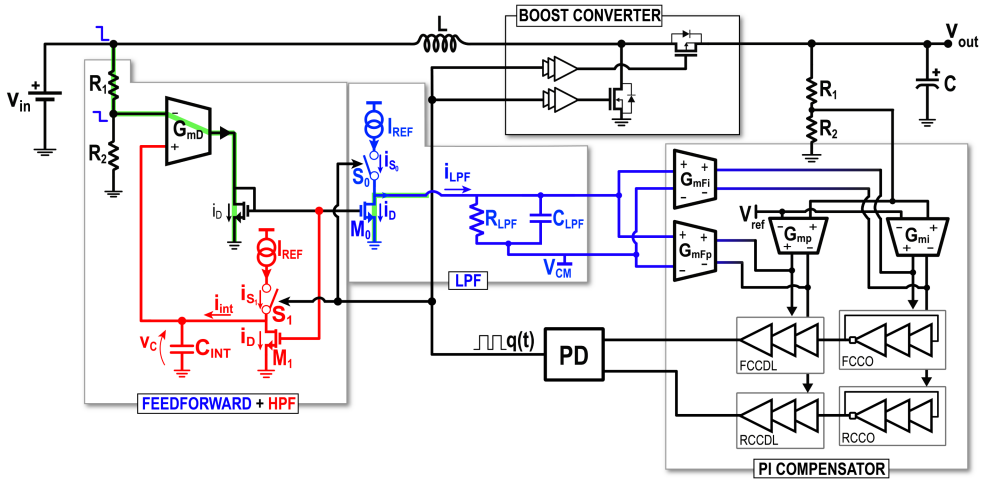


Fig. 9. Schematic diagram of the proposed boost converter with F-PID controller and line feedforward compensation.

eventually settles to

$$V_C = V_{ref} + (1-\eta)\cdot V_{ref}\cdot V_{in}/V_{out}. \quad (22)$$

where $V_{ref} = 1V$ in our design. This voltage ensures that the average current injected into the LPF is zero at steady state. In other words, the transconductor current i_D will match, at steady state, the average value of the current flowing through the switches S_0/S_1.

A key feature of the proposed solution is that the average current injected into the CCOs/CCDLs is zero at steady state, thus requiring the CCDLs to be linear just around their nominal working point. This is a distinct advantage over alternative feedforward methodologies based on the direct injection of feedforward signals into the proportional CCDLs to obtain the desired phase-shift.

A well-known issue in time-based control is the frequency mismatch of the VCO's outputs, which translates in an offset (V_{os}) on the regulated output voltage given by

$$V_{os} = \frac{\Delta f_{VCO}}{K_{VCO}} \quad (23)$$

where Δf_{VCO} is the mismatch between the free-running frequency of the VCO's output square-waves, and $K_{VCO} = K_I$ is the VCO gain. The mismatch is difficult to mitigate without affecting the switching frequency. Solutions such as frequency-locked loops can be used to minimize this effect [28], at the cost of increased controller area occupation and power consumption. The proposed F-PID provides, in this context, an additional advantage, which comes from the decoupling of the PI and F-PID integral gains (K_I and $1/K_B$, respectively). This topology makes it possible to select a much larger K_I compared with a conventional time-based PID as illustrated in Section V.

IV. Transistor-Level Implementation

In this section, the transistor-level implementation of the main building blocks employed in the proposed F-PID controller is discussed. The circuit parameters will be derived in their analytical form.

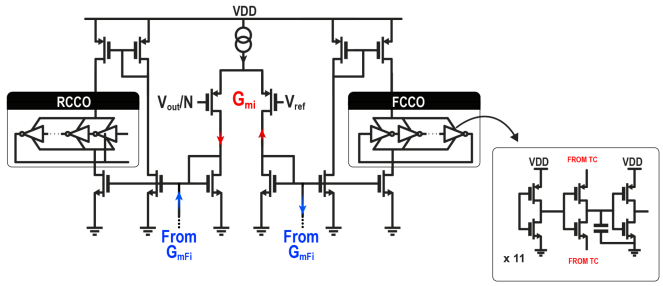


Fig. 10. Simplified schematic diagram of the VCO.

A. Differential Voltage-Controlled Oscillator

As shown in Fig. 10, the differential VCO is composed of two CCOs driven by a pair of TCs, namely, G_{mi} and G_{mFi}. The CCOs are based on a chain of 11 current starved inverters closed in feedback. Each inverter in the delay chain includes one current starved inverter, loaded with a capacitance to increase the cell delay, and two inverters to provide a rail-to-rail almost square output signal. The CCO gain, K_{CCO}, is 33.25 kHz/μA.

The first TC, G_{mi}, takes as inputs the voltage reference V_{ref} and the output voltage scaled by a factor $N = 5$. The transconductor's outputs are mirrored to provide both the bias current and the gain current to the current-starved inverters in the delay chain. The second TC, G_{mFi}, takes as input the voltage across the LPF in the feedforward path. This TC injects the gain current (without bias) in the low-impedance nodes in the mirroring path of the TC G_{mi}. The two TCs have the same transconductance $G_{mi} = G_{mFi} = 70$ μA/V.

Therefore, the gain of the VCO from either the G_{mi} or the G_{mFi} input to the output is $K_{VCO} = G_{mi}\cdot K_{CCO} = 2.2$ MHz/V.

B. Differential Voltage-Controlled Delay Line

Similarly to the VCO, each branch of the differential VCDL has been implemented as a chain of current starved inverters driven by TCs G_{mp} and G_{mFp}, as depicted in Fig. 11. The two

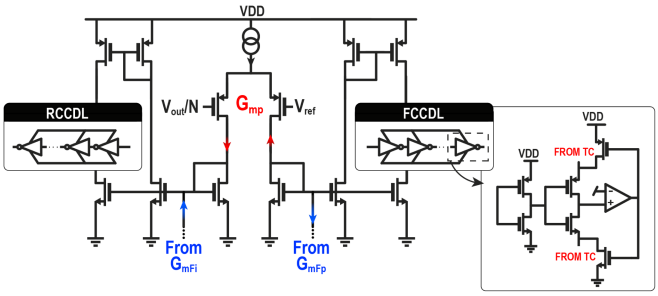


Fig. 11. Simplified schematic diagram of the VCDL.

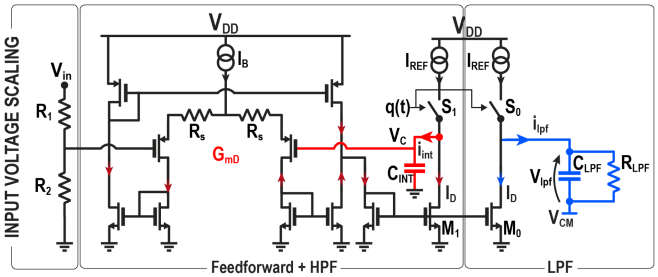


Fig. 12. Simplified schematic diagram of the feedforward injection and HPF.

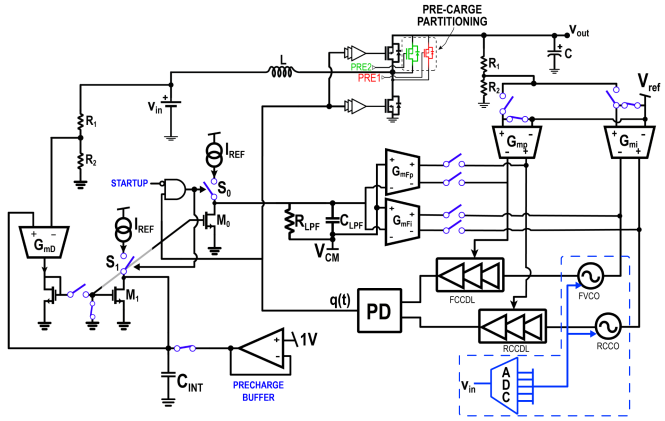


Fig. 13. Schematic diagram of the proposed boost converter during the startup.

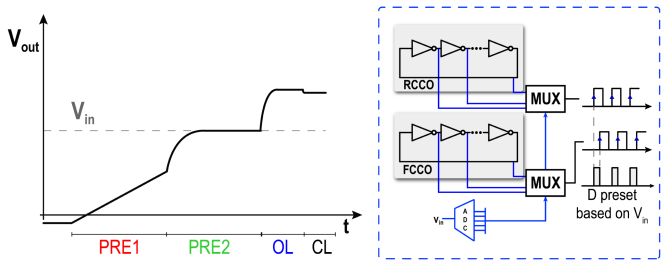


Fig. 14. Output voltage waveform during the startup (left); phase-shift presetting technique (right).

TCs have identical transconductance $G_{mp} = G_{m\mathrm{Fp}} = 65\ \mu$A/V. The CCDLs are realized as a cascade of current starved inverters, as shown in Fig. 11. Each inverter in the delay chain includes one simple inverter, a current starved inverter, and a comparator, connected to two transistors. The pMOS is connected to the upper side of the current starved inverter, in order to boost the low-to-high transition at the comparator's input. In the same fashion, the nMOS is connected to the lower side of the current starved inverter, in order to boost the high-to-low transition at the comparator's input.

The fixed delay of each CCDL, in typical conditions, is $\tau_{\mathrm{CCDL}} = 1\ \mu$s. The CCDL gain is $K_{\mathrm{CCDL}} = 300$ ns/μA. The overall VCDL gain is $K_{\mathrm{VCDL}} = G_{mp} \cdot K_{\mathrm{CCDL}} = 19.5\ \mu$s/V.

C. Feedforward Control and Band-Pass Filter

The feedforward control is composed of three stages, as depicted in Fig. 12. The first stage is a simple resistive divider with ratio $1/N = R_2/(R_1 + R_2)$ used to scale the input voltage. The gain stage, $G_{m\mathrm{D}}$, takes as input the voltage difference $v_{\mathrm{C}} - v_{\mathrm{in}}/N$, which ranges from 0.02 to 0.55 V. To provide a high linearity, the transconductor $G_{m\mathrm{D}}$ is degenerated with two identical resistances $R_s = 300\ \mathrm{k}\Omega$. The gain of the transconductor is $G_{m\mathrm{D}} = 3\ \mu$A/V.

The band-pass filtering action in the feedback path of the F-PID is obtained by cascading a HPF and a LPF. The high-pass transfer function, from the duty-cycle to the integration capacitor current, i_{int} is given by

$$G_{\mathrm{HPF}}(s) = \frac{\tilde{i}_{\mathrm{int}}}{\tilde{d}} = \frac{s \cdot I_{\mathrm{REF}} \cdot C_{\mathrm{INT}}/G_{m\mathrm{D}}}{1 + sC_{\mathrm{INT}}/G_{m\mathrm{D}}}. \tag{24}$$

The current i_{int} is mirrored and low-pass filtered by the parallel of C_{LPF} and R_{LPF}, providing an overall BPF transfer function given by

$$G_{\mathrm{BPF}}(s) = \frac{\tilde{v}_{\mathrm{lpf}}}{\tilde{d}} = \frac{s \cdot I_{\mathrm{REF}} \cdot R_{\mathrm{LPF}} \cdot C_{\mathrm{INT}}/G_{m\mathrm{D}}}{(1 + sC_{\mathrm{INT}}/G_{m\mathrm{D}})\,(1 + sC_{\mathrm{LPF}}R_{\mathrm{LPF}})} \tag{25}$$

To minimize the mismatches between the replicas in the HPF and LPF paths, the voltage v_{C} is buffered as common mode voltage at the bottom of the $R_{\mathrm{LPF}}C_{\mathrm{LPF}}$ filter. In this way, the average voltage at the drain of transistors M_0-M_1, at steady state, will be the same.

From (25), the BPF singularities and gain can be chosen. The first pole of the BPF, is placed right before the complex and conjugate pole doublet of the boost converter, with angular frequency $\omega_1 = G_{m\mathrm{D}}/C_{\mathrm{INT}} = 2\pi \cdot 6$ krad/s. The second pole of the BPF is placed after the boost converter's pole doublet at the angular frequency $\omega_2 = 1/(R_{\mathrm{LPF}}C_{\mathrm{LPF}}) = 2\pi \cdot 15$ krad/s. The middle-frequency gain of the BPF is $i_{\mathrm{REF}}R_{\mathrm{LPF}} = 0.3$ V.

D. Startup Procedure

The startup technique employed in the proposed boost converter is based on presetting the phase-shift between the CCOs output, as described in [35].

A schematic diagram of the proposed boost converter during the startup is shown in Fig. 13. Fig. 14 shows the output voltage waveform during the startup, which is based on two precharge phases (PRE1, PRE2), and an open-loop phase (OL). After the OL

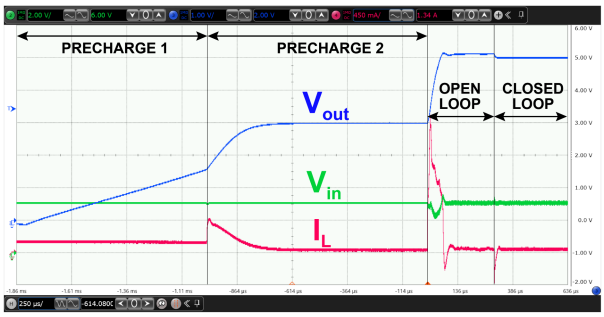


Fig. 15. Measured startup waveforms of the proposed boost converter.

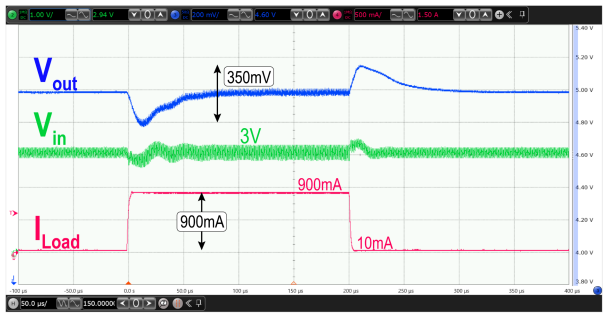


Fig. 17. Measured response of the proposed boost converter to a step load transient from 10 to 900 mA. The operating input voltage is 3 V.

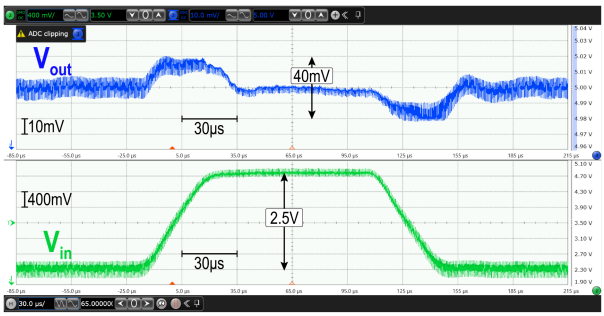


Fig. 16. Measured response of the proposed boost converter to a line transient from 2.3 to 4.8 V with a slope of 0.1 V/μs. Operating load current is 300 mA.

phase, the control loop is closed and the output voltage reaches the steady-state (CL). During phase PRE1, a small partition (high $R_{ds,ON}$) of the high-side power MOSFET is turned ON, and the output capacitor is slowly charged for 1 ms. During phase PRE2, an additional partition of the high-side is turned ON to decrease the resistance and fasten the precharge, making the output voltage to be $V_{out} = V_{in}$. Once the precharge is completed, the boost converter is operated in PWM forcing the duty-cycle of the signal $q(t)$.

The duty-cycle is chosen based on the input voltage, which is converted, by a flash ADC, into a digital word employed to select the CCOs phase-shift, as shown in Fig. 14. The oscillator can provide a phase-shift with a resolution of T_{sw}/N_{stage}, where N_{stage} is the number of inverter stages of the CCOs. The coarse phase shift is read by the PD, which produces the signal $q(t)$, with duty-cycle D_{SU}, and provides it to the boost converter. As shown in Fig. 13, during this phase, the forward path is disabled and the input of TCs G_{mi} and G_{mp} are shorted to V_{ref}, by means of the switches controlled by the signal STARTUP, to avoid unwanted current injection in the CCOs/CCDLs. The TCs in the feedback path of the F-PID are disconnected from the forward path by means of four switches. The capacitor C_{INT} is precharged to 1 V by a voltage buffer.

Once the signal $q(t)$ is provided to the driver of the boost converter, the output voltage starts to increase until it reaches its steady state voltage equal to $V_{out,OL} = V_{in}/(1 - D_{SU})$. Once this condition is reached, the STARTUP signal is set to the logical 0 and the loop is closed. At this point, the output voltage reaches the correct steady state voltage $V_{out} = N \cdot V_{ref}$.

V. Measurement Results

The boost converter with F-PID control and line feedforward was implemented in a 180-nm BCD process. It operates in CCM at a switching frequency of $f_{sw} = 1.5$ MHz, providing a fixed output voltage of 5 V and a maximum load current of 900 mA. Other relevant parameters are summarized in Table I.

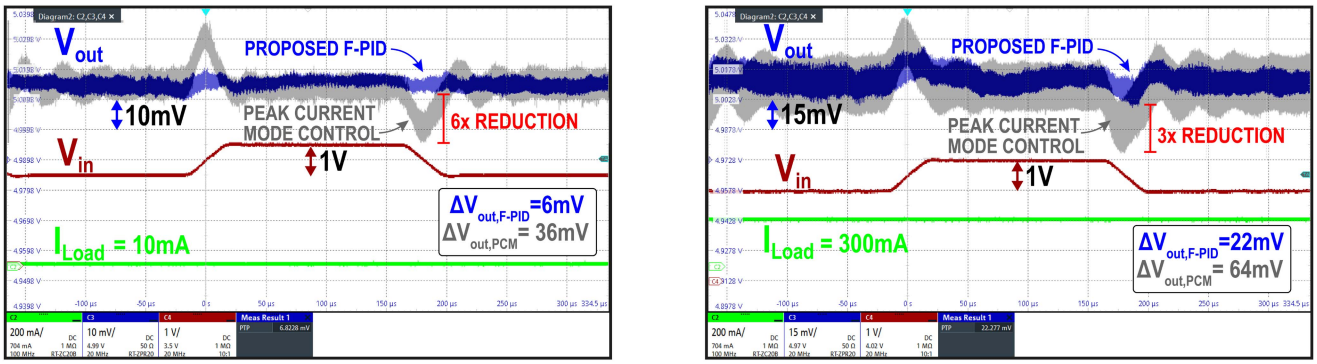
Fig. 15 shows the measured startup waveform with an input voltage of $V_{in} = 3$ V. During the PRE1 (1 ms) the output voltage increase linearly thanks to the high resistivity of the high-side switch segment. When the additional segment of the power-MOSFET is turned ON during the phase PRE2 (1 ms), the input current increase to about 450 mA, bringing the output voltage to $V_{out} = V_{in} = 3$ V. Once the last condition is reached, the boost converter is driven by the duty-cycled waveform $q(t)$ using the phase-shift preset technique. At the end of the OL phase, the loop is closed, and the output voltage reaches the steady-state voltage $V_{out} = 5$ V.

Fig. 16 shows the measured line transient response of the proposed boost converter when the input voltage changes from 2.3 to 4.8 V with a slope of 0.1 V/μs. The large input voltage variation produces a peak-to-peak fluctuation of only 40 mV on the output voltage, proving the effectiveness of the proposed feedforward technique.

Fig. 17 shows the boost converter's load transient response when the input voltage is $V_{in} = 3$ V, and the load current steps from 10 mA to the maximum current of 900 mA. The peak-to-peak output voltage variation is of about 350 mV while the settling time is about 50 μs.

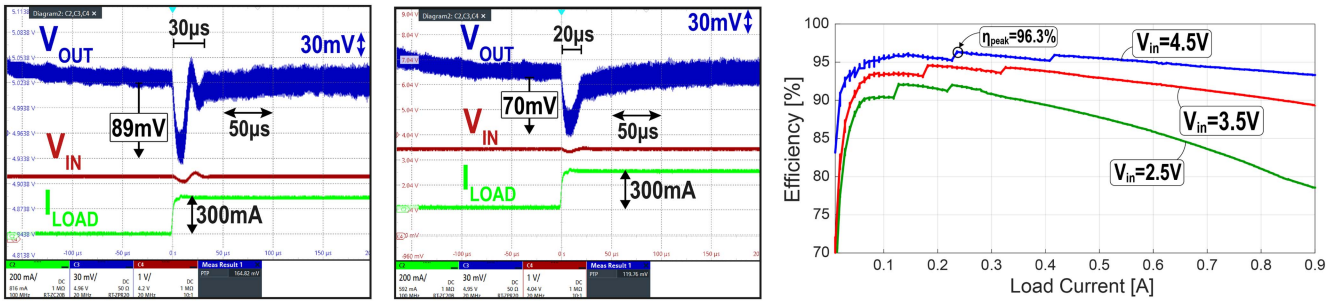
Fig. 18 shows the measured line transient response of the time-based boost converter compared with that of a PCM-controlled boost converter [9], for an input voltage varying from 3 to 4 V with a slope of $1/30$ V/μs. At 10 mA load current, the response of the prototype converter is almost flat, showing a peak-to-peak variation of only 6.8 mV, barely distinguishable from the output voltage ripple. The output voltage variation is a factor $\simeq 6\times$ smaller than that of a boost converter employing PCM control [9] working in the same operating conditions. This factor reduces to about $3\times$ at 300 mA load current.

Fig. 19(a) and (b) shows the measured transient response of the prototype boost converter to a load current step from 10 to 300 mA. When the input voltage is set to 2.5 V the response shows a settling time of about 35 μs and an output voltage



(a) (b)

Fig. 18. Measured line transient response of the proposed time-based boost converter compared to that of a PCM boost converter when the load current is set to (a) 10 mA and (b) 300mA. Input voltage steps from 3 to 4 V with a slope of $1/30$ V/μs.



(a) (b) (c)

Fig. 19. Measured transient response of the prototype boost converter to a load current step from 10 to 300 mA for an input voltage of (a) 2.5 V and (b) 3.5 V. (c) Measured efficiency versus load current.

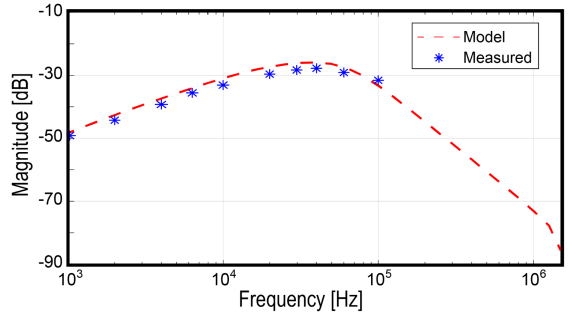


Fig. 20. Theoretical (dash) and measured (*) magnitude Bode plot of the closed-loop line-to-output transfer function $G_{\text{ol}_{\text{FF-CL}}}(s)$.

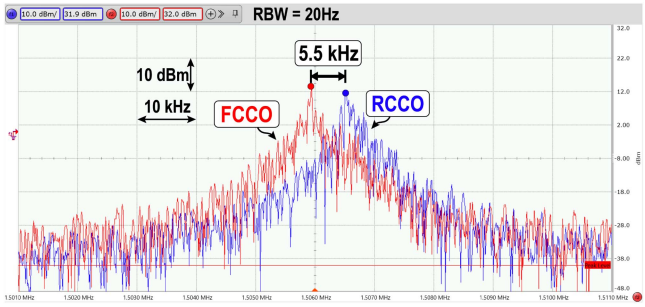


Fig. 21. Measured frequency spectra of the RCCO and the FCCO.

variation of 89 mV. When the input voltage is set to 3.5 V the response shows a settling time of about 20 μs and an output voltage variation of 70 mV.

Fig. 19(c) shows the converter efficiency, with a 96.3% peak at $\simeq 230$ mA load current. The efficiency curve shows two discontinuity points due to a three-level power-MOS segmentation [36].

Fig. 20 shows the measured and the theoretical $G_{\text{ol}_{\text{FF-CL}}}(s)$. The measurements were performed up to 100 kHz, the maximum frequency at which the power supply can provide sinusoidal waveforms. The measurements are in strong agreement with the model, proving the effectiveness of the proposed feedforward technique.

Fig. 21 shows the free-running frequency mismatch between the FCCO and the RCCO. The $\Delta f_{\text{VCO}} = 5.5$ kHz causes an offset on the regulated output voltage of

$$V_{\text{os,F-PID}} = \frac{\Delta f_{\text{VCO}}}{K_{\text{VCO,F-PID}}} \cdot N = \frac{5.5\,\text{kHz}}{2.2\,\text{MHz/V}} \cdot 5 = 12.5\ \text{mV}. \tag{26}$$

The advantage of the proposed F-PID over a conventional T-PID structure (see Fig. 2) can be evaluated by computing the output voltage offset caused by the same frequency mismatches,

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This work	[31] TPEL '22	[9] STMP30	[32] TPEL '17	[33] TPEL '19	[10] TPS65632	[34] MAX18000	[35] MP5611
Technology	**180nm-BCD**	180nm-BCD	180nm-BCD	180nm-BCD	180nm-BCD	N/A	N/A	N/A
V_{in} [V]	**2.3 - 4.8**	2.3 - 4.5	2.5 - 4.8	1.55 - 1.8	2.9 - 4.5	2.9- 4.5	2 - 4.8	2.9 - 4.3
V_{out} [V]	**5**	5	5	2.5	4.6	4.6	5	4.6
$I_{load,max}$ [mA]	**900**	800	550	200	800	300	1000	500
L[μH]	**2.2**	2.2	2.2	10	4.7	4.7	0.47	4.7
C [μF]	**44**	44	44	10+10**	10+10**	10	44	10
f_{sw} [MHz]	**1.5**	1.5	1.5	1	1	1.7	2	1.35
η_{peak} [%]	**96.3**	96	96.5	95.7	93	92*	95*	94*
Control method	**VM F-PID**	ICF	CM	CM	CM	N/A	N/A	N/A
Controller Area [mm]	**0.21**	0.29*	0.3	0.29*	0.62*	N/A	N/A	N/A
ΔI_{load} [mA]	**300**	300	300	150	400	90	985	90
Recovery time [μs]	**20**	20	20	48	20	30*	100*	100*
ΔV_{out} [mV]	**70**	58.5	60	90	190	90	200*	36*
Conversion Ratio	**1.3**	1.4	1.2	1.38	1.3	1.3	1.38	1.25
ΔV_{in} [V]	**1**	1	1	N/A	N/A	1.2	0.7	N/A
Voltage slope [V/μs]	**0.033**	0.1	0.033	N/A	N/A	0.024	0.07	N/A
$\Delta V_{out,pp}$ [mV]	**6**	87	36	N/A	N/A	20	80	N/A
Line Regulation [mV/V]	**1.25**	1.5	3.75	12	N/A	1	12.7*	1
Load Regulation [mV/A]	**8.9**	10.63	17.5	166	N/A	16	72*	9.2
FoM***	**0.18**	0.87	1.08	N/A	N/A	0.69	1.63	N/A

*estimated from figure,**extra flying capacitor, ***smaller values are better.

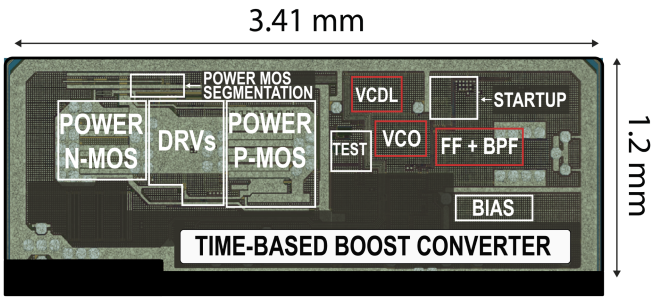


Fig. 22. Die micrograph of the proposed boost converter.

for an equivalent T-PID having the same singularities. The T-PID integral gain can be computed assuming a proper pole-zero compensation, leading to a loop gain transfer function given by

$$T(s) \simeq \frac{G_{od}(0)}{N} \cdot \frac{K_{VCO,T\text{-}PID}}{s}. \tag{27}$$

In order to limit the loop crossover frequency to about one-third of the RHP zero in the worst-case conditions, i.e., $G_{od}(0) = 10$ and maximum load current, the equivalent VCO gain should be $K_{VCO,T\text{-}PID} = 100$ kHz/V. Thus, with an equivalent T-PID structure, the output voltage offset calculated by using (26) would be $\simeq 275$ mV.

The die micrograph of the boost converter with the proposed time-based F-PID is shown in Fig. 22. The die area is 4.1 mm^2, while the controller, highlighted in red, occupies only 0.21 mm^2.

To provide a fair comparison, a figure of merit (FoM) [14] is used to compare the implemented converter with state-of-the-art and commercially available boost converters for the same application.

The FoM, used to compare the line transient response of the boost converters, is

$$\text{FoM} = \frac{\Delta V_{out,pp}}{\Delta V_{in} \cdot \text{SL}}. \tag{28}$$

The first term in the FoM provides the output voltage deviation with respect to the nominal value; the second term quantifies the input voltage variation and its slope (SL). For both the FoM smaller values result in a better converter's response.

The comparison of the proposed boost converter with other published and commercially available boost converters for the same application is reported in Table II. The proposed boost converter provides a load transient response competitive with those of the best state-of-the-art boost converter, while it provides a superior line transient response. In addition, this proposed converter achieves better performance with a controller area of only 0.21 mm^2, representing a reduction of nearly 30% compared with other boost converters.

VI. CONCLUSION

In this article, a time-based boost converter for AMOLED application with a novel feedback-PID compensator was discussed. The prototype, fabricated in a 180-nm BCD technology, works with a switching frequency of 1.5 MHz and provides an output voltage of 5 V for an input voltage ranging from 2.3 to 4.8 V. The proposed F-PID offers an additional path, which is exploited to introduce a feedforward from the input voltage to the duty-cycle. Thanks to the proposed F-PID architecture, the load transient response are comparable with those of a boost converter with PCM control, while the line transient response is improved by a factor up to 6×. Compared with an equivalent T-PID architecture, the offset introduced by the frequency mismatch in the differential VCO is reduced by a factor larger than 20×. These performances are achieved with a controller area of only 0.21 mm^2, almost 30% smaller than the controllers used in the best state-of-the-art boost converters.

REFERENCES

[1] S. Forrest, P. Burrows, and M. Thompson, "The dawn of organic electronics," *IEEE Spectr.*, vol. 37, no. 8, pp. 29–34, Aug. 2000.

[2] M. K. Barwar et al., "Demystifying the devices behind the LED light: LED driver circuits," *IEEE Ind. Electron. Mag.*, vol. 17, no. 1, pp. 55–66, Mar. 2023.
[3] M. Kimura et al., "Low-temperature polysilicon thin-film transistor driving with integrated driver for high-resolution light emitting polymer display," *IEEE Trans. Electron Devices*, vol. 46, no. 12, pp. 2282–2288, Dec. 1999.
[4] J.-S. Kim, J.-O. Yoon, and B.-D. Choi, "A high-light-load-efficiency low-ripple-voltage PFM buck converter for IoT applications," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5763–5772, May 2022.
[5] F. Mao, Y. Lu, F. Maloberti, and R. P. Martins, "A hybrid single-inductor bipolar triple-output DC–DC converter with high-quality positive outputs for AMOLED displays," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 1, pp. 506–517, Jan. 2023.
[6] P. Cao, D. Lu, J. Xu, X. Zeng, and Z. Hong, "A time-domain-controlled single-inductor step-up converter with symmetric bipolar output voltages," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1087–1100, Jan. 2024.
[7] F. Mao et al., "A hybrid single-inductor bipolar-output DC–DC converter with floating negative output for AMOLED displays," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2760–2769, Sep. 2021.
[8] H.-J. Park et al., "A simultaneous energy transferring SIBO converter achieving low ripple and high efficiency for AMOLED applications," *IEEE J. Solid-State Circuits*, vol. 59, no. 5, pp. 1497–1508, May 2024.
[9] 3-channel "PMIC for mobile AMOLED display," STMicroelectronics, Rev. 1, Feb. 2022. [Online]. Available: https://www.st.com/en/power-management/stmp30.html
[10] "TPS65632 triple-output AMOLED display power supply," Texas Instruments, Jan. 2016. [Online]. Available: https://www.ti.com/lit/gpn/TPS65632
[11] S. J. Kim et al., "High frequency buck converter design using time-based control techniques," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 990–1001, Apr. 2015.
[12] J.-G. Kang, J. Park, M.-G. Jeong, and C. Yoo, "A time-domain-controlled current-mode buck converter with wide output voltage range," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 865–873, Mar. 2019.
[13] M. Leoncini, A. Dago, A. Bertolini, A. Gasparini, S. Levantino, and M. Ghioni, "A compact high-efficiency boost converter with time-based control, RHP zero-elimination, and tracking error compensation," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3100–3113, Mar. 2023.
[14] P. Melillo et al., "A wide-input-range time-based buck converter with adaptive gain and continuous phase preset for seamless PFM/PWM transitions," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 7, pp. 3436–3447, Jul. 2024.
[15] M.-L. Chiu, I.-F. Lo, and T.-H. Lin, "A time-domain CCM/DCM current-mode buck converter with a PI compensator incorporating an infinite phase shift delay line," in *Proc. ESSCIRC 2023- IEEE 49th Eur. Solid State Circuits Conf.*, 2023, pp. 441–444.
[16] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Berlin, Germany: Springer Science & Business Media, 2007.
[17] P. Melillo, M. Leoncini, S. Levantino, and M. Ghioni, "Insights on the dynamic performance of nonminimum-phase boost converters exploiting inductor-current-feedback RHPZ mitigation," *IEEE Trans. Power Electron.*, vol. 39, no. 4, pp. 4160–4172, Apr. 2024.
[18] C. Y. Leung, P. Mok, and K. N. Leung, "A 1-V integrated current-mode boost converter in standard 3.3/5-V CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2265–2274, Nov. 2005.
[19] R. B. Ridley, "A new, continuous-time model for current-mode control (power convertors)," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, Apr. 1991.
[20] B. Bryant and M. Kazimierczuk, "Voltage loop of boost PWM DC-DC converters with peak current-mode control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 1, pp. 99–105, Jan. 2006.
[21] E. Dallago, M. Passoni, and G. Sassone, "Lossless current sensing in low-voltage high-current dc/dc modular supplies," *IEEE Trans. Ind. Electron.*, vol. 47, no. 6, pp. 1249–1252, Dec. 2000.
[22] W. Hong and M. Lee, "A 15–25-MHz and 1-μs/0.4-A load response AOT boost converter using an accurate feedforward-path current sensor," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1205–1209, Feb. 2022.
[23] T. E. D. Kizas, M. Bergo, G. Capodivacca, L. Scandola, P. Malcovati, and A. Baschirotto, "A 51-ns response-time, fully integrated, high-side current sensor for a 40-v 6-A dc–dc converter," *IEEE Solid-State Circuits Lett.*, vol. 5, pp. 300–303, Dec. 2022, doi: 10.1109/LSSC.2022.3227980.
[24] L. Calderone, L. Pinola, and V. Varoli, "Optimal feed-forward compensation for PWM DC/DC converters with 'linear' and 'quadratic' conversion ratio," *IEEE Trans. Power Electron.*, vol. 7, no. 2, pp. 349–355, Apr. 1992.
[25] D. Maksimovic and B. Arbetter, "Feedforward pulse-width modulator for boost DC-DC power converters," *Electron. Lett.*, vol. 31, no. 7, pp. 513–514, 1995.
[26] M. Kazimierczuk and A. Massarini, "Feedforward control of DC-DC PWM boost converter," *IEEE Trans. Circuits Syst. I. Fundam. Theory Appl.*, vol. 44, no. 2, pp. 143–148, Feb. 1997.
[27] M. Kazimierczuk and L. Starman, "Dynamic performance of PWM DC-DC boost converter with input voltage feedforward control," *IEEE Trans. Circuits Syst. I. Fundam. Theory Appl.*, vol. 46, no. 12, pp. 1473–1481, Dec. 1999.
[28] S. J. Kim, R. K. Nandwana, Q. Khan, R. C. Pilawa-Podgurski, and P. K. Hanumolu, "A 4-phase 30–70 MHz switching frequency buck converter using a time-based compensator," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2814–2824, Dec. 2015.
[29] N. J. Dahl, P. L. Muntal, and M. A. E. Andersen, "Fully time-based PID controller for a high frequency buck converter," in *2023 21st IEEE Interregional NEWCAS Conf.*, 2023, pp. 1–5.
[30] M. Kazimierczuk and D. Czarkowski, "Application of the principle of energy conservation to modeling the PWM converters," in *Proc. IEEE Int. Conf. Control Appl.*, 1993, pp. 291–296.
[31] X. Jing and P. K. T. Mok, "A fast fixed-frequency adaptive-on-time boost converter with light load efficiency enhancement and predictable noise spectrum," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2442–2456, Oct. 2013.
[32] Y. Zhang et al., "Analysis and implementation of a high-performance-integrated KY converter," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9051–9064, Dec. 2017.
[33] S.-U. Shin, S.-W. Hong, H.-M. Lee, and G.-H. Cho, "High-efficiency hybrid dual-path step-up DC–DC converter with continuous output-current delivery for low output voltage ripple," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6025–6038, Jun. 2020.
[34] "500 mV to 5.5 V input nanoPower boost converter with short-circuit protection, analog devices," Rev. 0, Feb. 2023. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/max18000.pdf
[35] T. Rosa, M. Leoncini, and S. L. M. Ghioni, "A novel start-up technique for time-based boost converters with seamless PFM/PWM transition," in *2020 IEEE Int. Symp. Circuits Syst.*, 2020, pp. 1–5.
[36] S. Musunuri and P. Chapman, "Improvement of light-load efficiency using width-switching scheme for CMOS transistors," *IEEE Power Electron. Lett.*, vol. 3, no. 3, pp. 105–110, Sep. 2005.

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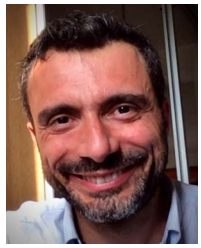

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