A 2.5D Multichip SiC MOSFET Power Module With Low Parasitic Inductance and High Dynamic Current Sharing Performance

Zexiang Zheng, Jianwei Lv, Yiyang Yan, Jiaxin Liu, *Member, IEEE*, Cai Chen, *Member, IEEE*, and Yong Kang, *Fellow, IEEE*

***Abstract*—The parasitic inductance and dynamic current sharing performances of multichip silicon carbide power module packaging limit the device's performance. Moreover, high electrical properties cannot be achieved in traditional 2-D packaging, and the 3-D packaging manufacturing process is complicated with a necessity for further reliability verification. To solve these problems, a novel 2.5-D wire-bonding packaging was designed in this article, which combines the advantages of the simple structure of 2-D packaging and the high electrical performance of 3-D packaging. Without introducing any additional substrates, a highly symmetrical 3-D commutation loop is formed solely through a distinctive layout and terminal structure. The terminal structure was optimized to achieve extremely low parasitic inductance and excellent dynamic current sharing performance considering the mutual inductance coupling. Due to the compact commutation loop, the proposed power module with a 2.5-D packaging structure could attain a parasitic inductance of 2.31 nH and balanced dynamic currents. A 1200 V/520 A 2.5-D power module was fabricated for verification. The experimental results effectively validated the low parasitic inductance and high dynamic current sharing performances.**

***Index Terms*—2.5-D packaging structure, high dynamic current sharing performance, low parasitic inductance, silicon carbide (SiC) power module.**

I. Introduction

RECENTLY, the transportation system has proposed higher requirements for the power capacity and power density of power electronic systems. Semiconductor devices are the core of power electronics systems [1], [2], [3], [4]. Wide bandgap power devices, such as silicon carbide (SiC) devices have been widely used in medium voltage applications in recent years. Due to the high critical electric field strength, band gap energy, electron velocity, melting point, and thermal conductivity of SiC material, the SiC MOSFETs perform higher switching speed, voltage, and operating temperature compared with Si-based IGBT [5].

Received 23 January 2024; revised 28 June 2024 and 18 August 2024; accepted 12 September 2024. Date of publication 17 September 2024; date of current version 12 December 2024. This work was supported by the National Natural Science Foundation of China under Grant 52077094. Recommended for publication by Associate Editor D. Tao. *(Zexiang Zheng and Jianwei Lv contributed equally to this work.) (Corresponding author: Jiaxin Liu.)*

The authors are with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: liujx711@hust.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3462749.

Digital Object Identifier 10.1109/TPEL.2024.3462749

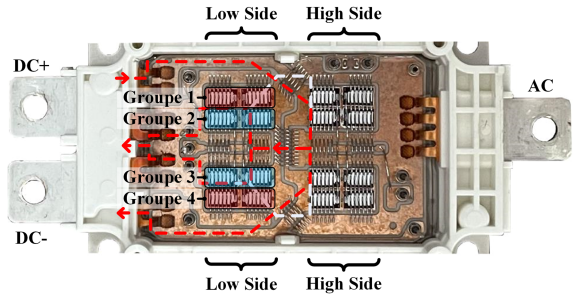


Fig. 1. Schematic of HybridPACK Drive SiC power module with double-loop.

Therefore, the application of SiC devices contributes to the trend of high-power density in power electronic systems. However, the performance of SiC MOSFETs brings serious challenges to the parasitic inductance of power module packaging and dynamic current sharing performance between multiple parallel chips [6], [7].

The low output capacitance (C_{oss}) and storage charge (Q_g) of SiC devices result in high *dv/dt* and *di/dt* during the switching process. High *di/dt* results in high voltage overshoot and oscillations, and high *dv/dt* leads to electromagnetic compatibility issues, which make SiC power modules more sensitive to the parasitic inductance value [8], [9]. Therefore, high-performance SiC power modules require packaging with low parasitic inductance. Aiming to reduce parasitic inductance, previous research focused on traditional 2-D packaging and advanced 2.5-D and 3-D packaging.

2-D packaging structure establishes a planar commutation loop through bonding wires. In industry, the dual-loop commutation structure of the HybridPACK Drive SiC power module forms two interleaved parallel loops to reduce parasitic inductance, which was adopted by many other commercial power modules [10], [11], as shown in Fig. 1. In academia, much research has also been conducted on 2-D packaging with low parasitic inductance [12], [13], [14], [15]. The P-cell and N-cell layout was proposed in [12], and [13], which effectively decreased the parasitic inductance by reducing the commutation path length. In [14], split damping capacitors were integrated into the module to decouple the parasitic inductance. In [15], a double-end sourced wire-bonding multichip power module was proposed, which reduced parasitic inductance to 7.2 nH through

paralleled commutation loops. A low parasitic inductance 2-D packaging structure is easy to implement, but its effectiveness is limited.

Advanced 2.5-D and 3-D packaging structures establish 3-D commutation loops by adding additional substrates [such as printed circuit board (PCB), flexible printed circuit (FPC), or DBC] [9], [16], [17], [18], [19], [20], [21], [22], which can achieve low parasitic inductance through mutual inductance cancellation. In industry, the SKiN technology from Semikron replaces bond wires with sintered FPC to form 3-D loops, achieving low parasitic inductance [16], [17]. However, additional FPCs are needed, and the sintering process between the FPC and chips is challenging, which has prevented large-scale adoption. In academia, 3-D commutation loops are formed by stacking additional PCB, FPC, and DBC on the basic DBC substrate [9], [18], [19], achieving a parasitic inductance below 3 nH. In [20], [21], and [22], double-sided power modules with 3-D commutation loops were designed with a parasitic inductance below 3 nH, which uses DBC and spacers to replace bonding wires. In [23], the 3-D prismatic packaging methodology was proposed to achieve low parasitic inductance. However, the above 3-D packaging structures, in addition to the basic DBC, require the incorporation of extra substrates (such as PCB or DBC) to establish the 3-D commutation loop. Therefore, the fabrication process is complex. For instance, the metallization of chip electrodes is necessary for the double-side soldering process. In general, the 2-D packaging structures make it difficult to achieve ultralow parasitic inductance while exiting 2.5-D and 3-D packaging requires more complex manufacturing processes and higher costs.

On the other hand, limited by the manufacturability of SiC dies, the effective area of a bare chip is limited [24]. To meet the demand of current capacity, paralleled SiC MOSFETs are frequently used in power modules [25], [26]. However, the unbalanced parasitic inductances of paralleled chips could lead to unbalanced dynamic currents during switch transients, which brings unbalanced losses, and further causes uneven junction temperature of parallel chips. For SiC devices, high junction temperature can result in a low threshold voltage (V_{th}), and increase the junction temperature further, which causes positive feedback and may lead to thermal runaway. Therefore, it is necessary to achieve balanced dynamic currents in multichip SiC power modules.

The dynamic current sharing optimization methods could be divided into active method, passive method, and optimization layout method. The active method improves dynamic current sharing performance by controlling the driving signals in real-time. In [27], [28], [29], researchers measured each device's current with a current sensor and changed the driving signal based on the real-time measured currents to achieve balanced dynamic currents. The active compensation method can achieve an excellent effect on current sharing performance, but the circuit structure is relatively complex and costly.

The passive method improves the dynamic current sharing performances by appending the additional passive components. In [30] and [31], decoupling capacitors and *RC* snubber were added to alleviate imbalanced currents. In [32], a different mode choke was used to suppress the current imbalance. The passive compensation method has a low cost but requires the addition of additional components in circuits, which still limits various practical applications.

Optimizing the layout is the lowest cost and easiest method. In industry, the symmetrical dual-loop commutation structure shown in Fig. 1 is used widely, which enables excellent dynamic current sharing performances between the parallel chips of symmetrical group 1 and group 4 (or group 2 and group 3). However, group 1 and group 2 (or group 3 and group 4) located on the same side cannot achieve balanced currents. In academia, the connection points of bonding wires are adjusted to alleviate imbalanced dynamic currents [33], [34]. However, the method requires strict control over the length, shape, and connection points of the actual bonding wires. In [15], a wire-bonding power module with a double-bonded sourced layout was proposed to improve dynamic current sharing performance. Li et al. [35] and [36] alleviated nonuniform dynamic currents through a split-out DBC layout. It similarly fails to improve the current sharing performances of paralleled MOSFETs on the same side. Zhao et al. [37] pointed out that the current imbalance is alleviated when the drain confluence point and power source confluence point are on one side rather than both sides. However, the layout optimization effect of wire-bonding packaging for dynamic current sharing performance still needs further improvement.

To address the above issues, this article presents a novel 2.5-D multichip wire-bonding SiC power module with a 3-D commutation loop and a highly symmetrical layout. It can achieve ultralow parasitic inductance and high dynamic current performance while ensuring simple processing and low cost. The innovation and contribution are as follows.

1) A wire-bonding 2.5-D packaging with a 3-D commutation loop is proposed, requiring no additional components (DBC, PCB, or FPC). It not only achieves ultralow parasitic inductance similar to advanced 3D packaging, but also realizes simpler manufacturing processes and lower costs.
2) The 2.5-D packaging also achieves high dynamic current sharing performance. Based on a high-symmetrical layout and terminal optimization considering all mutual inductances, balanced dynamic currents are achieved.

The rest of this article is organized as follows. Section II provides a detailed introduction to the structure of the proposed 2.5-D power module. In Section III, the proposed 2.5-D power module is analyzed and optimized to achieve extremely low parasitic inductance and balanced dynamic currents considering mutual inductance coupling. Section IV describes the detailed manufacturing process and performs the dynamic test, impedance test, and dynamic current sharing test to verify the superior performance of the proposed 2.5-D power module. Finally, Section V concludes this article.

II. Structure of Proposed 2.5-D Power Module

The structure of the proposed 2.5-D power module is shown in Fig. 2. The half-bridge power module includes eight SiC MOSFETs. Among them, four SiC MOSFETs are connected in parallel

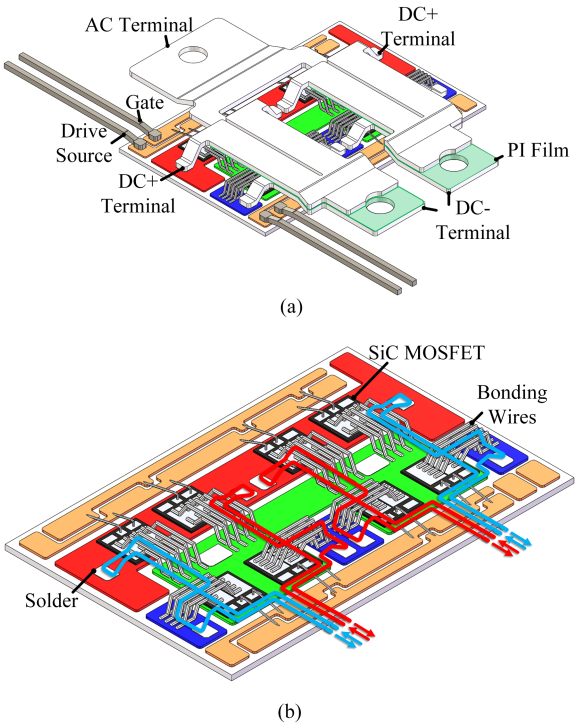


Fig. 2. The structure of the proposed 2.5-D power module. (a) Power module. (b) Internal view (the terminals are omitted).

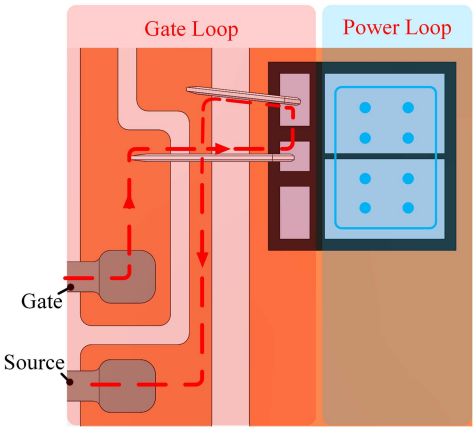


Fig. 3. Kelvin connection diagram of driving circuit.

as high-side switches ($Q5$–$Q8$), while the others are connected in parallel as low-side switches ($Q1$–$Q4$). The SiC MOSFETs are S4651 from ROHM with 1200 V rated voltage, 130 A rated current, and 11 mΩ. The body diodes of the SiC MOSFETs are directly used as the parallel antidiodes. Aluminum wires are bonded to connect the gate and source of the MOSFETs to the upper copper layer of the DBC substrate. The materials of DBC layers are Cu/Si_3N_4/Cu with a thickness of 0.25/0.32/0.25 mm and a size of 43.2 mm × 28.6 mm. A pair of symmetrical dc terminals are utilized, extending from one side of the DBC. The thickness of the copper terminal is 0.8 mm. The common source inductance is eliminated through the Kelvin connection to maximize the performance of SiC MOSFETs, as shown in Fig. 3.

As shown in Fig. 2(a), the dc+ and dc− terminals are tightly stacked with a terminal gap of 0.15 mm, which is closer than traditional stacked terminals [16]. A polyimide (PI) film with an insulation strength of 200 kV/mm is filled between two terminals, which fully meets the insulation requirements of 1200 V. Each terminal has two solder joints symmetrically distributed on both sides of the parallel SiC MOSFETs. The commutation loop of the 2.5-D power module is shown in Fig. 2(b). No additional substrates are required, and a compact 2.5-D power module with 3-D commutation loops and a symmetrical layout is realized by introducing the solder joints of the horizontally stacked terminals into the power module. The drive terminals are distributed in parallel on one side of the power terminals. In practice, the drive terminals can be simply bent to reduce the coupling between the drive and power loops, and this process is convenient. Based on the module, the structure is further analyzed and optimized in Section III to achieve extremely low inductance and balanced dynamic currents.

III. Analysis and Optimization of Inductance and Current Sharing of the Proposed 2.5-D Module

Mutual inductance coupling is an important factor affecting parasitic inductance [9], [16], [17], [18], [19], [20], [21], [22] and dynamic current sharing performance [20], [37], [38], [39], [40]. Therefore, mutual inductance coupling cannot be ignored in this compact 2.5-D power module. In this section, the parasitic inductance is first analyzed considering the mutual inductances. Then, to the completeness of the optimization process, the dynamic current sharing performance of four chips in parallel is analyzed in the 2.5-D power module. Finally, a comprehensive optimization analysis is conducted on the parasitic inductance and dynamic current sharing performance. Extremely low parasitic inductance and balanced dynamic currents can be achieved after optimization.

A. Analysis of Parasitic Inductance

The two main aspects of reducing parasitic inductance in power modules are: reducing the length of the commutation path and realizing mutual inductance cancellation between different current paths.

The first part is to reduce the power circuit self-inductance of the 2.5-D module. As shown in Fig. 2(b), four parallel SiC MOSFETs are arranged in two groups and the commutation loop is shown in red and blue lines. The solder joints between the terminals and DBC are introduced into the 2.5-D power module as close as possible to the chips, which reduces the length of the commutation path on the DBC through the 0.3 mm copper layer. The reduced path transforms into the path on dc terminals with a thickness of 0.8 mm, decreasing the self-inductance of the commutation loop. There are two soldering points between each terminal and substrate, which allows four parallel commutation loops in the power module, further lowering the self-inductance of the commutation loop.

Furthermore, mutual inductance coupling is considered to reduce parasitic inductance. As shown in (1), to reduce the total parasitic inductance (L_{loop}) of the loop composed of two

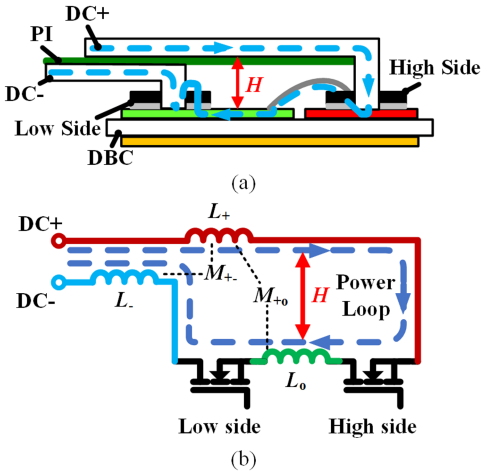


Fig. 4. Schematic diagram of commutation loop. (a) Power loop of 2.5-D power module. (b) Parasitic inductance distribution of 3-D commutation loop.

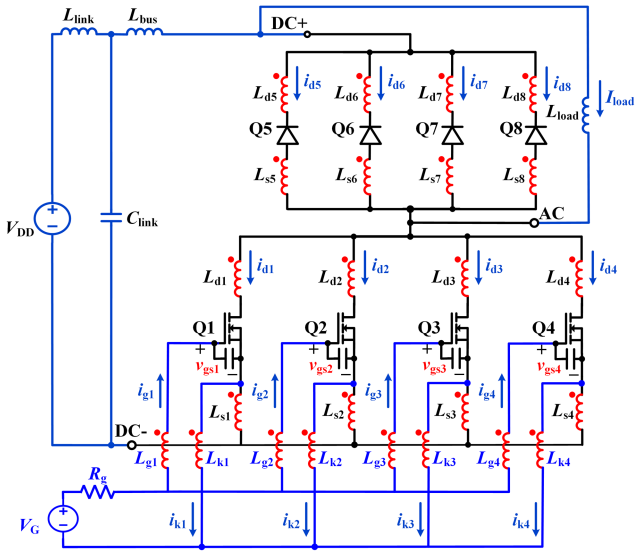


Fig. 5. Parasitic circuit model of 2.5-D power module with four MOSFETs connected in parallel.

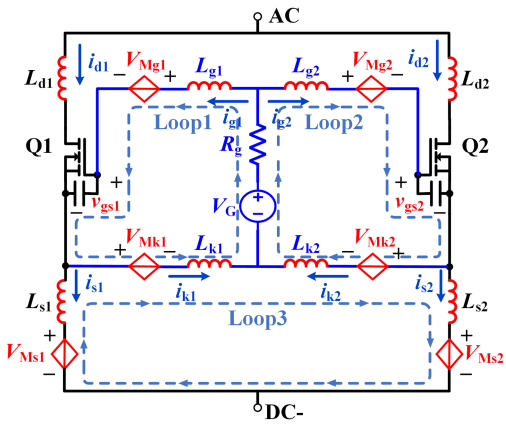


Fig. 6. Parasitic equivalent circuit of parallel $Q1$ and $Q2$ considers mutual inductance coupling.

segments (L_1 and L_2), negative mutual inductance coupling (M_{12}) is introduced inside the power circuit

$$L_{\mathbf{loop}} = L_1 + L_2 + 2M_{12} \tag{1}$$

where M_{12} depends on the distance between segments [19].

Based on the design criteria, from the side view of the power loop in Fig. 4(a), the parasitic inductance distribution can be obtained as shown in Fig. 4(b). Due to the special terminal structure, a 3-D commutation loop is formed between the terminal and the upper copper layer of the DBC. The parasitic inductance can be divided into three parts: the inductance L_+ from the dc+ terminals to the high-side MOSFETs' drain, the inductance L_o from the high-side MOSFETs' power source to the low-side MOSFETs' drain, and the inductance L_- from the low-side MOSFETs' power source to dc- terminals. Therefore, a mutual inductance cancellation effect (M_{+o} and M_{+-}) is formed between L_+ and L_o, L_-, which effectively reduces the module parasitic inductance. According to the module structure, M_{+o} and M_{+-} depend on the terminal height and gap, respectively, which significantly affects the total parasitic inductance ($L_{2.5\mathrm{D}}$) of the power module. However, considering the cost, the terminals in this article are fabricated by machining, which has a certain tolerance. Considering the tolerance, the gap of 0.15 mm is deemed sufficiently small. Therefore, the terminal gap is fixed, and the ultralow parasitic inductance is achieved only by optimizing the terminal height.

B. Analysis of Dynamic Current Sharing Performance

Due to the compact 3-D commutation loop of the 2.5-D module, the impact of mutual inductance coupling on dynamic current balancing needs to be considered. Based on the model in [39] and [40], the dynamic current sharing performances of the proposed 2.5-D power module are analyzed by considering the mutual inductance coupling between power branches and power branches on the driving branches.

Only the dynamic current balance of the low-side MOSFETs is analyzed due to symmetry. When low-side MOSFETs are used as the main switches and high-side MOSFETs are used as the freewheeling diodes, the parasitic inductance model considering mutual inductance coupling between the power branches and the power branches to the drive branches is shown in Fig. 5. Mutual inductance coupling exists between any two inductances with red dots.

The dynamic current sharing performances between $Q1$ and $Q2$ are analyzed, which is applicable to any two parallel MOSFETs. Considering the mutual inductance coupling, the parasitic equivalent circuits of $Q1$ and $Q2$ are shown in Fig. 6. The mutual inductance coupling between the two conductors can be equivalent to a voltage source on the conductor according to (A1) in Appendix. Since the driving-loop currents are far smaller than the power-loop currents, the influences of the magnetic coupling from the driving-loop to the power loop are ignored. Only the mutual inductance couplings between the power loops and the couplings form the power loops to the driving loops are

considered, which are equivalent to the voltage sources V_{Mg1}, V_{Mg2}, V_{Mk1}, V_{Mk2}, V_{Ms1}, and V_{Ms2}.

During switching transients, MOSFETs operated in the saturation region. They can be equivalent to current sources controlled by the gate-source voltages, which are expressed by

$$\begin{cases} i_{d\mathbf{1}} = g(v_{gs\mathbf{1}} - V_{\mathbf{th}})^2 \\ i_{d\mathbf{2}} = g(v_{gs\mathbf{2}} - V_{\mathbf{th}})^2 \end{cases} \tag{2}$$

where g is the transconductance and V_{th} is the threshold voltage. They depend on the performances of the SiC MOSFETs. Only layout-dominant dynamic current imbalances are considered, assuming the performances of parallel-connected chips are consistent. It can be inferred that

$$\begin{aligned} \Delta i_d &= i_{d\mathbf{1}} - i_{d\mathbf{2}} = g(v_{gs\mathbf{1}} - v_{\mathbf{gs2}})(v_{gs\mathbf{1}} + v_{gs\mathbf{2}} - 2V_{\mathbf{th}}) \\ &= g\Delta v_{gs\mathbf{12}}(v_{gs\mathbf{1}} + v_{gs\mathbf{2}} - 2V_{\mathbf{th}}) \end{aligned} \tag{3}$$

which indicates that balanced dynamic currents are achieved when the difference in gate-source voltage (Δv_{gs12}) between $Q1$ and $Q2$ is zero. Since gate currents (i_g) are very small, the KVL equations for drive loops 1 and 2 of $Q1$ and $Q2$ are obtained as follows:

$$\begin{cases} v_{gs1} = V_G - V_{Mg\mathbf{1}} - V_{Mk\mathbf{1}} - L_{k\mathbf{1}}\frac{di_{k\mathbf{1}}}{dt} \\ v_{gs2} = V_G - V_{Mg\mathbf{2}} - V_{Mk\mathbf{2}} - L_{k2}\frac{di_{k\mathbf{2}}}{dt}. \end{cases} \tag{4}$$

Equation (4) is further derived as follows:

$$\begin{aligned} \Delta v_{gs\mathbf{12}} &= V_{Mg\mathbf{2}} - V_{Mg\mathbf{1}} + V_{Mk\mathbf{2}} - V_{Mk\mathbf{1}} \\ &\quad + L_{k\mathbf{2}}\frac{di_{k\mathbf{2}}}{dt} - L_{k\mathbf{1}}\frac{di_{k\mathbf{1}}}{dt}. \end{aligned} \tag{5}$$

The KVL equation for loop 3 consisting of the power source and driving source of $Q1$ and $Q2$ is as follows:

$$\begin{aligned} &L_{s\mathbf{1}}\frac{di_{s\mathbf{1}}}{dt} - L_{s\mathbf{2}}\frac{di_{s\mathbf{2}}}{dt} + V_{Ms\mathbf{1}} - V_{Ms\mathbf{2}} + L_{k\mathbf{2}}\frac{di_{k\mathbf{2}}}{dt} \\ &\quad - L_{k\mathbf{1}}\frac{di_{k\mathbf{1}}}{dt} + V_{Mk\mathbf{2}} - V_{Mk\mathbf{1}} = 0. \end{aligned} \tag{6}$$

From (5) and (6), Δv_{gs12} can be derived as

$$\begin{aligned} \Delta v_{gs\mathbf{12}} &= V_{Mg\mathbf{2}} - V_{Mg\mathbf{1}} + V_{Ms\mathbf{2}} - V_{Ms\mathbf{1}} \\ &\quad + L_{s\mathbf{2}}\frac{di_{s\mathbf{2}}}{dt} - L_{s\mathbf{1}}\frac{di_{s\mathbf{1}}}{dt}. \end{aligned} \tag{7}$$

When dynamic current balancing is achieved in $Q1$–$Q4$, it can be considered that

$$\begin{cases} i_{d\mathbf{1}} = i_{d\mathbf{2}} = i_{d\mathbf{3}} = i_{d\mathbf{4}} = i_{Ld} \\ i_{s\mathbf{1}} = i_{s\mathbf{2}} = i_{s\mathbf{3}} = i_{s\mathbf{4}} = i_{Ls}. \end{cases} \tag{8}$$

To simplify the analysis, the currents of $Q5$–$Q8$ on the high side are assumed to be equal

$$\begin{cases} i_{d\mathbf{5}} = i_{d\mathbf{6}} = i_{d\mathbf{7}} = i_{d\mathbf{8}} = i_{Hd} \\ i_{s\mathbf{5}} = i_{s\mathbf{6}} = i_{s\mathbf{7}} = i_{s\mathbf{8}} = i_{Hs}. \end{cases} \tag{9}$$

The specific expressions for V_{Mg1}, V_{Mg2}, V_{Ms1}, and V_{Ms2} can be derived in Appendix (A2) and (A5). The gate current (i_g) and driving-source current (i_k) are much lower than the drain current (i_d) and power-source current (i_s). Therefore, it can be considered that

$$\begin{cases} i_{Hd} = i_{Hs} \\ i_{Ld} = i_{Ls}. \end{cases} \tag{10}$$

The KCL equation for the half-bridge midpoint ac is expressed as

$$i_{Hs} = i_{Ld} - \frac{I_{\mathbf{load}}}{4}. \tag{11}$$

By substituting (A2), (A3), and (8), (9), (10), (11) into (7), it can be derived that

$$\Delta v_{gs\mathbf{12}} = M_{12}\frac{di_{Hd}}{dt}. \tag{12}$$

The specific expression for the dynamic current sharing coefficient M_{12} is shown in Appendix (A4). It indicates that M_{12} could evaluate the dynamic current sharing performances between $Q1$ and $Q2$ when considering mutual inductance coupling. When M_{12} equals zero, $Q1$ and $Q2$ can achieve dynamic current balancing. Similarly, M_{13} and M_{14} could also be derived to evaluate the dynamic current sharing performances between $Q1$, $Q3$, and $Q4$. Meanwhile, according to (A4) and (A5), M_{Hd12} represents the influence level of high-side drains on the dynamic current sharing performance between $Q1$ and $Q2$ through the magnetic coupling of the high-side drains to the power sources and gates. Similarly, M_{Hs12}, $M_{Ld12,}$ and M_{Ls12} represent the influence level of high-side power sources, low-side drains, and power sources on dynamic current sharing performances, respectively.

Due to the influence of terminal height H on the self-inductance and mutual inductance coupling of the power module, the dynamic current sharing performances can be optimized by adjusting the terminal height to make M_{12}, M_{13}, and M_{14} close to 0.

C. Comprehensive Optimization of Parasitic Inductance and Current Sharing Performances

Based on the analysis of the above two parts, the terminal height H needs to be optimized to achieve extremely low parasitic inductance and high current sharing performances of the 2.5-D power module.

ANSYS Q3D was used to extract the parasitic inductance of the module with a frequency of 20 MHz at different terminal heights (from 2.1 to 6.5 mm), as shown by the blue line in Fig. 7, which indicates that the parasitic inductance of the module decreases with the decreasing terminal height. Considering the simple processing conditions in the laboratory and the insulation requirements, 2.5 mm is selected. At this time, the whole parasitic inductance is only 1.9 nH. The ultralow parasitic inductance is mainly attributed to two parts: a decrease in terminal height leads to a decrease in the self-inductance introduced by the terminals; and the reduction of terminal height significantly increases the mutual inductance cancellation effect of M_{+o} on the parasitic inductance of the commutation loop. When H is 2.5 mm, the parasitic inductance matrix of L_+, L_o, and M_{+o} is given in Table I. The total self-inductance of L_+ and L_o is 8.73 nH. The contribution of M_{+o} to the total loop inductance is twice that of M_{+o}, equal to -4.62 nH. Clearly, M_{+o} offsets 52.9% of L_+ and L_o, which is significant.

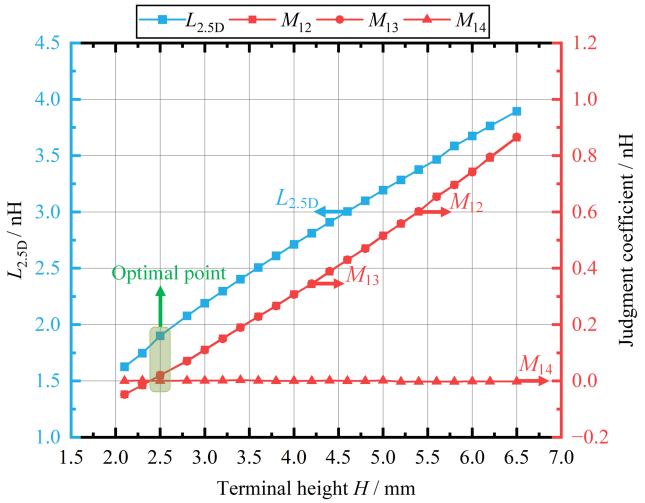


Fig. 7. Parasitic inductance ($L_{2.5D}$) and current sharing judgment coefficients (M_{12}, M_{13}, M_{14}) at different terminal heights (H).

TABLE I
PARASITIC INDUCTANCE MATRIX BETWEEN L_+ AND L_o

	L_+	L_o	M_{+o}
Inductance (nH)	7.16	1.57	-2.31

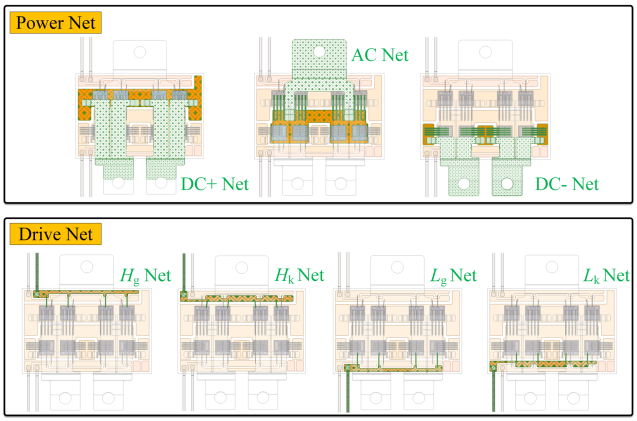


Fig. 8. ANSYS Q3D simulation nets.

Based on the analysis of Section III-B, as shown in Fig. 8, the parasitic inductance matrix was extracted by ANSYS Q3D to calculate the dynamic current sharing coefficients. First, the relationship between each part of the dynamic current sharing coefficient (M_{Hdxy}, M_{Hsxy}, M_{Ldxy}, M_{Lsxy}) and H is shown in Fig. 9. Take $Q1$ and $Q2$ as examples. As H increases, M_{Ld12} and M_{Ls12} increase, while M_{Hd12} and M_{Hs12} change little. It shows that low-side drains and power sources have a non-negligible influence on dynamic current sharing performances, while the influence of high-side drains and power sources can be ignored. Before analysis, the influence level of each part is unknown. Therefore, it is necessary to consider all mutual inductances and analyze them.

Furthermore, according to (A4), under different terminal heights, M_{12}, M_{13}, and M_{14} exhibit variations as illustrated by

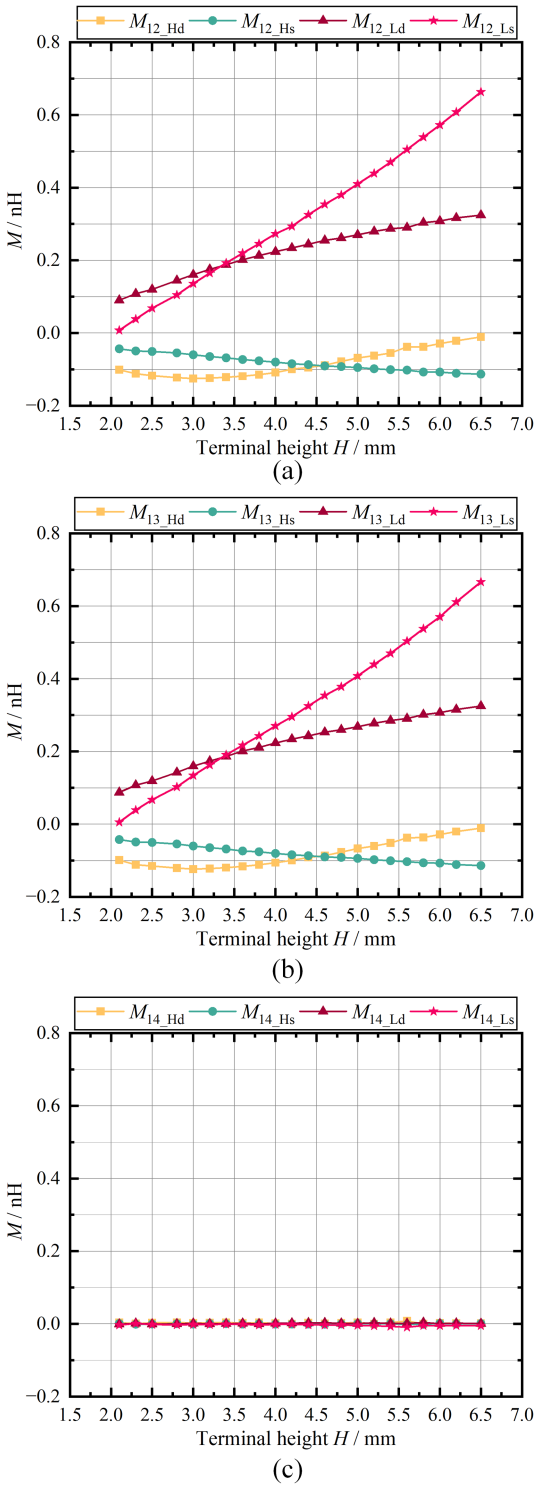


Fig. 9. Relationship between terminal height and each part of the current sharing coefficient. (a) $Q1$ and $Q2$. (b) $Q1$ and $Q3$. (c) $Q1$ and $Q4$.

the red lines in Fig. 7. To achieve absolutely balanced dynamic currents, it is necessary that M_{12}, M_{13}, and M_{14} concurrently are close to 0. Due to the symmetrical layout, M_{14} always approaches zero, which means that $Q1$ and $Q4$ always maintain balanced currents. When the terminal height H is 2.5 mm, M_{12} and M_{13} are close to zero, which means the dynamic currents

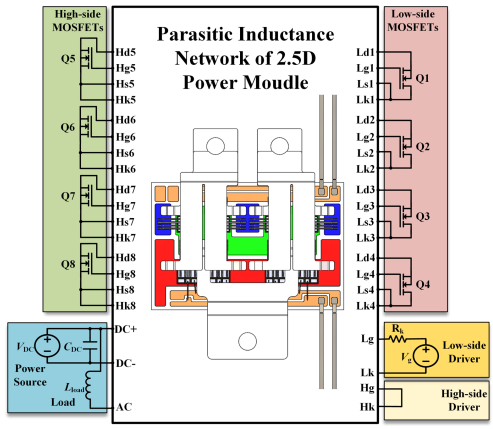


Fig. 10. Simulation schematic of the electromagnetic coupling for the low-side MOSFETs.

are balanced among $Q1$, $Q2$, and $Q3$. As the terminal height increases, M_{12} and M_{13} gradually increase, and the dynamic current sharing performances of $Q1$–$Q3$ gradually deteriorate.

In conclusion, the value of H is selected as 2.5 mm, considering the parasitic inductance and dynamic current sharing performances. The parasitic inductance of the 2.5-D power module is only 1.9 nH, and the dynamic currents between $Q1$ and $Q4$ can be balanced. In the future, as experimental conditions improve, it is expected that the terminal height can be further reduced to achieve lower parasitic inductance while ensuring balanced dynamic currents.

In order to verify the analysis and optimization of the dynamic current sharing performances of $Q1$–$Q4$, the parasitic inductance matrix extracted by ANSYS Q3D was imported into LTSPICE to build a double pulse testing circuit. The schematic diagram for the electromagnetic co-simulation is shown in Fig. 10. The bus voltage is 600 V and the load current is 180 A. When H is 6.5 mm the dynamic current waveforms of $Q1$–$Q4$ are shown in Fig. 11(a), where the maximum current difference among $Q1$–$Q4$ is 4.3 A. Under the optimized terminal height $H = 2.5$ mm, the maximum current peak-to-peak difference was reduced to only 1.1 A, as shown in Fig. 11(b).

IV. Fabrication and Test

In this section, the 2.5-D power module is fabricated and tested to verify the low parasitic inductance and high dynamic current sharing performance. Three different experiments are performed. On the one hand, the dynamic test is performed to verify the low parasitic inductance. However, limited to the inductance introduced by PCB, the low parasitic inductance can only be verified indirectly [18], [19], [20]. Therefore, the impedance test is additionally performed to directly demonstrate the ultralow parasitic inductance. On the other hand, to verify balanced dynamic currents directly, a dynamic current sharing test is conducted.

A. 2.5-D Power Module Fabrication

The fabrication process of the prototype of a multichip 2.5-D power module is shown in Fig. 12, and the materials used are

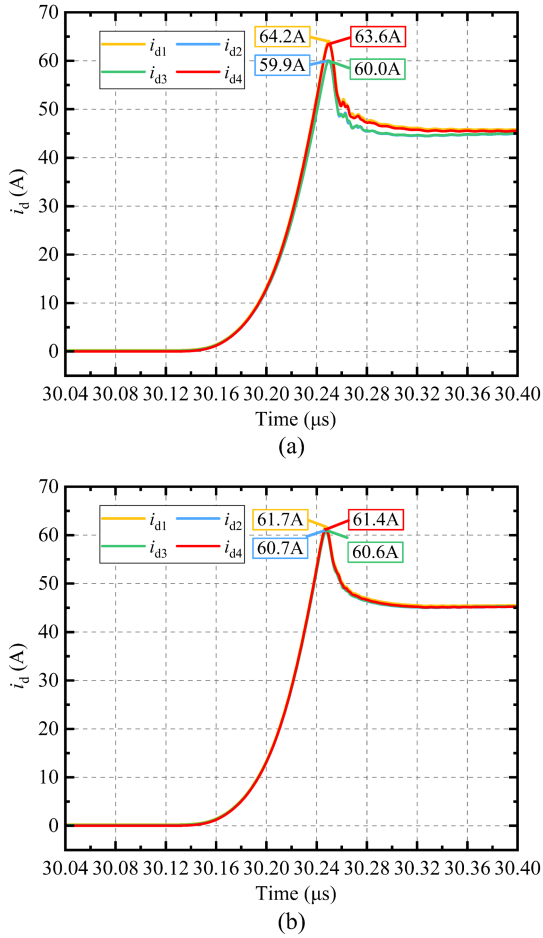


Fig. 11. Comparison of turn-on currents with different terminal heights. (a) $H = 6.5$ mm. (b) $H = 2.5$ mm.

TABLE II
Material List in Fabrication Process

	Material	Specifications
SiC MOSFET	S4651	1200 V/130 A (25 °C)
DBC	Si3N4 DBC	Cu/ Si3N4/Cu thickness: 0.25 mm/0.32 mm/0.25 mm Dimension:43.2 mm×28.6 mm
Bonding wires	Aluminum	Diameter for power: 15 mil Diameter for drive: 8 mil
Terminals	Copper	Thickness: 0.8 mm
Die to attach solder	Sn90Sb10	Melting point: 240 °C
Terminals attach solder	SAC305	Melting point: 217 °C

given in Table II. In the first step, eight SiC MOSFETs were soldered using Sn90Sb10 with a melting point of 240 °C. Then, the bonding wires of the power circuit and the driving circuit were bonded to connect the chip electrodes to the DBC Subsequently, the power terminals with PI film and the driving terminals were soldered using SAC305 with a melting point of 217 °C, whose

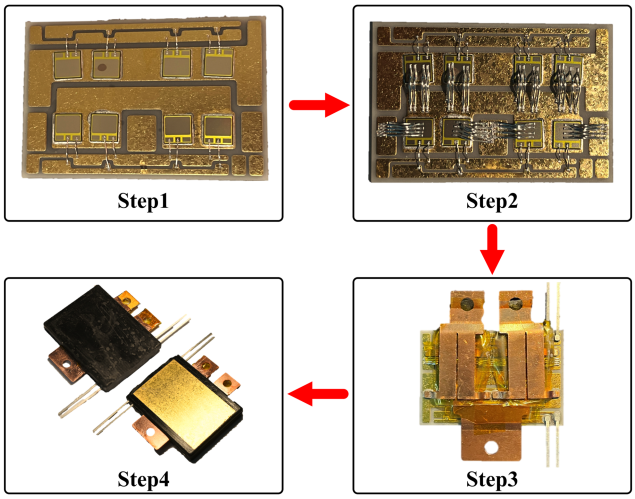


Fig. 12. Proposed 2.5-D power module fabrication progress.

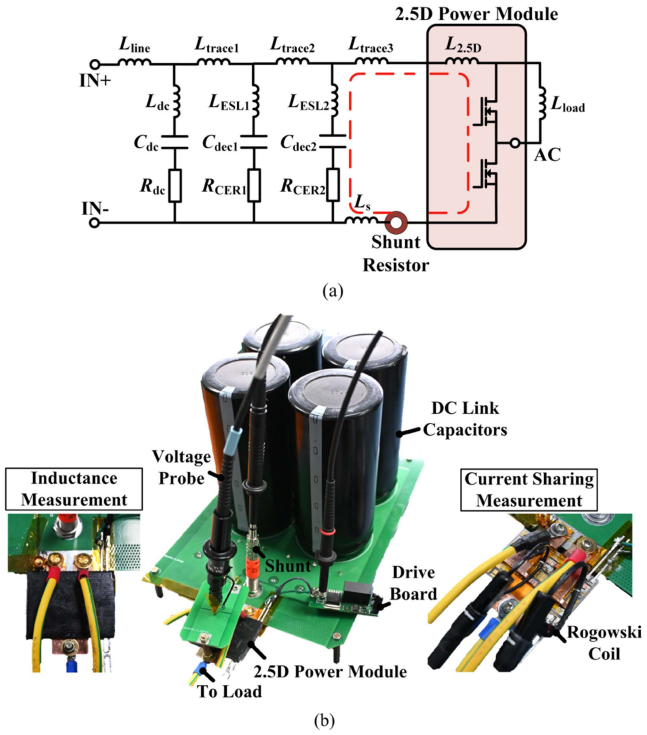


Fig. 13. Double pulse test for designed modules. (a) Circuit schematic of the power circuit. (b) Dynamic test PCB and measured 2.5-D power module.

melting point is lower than that of Sn90Sb10. Finally, epoxy resin was used to insulate during the molding process.

B. Dynamic Test and Results

First, dynamic testing is performed to verify the parasitic inductance of the 2.5-D power module, and the testing platform is shown in Fig. 13. The schematic diagram of the connection between the dc+ and dc- terminals and the PCB is shown in Fig. 14. The busbar dc+ of PCB is connected to the dc+ terminal through screws, and the busbar dc- and dc- terminals are directly connected in contact. The middle part of the screw was wrapped

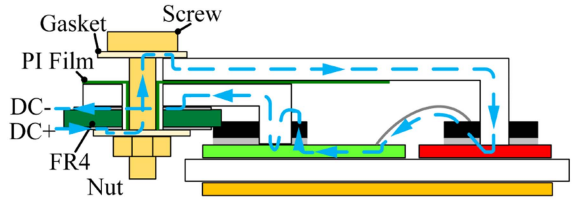


Fig. 14. Schematic diagram of the connection between the module and PCB.

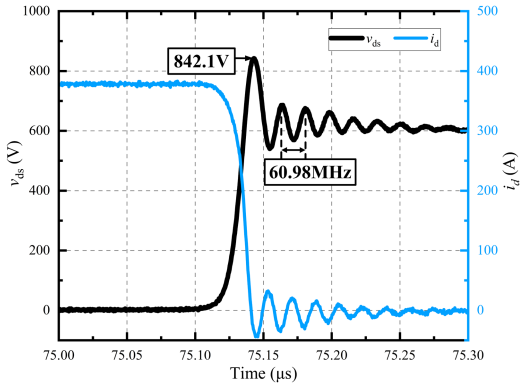


Fig. 15. Drain-source voltage ($v_{\rm ds}$) and total current(i_d) of the 2.5-D power module.

with PI film to ensure the insulation between the screw and the dc- terminal. High-side MOSFETs were used as diodes and the low-side MOSFETs were switched. T&M SSDN-10 (0.1 Ω, 2 GHz) shunt resistor was utilized to measure the load current. Decoupling capacitors were used to decouple the parasitic inductance introduced by the PCB and capacitors. Drain-source voltage was measured by a P5100A 1000 V/500 MHz voltage probe. The dc voltage is set to 600 V and the driving resistance is 1 Ω. +18/-2 V driving voltage was supplied to low-side MOSFETs through the drive board, and the load inductance was 77.6 μH.

The drain-source voltage (v_{ds}) and total current (i_d) of low-side MOSFETs during turn-OFF are shown in Fig. 15. The turn-OFF spike voltage is 842.1 V. The voltage oscillation frequency is 60.98 MHz. The parasitic inductance calculation formula is expressed as

$$f = \frac{1}{2\pi\sqrt{LC}}. \tag{13}$$

In (13), f is the voltage oscillation frequency, which is equal to 60.98 MHz, and C is the parasitic capacitance, composed of the output capacitance of the four MOSFETs and the parasitic capacitance of the electrode copper layer. Static testing was performed to measure the output capacitance of the processed module using the Keysight Power Device Analyzer B1505A. When the drain-source voltage is 600 V, the output capacitance is equal to 930 pF. Substituting C and f into (13), the parasitic inductance value calculated from the oscillation frequency is 7.32 nH. This parasitic inductance is higher than that obtained from the simulation, which is mainly caused by the additional parasitic inductance ($L_{\rm trace3} + L_{\rm ESL2} + L_s$) introduced by the PCB, final decoupling capacitor, and shunt, as shown in Fig. 13(a). The geometry containing both the PCB test board and

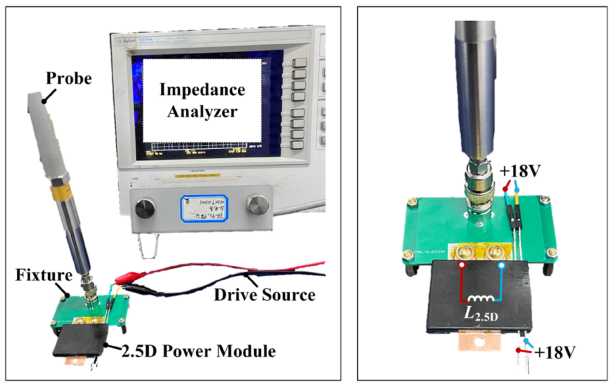


Fig. 16. Impedance test. (a) Overall platform diagram. (b) Module measurement diagram.

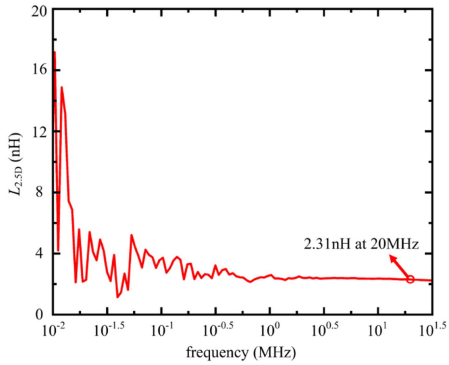


Fig. 17. Experimental results of 2.5-D module parasitic inductance.

power module was established in Q3D, and the overall parasitic inductance ($L_{2.5\mathrm{D}} + L_{\mathrm{trace3}} + L_{\mathrm{ESL2}} + L_s$) was extracted. The result is 6.95 nH, which is close to the experimental results. Therefore, the parasitic inductance of the proposed 2.5-D module is validated indirectly.

C. Impedance Test and Results

Furthermore, to directly validate the low parasitic inductance of the proposed 2.5-D power module, an impedance test was conducted on the fabricated module, as shown in Fig. 16. The Keysight 4294 A impedance analyzer, operating in the frequency range from 40 to 110 MHz, was utilized for measuring the module's parasitic inductance ($L_{2.5\mathrm{D}}$). The impedance analyzer injects high-frequency current into the conductors and obtains the parasitic inductance by measuring the voltage across the conductors. A probe and fixture were employed to connect the power module to the impedance analyzer. Due to the low parasitic inductance of the power module, the probe and fixture are carefully calibrated before testing to compensate for their introduced parasitic inductances.

During the measurement, +18 V driving voltages are applied to both the high-side and low-side driving terminals to turn on the internal MOSFETs. Fig. 17 illustrates the experimental results of the parasitic inductance. The frequency scan range is from 10 to 30 MHz. Consistent with the simulated frequency,

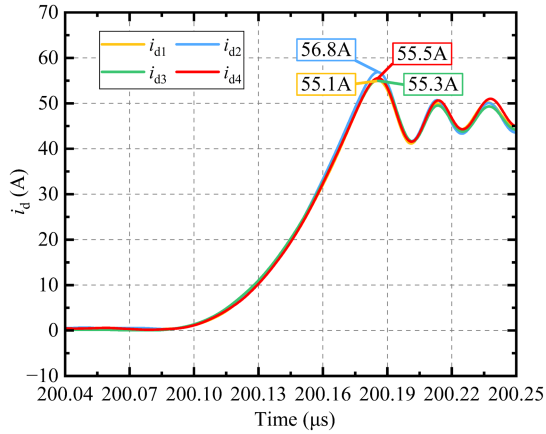


Fig. 18. Dynamic current sharing waveforms of fabricated 2.5-D power module.

at 20 MHz, the parasitic inductance of the module is measured as 2.31 nH. There is a certain discrepancy between the results and simulations. It may be due to incomplete calibration of the fixture's parasitic inductance and some differences between the fabricated module and the simulation model. For instance, the terminal height and gap are not strictly controlled due to the tolerances of terminals. However, the experimental result is enough to validate the low parasitic inductance of the proposed module.

D. Dynamic Current Sharing Test and Results

Finally, the dynamic currents of each MOSFET are measured to verify the dynamic current sharing performance of the designed power module. Before the experiment, the static performances of SiC MOSFETs were measured. MOSFETs with similar parameters are used to ensure consistent static parameters between parallel chips. Rogowski coils were mounted on the power source bonding wires of each MOSFET to measure the dynamic current of each chip. Due to terminal height limitations, only two bonding wires are bonded on each chip to allow enough space for current measurement. Due to symmetry, it has little effect on the current sharing performances of parallel chips. Meanwhile, for the measurement requirements, the module cannot be sealed, as shown in Fig. 13(b). Therefore, the power module was tested under 150 V for safety, which can already demonstrate the dynamic current sharing performances of the module. The dynamic current measured is shown in Fig. 18. i_{d1}–i_{d4}, respectively, represent the currents flowing through MOSFETs Q1-Q4. The maximum peak dynamic current difference of low-side MOSFETs in parallel is only 1.7 A, indicating that the dynamic current balancing performances of the four SiC MOSFETs in parallel in the designed 2.5-D power module were fully verified.

V. Conclusion

This article proposed a novel 2.5-D wire-bonding multichip SiC power module with low parasitic inductance and high dynamic current sharing performance. A compact, highly symmetrical 3-D commutation loop was formed through a special structure without any additional substrates. Parasitic inductance and dynamic current-sharing performances are analyzed

and optimized considering mutual inductance coupling. A 1200 V/520 A half-bridge power module was fabricated after optimizing the terminal structure. The ultralow parasitic inductance and high dynamic current sharing performance of the 2.5-D power module were experimentally verified via dynamic test, impedance test, and dynamic current sharing test. Due to the outstanding mutual inductance cancellation of the 3-D commutation loop, the parasitic inductance of the fabricated module is only 2.31 nH from impedance testing, which leads to good dynamic performances during the transient process. Based on the high symmetry of the power module layout, the maximum dynamic current difference of parallel SiC MOSFETs is only 1.7 A, which achieves balanced dynamic currents. Therefore, the proposed power module not only retains the simple and low-cost performances of 2-D packaging structure but also achieves the high electrical performance of 3-D packaging, which promotes widespread application in the packaging industry.

APPENDIX

A. Equivalent Voltage Sources of Mutual Inductance Coupling

The mutual inductance coupling between two conductors can be regarded as additional voltage sources determined by the other party's current and mutual inductance value. The expressions of the extra voltages generated are shown as

$$\begin{cases} V_{M\mathbf{1}} = M\frac{di_2}{dt} \\ V_{M\mathbf{2}} = M\frac{di_1}{dt} \end{cases} \tag{A1}$$

where V_{M1} and V_{M2} are the equivalent voltage drops of the two conductors due to mutual inductance coupling. M is the mutual inductance value between conductors. i_1 and i_2 are the currents flowing through the two conductors, respectively,

In theory, mutual inductance exists between any two parasitic inductances. However, both the gate current i_{g} and the driving source current $\mathrm{i_k}$ of the drive loop are much smaller than the power-loop current. According to expression (A1), the equivalent voltage drops in the power branches caused by the drive currents can be ignored. Therefore, the parasitic circuit model only considers the magnetic coupling between the power loops and the coupling from the power loop to the driving loop. Therefore, combining (8) and (9), the specific expressions of V_{Mg1}, V_{Mg2}, V_{Ms1}, and V_{Ms2} can be written as shown in (A2) and (A3) shown at the bottom of this page.

B. Dynamic Current Sharing Judgment Coefficients

The specific expression of the dynamic current sharing judgment coefficient M_{12} between $Q1$ and $Q2$ is as follows:

$$M_{12} = M_{Hd\mathbf{12}} + M_{Hs\mathbf{12}} + M_{Ld\mathbf{12}} + M_{Ls\mathbf{12}} \tag{A4}$$

where the specific expressions of M_{Hd12}, M_{Hs12}, M_{Ld12}, and M_{Ls12} are shown in (A5) shown at the bottom of this page. Similar judgment coefficients M_{13} and M_{14} between $Q1$, $Q2$, and $Q3$ can be derived. Only the subscripts are different. So, they are not shown here

REFERENCES

[1] D. Zhang, J. He, and D. Pan, "A megawatt-scale medium-voltage high-efficiency high power density 'SiC+Si' hybrid three-level ANPC inverter for aircraft hybrid-electric propulsion systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2018, pp. 806–813.

[2] J. Liu, W. Su, X. Tai, W. Sun, L. Gu, and X. Wen, "Development of an inverter using hybrid SIC power module for EV/HEV applications," in *Proc. 19th Int. Conf. Electr. Mach. Syst.*, 2016, pp. 1–5.

[3] J. Feng, W. Q. Chu, Z. Zhang, and Z. Q. Zhu, "Power electronic transformer-based railway traction systems: Challenges and opportunities," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 1237–1253, Sep. 2017.

[4] S. S. Williamson, A. K. Rathore, and F. Musavi, "Industrial electronics for electric transportation: Current state-of-the-art and future challenges," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3021–3032, May 2015.

[5] C. Chen, F. Luo, and Y. Kang, "A review of SiC power module packaging: Layout, material system, and integration," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 170–186, Sep. 2017.

[6] H. Lee, V. Smet, and R. Tummala, "A review of SiC power module packaging technologies: Challenges, advances, and emerging issues," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 239–255, Mar. 2020.

$$\begin{bmatrix} V_{Ms\mathbf{1}} \\ V_{Ms\mathbf{2}} \end{bmatrix} = \begin{bmatrix} M_{s\mathbf{1}d\mathbf{5}} + M_{s\mathbf{1}d\mathbf{6}} & M_{s\mathbf{1}s\mathbf{5}} + M_{s\mathbf{1}s\mathbf{6}} & M_{s\mathbf{1}d\mathbf{1}} + M_{s\mathbf{1}d\mathbf{2}} & M_{s\mathbf{1}s\mathbf{2}} + M_{s\mathbf{1}s\mathbf{3}} \\ +M_{s\mathbf{1}d\mathbf{7}} + M_{s\mathbf{1}d\mathbf{8}} & +M_{s\mathbf{1}s\mathbf{7}} + M_{s\mathbf{1}s\mathbf{8}} & +M_{s\mathbf{1}d\mathbf{3}} + M_{s\mathbf{1}d\mathbf{4}} & +M_{s\mathbf{1}s\mathbf{4}} \\ M_{s\mathbf{2}d\mathbf{5}} + M_{s\mathbf{2}d\mathbf{6}} & M_{s\mathbf{2}s\mathbf{5}} + M_{s\mathbf{2}s\mathbf{6}} & M_{s\mathbf{2}d\mathbf{1}} + M_{s\mathbf{2}d\mathbf{2}} & M_{s\mathbf{2}s\mathbf{1}} + M_{s\mathbf{2}s\mathbf{3}} \\ +M_{s\mathbf{2}d\mathbf{7}} + M_{s\mathbf{2}d\mathbf{8}} & +M_{s\mathbf{2}s\mathbf{7}} + M_{s\mathbf{2}s\mathbf{8}} & +M_{s\mathbf{2}d\mathbf{3}} + M_{s\mathbf{2}d\mathbf{4}} & +M_{s\mathbf{2}s\mathbf{4}} \end{bmatrix} \begin{bmatrix} \frac{di_{Hd}}{dt} \\ \frac{di_{Hs}}{dt} \\ \frac{di_{Ld}}{dt} \\ \frac{di_{Ls}}{dt} \end{bmatrix} \tag{A2}$$

$$\begin{bmatrix} V_{Mg1} \\ V_{Mg2} \end{bmatrix} = \begin{bmatrix} M_{g1d5} + M_{g1d6} & M_{g1s5} + M_{g1s6} & M_{g1d1} + M_{g1d2} & M_{g1s1} + M_{g1s2} \\ +M_{g1d7} + M_{g1d8} & +M_{g1s7} + M_{g1s8} & +M_{g1d3} + M_{g1d4} & +M_{g1s3} + M_{g1s4} \\ M_{g2d5} + M_{g2d6} & M_{g2s5} + M_{g2s6} & M_{g2d1} + M_{g2d2} & M_{g2s1} + M_{g2s2} \\ +M_{g2d7} + M_{g2d8} & +M_{g2s7} + M_{g2s8} & +M_{g2d3} + M_{g2d4} & +M_{g2s3} + M_{g2s4} \end{bmatrix} \begin{bmatrix} \frac{di_{Hd}}{dt} \\ \frac{di_{Hs}}{dt} \\ \frac{di_{Ld}}{dt} \\ \frac{di_{Ls}}{dt} \end{bmatrix}. \tag{A3}$$

$$\begin{cases} M_{Hd12} = (M_{s2d5} + M_{s2d6} + M_{s2d7} + M_{s2d8}) - (M_{s1d5} + M_{s1d6} + M_{s1d7} + M_{s1d8}) \\ +(M_{g2d5} + M_{g2d6} + M_{g2d7} + M_{g2d8}) - (M_{g1d5} + M_{g1d6} + M_{g1d7} + M_{g1d8}) \\ M_{Hs12} = (M_{s2s5} + M_{s2s6} + M_{s2s7} + M_{s2s8}) - (M_{s1s5} + M_{s1s6} + M_{s1s7} + M_{s1s8}) \\ +(M_{g2s5} + M_{g2s6} + M_{g2s7} + M_{g2s8}) - (M_{g1s5} + M_{g1s6} + M_{g1s7} + M_{g1s8}) \\ M_{Ld12} = (M_{s2d1} + M_{s2d2} + M_{s2d3} + M_{s2d4}) - (M_{s1d1} + M_{s1d2} + M_{s1d3} + M_{s1d4}) \\ +(M_{g2d1} + M_{g2d2} + M_{g2d3} + M_{g2d4}) - (M_{g1d1} + M_{g1d2} + M_{g1d3} + M_{g1d4}) \\ M_{Ls12} = (M_{s2s1} + L_{s2} + M_{s2s3} + M_{s2s4}) - (L_{s1} + M_{s1s2} + M_{s1s3} + M_{s1s4}) \\ +(M_{g2s1} + M_{g2s2} + M_{g2s3} + M_{g2s4}) - (M_{g1s1} + M_{g1s2} + M_{g1s3} + M_{g1s4}) \end{cases}. \tag{A5}$$

[7] G. Yadav and S. S. Nag, "Review of factors affecting current sharing and techniques for current balancing in paralleled wide bandgap devices," in *Proc. 3rd Int. Conf. Energy, Power Environ.: Towards Clean Energy Technol.*, , pp. 1–6.
[8] S. Tiwari, O.-M. Midtgard, and T.M. Undeland, "Comparative evaluation of a commercially available 1.2 kV SiC MOSFET module and a 1.2 kV Si IGBT module," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, 2016, pp. 1093–1098.
[9] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, and Y. Kang, "An SiC-based half-bridge module with an improved hybrid packaging method for high power density applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8980–8991, Nov. 2017.
[10] W. Jakobi et al., "Benefits of new CoolSiCTM MOSFET in HybridPACKTM Drive package for electrical drive train applications," in *Proc. 10th Int. Conf. Integr. Power Electron. Syst.*, 2018, pp. 1–9.
[11] 2024. [Online]. Available: https://www.danfoss.com/en-us/about-danfoss/our-businesses/silicon-power/danfoss-dcm-1000-power-module-technology-platform/
[12] S. Li, L. M. Tolbert, F. Wang, and F. Z. Peng, "Stray inductance reduction of commutation loop in the P-cell and N-cell-based IGBT phase leg module," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3616–3624, Jul. 2014.
[13] Z. Wang, F. Yang, S. L. Campbell, and M. Chinthavali, "Characterization of SiC trench MOSFETs in a low-inductance power module package," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4157–4166, Jul./Aug. 2019.
[14] L. Qiao et al., "Performance of a 1.2kV, 288A full-SiC MOSFET module based on low inductance packaging layout," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, , 2017, pp. 3038–3042.
[15] M. Wang, F. Luo, and L. Xu, "A double-end sourced wire-bonded multichip SiC MOSFET power module with improved dynamic current sharing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1828–1836, Dec. 2017.
[16] P. Beckedahl, M. Spang, and O. Tamm, "Breakthrough into the third dimension - sintered multi-layer flex for ultra-low inductance power modules," in *Proc. 8th Int. Conf. Integr. Power Electron. Syst.*, 2014, pp. 1–5.
[17] I. Kasko, S. E. Berberich, M. Gross, P. Beckedahl, and S. Buetow, "High efficient approach to utilize SiC MOSFET potential in power modules," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's*, 2017, pp. 259–262.
[18] C. Chen, Z. Huang, L. Chen, Y. Tan, Y. Kang, and F. Luo, "Flexible PCB-based 3-D integrated SiC half-bridge power module with three-sided cooling using ultralow inductive hybrid packaging structure," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5579–5593, Jun. 2019.
[19] Z. Huang, C. Chen, Y. Xie, Y. Yan, Y. Kang, and F. Luo, "A high-performance embedded SiC power module based on a DBC-stacked hybrid packaging structure," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 351–366, Mar. 2020.
[20] Y. Yan, C. Chen, Z. Wu, J. Guan, J. Lv, and Y. Kang, "A high power density double-side-end double-sided bonding SiC half-bridge power module," *IEEE Trans. Transp. Electrific.*, vol. 9, no. 2, pp. 3149–3163, Jun. 2023.
[21] F. Yang, Z. Wang, Z. Liang, and F. Wang, "Electrical performance advancement in SiC power module package design with kelvin drain connection and low parasitic inductance," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 84–98, Mar. 2019.
[22] A. I. Emon, Y. Wu, Y. Li, A. B. Mirza, S. Deng, and F. Luo, "A double-sided cooled split-phase SiC power module with fuzz button interposer," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 5, pp. 4918–4928, Oct. 2023.
[23] H. Ke, U. Mehrotra, and D. C. Hopkins, "3-D prismatic packaging methodologies for wide band gap power electronics modules," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13057–13066, Nov. 2021.
[24] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance evaluation of high-power SiC MOSFET modules in comparison to Si IGBT modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019.
[25] Ó. Lucía, X. She, and A. Q. Huang, "Wide bandgap devices and power conversion systems—Part I," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8190–8192, Oct. 2017.
[26] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.
[27] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 1563–1569.
[28] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active compensation of current unbalance in paralleled silicon carbide MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1471–1477.
[29] S. G. Kokosis, I. E. Andreadis, G. E. Kampitsis, P. Pachos, and S. Manias, "Forced current balancing of parallel-connected SiC JFETs during forward and reverse conduction mode," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1400–1410, Feb. 2017.
[30] J. Lv, C. Zhang, C. Chen, and Y. Kang, "A dynamic current sharing method in multi-chip SiC power module using stacked DBC bridges and decoupling capacitors based on the original simple module layout," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, 2021, pp. 184–188.
[31] J. Lv, C. Chen, B. Liu, Y. Yan, and Y. Kang, "A dynamic current balancing method for paralleled SiC MOSFETs using monolithic Si-RC snubber based on a dynamic current sharing model," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13368–13384, Nov. 2022.
[32] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with aid of a differential mode choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, Feb. 2020.
[33] S. Bęczkowski, A. B. Jørgensen, H. Li, C. Uhrenfeldt, X. Dai, and S. Munk-Nielsen, "Switching current imbalance mitigation in power modules with parallel connected SiC MOSFETs," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.8.
[34] B. Zhang et al., "Common source inductance compensation technique for dynamic current balancing in SiC MOSFETs parallel operations," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13944–13956, Nov. 2023.
[35] H. Li, S. Munk-Nielsen, S. Beczkowski, and X. Wang, "A novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power modules," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 704–708.
[36] H. Li, S. Munk-Nielsen, S. Bęczkowski, and X. Wang, "A novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8042–8045, Dec. 2016.
[37] B. Zhao, J. Ke, Q. Yu, P. Sun, Y. Cai, and Z. Zhao, "Effect of common branch impedance coupling and mutual inductance on current sharing of paralleled SiC MOSFETs with different layouts," *IET Power Electron*, vol. 15, pp. 43–56, 2022.
[38] Y. Ge, Z. Wang, Y. Yang, C. Qian, G. Xin, and X. Shi, "Layout-dominated dynamic current balancing analysis of multichip SiC power modules based on coupled parasitic network model," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2240–2251, Feb. 2023.
[39] Z. Zheng, C. Chen, J. Lv, Y. Yan, J. Liu, and Y. Kang, "A dynamic current sharing model of multichip parallel SiC MOSFETs considering layout-dominated mutual inductance coupling," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 11060–11073, Sep. 2024.
[40] J. Lv, C. Chen, B. Liu, Y. Yan, Z. Zheng, and Y. Kang, "Dynamic current sharing mechanism analysis of paralleled SiC MOSFETs considering parasitic mutual inductances based on an improved model," *IEEE Trans. Power Electron.*, vol. 39, no. 6, pp. 7536–7559, Jun. 2024.

Zexiang Zheng received the B.S. degree in electrical and electronic engineering in 2023 from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

His current research interests include wide-bandgap devices modeling, packaging, and high power density inverters.

Jianwei Lv received the B.S. degree in electrical and electronic engineering in 2020 from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

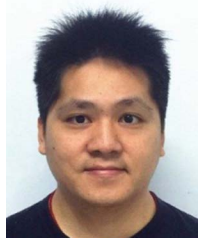
His current research interests include WBG devices modeling, packaging and integration.

Yiyang Yan received the B.S. degree in functional material and electrical and electronic engineering and the M.S. degree in electrical engineering in 2018 and 2021, respectively, from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

His current research interests include wide-bandgap devices double-sided cooling package, high power density inverters, and package thermal modeling.

Jiaxin Liu (Member, IEEE) was born in Liaoning, China, in 1995. She received the B.S. degree in material processing engineering from the School of materials science and engineering, Northeastern University, Shenyang, China, in 2018, and the Ph.D. degree in mechanical manufacturing and automation from the School of mechanical science and engineering, Huazhong University of Science and Technology, Wuhan, China, in 2023.

In 2023, she was with the Advanced Semiconductor, Packaging and Integration Laboratory, Huazhong University of Science and Technology, as a Post-Doctoral Researcher. Her research interests include wide-bandgap device packaging, micro/nano low-temperature bonding technology, and electronic packaging reliability.



Cai Chen (Member, IEEE) received the B.S. and Ph.D. degrees in electrical and electronic engineering from Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2014, respectively.

He is currently an Associate Research Fellow with Huazhong University of Science and Technology. From March to December 2013, he was an Intern with GE Global Research Center, Shanghai, China. From 2014 to 2016, he was with the Advanced Semiconductor, Packaging and Integration Lab, Huazhong University of Science and Technology, Wuhan, China, as a Postdoctoral Researcher. From 2016 to 2017, he was a Visiting Scholar with the Center for High Performance Power Electronics, The Ohio State University, Columbus, OH, USA. From 2017 to 2018, he was a Visiting Scholar with the College of Engineering, University of Arkansas, Fayetteville, AR, USA. In 2019, he was with the Huazhong University of Science and Technology, Wuhan, China, as an Associate Research Fellow. His research interests include WBG devices packaging, integration, packaging EMI issues, packaging reliability and high-density applications.

Yong Kang (Fellow, IEEE) was born in Hubei Province, China, in 1965. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan China, in 1988, 1991, and 1994, respectively.

In 1994, he was a Lecturer with Huazhong University of Science and Technology and was promoted to an Associate professor in 1996 and a Full Professor in 1998. He is the author of more than 60 technical papers. His research interests include power electronic converter, ac drivers, electromagnetic compatibility, their digital control techniques, WBG device packaging and applications.