Smoothed TCM-DPWM and Input Current Ripple Reduction for Three-Phase DC–AC ZVS Inverters

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***Abstract*—With the development of wide bandgap devices, the research and development of wide-frequency, high-efficiency, high-power-density three-phase inverters can play a positive role in the fields of electric vehicles, and microgrid. However, existing three-phase inverter schemes struggle to keep balance among wide output frequency range, high efficiency, high power density, and low EMI, while maintaining simple hardware structure and control strategies. In this article, based on the three-phase two-level inverter topology with dc-link connected output capacitors, a novel triangular current mode discontinuous pulsewidth modulation (TCM-DPWM) method is proposed. This method achieves the aforementioned advantages with a simple hardware and offers higher efficiency compared to existing modulation techniques. Initially, a smoothed DPWM method is introduced to enable smooth transitions at unsmooth points. Building on this method, a TCM-based approach is further proposed to achieve zero voltage switching (ZVS) soft-switching, significantly reducing the turn-ON losses of the switching devices. As the connection to dc-link of the output capacitors may lead to substantial input current ripple, two methods using resonant input filter and split output capacitors are presented to reduce this ripple. Employing the proposed methods, a prototype using GaN devices is constructed, achieving a full-load (490 W) efficiency of 98.478% and a power density of 245 W/in^3. The prototype could reach an output frequency of up to 400 Hz, with the input current ripple reduced to about 10%.**

***Index Terms*—DC–AC converter, discontinuous pulsewidth modulation, three-phase inverter, triangular current mode, wide band-gap devices, zero voltage switching.**

I. Introduction

THREE-phase dc–ac conversion has wide applications such as motor drives and microgrids [1]. By improving inverter technology, not only can the conversion efficiency be improved, but also the EMI reduced, which contributes to the achievement of zero-carbon goals. The application of wide-bandgap devices in power electronics conversion is increasing [2]. Due to their superior switching characteristics, they can improve the overall efficiency and power density of converters, making it easier for the converter to be adopted and integrated. Therefore, research for high-efficiency, high-power-density, and low-EMI three-phase inverters based on wide-bandgap devices holds significant theoretical and practical importance. This work is based on the 9th "GaN Systems Cup" power electronics application design competition, which is a 500 W three-phase inverter. For photovoltaic and fuel cell applications, the current ripple has negative influences on the whole systems [3], [4], due to the low input current ripple and high efficiency operation of proposed techniques, it will be also suitable for this dc–ac inverter in photovoltaic based microgrid and motor drive for fuel cell vehicles.

The three-phase two-level inverter, with its simple topology and lower implementation cost, is widely used in the low-voltage fields [5]. Its topology includes pure inductor filter in [6], differential-mode filter in [7] and [8], and dc-link connected filter in [9], [10], and [11]. For the differential-mode filter topology, compared with dc-link connected filter, the pressure of the filter is smaller, which is beneficial for efficiency improvement. However, the output three-phase voltages of a inverter often contain a high amplitude high frequency common-mode voltage, and additional filters is needed to address this issue, otherwise, significant EMI may occur [12]. When the inverter is used for motor drives, the high amplitude high frequency common-mode voltage can lead to bearing currents and related corrosion [13]. For three-phase two-level dc–ac conversion, the triangular current mode (TCM) is commonly used to achieve soft turn-ON of switching devices [6], [10], [14], while reducing the inductor volume to achieve higher power density. Since the turn-ON losses of GaN devices are much greater than their very low turn-OFF losses [15], optimizing the zero voltage switching (ZVS) turn-ON of GaN devices has become an important research direction. The B-TCM and S-TCM modulation methods proposed for achieving ZVS soft turn-ON in dc–ac inverters [9], [10] are based on sinusoidal pulse width modulation (SPWM) method, where the three-phase switches are at high switching frequency all the time. In contrast, the discontinuous pulsewidth modulation (DPWM) method allows for no switching action for 1/3 of the whole period per phase [16], which may reduce switching losses and losses at output filter [17], [18]. For dc–ac converters using pure inductor filter and differential-mode filter, various DPWM control schemes realizing ZVS have been developed and achieving good results [6], [7], [8]. However, for dc-link connected

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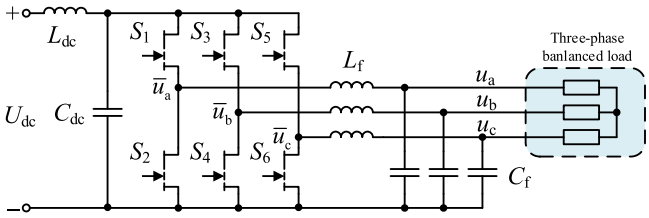

Fig. 1. Three-phase two-level DC–AC inverter with input and output filter.

TABLE I
PARAMETERS OF DC–AC INVERTER

P_o	U_{dc}	U_{ac}	f_{ac}
500 W	350 V	220 V	50–400 Hz

filter, the conventional DPWM method is difficult to apply due to the sudden changes of the three-phase common-mode voltage. There are existing methods for implementing DPWM through TCM in two-level three-phase inverters, but significant spikes occur at the discontinuous points [11]. The TCM for ZVS Buck converter have also been studied, including its soft-switching mechanism [19], state plane trajectory [20], optimal dead-time [20], [21], and TCM can be simply achieved by increasing the inductor ripple [22], [23]. These researches could also be used in this topology.

A new DPWM method for three-phase inverter achieving ZVS turn-ON through TCM is proposed in this article. This method employs a smoothed DPWM modulation technique and achieves TCM soft switching through frequency variation. It enables ZVS turn-ON of the switching devices, and it is free from voltage and current spikes. This method facilitates the soft turn-ON of devices across a wide output power and power factor (PF) range, with small input current ripple, and the output voltage is devoid of high-frequency common-mode components.

II. TOPOLOGY AND MODULATION ANALYSIS

Fig. 1 presents the schematic diagram of the selected topology, which is based on a three-phase two-level inverter, with the addition of *LC* filtering stages at both the input and output. The output filter capacitors are connected to the dc-link, allowing for independent control of the three phases, and enabling the output filter to suppress the common-mode voltage at the output. The input filter is employed to attenuate the ripple in the input current, thus preventing adverse effects on the power source. The topology is selected to generate a three-phase three wire output and no neutral connection, it can only work with Δ-connection load or balanced Y-connection load.

The parameters of the converter designed in this article are shown in Table I. The output power of the inverter is denoted by P_o, while U_{dc} represents the input dc voltage, and U_{ac} represents the rms value of the output ac voltage. The term f_{ac} refers to the output frequency range of the converter.

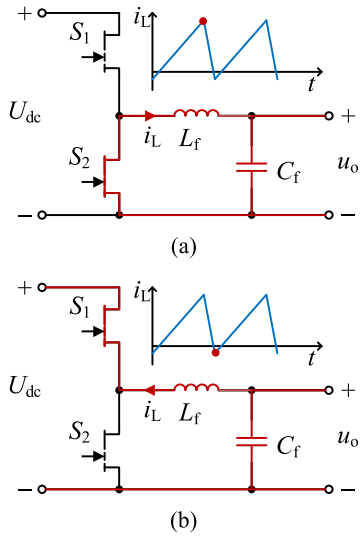

Fig. 2. Current path in the deadtime of a half-bridge. (a) Peak current of the inductor. (b) Valley current of the inductor.

A. ZVS Achieving Concept

By independently control the switching frequencies of each phase, the magnitude of the peak-to-peak inductor current can be regulated, allowing the current to reverse within each switching cycle. This ensures that both the top and bottom transistors of the half-bridge can realize ZVS turn-ON [14], [19]. For one half-bridge, when the inductor current peak-to-peak ripple is sufficient to reverse the current, the flow of current during the dead-time of both transistors is illustrated in Fig. 2. As shown in Fig. 2(a), when the inductor current is at its peak, it can discharge the parasitic capacitance of S_2, enabling ZVS upon subsequent turn-ON. As shown in Fig. 2(b), when the inductor current is at its valley and if reverses to a negative value, the inductor current during the dead-time can discharge the parasitic capacitance of S_1, facilitating ZVS upon turn-ON. However, if the inductor current does not reverse, the parasitic capacitance of S_1 cannot be discharged, preventing ZVS turn-ON for S_1. TCM regulates the inductor current ripple to achieve zero-crossing of inductor current in each switching cycle, thus enabling ZVS turn-ON for both top and bottom switches of each half-bridge. The detailed waveforms and state plane trajectory analysis for ZVS realization have been analyzed in [20].

B. Modulation Method of Output Voltage

The DPWM method allows each phase for no switching actions within 1/3 output voltage period, thereby reducing the switching losses of the switching devices as well as the filter losses. For the topology used, due to the presence of dc-link connected capacitors at the output, the conventional DPWM method causes spikes in the output voltages at the unsmooth points, resulting in significant ripple in the input current at the same time, which limits the application of DPWM in TCM three-phase inverters.

To address this issue, a method of smoothed DPWM method for three-phase inverter is proposed. Under given input and

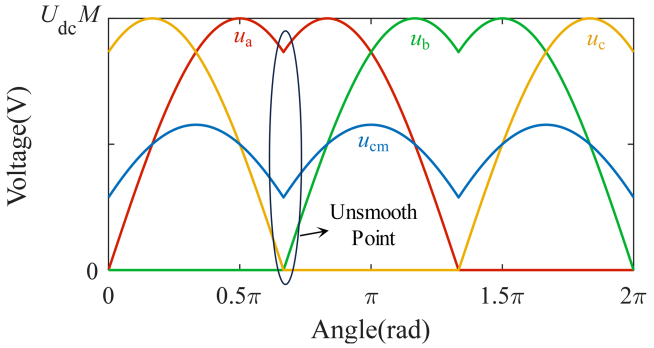

Fig. 3. DPWMNIN generated phase voltages and common-mode voltage.

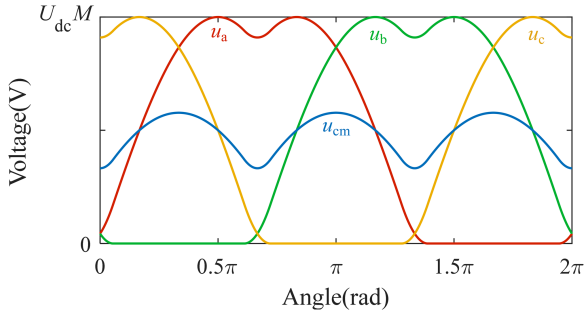

Fig. 4. Smoothed DPWMNIN generated phase voltages and common-mode voltage.

output voltages, the modulation ratio for the three-phase DPWM can be calculated as

$$M = \frac{\sqrt{2}U_{ac}}{U_{dc}}. \tag{1}$$

Given that the DPWMMIN and DPWMMAX methods [16] do not exhibit sudden changes in the amplitude of the output voltage compared to other DPWM methods, but only in the voltage slope, they are more amenable to be smoothed. DPWMMAX clamps the output voltage to the dc positive rail for a long time without switching actions, resulting in the top switches being continuously on. This may lead to the top switches failing to maintain its ON-state when using bootstrap power supply. However, the corresponding bottom switches in DPWMMIN does not encounter this issue, thus, DPWMMIN is selected as the basis for improvement. Starting from the conventional DPWMMIN approach, one cycle of the phase-a output voltage can be represented as (2). The waveforms of output voltages and the common-mode voltage is shown in Fig. 3, and there are unsmooth points between two sectors

$$u_{d,a}(\theta) = \begin{cases} U_{dc}M\sin(\theta), & 0 \le \theta < \frac{2\pi}{3} \\ U_{dc}M\sin\left(\theta - \frac{\pi}{3}\right), & \frac{2\pi}{3} \le \theta < \frac{4\pi}{3} \\ 0, & \frac{4\pi}{3} \le \theta < 2\pi \end{cases}. \tag{2}$$

Parameter $\theta = \omega_{ac}t = 2\pi f_{ac}t$ represents the angle corresponding to a full cycle of the time. Near the sector separation points, to address the issue of discontinuity, a smoothing function is superimposed near the unsmooth points to ensure that the slope of the output voltage changes continuously, thereby achieving smoothness. The derivative of $u_{d,a}(\theta)$ at point $\theta = 0$ is $U_{dc}M$, before this point, the derivative is zero. As the function can be approximated as straight lines within a small range. Assuming that the voltage is smoothed within a small range $-\beta \le \theta \le \beta$ and treated as

$$u(\theta) = \begin{cases} 0, & -\beta \le \theta < 0 \\ U_{dc}M \times \theta, & 0 \le \theta \le \beta \end{cases}. \tag{3}$$

To achieve a continuous transition of the derivative from 0 to $U_{dc}M$, the derivative can be gradually varied according to

$$d(\theta) = U_{dc}M\left(\frac{\theta}{2\beta} + \frac{1}{2}\right), \quad -\beta \le \theta \le \beta. \tag{4}$$

Integrate (4) and align the starting point with (3) to obtain the smoothed voltage, as shown in

$$u_s(\theta) = U_{dc}M\left(\frac{\theta^2}{4\beta} + \frac{\theta}{2} + \frac{\beta}{4}\right), \quad -\beta \le \theta \le \beta. \tag{5}$$

Subtracting $u(\theta)$ from the smoothed $u_s(\theta)$ and define the function value equals to zero when the angle θ *is* outside the range $-\beta \le \theta \le \beta$, then the smoothing function is obtained in

$$\delta(\theta) = \begin{cases} U_{dc}M\left(\frac{\theta^2}{4\beta} + \frac{\theta}{2} + \frac{\beta}{4}\right), & -\beta \le \theta < 0 \\ U_{dc}M\left(\frac{\theta^2}{4\beta} - \frac{\theta}{2} + \frac{\beta}{4}\right), & 0 \le \theta \le \beta \\ 0, & \text{other.} \end{cases} \tag{6}$$

The parameter β represents the angle range of the smoothing function's influence. A larger value of β yields a better smoothing effect, but it also reduces the angle range where the switches remain nonswitching. By shifting this function to coincide with each unsmooth points in the output voltage generated by the three-phase DPWMMIN in (2) and add them together, a three-phase smoothed DPWM modulation waveform can be obtained as

$$u_a(\theta) = u_{d,a}(\theta) + \delta(\theta) + \delta\left(\theta - \frac{2\pi}{3}\right) + \delta\left(\theta - \frac{4\pi}{3}\right) + \cdots. \tag{7}$$

Output voltages in phase-b and phase-c can be derived by lagging u_a by $2\pi/3$ and $4\pi/3$, and three output voltages can be obtained. The common-mode voltage is shown in

$$u_{cm}(\theta) = \left[u_a(\theta) + u_b(\theta) + u_c(\theta)\right]/3. \tag{8}$$

For β set at $\pi/18$, which corresponds to 10°, the resulting waveforms for the three-phase output line voltages and the common-mode voltage are illustrated in Fig. 4.

C. Modulation Method of Switching Frequency

Taking phase-a as an example, consider how to realize ZVS turn-ON of the transistors by using TCM. Based on the smoothed DPWM output voltage waveforms presented before, by controlling the switching frequency, the peak-to-peak value of the inductor current ripple can be tuned to be constant, and greater than twice the maximum value of the output current for that phase. This ensures that the inductor current reverses in every switching cycle throughout the entire output frequency period,

thereby achieving ZVS turn-ON for each half-bridge. To establish conditions for ZVS turn-ON of the devices during the dead-time, a simple solution is using deadtime to calculate [22], the inductor current ripple should at least be

$$\Delta I_{\mathrm{L}} \geq 2I_{\mathrm{a,max}} + \frac{Q_{\mathrm{HB}}}{t_{\mathrm{dead}}}. \tag{9}$$

The charge stored in half-bridge circuit $Q_{\mathrm{HB}} = 2Q_{\mathrm{oss}} + Q_{\mathrm{stray}}$ is composed of two parts, including the charge in the parasitic capacitors of the two switching devices Q_{oss} and the charge stored in the stray capacitors of the PCB and the output filter inductor. The dead-time of the half-bridge is denoted as t_{dead}. The inductor current should cross zero in order to completely discharge the half-bridge parasitic capacitors within the dead-time, thereby achieving ZVS turn-ON of the devices.

For the half-bridge inverter circuit, the relationship between the inductor current ripple and the switching frequency can be expressed as

$$\Delta I_{\mathrm{L}} = \frac{U_{\mathrm{out}}}{f_{\mathrm{s}} \cdot L}\left(1 - \frac{U_{\mathrm{out}}}{U_{\mathrm{in}}}\right). \tag{10}$$

Substituting the input and output voltages from the previously mentioned modulation method, a constant inductor current ripple can be achieved by modulating the switching frequency, as shown in

$$f_{\mathrm{s,a}}(t) = \frac{u_{\mathrm{a}}(t)}{\Delta I_{\mathrm{L}} \cdot L}\left(1 - \frac{u_{\mathrm{a}}(t)}{U_{\mathrm{dc}}}\right). \tag{11}$$

To prevent resonance in the output filter when the switching frequency is too low, and to avoid excessive switching losses when the frequency is too high, it is necessary to clamp the range of the switching frequency while maintaining a nearly constant inductor current ripple. The switching frequency can be calculated as

$$f_{\mathrm{sc,a}}(t) = \max\left(\min\left(\frac{u_{\mathrm{a}}(t)}{\Delta I_{\mathrm{L}} \cdot L}\left(1 - \frac{u_{\mathrm{a}}(t)}{U_{\mathrm{dc}}}\right), f_{\mathrm{s,max}}\right), f_{\mathrm{s,min}}\right). \tag{12}$$

In a similar manner, the switching frequencies for phase-b and phase-c can be calculated by lagging $f_{\mathrm{sc,a}}$ by $2\pi/3$ and $4\pi/3$. Based on the prototype parameters, the full-load frequency variation curve is computed and shown in Fig. 5 along with the simulated output inductor current. Fig. 5(a) illustrates the frequency variation curve and inductor current waveform under heavy load conditions, where the switching frequency is only constrained by the frequency low limit just before and after entering the no switching region. Fig. 5(b) illustrates the frequency variation curve under light load conditions, which is limited by both the high and low limits due to the very high switching frequency required to achieve a small current ripple under the same hardware conditions.

From the simulation result, the whole cycle of output frequency can be divided into three regions: ZVS region, low frequency switching region, and no switching region. Within one cycle, most of the switching actions meets the conditions for achieving ZVS turn-ON. The low frequency switching region before and after the no switching region may not achieve ZVS for the top transistor in a half-bridge, due to clamped switching frequency and insufficient inductor current ripple, but the time proportion and switching frequency is very low, which will not cause much switching loss. From the simulation result, only 1.67% of switching actions at 50 Hz may not realize ZVS turn-ON, for 400 Hz, the proportion is 1.61%, and the bottom switch in a half-bridge can always realize ZVS turn-ON. Additionally, there is approximately 1/3 of the period without any switching actions in the no switching region.

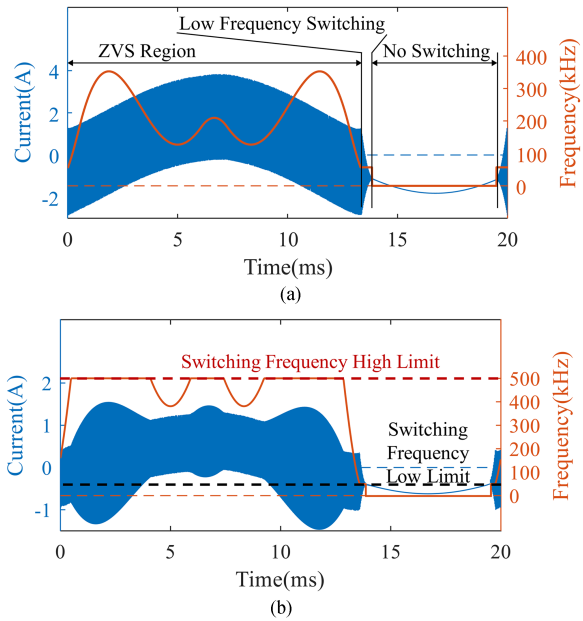

Fig. 5. Inductor current and switching frequency variation. (a) Heavy load condition. (b) Light load condition.

This modulation method can also achieve a wide range of ZVS for both inductive and capacitive output loads, only if the output apparent power does not exceed the rated power. The requirement for a phase current sensor with this modulation approach is optional, and there is no need for a high-bandwidth current sensor. If an output current sensor is not used, it is necessary to calculate the required inductor current ripple based on the maximum load.

This section proposes a smoothed DPWM technique and a corresponding TCM soft-switching method that can achieve ZVS for most of the switching actions. This improves efficiency and power density. Furthermore, the method can achieve soft-switching across wide load power and PF range with a simple hardware. Compared to existing control methods for three-phase two-level inverters, this approach offers certain advantages.

III. Input Current Ripple Reduction Method

When the input filter is not applied, the circuit exhibits substantial input current ripple. The high-frequency current ripple originates from the high-frequency switching actions of the three-phase half-bridges, while the low-frequency current ripple is due to the common-mode voltages of the three phases

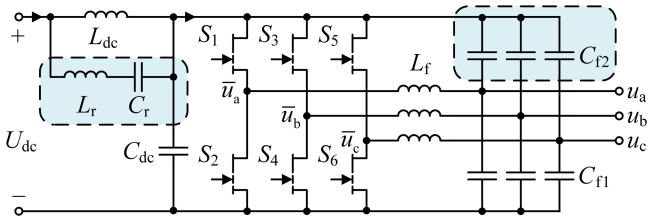

Fig. 6. Topology with modified input filter.

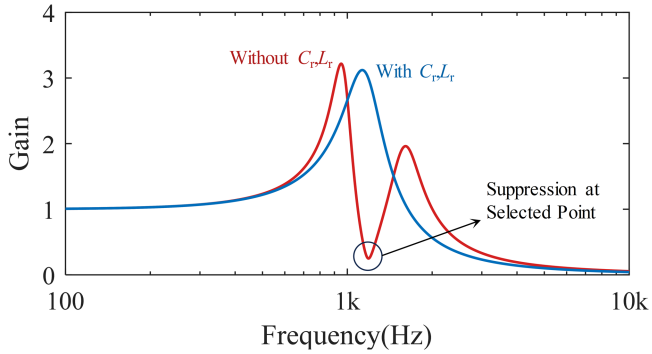

Fig. 7. Current gain of the input filter with and without added resonant circuit.

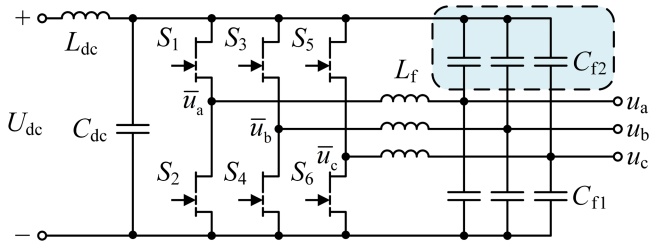

Fig. 8. Topology with modified output filter.

simultaneously charging and discharging the output filter capacitors, with a frequency three times of the output frequency. When the inverter operates at relative high output frequencies, the energy exchange between the output filter capacitors and the power source increases, leading to a significant rise in the low-frequency input current ripple, which may cause negative effects on the dc supply and additional filters is needed [24], [25]. A common method to attenuate the input current ripple is to add a *LC* filter at the input [26], which can significantly reduce the high-frequency components, but this is less effective for attenuating lower frequency ripples.

A. Input Filter Modification

When achieving effective suppression of low-frequency input current ripple by reducing the cutoff frequency of the *LC* filter circuit, the large dc bias on the inductor and capacitor leads to a substantial increase in static energy, which results in a notable increase in volume, affecting the power density.

To address the issue, a series *LC* branch can be paralleled with the input filtering inductor to create a series resonant circuit, as shown in Fig. 6. This resonant path can suppress low frequency current ripples at certain point, but also keep the capability of attenuating high frequency current ripple. Since only ac components exist on the added L_r and C_r, it is possible to select larger inductance and capacitance for better suppression performance without significantly increasing the static energy, thereby mitigating the increase in volume and negative impact on power density. The components L_{dc}, L_r, and C_r constitute a series resonant circuit, with the resonant frequency given by

$$f_r = \frac{1}{2\pi\sqrt{C_r(L_{dc}+L_r)}}. \tag{13}$$

To attenuate the input current ripple, set the resonant frequency of the circuit to three times the output frequency then calculates L_r and C_r.

When the input is powered by a voltage source and the output current i_{out} changes, the transfer function from the output current to the input current i_{in} can be expressed as

$$i_{in}(s) = \frac{C_r(L_{dc}+L_r)s^2+1}{C_{dc}C_rL_{dc}L_rs^4+(C_{dc}L_{dc}+C_r(L_{dc}+L_r))s^2+1} i_{out}(s). \tag{14}$$

The circuit has a pair of conjugate zeros at the resonance frequency f_r of the L_{dc}, L_r, C_r resonant loop, which is effective in attenuating the ripple of the input current at this frequency.

Considering the intrinsic resistance of the components, and based on the parameters of the experimental prototype, the gain to the frequency of the selected input filter before and after the addition of L_r and C_r at various frequencies is depicted in Fig. 7.

After added L_r and C_r, the input filter's effect at the original resonant frequency shifts from amplification to attenuation, thereby effectively suppressing the input current ripple at this frequency point, with minimal influence on the high-frequency filtering performance.

B. Output Filter Modification

The low-frequency input current ripple is generated by the energy exchange between the output filtering capacitor and the input. This energy exchange can be mitigated by splitting the output filtering capacitor into two parts connect separately to the dc positive and dc negative for energy cancelling, thereby reducing the input current ripple, as shown in Fig. 8.

As the output voltages of each phase varies, the energy stored in C_{f1} and C_{f2} changes inversely, thereby cancelling the total energy change caused by the output common-mode voltage, then lowering the input current ripple. Due to the bias of the common-mode voltage relative to the midpoint of the dc voltage, it is necessary to have unequal capacitances for C_{f1} and C_{f2} for energy cancelling, to achieve effective reduction of the input current ripple.

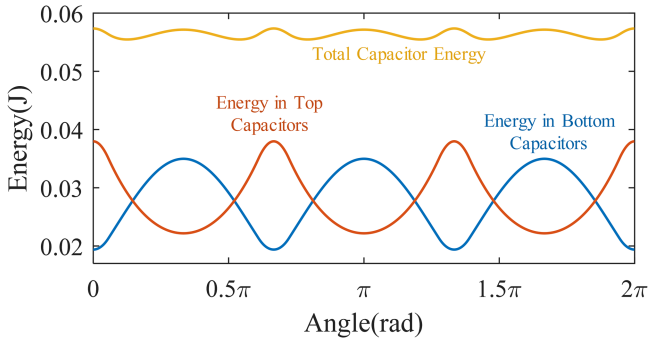

Fig. 9. Energy ripple cancellation of the output capacitors.

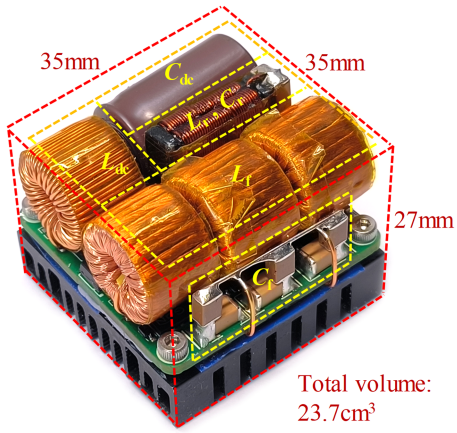

Fig. 10. Tested prototype.

The energy stored in one phase of the three-phase output filter capacitor is shown in

$$E_{\mathrm{a}}(\theta)=\frac{1}{2}C_{\mathrm{f1}}u_{\mathrm{a}}(\theta)^2+\frac{1}{2}C_{\mathrm{f1}}[U_{\mathrm{dc}}-u_{\mathrm{a}}(\theta)]^2. \tag{15}$$

The values of E_{b} and E_{c} can be derived from u_{b} and u_{c}, respectively. The total energy storage of the three phases is represented by

$$E_{\mathrm{tot}}(\theta)=E_{\mathrm{a}}(\theta)+E_{\mathrm{b}}(\theta)+E_{\mathrm{c}}(\theta). \tag{16}$$

Based on the Fourier series, the amplitude of the component at three times the output frequency can be expressed by

$$a_3=\left|\frac{1}{\pi}\int_0^{2\pi}E_{\mathrm{tot}}(\theta)\cos(3\theta)\,\mathrm{d}\theta\right|. \tag{17}$$

When the common-mode voltage changes from its minimum to maximum, the energy change in C_{f1} and C_{f2} should be equalized, resulting in the following relationship between C_{f1} and C_{f2}, as expressed in

$$\frac{C_{\mathrm{f2}}}{C_{\mathrm{f1}}}=\frac{U_{\mathrm{cm,max}}^2-U_{\mathrm{cm,min}}^2}{(\mathrm{U_{dc}}-U_{\mathrm{cm,min}})^2-(U_{\mathrm{dc}}-U_{\mathrm{cm,max}})^2}. \tag{18}$$

Allocate the capacitances of C_{f1} and C_{f2} proportionally and calculate the component a_3 in (17), which is three times the output frequency, is almost zero. In this case, the energy exchange caused by the output common-mode voltage mainly occurs between the top and bottom capacitors, rather than between the dc source and output capacitors. This approach can significantly reduce the low frequency input current ripple, which is at three times the output frequency, for the remaining energy ripple being very small, as shown in Fig. 9.

This section introduces two methods to attenuate the input current ripple caused by the common-mode voltage variation on the output capacitors. The first method involves paralleling an additional series *LC* to the inductor of the input *LC* filter to form a series resonant circuit, which suppresses the current ripple at a specific frequency. The effectiveness of this method depends on the output frequency of the inverter, making it suitable for application scenarios with fixed output frequency. The second method splits the output filtering capacitors, connecting to the positive rail and negative rail, allows the energy changes between the two sets of capacitors to cancel the energy ripple between each other when the output common-mode voltage varies. The effectiveness of this method depends on the output common-mode voltage, making it suitable for scenarios where the inverter output common-mode voltage changes not much.

TABLE II
SPECIFICATIONS OF TESTED PROTOTYPE

Parameters	Value
S_1-S_6	GS-065-011-1-L
L_{dc}	440 μH (High Flux)
C_{dc}	47 μF (EC) + 2.28 μF (MLCC)
L_{f}	62 μH (POCO-NPX)
C_{f1}	0.47 μF (MLCC)
C_{f2}	0.33 μF (MLCC)
L_{r}	1.3 mH (PC95)
C_{r}	10 μF (MLCC)
f_{s}	57 kHz - 353 kHz
$P_{\mathrm{o,max}}$	500 W
Controller	STM32G474CEU6
Power Density	245 W/inch³

IV. Experiment Result and Comparison

To validate the performance of the prototype, a test prototype shown in Fig. 10 was constructed, with a rated power of 500 W, an input voltage of 350 V, an output voltage of 220 V, the output frequency range is 50 to 400 Hz. The detailed specifications are presented in Table II.

The prototype employs GaN devices [27] from GaN Systems to achieve high efficiency and power density, with a full-load efficiency exceeding 98% and a power density of 245 W/inch³ (including heatsink and fan). The input and output filter inductors were self-made using toroidal magnetic cores. The input filtering inductor L_{dc} using two CH127060 [28] toroid magnetic cores, with its Fe-Ni material, it can withstand high dc bias current to achieve small volume. The coil is made by one single 0.55 mm diameter enameled wire to achieve low dc resistance, and the wire is tightly wounded around the magnetic core in 90 turns, which gives a 440 μH inductance at no dc bias. The output filtering inductor L_{f} using two NPX050060 [29] toroid

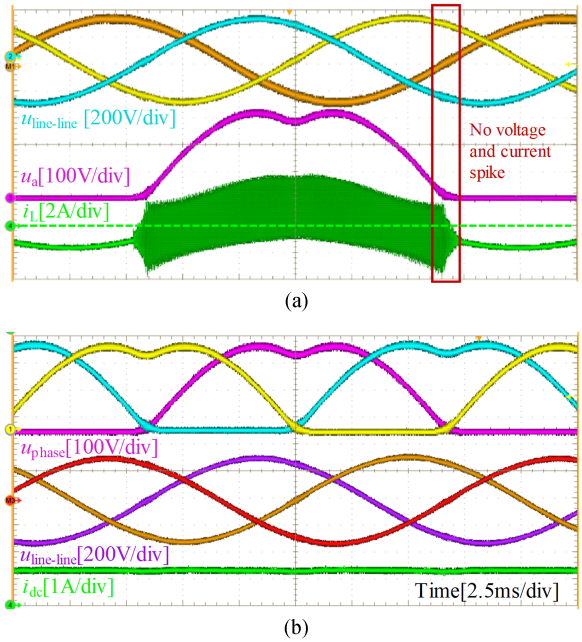

Fig. 11. Output line voltages, phase voltages, output inductor current, and DC input current under 490 W resistive load. (a) Output line-to line voltages $u_{\text{line–line}}$, phase-a voltage u_{a}, and inductor current i_{L}. (b) Output phase voltages u_{phase}, calculated line voltages $u_{\text{line–line}}$, and input DC current i_{dc}.

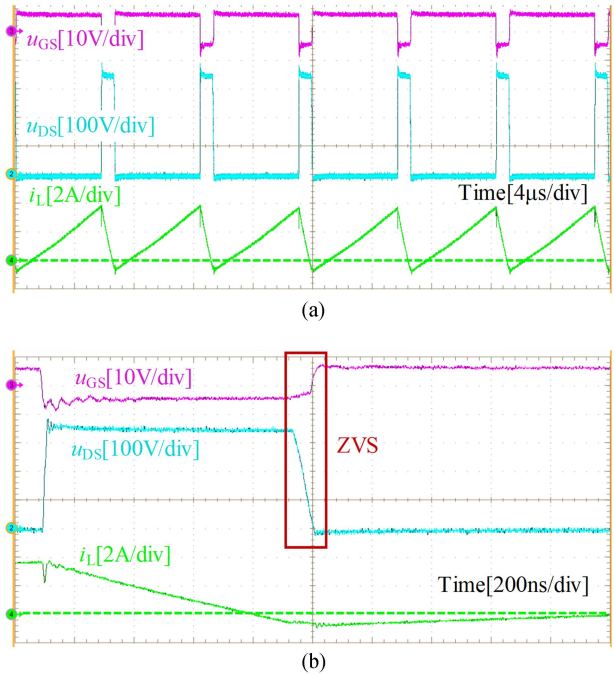

Fig. 12. Operating waveforms and ZVS waveforms of top switches. (a) u_{GS}, u_{DS} of the switch and inductor current i_{L}. (b) ZVS realization.

magnetic cores, three output inductors using six magnetic cores in total. The NPX magnetic material can achieve very low core losses similar to ferrite, and there no need to address the air-gap related losses. The coil is made by Litz wire, which is composed of 35 strands of 0.1 mm diameter enameled wire, lowering the resistance under high frequency, and the wire is tightly wounded around the magnetic core in 34 turns, which gives a 62 μH inductance at no dc bias. The resonant inductor L_{r} in the modified input filter using two 14 × 5 × 1.5 mm and two 3 × 5 × 1.5 mm ferrite pieces, whose materials are PC95, with the two longer ferrite is wounded in 45 turns separately, 90 turns in total, by single 0.3 mm diameter enameled wire with no air-gap, achieving a 1.3 mH inductance at no dc bias. For the MLCCs used in the input and output filters, several TDK capacitors [30] have been selected.

The control method of this prototype is using open-loop control by preprogrammed output voltage table and frequency variation table for fixed filter inductor current ripple calculated for the rated load, without a feed-back or feed-forward control.

A. *Operating Waveforms for the Main Circuit*

To test the prototype, adjust the input and output voltages to the rated values, with the output frequency set at 50 Hz, then connect a three-phase 490 W resistor load. Measure the voltage between each pair of the output lines, the output voltage of one phase, and the inductor current of that phase, as shown in Fig. 11(a). Each output phase voltages and the input current also have been measured at the same time, then calculates the line voltages, as shown in Fig. 11(b). As indicated in Fig. 11, the waveforms are corresponded with theory and simulation, they are smoothly transitioned between different DPWM sectors without any spike.

The u_{DS}, u_{GS} waveforms of the top switch in a half-bridge and the inductor current of that phase have been measured, as shown in Fig. 12(a). A detailed view near the switching instant is shown in Fig. 12(b). Due to the inversion of inductor current, the circuit is capable of discharge the parasitic capacitance nearly the entire cycle. It is evident from the figure that the rise of u_{GS} occurs after u_{DS} has already dropped to zero, proving that ZVS turn-ON of the transistor have been achieved.

When connected with low PF load, measure the output current of one phase, the inductor current, and the phase voltage relative to the neutral point of the three-phase load, which is denoted by $u_{\text{phase(load)}}$ in order to distinguishing between the phase voltage of the converter u_{phase}. The waveforms are shown in Fig. 13, where Fig. 13(a) shows the results with capacitive load, Fig. 13(b) shows the results with highly capacitive load, Fig. 13(c) shows the results with inductive load, Fig. 13(d) shows the results with the load of a three-phase induction motor in series with three additional inductors. It can be observed that the inductor current could invert with fixed current ripple under various inductive and capacitive loads, which indicates good ZVS performance for TCM. For the highly capacitive load, the load capacitor is much larger than the filter capacitor inside the converter, thus, much ripple current flows into the load capacitor, causing large current ripple in the output current. The THD of output voltages under resistive load, highly inductive load, and highly capacitive load has also been measured, using precision power scope PX8000 [31], and the result is shown in Table III. Although there is no feedback control in the prototype, the THD of output voltages under various load conditions is relatively low.

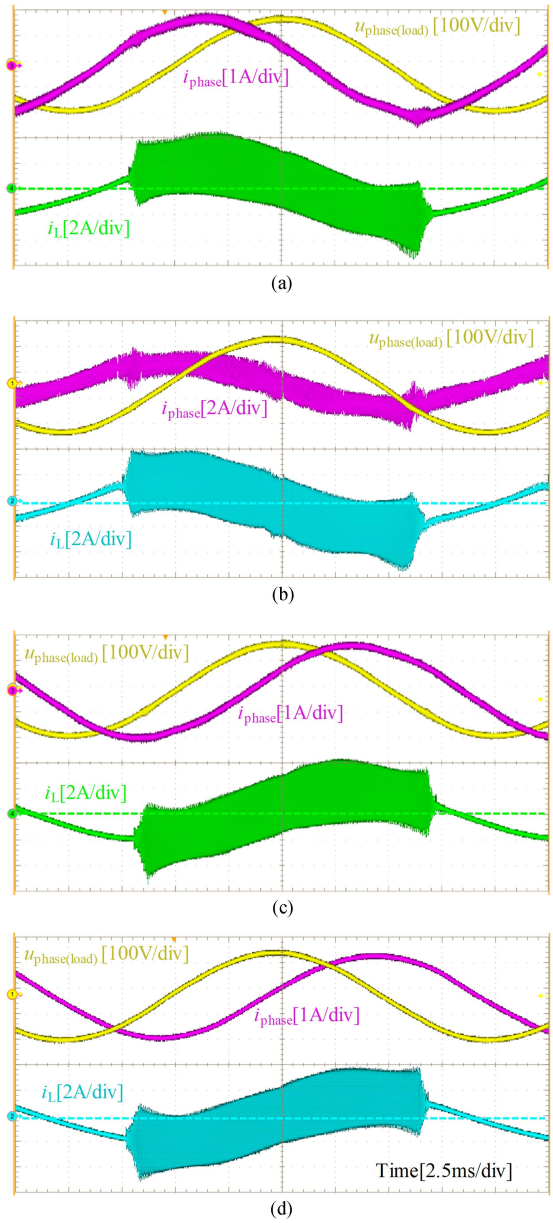

Fig. 13. Load phase voltage $u_{\mathrm{phase(load)}}$, output phase current i_{phase}, and output inductor current i_{L} under low PF load. (a) 222 W capacitive load, PF = 0.44. (b) 468 VA for fundamental power, capacitive load, PF = 0.03. (c) 284 W inductive load, PF = 0.51. (d) 440 VA inducive load, PF = 0.15.

TABLE III
VOLTAGE THD MEASUREMENTS OF TESTED PROTOTYPE

PF	Load Type	f_{ac}	S_o	vTHD
1	Resistive	50Hz	490.7VA	0.714%
1	Resistive	400Hz	490.3VA	1.004%
0.1539	Inductive	50Hz	439.9VA	1.069%
0.0313	Capacitive	50Hz	468.2VA$_{(Fundamental)}$	1.468%

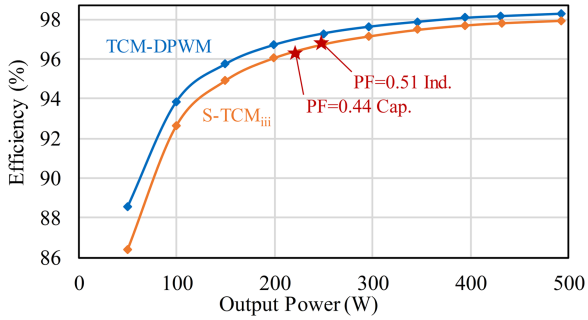

Fig. 14. Efficiency under different power.

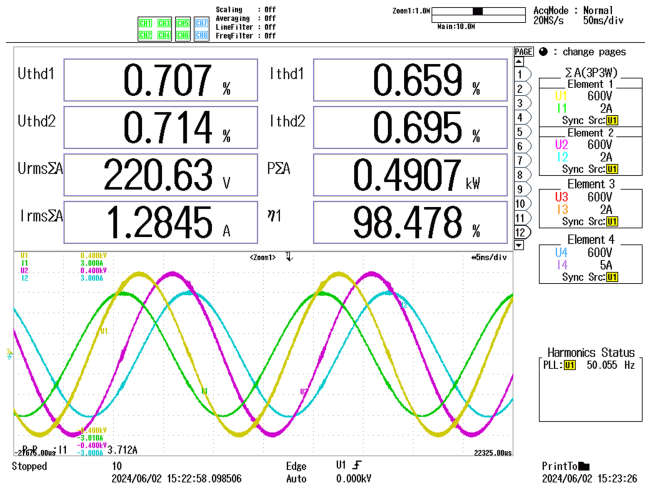

Fig. 15. Screen print of the power scope when achieving highest efficiency (fan removed for about 0.2% efficiency improvement).

B. Efficiency and Comparisons

The efficiency curve of the prototype is tested using precision power scope PX8000 [31] at rated load and compare it with the S-TCM$_{iii}$ method [10] under the same hardware, input and output voltage, output power, and inductor current ripple. The only difference is whether the tested prototype is running on S-TCM$_{iii}$ or TCM-DPWM, where the S-TCM method involved the injection of the third harmonic to achieve the same output voltage. When the output frequency is set to 50 Hz, the results of the efficiency test are shown in Fig. 14, the screen print of the power scope when achieving highest efficiency is shown in Fig. 15. The efficiency curves of the tested prototype under rated voltage full load at different output frequencies are shown in Fig. 16. Under various load conditions, the efficiency of the prototype is higher with the proposed TCM-DPWM control compared to the S-TCM$_{iii}$ control in this hardware setup.

C. Input Current Ripple

Calculate parameters for the two methods of reducing input current ripple at 400 Hz output frequency and 220 V output voltage, then start experiment at rated load measuring input current ripple ratio under different output frequencies and different output voltages, as shown in Figs. 17 and 18. The calculation method for input current ripple is the peak-to-peak value of input current divided by the average value of the input current. The tested cases include: The original prototype without L_{r}, C_{r}, C_{f2}, only L_{dc}, C_{dc}, C_{f1} installed; No C_{f2}, with L_{dc}, C_{dc}, C_{f1} and

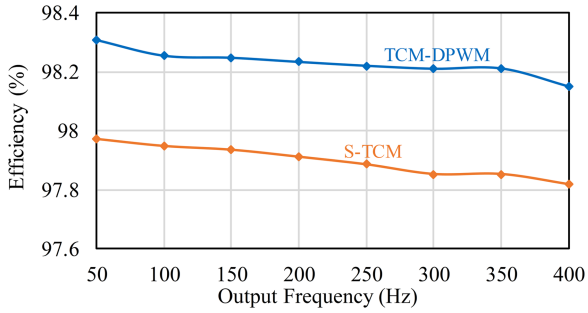

Fig. 16. Efficiency under different output frequency.

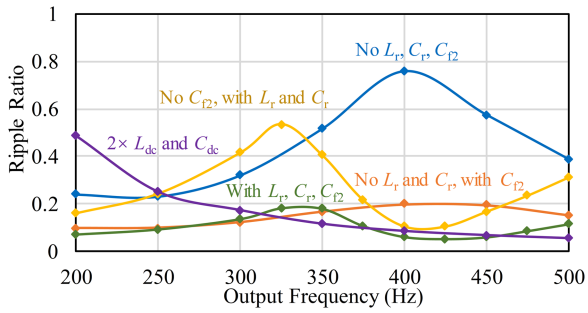

Fig. 17. Input current ripple under different output frequency.

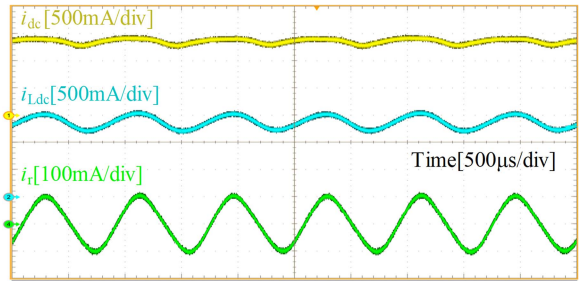

Fig. 18. Currents of the input filter current with series resonant circuit.

resonant components L_r and C_r on the prototype; No L_r and C_r, with L_{dc}, C_{dc}, C_{f1} and energy cancelling capacitor C_{f2} on the prototype; With the resonant components L_r and C_r and energy cancelling capacitor C_{f2}, together with L_{dc}, C_{dc}, C_{f1} on the prototype; No L_r, C_r, C_{f2}, with only L_{dc}, C_{dc}, C_{f1} on the prototype, but twice the inductance and capacitance of L_{dc} and C_{dc}. When only C_{f1} installed on the prototype, its capacitance equals to the sum of C_{f1} and C_{f2}.

For the test results under different output frequencies, the method by installing C_{f2} for energy ripple cancellation shows good performance. The method by adding series resonant can well suppress the current ripple at 400 Hz as good as double the inductance and the capacitance of the original filter L_{dc}, C_{dc} (the tested L_{dc}, C_{dc} in the doubled case is 910 μH and 94 μF), but the volume can shrink a lot, as shown in Fig. 19. The current waveforms of input filter using resonant components L_r and C_r for input current ripple suppression are shown in Fig. 20. However, as the frequency deviates from this point,

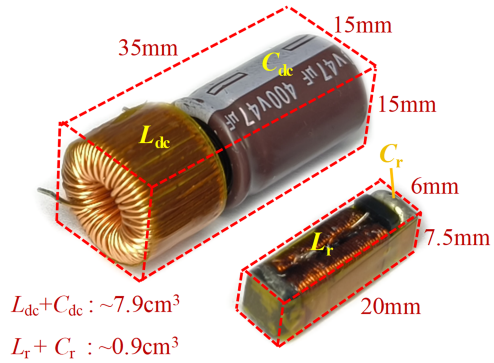

Fig. 19. Volume comparison for the input filter components.

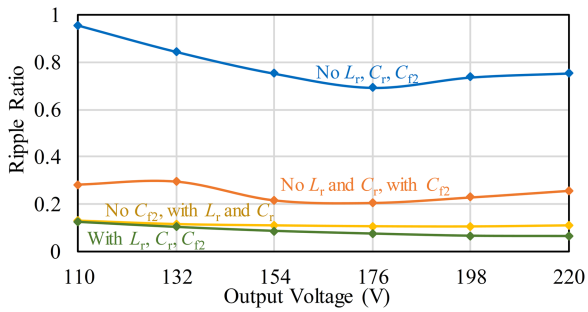

Fig. 20. Input current ripple under different output voltages.

the suppression effect deteriorates and reaches the worst case at about 325 Hz, but it still lower than the peak input current ripple at 400 Hz of the original *LC* filter, and similar to the effect at 200 Hz using twice the inductance and capacitance of L_{dc} and C_{dc}. When using both methods could make the current ripple lowest at 400 Hz, while maintaining good effect under wide output frequencies.

For the test result under different output voltages, it is observed that in the entire range of tested output voltages, all cases expect the original prototype effectively suppress the input current ripple, with the addition of L_r and C_r producing superior suppression performance, using both methods could make the current ripple a little lower. Theoretically, as the output voltage deviates away from the rated value, the ripple suppression effect by installing C_{f2} is expected to deteriorate, because the energy fluctuations of C_{f1} and C_{f2} can no longer cancel each other. However, the MLCCs used in the prototype have a prominent dc bias effect. When applied larger dc voltage on a MLCC, its ac capacitance would become smaller. As for the prototype, when the output voltage becomes smaller, the top capacitors C_{f2} becomes smaller and the bottom capacitors C_{f1} becomes larger, which have the same tendency of the capacitance ratio for energy cancelling and mitigates the sensitivity in response to the output voltage, resulting in a low input current ripple over a wide range of output voltage in the experiment. Considering the previously mentioned low input current over a wide output frequency range, the split capacitor method for energy cancelling and using two

methods together would be suitable for the inverter working as variable frequency drives for motors.

When realizing three-phase dc–ac inversion with the proposed method, if the inverter hardware is equipped with an output current sensor, the inductor current ripple can be modulated according to the load situation. This allows the converter to reduce inductor losses at light load and achieve soft switching across a wider load range.

V. Conclusion

This article presents a novel smoothed DPWM method and a ZVS soft-switching technique employing TCM for a three-phase two-level inverter with dc-link connected capacitors, making TCM fully feasible in DPWM applications for higher efficiency. Compared to conventional DPWM methods, the proposed approach eliminates the unsmooth points in the output voltages. Additionally, two methods are proposed to reduce the input current ripple generated by this modulation technique, when using together, the input current ripple can be well suppressed under various output frequencies and voltages. The presented methods have been validated by experiment, proving their effectiveness. The prototype developed using the proposed methods exhibits high efficiency, high power density, soft-switching over wide power, and PF range, simple to control, making it suitable for various applications such as microgrids and electric vehicles.

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