Reliability Estimation of Wired and Wireless Fast Electric Vehicle Charging Systems

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***Abstract*—Power electronic components in fast electric vehicle charging systems (FEVCSs) are invariably subjected to high electrical stresses, compromising the reliability of the entire charging system. Therefore, to ensure a robust and cost-effective operation, reliability estimation must be considered as an integral aspect of the design process of FEVCSs. This article presents a comprehensive reliability analysis strategy, which is applicable for both wired and wireless FEVCSs. The proposed strategy estimates the reliability at component to system-level and analyzes the impact of rest periods on FEVCS reliability. This is achieved through two modeling steps, consisting of an electro-thermal model and a reliability estimation model. Experimental results are presented to validate the proposed strategy. The findings, based on a case study of two 80 kW wired and wireless FEVCSs, are presented to demonstrate how the lifetime and reliability of semiconductor switches, capacitors, and overall chargers are influenced by the fast charging conditions. The study also shows how the introduction of rest periods to the charging schedule will substantially influence the reliability of both wired and wireless FEVCSs.**

***Index Terms*—Capacitors, lifetime, mission profiles, reliability, semiconductor switches, wired and wireless fast electric vehicle charging systems (FEVCSs).**

I. Introduction

As the global automotive industry continues its transition towards sustainable transportation, the demand for fast electric vehicle charging systems (FEVCSs) has grown in recent years. The FEVCSs are designed to offer accelerated charging speeds, addressing the time limitations associated with traditional electric vehicle (EV) charging methods. Consequently, FEVCSs encourage wider adoption of EVs, leading to reduced greenhouse gas emissions and air pollutants. Hence, the transition towards EVs fosters enhanced air quality and environmental sustainability. However, although these FEVCSs are time-efficient, fast charging involves delivering substantial power within a short period. Consequently, high charging power subjects the power electronic (PE) components within FEVCSs to significant temperature fluctuations. These fluctuations engender PE component failures, thus impacting the reliability of the overall charging system.

In a typical PE system, semiconductor switches and capacitors are identified as the components most susceptible to failure [1]. The failure mechanisms of these components can be classified into overstress and wear-out failures. Overstress failure arises when the system is operated beyond its safe operation boundaries, while wear-out failure results from cumulative damage. For semiconductor switches and capacitors, reliability is mainly associated with the wear-out failures and the adverse effects these failures impose on the normal operation of a PE circuit. The semiconductor switches in FEVCSs experience significant power losses due to the high charging power level. This causes an increase in the junction temperature (T_j) of the semiconductor switches. Inside the material layers of semiconductor switches, there are different thermal expansion coefficients. Consequently, when subjected to temperature fluctuations at high temperatures, micro-scale movements occur between the inside layers. These movements primarily affect soldering and wire bonding [2], [3], eventually leading to wear-out failure. One of the critical failure mechanisms identified in semiconductor switches is bond wire lift-off [4]. Due to excessive heat, bond wires have a tendency to detach or lift away from the internal structure of the component. This detachment disrupts the electrical connections, resulting in malfunction or complete failure of the component, compromising the overall performance of the system. In capacitors, high charging power increases the power losses and thereby elevates the hot-spot temperature (T_h). This leads to several failure mechanisms such as degradation of oxide film, capacitance reduction in cathode and anode foils, and deterioration of dielectric material [5], [6]. Hence, the semiconductor switches and capacitors in FEVCSs tend to experience accelerated wear-out, potentially necessitating multiple replacements over the lifespan of the charging system. Therefore, evaluating the reliability of semiconductor switches and capacitors in FEVCSs becomes crucial to assure reliable operation, and reduce the cost associated with the operation and maintenance.

The reliability analysis presented previously was applied predominantly in the design of PE converters in wind and photovoltaic (PV) power applications [7]. In [8], the reliability

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analysis of a solar inverter during reactive power injection has been examined. In this study, a mission profile-based lifetime estimation has been conducted, comparing the lifetime of the inverter under normal and periodic reactive power injection operations. An electrical transient analyzer program-based reliability analysis of a power converter system with wind energy interfacing has been presented in [9]. In this study, machine learning regression techniques have been utilized for reliability prediction. In [10], a robust artificial neural network model has been proposed for predicting the accumulated damage per cycle in PV systems. A thermal model of a dc/ac inverter coupled with a Monte Carlo simulation has been used to estimate unreliability and remaining operational lifetime. The reliability of PE converters in EVs has been discussed in several studies. In [11], a flexible experimental setup for investigating a system-level lifetime analysis approach for EVs has been presented. A comparative analysis of power loss estimation models based on two standard driving cycles for EV converters has been conducted in [12]. A considerable impact of driving cycles on the lifetime of insulated-gate bipolar transistors (IGBTs) used in EVs has been highlighted in [13]. In this study, the lifetime of three different power modules within an EV converter has been investigated across two distinct driving cycles. A multistate Markov analysis approach for assessing the reliability of an interleaved dc/dc converter in EVs has been introduced in [14]. An MILHDBK-217F-based lifetime analysis technique has been used and the degradation progression of the converter over time has been presented. In [15], the reliability of a permanent magnet synchronous motor drive processor for EV utility has been analyzed. A thermal analysis followed by a reliability study of a motor controller and processor under different temperature stress conditions has been conducted. However, according to the literature, the reliability of FEVCSs has not been investigated to date. The reliability of FEVCSs is important as these systems enable faster charging times for EVs, encouraging more people to switch from conventional internal combustion engine vehicles to EVs. Hence, in order to create more reliable FEVCSs, research is needed in this area to identify the potential failure modes and understand the factors that accelerate the degradation of components under fast charging conditions.

This study fulfills this need by conducting a comprehensive reliability analysis of FEVCSs, adding novelty to the existing literature in terms of three aspects. The primary objective of the study is to investigate the impact of fast charging on the lifetime and reliability of critical components in FEVCSs at the component, converter, and system-levels. Hence, a reliability analysis strategy consists of an electro-thermal model and a reliability estimation model is first proposed for FEVCSs. The focus of the proposed strategy, together with laboratory experimental validation is to analyze the reliability of semiconductor switches and capacitors, thereby assessing the reliability of the overall FEVCS. Secondly, using the proposed strategy, a comparative reliability analysis is carried out based on a case study of two different FEVCSs, comprising a typical three-phase 80 kW wired and a wireless FEVCS. This enables a comparison of how reliability differs in each system when delivering the same fast charging power. Thirdly, the reliability estimation model is extended to analyze the impact of rest periods on the reliability of FEVCSs, aiding in planning charging schedules to achieve a desired level of reliability. All these three aspects are especially relevant when operating under fast charging conditions, thereby adding significant novelty to the existing literature.

The rest of this article is organized as follows. An electro-thermal model, which derives stress parameters that impact the reliability of the semiconductor switches and capacitors, is presented in Section II. A reliability estimation model is described in Section III, which estimates the reliability at component to system-level and analyzes the impact of rest periods on FEVCS reliability. A description of the verification of the proposed strategy is presented in Section IV, together with an experimental analysis. Using the proposed strategy, the reliability of a case study of wired and wireless FEVCSs is investigated in Section V. In Section VI, the effect of integrating rest periods on FEVCS reliability is analyzed. Finally, Section VII concludes this article.

II. Electro-Thermal Model

Electro-thermal model is the initial stage of the proposed reliability analysis strategy, as depicted in Fig. 1. The electro-thermal model considers the mission profile as its input and derives the stress parameters required for the subsequent reliability estimation model. Therefore, it is essential to establish a mission profile, representing the factors that mainly influence the lifetime and reliability of PE components in FEVCSs. Due to the operating conditions with high charging power, PE components in FEVCSs are exposed to high electrical and thermal stresses, leading to the wear-out of these components. The operating conditions of the FEVCSs are directly associated with the charging profile, and therefore, it is considered as the mission profile. Amongst various EV charging strategies, multistage constant current (MSCC) charging is the most preferable strategy for fast charging [16]. Hence, an MSCC charging profile is considered the mission profile in this study. The proposed approach in [17] and [18] is used to design the optimal current pattern in the MSCC charging profile, which gives the minimum charging time. The MSCC charging profile is designed with five current stages. The battery in the FEVCSs, described in Section II-A, is charged according to the currents (I) of each stage until the battery voltage reaches its highest allowed value.

A. Fast EV Charging Systems

FEVCSs offer rapidly recharging the battery of an EV with higher power levels compared to slow charging systems. As per the description in the Society of Automotive Engineers J1772 standard, EV charging can be categorized through different power levels, each offering varying charging speeds. AC Level 1 is defined as slow charging with a charging power of less than 2 kW. AC Level 2 uses power levels ranging from 5 to 19.2 kW and is commonly located at residential and some public charging locations. DC fast charging, also defined as DC Level 1 and DC Level 2, offers significantly higher power levels from 50 to 350 kW and beyond. DC fast charging provides power to the vehicle as dc, while AC Level 1 and AC Level 2 typically employ onboard charging equipment in the EV to transform ac power into dc. DC fast charging stations are usually found along

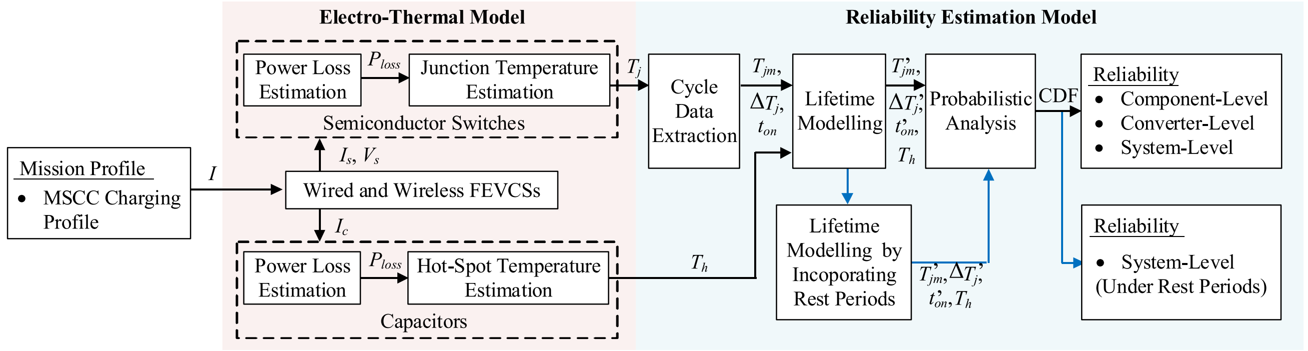

Fig. 1. Reliability analysis strategy.

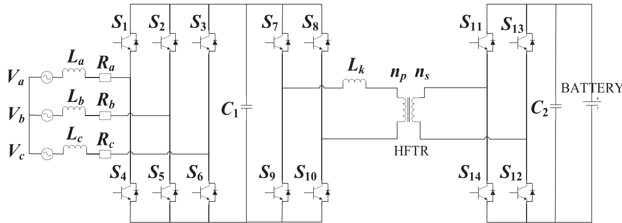

Fig. 2. Typical three-phase wired FEVCS.

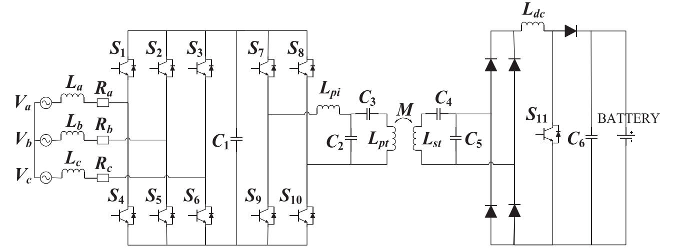

Fig. 3. Typical three-phase wireless FEVCS.

highways, major routes, and urban areas, enabling EV drivers to quickly charge their battery. However, the high-power levels used in DC fast chargers put stress on various components, including PE components, batteries, connectors, and cooling systems. Hence, these components are vulnerable to failure more easily leading to charging interruptions and therefore, it is important to analyze the reliability issues in FEVCSs. FEVCSs can be either wired or wireless, and in this study, reliability analysis of two fast EV charging configurations, a typical three-phase 80 kW wired and wireless FEVCSs are considered.

A typical wired FEVCS is illustrated in Fig. 2, comprising two interconnected ac/dc and dc/dc converters. The ac/dc converter is fed by a three-phase, 400 V ac input source and maintains 600 V dc at its output. The dc/dc converter is implemented using a phase-shift controlled dual active bridge, operating at 20 kHz. The dc/dc converter regulates the necessary power flow to charge the battery while incorporating galvanic isolation through a high-frequency transformer [19], [20]. The reference currents in the current controller of the dc/dc converter are obtained according to the current levels at different stages of the MSCC charging profile.

Fig. 3 shows a typical wireless FEVCS which consists of a three-phase ac/dc low-frequency grid-side converter, a dc/ac high-frequency converter on the primary side, and an ac/dc converter on the secondary side. The three-phase ac/dc converter is connected to a 400 V ac input source and regulates 600 V dc-link voltage at its output. The dc/ac converter on the primary side is controlled through phase-shift modulation at a frequency of 85 kHz, to achieve a constant ac current in the primary winding. Inductive power transfer technology is utilized to achieve wireless transfer of power from the primary side to the secondary side. In this case, the primary winding is magnetically coupled through a mutual inductance (M) to the secondary winding, and the windings are separated by an air gap. The primary and secondary sides are connected to a resonant network to provide var compensation as well as to achieve efficient and maximum power delivery. The ac/dc converter on the secondary side regulates the current required to charge the battery. The current supplied to the battery is controlled by the duty cycle of switch $S_{11,}$ which is determined according to the current at each stage of the MSCC charging profile [21], [22]. During the charging period of the battery in both wired and wireless FEVCSs, current (I_s) and voltage (V_s) through the semiconductor switches and current (I_c) through the capacitors are measured, which are required as crucial data for the stress parameter estimation of each component.

B. Stress Parameter Estimation

As per field observations, various components, including semiconductor switches, capacitors, gate drivers, and cooling systems, can cause malfunctions in PE systems [1], [23]. The failure mechanism of each component can have a reciprocal impact on the reliability of other components in the system, leading to a highly complicated analysis. In this study, the wear-out failure mechanisms of semiconductor switches and capacitors, which are recognized as the reliability critical components [1], are focused on the reliability estimation.

One of the key factors that can lead to the failure of semiconductor switches is an elevated T_j. The high T_j occurs during operation, especially under demanding conditions such as high currents in FEVCSs. To address this issue, the mission profile

must be accurately translated into T_j fluctuations in order to have a comprehensive understanding of the thermal behavior of the semiconductor switch. Hence, during the charging process, I_s and V_s are measured, and the corresponding power losses are obtained using look-up table (LUT) method on PLECS simulation environment in MATLAB. This enables the initiation of the power losses, conduction losses (P_{cond}), and switching losses (P_{sw}) of the semiconductor switch for specific operating conditions in advance. The LUT can then be used to estimate the P_{cond} and P_{sw} for desired operating conditions. The T_j fluctuations caused by the power losses (P_{loss}) can then be determined through the thermal model of semiconductor switches which employs a Foster model. The parameters for this model are derived using a fitting algorithm within PLECS, which utilizes thermal impedance curves typically found in datasheets.

The high ripple currents (I_c) through capacitors in FEVCSs contribute to high P_{loss}. Due to this P_{loss}, internal heating of the capacitor can occur, which leads to an increase in the T_h. The high T_h is one of the primary causes of failure mechanisms in capacitors [5], [24]. In order to address this issue, the T_h must be carefully determined according to the operating conditions represented by the mission profile. Since the electrical and thermal characteristics of capacitors are interdependent, it is essential to calculate P_{loss} at specific frequencies and thereby calculate the T_h. To achieve this, the fast Fourier transform (FFT) can be applied to the I_c of the capacitor [5], [25] and the total P_{loss} can be calculated as

$$P_{loss} = \sum_{h=1}^{N} I_{ch}^2 \times R_{ESR}(f_h) \tag{1}$$

where N represents the number of points in the time series of the I_c, I_{ch} is the harmonic amplitude of the I_c, and $R_{ESR}(f_h)$ is the R_{ESR} at the relevant harmonic frequency, which can be obtained from the capacitor's datasheet. By incorporating the obtained P_{loss}, the steady-state T_h of the capacitor can be determined as [5], [25]

$$T_h = P_{loss} \times R_{th} + T_a \tag{2}$$

where R_{th} is the thermal resistance of the capacitor, which can be found in the datasheet, and T_a is the ambient temperature. T_h estimation typically involves steady-state analyses for assessing long-term thermal performance and reliability [6], [24]. Hence, transient effects captured by thermal capacitance are considered negligible compared to R_{th} in T_h estimation.

The stress parameters, T_j and T_h are considered as the main input parameters in the lifetime modeling step in the reliability estimation model. The lifetime model of semiconductor switches requires cycling data of T_j, and therefore, a cycle counting technique such as Rainflow cycle counting is utilized to distinguish thermal cycle data within the T_j profile [26]. Hence, certain details, such as mean T_j (T_{jm}), temperature cycle amplitude (ΔT_j), and cycle duration (t_{on}) are extracted from the T_j profile, which can then be directly applied to the lifetime model of the semiconductor switches.

TABLE I
LIFETIME MODEL PARAMETERS OF SEMICONDUCTOR SWITCHES [27]

Parameter	Value	Parameter	Value
A	3.4368×10^{14}	C	1.434
α	-4.923	γ	-1.208
ar	0.31	f_d	0.6204
β_1	-9.012×10^{-3}	E_a	0.06606 eV
β_0	1.942	k_B	8.6173324×10^{-5} eV/K

III. Reliability Estimation Model

In this section, a detailed description of the steps that translate the stress profiles into the reliability of FEVCSs is presented. Initially, the lifetime modeling is incorporated to obtain the lifetime of semiconductor switches and capacitors. The model is further extended to analyze the lifetime under different rest periods. Moreover, a probabilistic analysis is presented, which estimates the reliability of FEVCSs.

A. Lifetime Modeling

Based on a specific lifetime model, number of cycles to failure (N_f) or time until the failure (L_f) of a component can be predicted, and the lifetime of the component can be estimated. In this study, a standard lifetime model based on the Coffin-Manson law is considered to analyze the N_f of semiconductor switches. The standard lifetime model, which describes that the N_f is proportional to the ΔT_j [27], is given as

$$N_f = A \times (\Delta T_j)^{\alpha} \times (ar)^{\beta_1 \Delta T_j + \beta_0} \times \left[\frac{C + (t_{on})^{\gamma}}{C+1}\right] \times \exp\left(\frac{E_a}{k_b \times T_{jm}}\right) \times f_d \tag{3}$$

where the inputs to this lifetime model are the T_{jm}, ΔT_j, and t_{on}. The remaining constant parameters are listed in Table I [27]. Typically, the lifetime data of semiconductor switches are described as lifetime consumption (LC). The LC indicates the amount of lifetime of the component that has been depleted during its operation. Using the Palmgren-Miner's rule, the LC of semiconductor switch (LC_S) can be determined by taking the summation of the LC for each cycle as [26]

$$LC_S = \sum_i \frac{n_i}{N_{fi}} \tag{4}$$

where n_i is the number of cycles at a specific operating condition and N_{fi} is the number of cycles to failure at that particular operating condition.

The lifetime of capacitors is mainly affected by various parameters such as the T_h, the operating voltage (V_{op}) and humidity. In particular, when the V_{op} falls below the rated voltage (V_{rated}), its impact on the reliability of the capacitor can be disregarded. Hence, the impact of high T_h, due to high charging currents, on the lifetime of capacitors is focused on this study. The L_f of capacitors is obtained using a standard lifetime model

described as [5]

$$L_f = L_m \times \left(\frac{V_{rated}}{V_{op}}\right)^8 \times 2^{\left(\frac{T_m - T_h}{10}\right)} \quad (5)$$

where L_m and T_m represent the rated lifetime and the rated operating temperature of the capacitor, respectively. According to the Palmgren-Miner's rule [26], the LC of capacitor (LC_C) can be determined as

$$LC_C = \sum_i \frac{l_i}{L_{fi}} \quad (6)$$

where l_i is the operating time under a particular operating condition and L_{fi} is the time until the failure of the capacitor under that specific operating condition. By employing Palmgren-Minor's rule [28], it is assumed that the damage from each power cycle is linearly accumulated, which is a validated and widely accepted approach for lifetime estimation in reliability engineering [29], [30].

Once the LC accumulates to unity after multiple operation cycles, it is considered that the component has reached its end of life, and its lifetime can be predicted. Consequently, the LC per year can be calculated as

$$LC_{Sy} = \frac{LC_S}{t_c} \times t_y,\ LC_{Cy} = \frac{LC_C}{t_c} \times t_y \quad (7)$$

where LC_{Sy} and LC_{Cy} are LC per year of semiconductor switches and capacitors, respectively. t_c and t_y represent the time per one operation cycle and time per year in seconds, respectively. Hence, the lifetime can be obtained as

$$LT_S = \frac{1}{LC_{Sy}},\ LT_C = \frac{1}{LC_{Cy}} \quad (8)$$

where LT_S and LT_C are the lifetime of semiconductor switches and capacitors, respectively.

B. Lifetime Modeling by Incorporating Rest Periods

In order to analyze the impact of different rest periods on the reliability of FEVCSs, the rest periods were introduced with different time durations (t_r) after each charging period. Hence, the LC per year which incorporates rest periods can be calculated as

$$LC_{Syr} = \frac{LC_S}{(t_c + t_r)} \times t_y,\ LC_{Cyr} = \frac{LC_C}{(t_c + t_r)} \times t_y \quad (9)$$

where LC_{Syr} and LC_{Cyr} are the LC per year of semiconductor switches and capacitors under different rest periods, respectively. Thus, the lifetime under different rest periods can be obtained as

$$LT_{Sr} = \frac{1}{LC_{Syr}},\ LT_{Cr} = \frac{1}{LC_{Cyr}} \quad (10)$$

where LT_{Sr} and LT_{Cr} are the lifetime of semiconductor switches and capacitors when operating under rest periods, respectively.

C. Probabilistic Analysis

The predictions obtained for the lifetime of semiconductor switches and capacitors are based on the assumption that all components will fail at the same rate. This is not true in real-world conditions due to the variations in stress and lifetime model parameters, and production processes. Therefore, it is important to present the lifetime predictions as a statistical value rather than a fixed value. This can be achieved through Monte Carlo analysis [31], which allows for random variations in the parameters affecting lifetime and determines the lifetime with a significant number of samples. The results of this analysis through many samples can be used to find a more accurate value for the lifetime of the components. In this method, the parameters in the lifetime models outlined in (3) and (5) are modeled using a normal distribution function that has a defined range of variation. Random samples are then selected from each parameter distribution to determine the lifetime of components. This process results in a set of lifetime predictions, which follows a certain lifetime distribution. Typically, the lifetime data of semiconductor switches and capacitors follows a Weibull distribution [31], which can be described by its probability distribution function (PDF) known as lifetime distribution $f(x)$.

Furthermore, by integrating the $f(x)$ over the operating period, cumulative distribution function known as the unreliability function $F(x)$ of the components can be determined. Using the $F(x)$, B_x lifetime, which represents the time when $x\%$ of the components in the population have failed can be obtained [32]. Usually, in critical applications, B_1 lifetime is considered as the reliability matrix among different B_x lifetime values. Hence, in this study, B_{15}, B_5, and B_1 lifetime of the semiconductor switches and capacitors are studied to gain knowledge on lifetime among different B_x values, and B_1 lifetime is considered as the reliability.

When designing PE converters, it is common for multiple semiconductor switches and capacitors to be included, each having its unique $F(x)$. Thus, the reliability block diagram, which represents the interconnections between the reliability of each component is employed to evaluate the overall reliability of the converter [1]. If the converter consists of n components, and it will not function if any of them fails, the converter-level unreliability function, $F_{con}(x)$, can be described as

$$F_{con}(x) = 1 - \prod_{k=1}^{n} (1 - F_k(x)) \quad (11)$$

where $F_k(x)$ is the unreliability function of the kth component. Once the $F_{\text{con}}(x)$ is determined, the reliability of the PE converter can be predicted. In order to analyze the reliability of FEVCSs at system-level, $F_{con}(x)$ presented in (11) is further modified and the system-level unreliability function $F_{sys}(x)$ can be expressed as

$$F_{sys}(x) = 1 - \prod_{k=1}^{n} (1 - F_{con,k}(x)) \quad (12)$$

where $F_{con,k}(x)$ is the unreliability function of the kth converter in a system with n converters. Using the $F_{sys}(x)$, the reliability of the entire FEVCS can be predicted.

Fig. 4. Schematic diagram of the power cycling test setup.

IV. Experimental Verification

The stress parameters, T_j and T_h are the crucial factors that impact the reliability of semiconductor switches and capacitors. Hence, the accuracy of the translation between the mission profile and the stress parameters is important. In order to verify the accuracy of the T_j estimation method described in Section II-B, an experiment was carried out using a standard 19-inch industrial rack for power cycling test at AAU Energy, Aalborg University, and results were compared with a simulation. A detailed schematic diagram of the power cycling test setup is shown in Fig. 4. In this setup, all the parameters related to the testing conditions and the testing strategy were customized through a National Instruments (NI) CompactRIO system together with the LabVIEW program. This system is responsible for data logging and real-time communication with the user. In the main circuit, a device under test (DUT) converter with four semiconductor switches, which are connected in two half bridges was considered. The S_t was considered as the test semiconductor switch, which is named DUT. An Itech IT6018C-1500-40 dc power supply was connected to provide power to the main circuit.

In order to derive the T_j of DUT, dc power cycling method, which is proposed in many reliability standards [33], [34], was used. The dc power cycling test was conducted with the configuration of 2 s on-time/2 s off-time under 30 A injection current, and the current was commutating between the two half bridges. Correspondingly, the DUT was heated up and cooled down in 2 s intervals during the entire process, and the T_j was monitored during this period. The applied control signals are shown in Fig. 4. The control signal was generated through a host PC running the LabVIEW program and an NI 9401 module in NI CompactRIO is used to provide the control signal. An NI 9202 module is used to log the T_j of DUT, measured through an optical fiber cable, which is connected to a fiber optic signal conditioner (FOSC) by OpSens. All the communications among the equipment are routed through a multichannel Ethernet switch. To ensure a constant baseplate temperature during the experiment, the DUT is placed on a cooling plate, which is connected to a Julabo Presto A40 chiller. The experimental power cycling test setup including the standard 19-inch industrial rack and the main circuit is shown in Fig 5. The arrangement of equipment

Fig. 5. Experimental power cycling test setup.

Fig. 6. Comparison of the T_j of S_t between the simulation and experiment results.

is optimized to ensure optimal accessibility to the DUT, which is positioned on a pull-out tray along with the DUT converter. Together with the host PC, an auxiliary (AUX) power supply for gate drivers is placed on the level next to the pull-out tray. An uninterruptible power supply (UPS) ensures the continued operation of the test circuit in the event of power outages and allows sufficient time for saving the data.

The obtained T_j measurements are compared with the simulation results as shown in Fig. 6. The results indicate that the simulation results are in well agreement with the measurements, verifying the accuracy of the T_j estimation method. It should be noted that, because of the power limitations in the laboratory setup, the semiconductor switch, FP50R12KT4 was considered as the DUT during the experiment, and it was not identical to the semiconductor switches used in the analysis. Hence, the

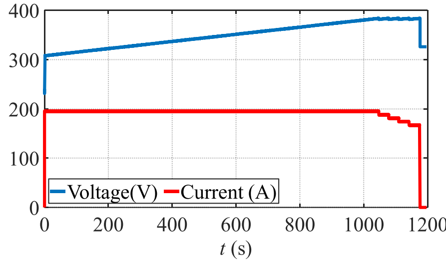

Fig. 7. MSCC charging profile.

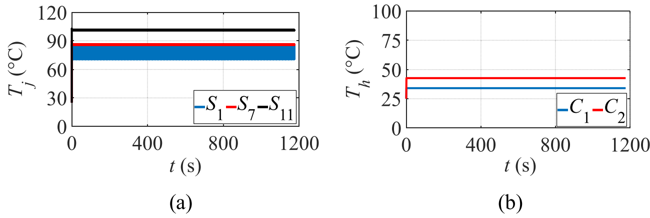

Fig. 8. Stress parameters: (a) T_j of semiconductor switches and (b) T_h of capacitors in the wired FEVCS.

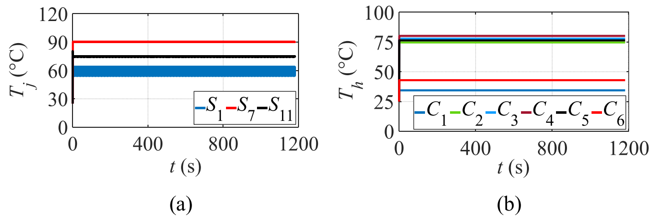

Fig. 9. Stress parameters: (a) T_j of semiconductor switches and (b) T_h of capacitors in the wireless FEVCS.

obtained experimental results were compared with a simulation following the same method described in Section II-B, which is identical to the system conditions in the laboratory. This analysis was aimed to verify the accuracy of the method of mission profile translation into T_j fluctuations, without the need for validating T_j profiles for each switch under various conditions, thus minimizing complexity and time.

The accuracy of the electro-thermal model for capacitors can be verified as it is based on established techniques and standard equations. Initially, the FFT is applied to I_c and P_{loss} is calculated. By incorporating the obtained P_{loss}, T_h of capacitors are determined using a standard and widely accepted method [5], [6], [24], [25]. Furthermore, the accuracy of the reliability estimation model can be verified as the calculation of component lifetime is based on empirical lifetime models, which are derived through experimental analysis. In order to estimate the reliability a probabilistic analysis is carried out which follows the standard Monte Carlo analysis. Hence, the reliability estimation strategy can be validated, and the strategy is used further to estimate the reliability of FEVCSs.

V. Reliability Estimation of FEVCSs

In this study, a case study of two configurations, 80 kW wired and wireless FEVCSs, shown in Figs. 2 and 3, were considered, and the reliability was estimated using the strategy detailed in

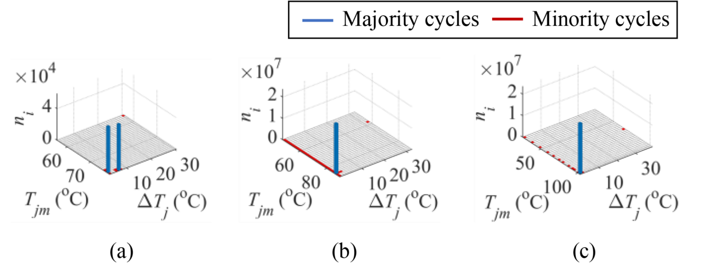

Fig. 10. Rainflow matrixes for T_j of: (a) S_1, (b) S_7, and (c) S_{11} in the wired FEVCS.

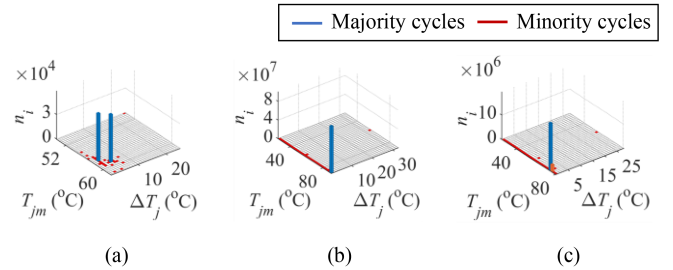

Fig. 11. Rainflow matrixes for T_j of: (a) S_1, (b) S_7, and (c) S_{11} in the wireless FEVCS.

Sections II and III. The analysis was focused on the reliability evaluation of critical components, semiconductor switches, and capacitors, at the component, converter, and system-levels. Hence, the stress parameters of the semiconductor switches and capacitors in both wired and wireless FEVCSs, illustrated in Figs. 2 and 3, were initially studied by applying an MSCC charging profile, as depicted in Fig. 7, across a 20 min charging period. The determination of the five charging current stages in the MSCC charging profile and the overall charging duration were accomplished as explained in Section II. The battery was charged using the specified current values corresponding to each stage until the battery voltage reached its maximum allowable limit of 384 V. During this process the I_s, V_s, and I_c through semiconductor switches and capacitors were measured and considered to estimate the stress parameters.

A. Stress Parameters

The stress parameters, T_j and T_h of the semiconductor switches and capacitors were obtained using the method described in Section II-B, and the results are presented in Figs. 8 and 9 for wired and wireless FEVCSs, respectively. Fig. 8(a) depicts the T_j of a single semiconductor switch in the ac/dc converter (S_1) and the primary and secondary side of dc/dc converter (S_7 and S_{11}) of the wired FEVCS shown in Fig. 2. In this analysis, IGBT switches from Semikron Danfoss were selected for S_1, S_7, and S_{11} in both wired and wireless FEVCSs. These switches are specially designed for FEVCSs in industrial applications [35]. The IGBT switch SKM150GB12T4 was selected for the S_1 and S_7, and SKM300GB12T4 was selected for the S_{11}, depending on the operating conditions. The current through the semiconductor switches and thereby the power losses increase in the order of S_1, S_7, and S_{11}. Hence, the results indicate that the T_j increases in the same order of S_1, S_7, and S_{11}. As depicted in Fig. 8(a), T_j reaches

TABLE II
RAINFLOW MATRIX DATA

Parameter	Wired FEVCS			Wireless FEVCS			Units
	S_1	S_7	S_{11}	S_1	S_7	S_{11}	
T_{jm}	77.3	86.1	101.4	58.4	90.2	74.7	°C
ΔT_j	2-6	1	1	2-5	1	1	°C

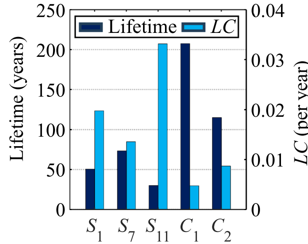

Fig. 12. *LC* and lifetime of semiconductor switches and capacitors in the wired FEVCS.

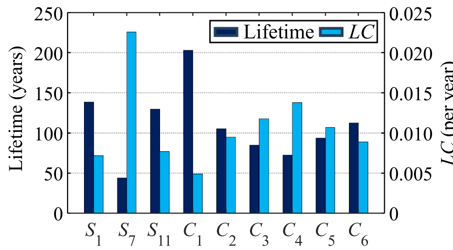

Fig. 13. *LC* and lifetime of semiconductor switches and capacitors in the wireless FEVCS.

its mean value at 77.3 °C in S_1, 86.1 °C in S_7, and 101.4 °C in S_{11}, while its minimum value is the ambient temperature of 25 °C in all the switches. Because of the advantage of long lifetime, a dc film capacitor, MKP1848C74060JY5 was selected for C_1 and C_2 in the wired FEVCS shown in Fig. 2. The obtained T_h of the capacitors are presented in Fig. 8(b). According to the results, the T_h of C_1 reaches 34.1°C, whereas that of C_2 reaches 42.6 °C.

Fig. 9(a) presents the T_j of a single semiconductor switch in the three-phase ac/dc converter (S_1), the dc/ac converter on the primary side (S_7) and the ac/dc converter on the secondary side (S_{11}) of the wireless FEVCS shown in Fig. 3. According to the operating conditions, the selected IGBT switch for S_1 and S_{11} is SKM300GB12T4, and for S_7 is SKM800GA125D. In the wireless FEVCS, the current and thereby the power losses through the semiconductor switches increase in the order of S_1, S_{11}, and S_7. Therefore, starting from the minimum value of 25 °C, the T_j increases in the same order and T_j of S_1, S_7, and S_{11} reach their mean values at 58.4, 90.2, and 74.7 °C, respectively. In this study, a dc film capacitor, MKP1848C74060JY5 was selected for C_1 and C_6, whereas ac film capacitors, MKP386M515200Y was selected for C_2 and C_4, and MKP386M368200J was selected for C_3 and C_6 in the wireless FEVCS shown in Fig. 3. Fig. 9(b) indicates the T_h of C_1–C_6 in the wireless FEVCS and the obtained T_h values are 34.4, 74.7, 77.8, 80.1, 76.4, and 42.9 °C, respectively. It should be noted that the temperature of each component varies according to many factors such as the operating current and thereby the induced power losses, and especially the rated operating conditions of the selected component.

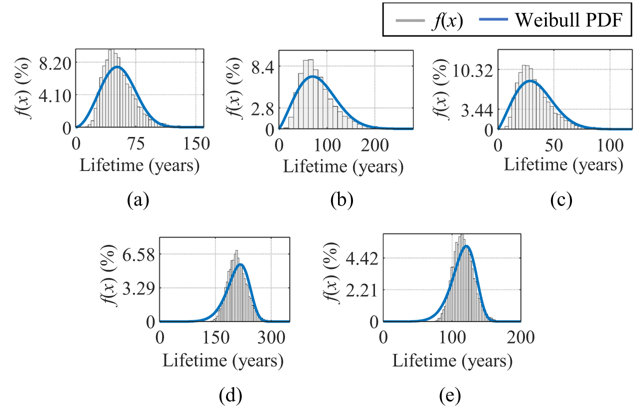

Fig. 14. *f*(*x*) and the corresponding weibull PDF of: (a) S_1, (b) S_7, (c) S_{11}, (d) C_1, and (e) C_2 in the wired FEVCS.

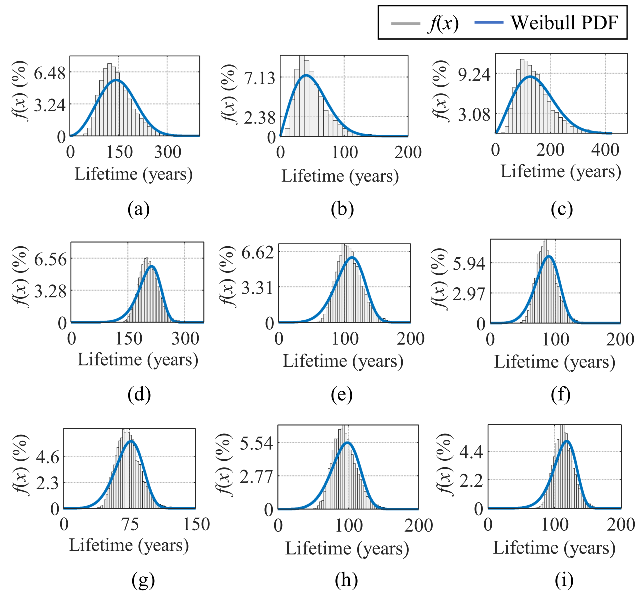

Fig. 15. *f*(*x*) and the corresponding weibull PDF of: (a) S_1, (b) S_7, (c) S_{11}, and (d)–(i) C_1–C_6 in the wireless FEVCS.

The T_j was further decomposed using the Rainflow cycle counting method as described in Section II-B to extract the T_j cycle data. The obtained Rainflow matrixes of T_j for the semiconductor switches in both the wired and wireless FEVCSs are shown in Figs. 10 and 11, respectively. Within the Rainflow matrixes, the majority of T_j cycles exhibit T_{jm} and ΔT_j values, as detailed in Table II .

B. Lifetime Evaluation

In order to determine the *LC* and thereby the lifetime of semiconductor switches and capacitors, the extracted T_j cycle data and T_h were applied to the lifetime model of each component as described in Section III-A. The resultant *LC* and corresponding lifetime data for wired and wireless FEVCSs are depicted in Figs. 12 and 13, respectively. The results indicate that, in the wired FEVCS, S_{11} experiences the highest *LC* of 0.0332 per year, which implies that it has the lowest lifetime

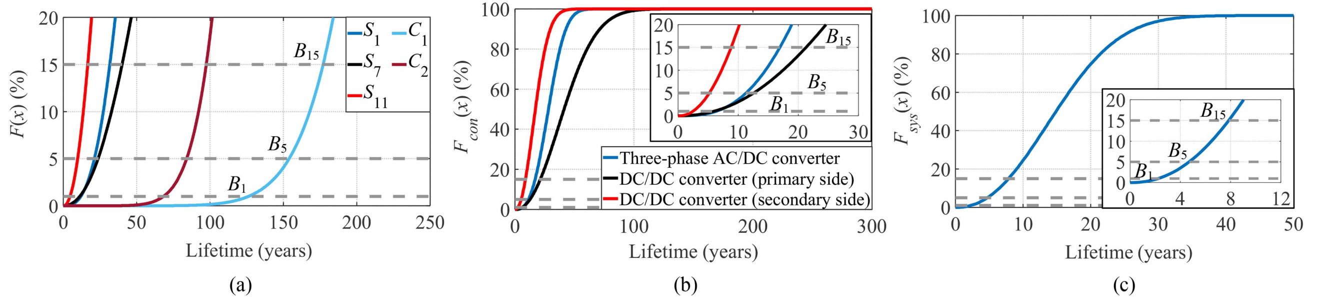

Fig. 16. $F(x)$ together with the B_x lifetimes for wired FEVCS: (a) component-level, (b) converter-level, and (c) system-level.

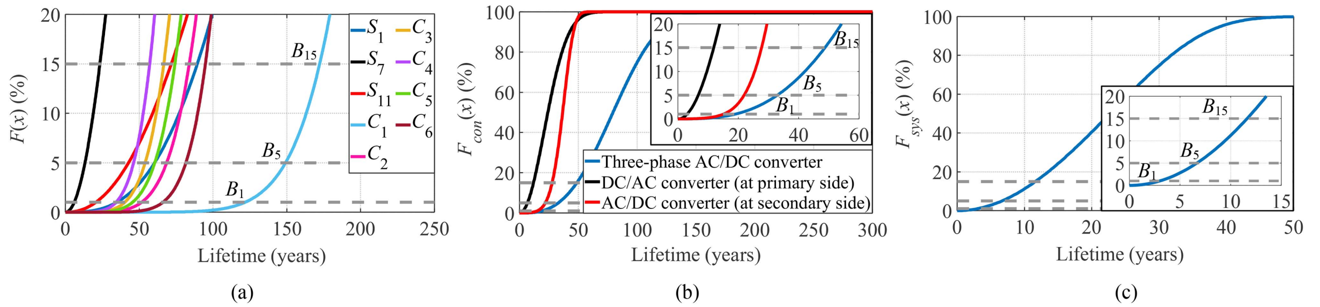

Fig. 17. $F(x)$ together with the B_x lifetimes for wireless FEVCS: (a) component-level, (b) converter-level, and (c) system-level.

and will reach the end of its operational life after 30.2 years. In the wireless FEVCS, S_7 experiences the highest LC of 0.0226 per year, implying that it has the lowest lifetime and will reach the end of its operational life after 44.2 years. However, the obtained lifetime predictions are based on the assumption that all the components will fail at the same rate. In reality, there are some uncertainties among the failure rates of components. Thus, the lifetime predictions were further analyzed in a probabilistic manner to estimate the reliability, which takes the parameter variations into account when determining the lifetime.

C. Reliability Estimation

To determine the lifetime of semiconductor switches and capacitors with a probability-based approach, a Monte Carlo analysis was conducted as described in Section III-C. The analysis was performed by introducing a normal distribution in which the variance is 5%, to the parameters of the lifetime models described in (3) and (5). Hence, the stress parameters, T_{jm}, ΔT_j, t_{on}, and T_h, which feed as the inputs to the lifetime models were also modeled with a normal distribution. In order to do that, the equivalent static values of the stress parameters were calculated and modeled with a 5% variation. This approach aims to improve the accuracy of lifetime estimation by considering potential variations in all stress and lifetime model parameters, while the 5% variation maintains computational efficiency and avoids excessive complexity [29], [31], [36]. Further, by including the obtained parameter variations, the Monte Carlo analysis was conducted with a sample population of 10 000. The results of this analysis indicate the lifetime of semiconductor switches and capacitors in terms of a static value with a certain distribution function. Usually, the lifetime distribution of the semiconductor switches and capacitors follows a Weibull distribution [32], [37], which can be described by its PDF as

$$f(x) = \frac{\beta}{\eta^{\beta}} x^{\beta - 1} \exp\left[-\left(\frac{x}{\eta}\right)^{\beta}\right] \tag{13}$$

where the scale parameter, η, indicates the time when 63.2% of the population has failed, while the shape parameter, β, usually corresponds to the mode of failure. The obtained $f(x)$ and the corresponding Weibull PDF of semiconductor switches and capacitors in the wired and wireless FEVCSs are shown in Figs. 14 and 15, respectively. As evident from the results, the majority of samples lie near the lifetime obtained with one sample. By integrating the $f(x)$ over the operating period, the $F(x)$ was obtained and the resultant $F(x)$ together with corresponding component-level B_1, B_5, and B_{15} lifetimes are depicted in Figs. 16(a) and 17(a) for wired and wireless FEVCS, respectively.

As described in Section III-C, the B_1 lifetime is considered the reliability matrix in this study. Hence, according to the results, the component-level reliability of S_1, S_7, and S_{11} in the wired FEVCS are 12, 11.2, and 4.7 years, respectively, and that of wireless FEVCS are 34.8, 6, and 20.6 years, respectively. The component-level reliability of C_1 and C_2 in the wired FEVCS is 126.2 and 68.3 years, and that of C_1–C_6 in the wireless FEVCS are 121.6, 51.6, 40.2, 34.3, 45.5, and 66 years, respectively. Hence, the findings reveal that S_{11} and S_7 as the least reliable components in the wired and wireless FEVCSs, respectively. In the analysis, different semiconductor switches and capacitors

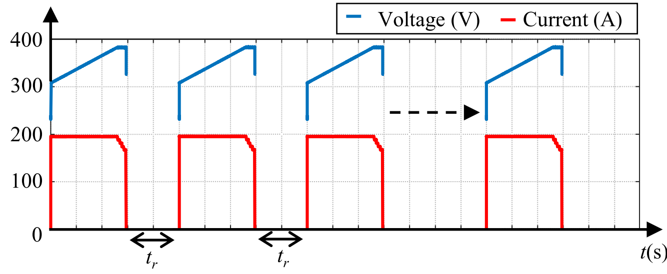

Fig. 18. Charging cycles with rest periods.

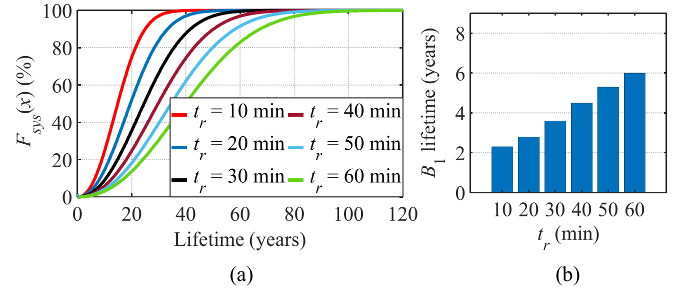

Fig. 19. (a) $F_{sys}(x)$ and (b) reliability of the wired FEVCS over t_r.

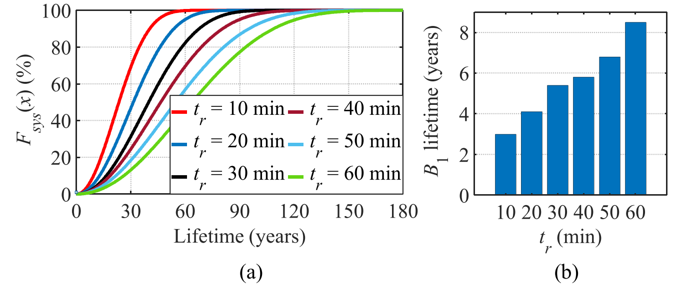

Fig. 20. (a) $F_{sys}(x)$ and (b) reliability of the wireless FEVCS over t_r.

were selected according to the operating conditions as described in Section V-A. The stress parameters, that impact the reliability, depend on the rated and actual operating conditions of the selected component. Therefore, the findings can be used as useful knowledge when determining the suitable components to design the FEVCSs with a desired reliability.

D. Converter and System-Level Reliability Evaluation

In order to evaluate the reliability at the converter-level, the reliability block diagram is employed as described in Section III-C. The wired and wireless FEVCSs consist of a different number of semiconductor switches and capacitors in each converter and these converters cannot function if any of the components fail. Within each converter, the stress conditions of semiconductor switches and capacitors are equal. Therefore, the $F(x)$ of each component is the same in the corresponding converter and it is different among the other converters. Thus, the $F_{con}(x)$ was obtained using (11) and the n is determined according to the number of components in each converter. The obtained $F_{con}(x)$ of converters are presented in Fig. 16(b), together with corresponding converter-level B_1, B_5, and B_{15} lifetimes for the wired FEVCS. Results imply that the reliability of the three-phase ac/dc converter, primary side of the dc/dc converter, and secondary side of the dc/dc converter in the wired FEVCS is 6.4, 6, and 2.5 years, respectively. Fig. 17(b) presents the $F_{\text{con}}(x)$ of converters in the wireless FEVCS, together with corresponding converter-level B_1, B_5, and B_{15} lifetimes. In the wireless FEVCS, the reliability of the three-phase ac/dc converter, dc/ac converter on the primary side, and ac/dc converter on the secondary side are 18.9, 3, and 15 years, respectively. According to the results it can be observed that when derived from the component-level to the converter-level, the reliability is reduced according to the number of components in each converter. Overall, results imply that the secondary side of dc/dc converter is the least reliable converter in the wired FEVCS, while the dc/ac converter on the primary side is the least reliable converter in the wireless FEVCS. Hence, the findings in this analysis can be considered a useful asset to identify the most prone-to-failure converter and taken into account when designing the FEVCSs with more reliable converters.

According to the method described in Section III-C, the analysis was further simplified to estimate the reliability of both the wired and wireless FEVCSs at the system-level. Thus, considering the $F_{con}(x)$ of each converter, the $F_{sys}(x)$ was derived for the wired and wireless FEVCSs. The $F_{sys}(x)$ and corresponding B_1, B_5, and B_{15} lifetimes of the wired and wireless FEVCSs are shown in Figs. 16(c) and 17(c), respectively. According to the results, the reliability of wired FEVCS is 2.3 years, while the reliability of wireless FEVCS is 3 years. The findings indicate that the mission profile has a significant impact on the reliability of each FEVCS, depending on the selected components and their actual and rated operating conditions. The insights gained from this analysis can drive improvements in designing the FEVCSs with the most suitable component selections ensuring their proper function. Further, such analysis can be useful when designing the FEVCSs in a cost-effective way by avoiding over designing with unexpected higher reliability. Hence, by carefully monitoring the T_j and T_h of semiconductor switches and capacitors, the best components can be selected and the FEVCSs can be designed with a known level of reliability.

VI. Impact of Rest Periods on FEVCS Reliability

The reliability analysis presented in this study was further extended to investigate the impact of rest periods on the reliability of both wired and wireless FEVCSs. In this case, the rest periods were introduced with different t_r values after each charging period as illustrated in Fig. 18. Accordingly, the reliability was estimated using the lifetime model, which incorporates the rest periods as described in Section III-B, and probabilistic analysis in Section III-C. The obtained $F_{sys}(x)$ and corresponding B_1 lifetime over t_r for wired and wireless FEVCSs are presented in Figs. 19 and 20, respectively. The results indicate a significant improvement in reliability by introducing rest periods in both wired and wireless FEVCSs. Further, it can be observed that reliability is increased when the t_r increases. In the wired FEVCS, reliability is improved maximum from 2.3 to 6 years, whereas, in

the wireless FEVCS, reliability is improved maximum from 3 to 8.5 years, after integrating rest periods with a t_r of 60 min. This is because once the rest periods are integrated, the total number of operational cycles can be reduced, and therefore, reliability is improved. Thus, the findings can be considered to design the charging schedules incorporating a certain rest period in order to achieve a desired reliability in FEVCSs.

VII. Conclusion

In this article, a reliability estimation strategy, comprising an electro-thermal model and a reliability estimation model, to analyze the reliability of FEVCSs has been presented. Using the proposed strategy, reliability analysis has been carried out on two configurations, wired and wireless FEVCSs, considering the reliability of semiconductor switches and capacitors at the component, converter, and system-level. The reliability has been estimated using lifetime models following the T_j cycling information of semiconductor switches and the T_h of capacitors. The accuracy of T_j profile has been validated through experimental results, and the T_h and proposed strategy have been validated, adhering to standard equations. Results have indicated S_{11} in wired FEVCS and S_7 in wireless FEVCS as the least reliable components, guiding component selection for desired reliability. Converter-level analysis has shown a decrease in reliability with increasing components, highlighting the secondary side of the dc/dc converter in wired FEVCS and the dc/ac converter on the primary side in wireless FEVCS as the least reliable converters. These findings serve as a useful guide for designing FEVCSs with more reliable converters. System-level analysis has emphasized a significant impact of mission profile on FEVCS reliability, suggesting improvements through optimal component selection and avoiding overdesign for higher reliability. Introducing rest periods has significantly improved reliability, resulting in an increase from 2.3 to 6 years for wired FEVCS and from 3 to 8.5 years for wireless FEVCS, with a 60 min rest period. This guides designing charging schedules to achieve desired reliability.

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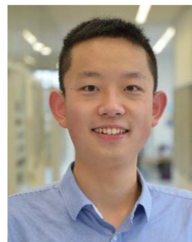

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