Optimization and Validation of Current Sharing in IGBT Modules With Multichips in Parallel

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***Abstract*—Multichips paralleled insulated gate bipolar transistor (IGBT) power modules are widely employed in industrial and automotive power conversion systems. The asymmetry of the circuit topology and the differences in chip characteristics are the main reasons for the unbalanced current distribution among parallel chips, leading to excessive electrical stress in power modules, which in turn forces the power modules to operate at a reduced rated current. Additionally, the unbalanced current distribution inevitably results in different chip losses, which are further amplified under high current loading conditions, causing some chips to be overheated, and significantly reducing the reliability. Optimizing the circuit topology is a common method to improve current distribution, but global changes often entail higher costs and longer development cycles. Moreover, the electrical parasitic of the fast recovery diodes (FRD) chip branches are not given sufficient attention in circuit topology research. Under rectification and blocked conditions in electric vehicles, FRDs often become the bottleneck for lifespan due to excessively high junction temperatures. Therefore, this article conducts a comparative analysis of the circuit parasitic in IGBT and FRD loops with several typical layouts, without changing the substrate and chip dimensions, and proposes a current sharing slot structure design to balance the parasitic parameters. Compared with the direct bonded copper (DBC) layout of the typical EconoDUAL power module, the optimized module reduces the current imbalance of FRD from 45.5% to 11.6% and the switching loss can be reduced by 8.6%. By adopting the current sharing groove, the parasitic parameter distribution can be further improved while maintaining a fixed DBC layout, considering the IGBT and FRD branches in concert. Finally, the steady-state and transient current sharing characteristics were verified under constant current and inverter conditions. Under constant current conditions, the temperature difference of FRD in the upper and lower parallel layout modules was reduced by 16.7 °C, and the junction temperature of IGBT was significantly lowered. Under inverter conditions, the highest junction temperature of the columnar layout modules could be reduced by 10 °C, and the temperature difference of FRD decreased by 62%. This article significantly optimizes the current imbalance issue through layout design, reduces the thermal equilibrium difference of the module under application conditions, and is conducive to improving the output capacity and fatigue life of the module, providing a solution for the design of power modules with high junction temperature operation capability and high-reliability.**

***Index Terms*—Dynamic sharing, parasitic parameters, reliability, static equilibrium, thermal equilibrium.**

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I. Introduction

INSULATED gate bipolar transistor (IGBT) modules are the core components of power conversion in industrial and automotive applications. With the rapid development of the new energy market, the demand for power density and reliability of IGBT modules has further increased. IGBT manufacturers have not only updated their chip technologies through multiple generations but also kept their packaging technologies up-to-date. High-capacity power modules typically with multichip in parallel, and due to the asymmetry of the packaging structure and the differences in chips, it is inevitable that there will be an imbalance in the current distribution among the chips [1], [2]. This unbalance leads to differences in power losses, voltage, and current stresses, and the "bottleneck" effect forces the entire module to operate at a derated capacity, which also results in increased failure rates and reduced lifespan of the module [3], [4], [5]. Therefore, enhancing the consistency of current distribution among paralleled chips in power modules and addressing the issue of excessive local junction temperatures caused by loss differences are key to improving the power output performance and reliability of power modules.

To address the issue of current sharing in multichip parallel configurations, various strategies have been developed, which can be broadly classified into three categories. First, the variability in the electrical properties of individual chips is a critical factor that affects current distribution within the module, necessitating careful consideration. Li et al. [6] highlighted the significant influence of ON-resistance and threshold voltage on steady-state and dynamic current sharing in parallel power modules. The impact of device parameter nonuniformity on the electrical and thermal imbalance of power modules under

short-circuit conditions has also been examined [7]. Strategies to mitigate these effects include reducing the rated current and implementing a rigorous chip selection process [8], [9]. Ke et al. [10] introduced a novel classification metric for chip parameter dispersion, known as the distance coefficient of transfer curves, and developed a hierarchical clustering algorithm to automate chip classification for parallel applications.

Second, the switching sequence of paralleled chips are governed by gate voltage, and an increase in switching speed can lead to dynamic losses and uneven current distribution due to driving signal delays. To counteract this, various driving compensation techniques have been proposed [11], [12], [13], [14], [15]. Martin et al. [13] identified that gate circuit asymmetry can disrupt the coupling of common-emitter inductance, resulting in current unbalance, which can be mitigated by optimizing gate-level wiring. Mao et al. [14] suggested passive compensation to equalize the peak currents of gate drivers, effectively reducing peak current disparities from 15% to 3% without compromising switching loss or voltage stress. Zeng and Li [15] focused on controlling gate resistance, gate-source capacitance, and gate voltage to dampen current oscillations and voltage overshoot in parallel chips.

From a packaging standpoint, enhancements in module design, such as optimizing the commutation loop, direct bonded copper (DBC) layout, and packaging pins, can alleviate static and dynamic current unbalance issues arising from parasitic resistance and inductance [16]. Matallana et al. [17] conducted equivalent circuit simulations to assess the impact of power device interconnect wiring on current distribution, emphasizing the importance of balancing the impedance between the collector and emitter for achieving balanced current distribution. Li et al. [18] introduced an innovative packaging approach for power electronic modules, leveraging the concepts of P-units and N-units to minimize crosstalk inductance during current commutation, thereby enhancing switching performance. A symmetric DBC layout was also proposed by Li et al. [19], which significantly reduced circuit mismatch and current coupling effects. Ning et al. [20] further advanced the field by proposing an automatic layout strategy based on genetic algorithms to achieve electrical parasitic parameter balance. It is evident that layout symmetry and mutual inductance cancellation are pivotal in optimizing commutation loops.

However, in industrial applications, module size and layout are often predetermined to accommodate specific applications, making global circuit matching design both costly and time-consuming. Thus, optimizing parasitic parameters within a fixed layout presents a significant industry challenge. Furthermore, in electric vehicle rectification and blocked conditions, fast recovery diodes (FRD) frequently encounter high junction temperatures, which can limit their lifespan. The current sharing issues of FRD chips in circuit topology research are often omitted, necessitating further investigation to address this critical aspect of power module longevity.

Considering the abovementioned issues, this study initiates with a finite element analysis of several representative DBC layouts to ascertain the disparities in parasitic parameters induced by layout variations. Following this, structural enhancements are applied to the established layout, introducing a current sharing slot design to further equalize the parasitic parameters across the branches. Moreover, a comparative analysis using double-pulse testing is conducted to evaluate the differences in the current distribution among various configurations. To further validate the findings, infrared thermography is utilized to examine the thermal profile of the chips, and the distinct impacts of static and dynamic losses under constant current and inverter conditions are assessed, providing insights into their influence on real-world operational scenarios.

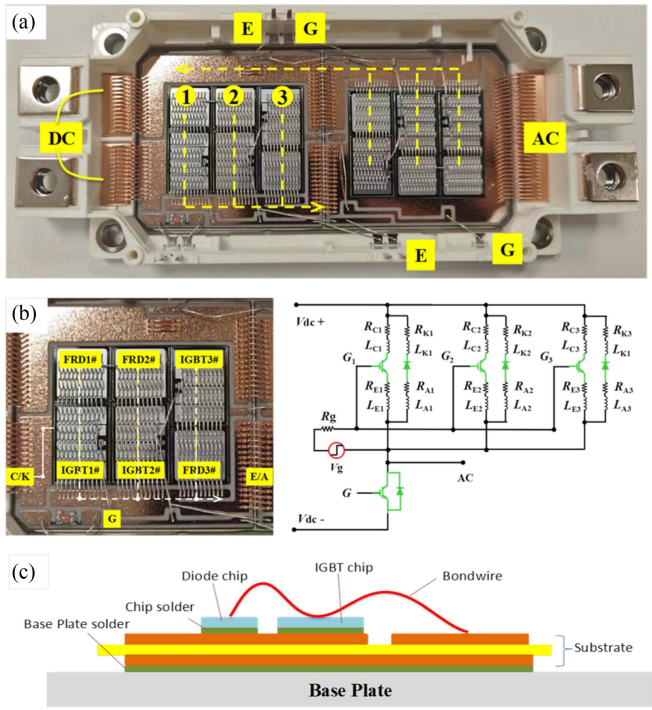


Fig. 1. Structural schematic diagram of EconoDUAL module structure. (a) Internal layout of the DUT. (b) Equivalent electrical resistance and inductance circuit for three chips in parallel. (c) Cross-section diagram of the power module.

II. Formulation of Current Sharing

A. Multichip Parallelled Current Sharing Analysis

In the context of multichip parallelled layout design, this article focuses on the EconoDUAL power module, a typical example with a rating of 1200 V/1000 A, as depicted in Fig. 1. Packaging structure of the module comprises a heat dissipation base plate, DBC substrate, solder layer, semiconductor chips, and bonding wires, with the upper and lower bridge arms each consisting of three parallel IGBT and FRD. Considering the external parasitic introduced by the module's packaging elements, such as bonding wires and DBC copper layers, the equivalent circuit is illustrated in Fig. 1(b), where R_{C1} and L_{C1} represent the parasitic resistance and inductance of the respective branches. The crux of achieving current sharing in parallel IGBT module design lies in ensuring the equilibrium of branch currents for each chip under both static and dynamic operating conditions.

The distribution of power across chips during conduction is primarily determined by static current sharing characteristics,

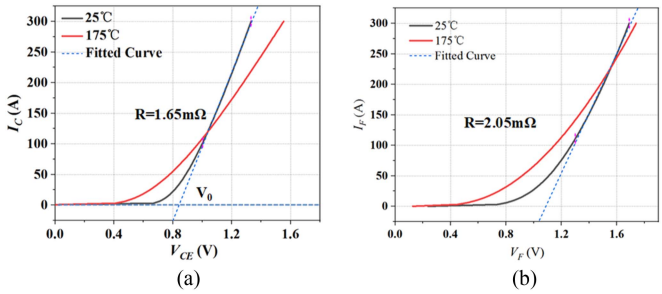


Fig. 2. Output characteristics of IGBT and FRD chips.

which can lead to disparities in conduction losses among various branches. Dynamic current sharing, in contrast, focuses on the device's switching dynamics, encompassing the design of stray inductance within the commutation loop and the synchronization of the device's turn-ON and turn-OFF events. In static current sharing scenarios, the conduction loss typically overshadows the switching one. The parasitic resistance encountered along the conduction path is composed of two distinct elements: 1) the intrinsic resistance of the chip itself and 2) the parasitic resistance inherent to the packaging loop.

The equivalent resistance of IGBT and FRD chips is the reciprocal of the slope of the *I-V* characteristics, as shown in Fig. 2. For the equivalent resistance of the bare chip, it can generally be expressed as

$$V'_{CE} = V_0 + R_1 \times I_{C1} \tag{1}$$

where V_0 is the turn-ON voltage, R is the equivalent resistance, I_{C1} is the collector current, and V_{CE} is the ON-state voltage of the bare chip. Since the IGBT on-resistance is small and sensitive to external parasitic of the package, the on-resistance of the module branch can be expressed as

$$V_{CE1} = V'_{CE1} + (R_{C1} + R_{E1}) \times I_{C1}. \tag{2}$$

Considering three chips in parallel and assuming that the static characteristics of IGBT chips are the same, the branch current is

$$I_{C1} = \frac{I_{C-sum}}{R_1 + R_{C1} + R_{E1}} \times \frac{1}{\left(\frac{1}{R_1+R_{C1}+R_{E1}} + \frac{1}{R_2+R_{C2}+R_{E2}} + \frac{1}{R_3+R_{C3}+R_{E3}}\right)}. \tag{3}$$

Similarly, for the FRD chip, there is

$$I_{A1} = \frac{I_{F-sum}}{R_1 + R_{A1} + R_{K1}} \times \frac{1}{\left(\frac{1}{R_1+R_{A1}+R_{K1}} + \frac{1}{R_2+R_{A2}+R_{K2}} + \frac{1}{R_3+R_{A3}+R_{K3}}\right)} \tag{4}$$

where R_{C1}, R_{E1}, R_{A1}, and R_{K1} are external parasitic brought by the package, and the static imbalance degree of the branch current can be expressed as

$$\delta I = \Delta I_{C,\max} / I_{C,\text{mean}} \tag{5}$$

where $\Delta I_{C,\max}$ is the difference between the maximum and minimum branch currents, and $I_{C,\text{mean}}$ is the average of the branch currents. The key to the static current sharing capability of the module is to balance the parasitic resistance brought by the module packaging.

For inverter application conditions, the switching frequency of the module can reach more than 5 kHz, and the conduction loss during operation cannot be ignored. Assuming the input current is sinusoidal, the loss of the inverter condition can be described as [21]

$$P_{\text{IGBT}} = P_{COND} + P_{SW} = I_C \times V_{\text{CESAT}} \left(\frac{1}{8} + \frac{d}{3\pi}\cos\theta\right) + \frac{1}{\pi} \times f \times (E_{\text{on}} + E_{\text{off}}) \tag{6}$$

where P_{COND} is the conduction loss, P_{SW} is the switching loss, $\cos\theta$ is the power factor, and d is the duty cycle. The switching loss of the FRD can be expressed as

$$P_{FWD} = P_F + P_{REC} = I_F \times V_F \left(\frac{1}{8} - \frac{d}{3\pi}\cos\theta\right) + \frac{1}{\pi} \times f \times E_{REC} \tag{7}$$

where P_F is the conduction loss, and P_{REC} is the reverse recovery loss. Therefore, the inverter process must consider the conduction, switching, and reverse recovery processes simultaneously. For the general dynamic process where external packaging introduces circuit parameter mismatches, the issue can be summarized as a switching time difference problem caused by the common-base parasitic inductance, and a high voltage overshoot problem caused by the total parasitic inductance of the branch. High *di/dt* during the turn-OFF process, leading to voltage overshoot, can be simply expressed as

$$\Delta U = \frac{di}{dt} \times L \tag{8}$$

where d*i*/d*t* is the current change rate, and L is the parasitic inductance. When chips are paralleled, the branch voltage drop is consistent, so the overshoot caused by the total loop inductance is consistent. Different parasitic inductances will lead to changes in the current change rate, thereby affecting the turn-OFF loss. Due to the complexity of the switching waveform, the dynamic current sharing issue can be simply described by the imbalance degree of the loss

$$\delta E_{tot} = \Delta E_{tot,\max} / E_{tot,\text{mean}} \tag{9}$$

$$\delta E_{REC} = \Delta E_{REC,\max} / E_{REC,\text{mean}}. \tag{10}$$

III. Parasitic Parameters Optimization

A. Design of DBC Layout

Considering the packaging structure of the EconoDUAL module, the research initially focuses in on the DBC layout. The wiring paths connecting the chips to the terminals have a direct impact on the parasitic properties of each branch. Additionally, since both the IGBT and FRD chips in this module exhibit positive temperature coefficients, meaning that the higher

TABLE I
PARASITIC RESISTANCES FOR DIFFERENT DBC LAYOUTS

Loop	Parasitic Resistances (mΩ)	Branch Parasitic Resistances	Imbalance Factor
Case 1 (Initial layout)			
Collector part (IGBT)	R_{C1}= 0.10 R_{C2}= 0.11 R_{C3}= 0.12	R_{T1}= 0.87 R_{T2}= 0.73	8.8%
Emitter part (IGBT)	R_{E1}= 0.76 R_{E2}= 0.61 R_{E3}= 0.82	R_{T3}= 0.94	
Cathode part (FRD)	R_{K1}= 0.14 R_{K2}= 0.15 R_{K3}= 0.17	R_{F1}= 1.21 R_{F2}=1.13	19.1%
Anode part (FRD)	R_{A1}= 1.06 R_{A2}= 0.98 R_{A3}= 0.47	R_{F3}= 0.61	
Case 2 (Sequential layout)			
Collector part (IGBT)	R_{C1}=0.10 R_{C2}= 0.10 R_{C3}= 0.11	R_{T1}= 0.87 R_{T2}= 0.71	12.9%
Emitter part (IGBT)	R_{E1}= 0.77 R_{E2}= 0.61 R_{E3}= 0.46	R_{T3}= 0. 57	
Cathode part (FRD)	R_{K1}= 0.24 R_{K2}= 0.15 R_{K3}= 0.26	R_{F1}= 1.45 R_{F2}= 1.28	9.6%
Anode part (FRD)	R_{A1}= 1.21 R_{A2}= 0.98 R_{A3}= 0.87	R_{F3}= 1.13	
Case 3 (Columnar layout)			
Collector part (IGBT)	R_{C1}=0.07 R_{C2}= 0.12 R_{C3}= 0.15	R_{T1}= 1.18 R_{T2}= 1.15	6.3%
Emitter part (IGBT)	R_{E1}= 1.52 R_{E2}= 1.39 R_{E3}= 1.26	R_{T3}= 1.01	
Cathode part (FRD)	R_{K1}= 0.07 R_{K2}= 0.14 R_{K3}= 0.17	R_{F1}= 1.21 R_{F2}= 1.08	5.8%
Anode part (FRD)	R_{A1}= 1.51 R_{A2}=1.39 R_{A3}= 1.25	R_{F3}= 1.03	

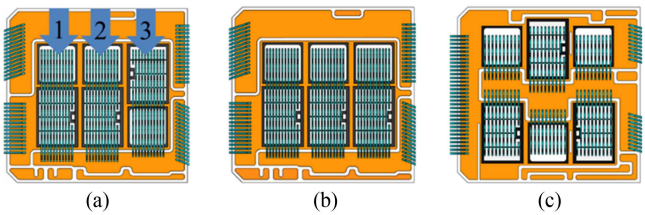


Fig. 3. Different chip layout designs. (a) Initial layout (Case 1). (b) Sequential layout (Case 2). (c) Columnar layout (Case 3).

the temperature, the higher the saturation conduction voltage drop, which implies an increase in the equivalent resistance of the chips. This phenomenon can diminish the current-carrying capacity of chips with elevated junction temperatures. Consequently, without modifying the substrate's dimensions, two contrasting initial layout schemes for the EconoDUAL can be proposed, as depicted in Fig. 3.

In Case 2, the positions of the IGBT and FRD are altered, arranging the chips sequentially, while in Case 3, the copper layer of emitter part is shifted to the center, and to achieve a more balanced common emitter inductance, the bonding point of the auxiliary emitter directly falls on the middle FRD chip. To evaluate the static current sharing performance of various

DBC layouts, the distribution of parasitic parameters was initially extracted using the finite element software AnsysQ3D. Since the equivalent switching frequency of the IGBT approaches 1 MHz according to the datasheet and literature [22], the parasitic parameters were extracted at a frequency of 1 MHz. with an ac excitation frequency of 1 MHz. The simulated parasitic parameter results are detailed in Table I, where the imbalance is assessed considering the chip's equivalent resistance. In Case 1, the FRD chip in the third branch has a shorter wire-bond path on the anode side, leading to a notable decrease in its parasitic resistance (R_{A3}) compared to other branches. As a result, this branch's parasitic resistance is significantly lower than the others, with an imbalance factor of 19.1%. The analysis of parasitic composition reveals that the parasitic resistance predominantly originates from the IGBT emitter and the FRD anode, which are primarily interconnected by bonding wires. This suggests that bonding wires are the principal contributors to module parasitics. Thus, a crucial aspect of current sharing design is to equalize the lengths of the bonding wires. In Case 2, the positions of the third branch FRD and IGBT chips are adjusted, resulting in a longer wire path for the FRD chip and a substantial increase in the parasitic parameter R_{A3} compared to the initial layout. This adjustment reduces the FRD part imbalance from 19.1% to 9.6%. However, due to the repositioning of the third branch, there is a 44% decrease in the parasitic resistance R_{E3} compared to Case 1. Consequently, the imbalance of the IGBT chip increases to 12.9%, indicating that the layout of Case 2 sacrifices the balance of the IGBT branch to mitigate the imbalance of the FRD chip, presenting a compromised solution.

Centering the copper layer on the emitter side, as illustrated in Case 3, effectively equalizes the lengths of the bonding wires. The variations in parasitic parameters for this layout are primarily attributed to the differences in the DBC copper layer, although the magnitude of these variations is relatively minor. Simulation outcomes indicate that the imbalance factor for the IGBT branch is 6.3%, and for the FRD, it is 5.8%, both of which represent a substantial improvement over the original layout. Specifically, the imbalance degree of the FRD has been reduced by 69.6% compared to the initial configuration.

B. Design of Current Equalization Groove

To optimize the module's parasitic parameters, especially considering the fixed DBC layout, the local structure of the DBC layout can be designed to reduce differences in current paths. As analyzed in Section III, the differences in parasitic parameters mainly originate from the emitter of the chips, with

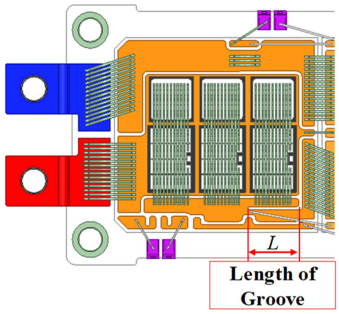


Fig. 4. Schematic diagram of current equalization groove.

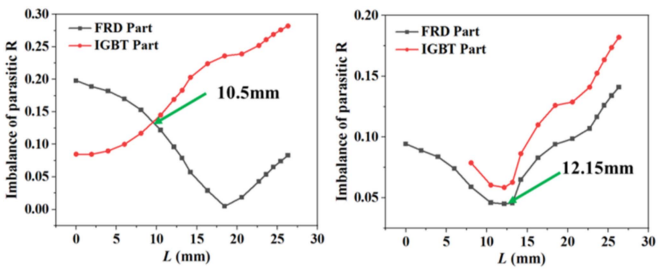


Fig. 5. Relationship between parasitic resistance imbalance and length of equalization groove. (a) Case 1. (b) Case 2.

the greatest imbalance occurring in Branch 3. Consequently, the copper layer at this site can be tailored by incorporating a groove, as depicted in Fig. 4. This innovative design is referred to as a current equalization groove.

The lengths of the current equalization grooves were meticulously adjusted to assess the variations in parasitic parameter differences for two distinct schemes, as illustrated in Fig. 5. The parasitic resistance here is also extracted at a frequency of 1 MHz [22]. By analyzing the trend of parasitic parameter differences in relation to the length of the current equalization slot, it is evident that the layout of Case 1 provides superior current equalization for the IGBT before the parasitic resistance is mitigated by the groove. Once the parasitic resistance of the FRD is compensated for using the groove, the current equalization effect for the FRD is markedly enhanced. However, this enhancement comes at the expense of the IGBT's current equalization performance. A balanced solution can be achieved by opting for the position at 10.5 mm, where the current imbalance for the FRD is reduced to 12.2%, and for the IGBT, it is 14.5%. Building upon the foundation of the Case 1 layout, we have incorporated a 10.5 mm current balancing groove. This revised configuration, henceforth referred to as Case 4, is slated for further exploration in our forthcoming experimental studies.

The current equalization effects for both the IGBT and FRD in Case 2 exhibit a synchronized response to the length variation of the current equalization groove. The optimal balance is achieved when the groove's length is set at 12.15 mm, at which point both the IGBT and FRD reach their respective optimal current equalization states. Here, the parasitic parameter imbalance for the IGBT is reduced to 5.6%, and for the FRD, it is an even lower 4.5%.

Fig. 6. Experimental test bench for evaluating collector current.

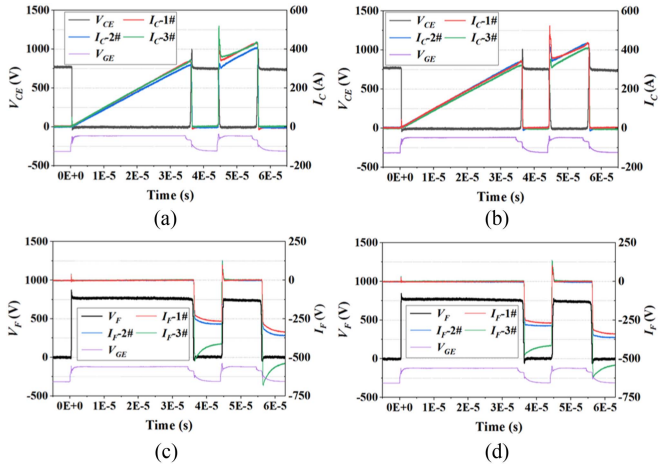


Fig. 7. Switching waveforms of Case 1 in (a) room temperature and (b) 125 °C, and recovery waveforms of Case 1 in (c) room temperature and (d) 125 °C.

IV. Experimental Validation of Current Sharing

The previous section offered an initial assessment of the parasitic parameter disparities across various packaging layouts, with the optimized layout, Case 3, demonstrating notable advantages. Upcoming experimental endeavors will assess the efficacy of layout adjustments and the incorporation of current equalization groove on enhancing the current sharing of the module. Consequently, the subsequent experimental analysis primarily targets Cases 1 and 3. The optimization of parasitic parameters inherently results in substantial alterations to the module's dynamic electrical characteristics, necessitating a precise quantification of current sharing through a double-pulse test. During the test, current sensors were wrapped around the bonding wires of each branch to measure individual branch currents, as depicted in Fig. 6. The experiment was conducted with the busbar voltage maintained at 750 V, and the total collector current ($I_{C\text{-all}}$) was regulated to 1000 A by adjusting the turn-ON time to match the module's rated operating conditions.

The switching and reverse recovery waveforms for Case 1, as depicted in Fig. 7, are presented under both room temperature and elevated conditions of 125 °C. At ambient temperature, the IGBT demonstrates only subtle variations in the distribution of branch currents during the phase of current rise, whereas the FRD displays pronounced discrepancies during the freewheeling phase, notably in the third branch, aligning with prior simulation outcomes. Upon elevating the testing temperature to 125 °C, the V_F of FRD, positively correlated with temperature, results in increased impedance, thereby partially mitigating the issue of

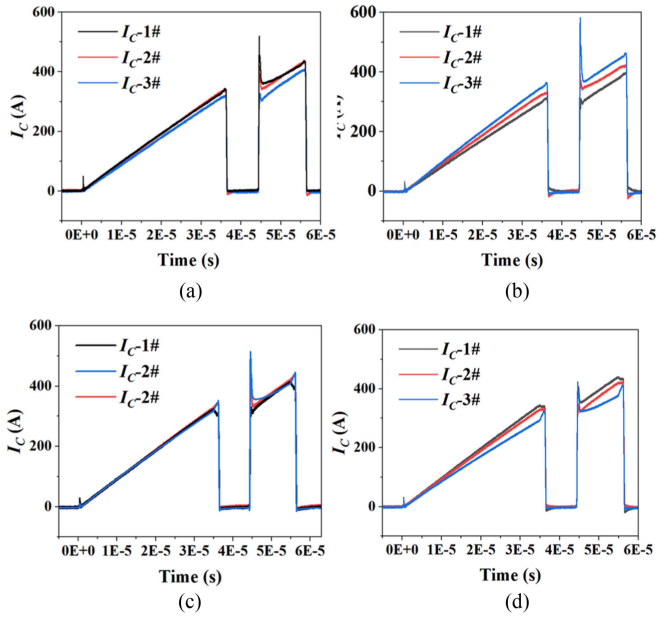


Fig. 8. Switching waveforms for double-pulse test of (a) case 1, (b) case 2, (c) case 3, and (d) case 4 (Case 1 with current equalization groove).

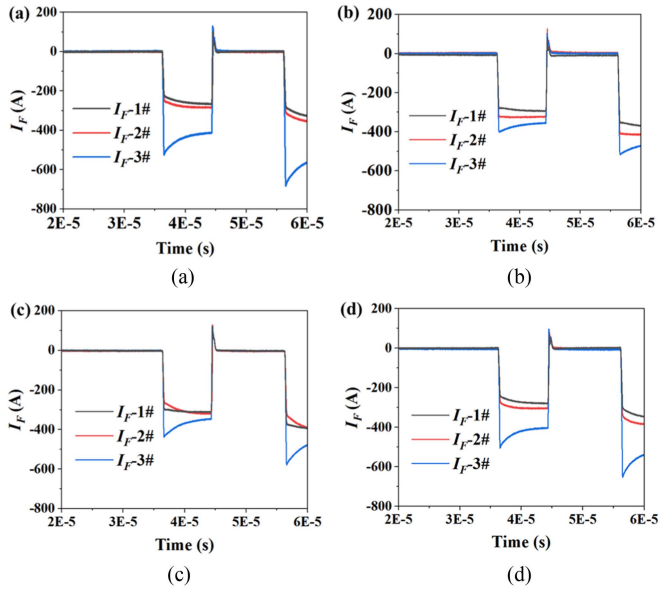


Fig. 9. Reverse recovery waveforms for (a) case 1, (b) case 2, (c) case 3, and (d) case 4 (Case 1 with current equalization groove).

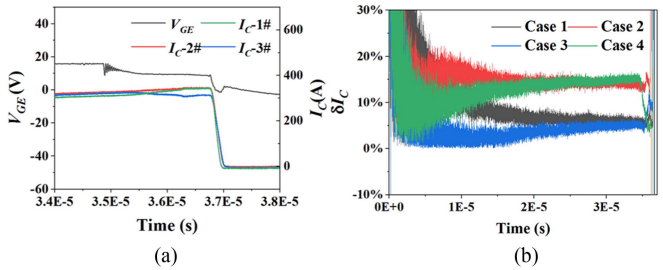


Fig. 10. (a) Turn OFF waveform for Case 3. (b) Current unbalanced factor of IGBT during the first pulse versus time.

uneven current distribution. Nonetheless, the effect of temperature on current balance is deemed less significant in comparison; hence, the subsequent discourse will concentrate on examining how various layouts influence static current balancing at room temperature.

The IGBT switching waveforms are illustrated in Fig. 8. It is evident that, in comparison to the initial layout, Case 3 marginally refines the current distribution among IGBTs during the current rise phase. Furthermore, when juxtaposed with Case 1, there is an observable decline in the static current balancing of the IGBTs within Cases 2 and 4. As indicated by previous simulation results, the unbalance factor of the parasitic resistance in the branches of Cases 2 and 4 has increased significantly, which is the primary cause of their uneven static current distribution.

Fig. 9 presents the reverse recovery waveforms across the FRD branches. The original layout, showing the worse performance of current sharing, demonstrated the most significant variance in branch currents during the period of freewheeling. This was primarily due to the static current imbalance stemming from parasitic resistance. Case 3 improved it by balancing the parasitic resistance across branches. Nonetheless, the implementation of the current balancing groove, while enhancing the current sharing of FRD branches, did so by compromising the IGBT's current sharing capabilities, a tradeoff that is in line with the expected outcomes.

Given that the EconoDUAL module is governed by a unified gate drive signal for IGBT switching, discrepancies in the turn-OFF sequence among the parallel IGBTs may arise, leading to the current crossover effect illustrated in Fig. 10(a). To ascertain the precision of the current imbalance assessment, the approach depicted in Fig. 10(b) has been adopted, which calculates the variation of the current imbalance over time during the first pulse period. Thereafter, the instant immediately preceding the turn-OFF of gate is selected as the reference point for quantifying the level of current imbalance.

Additionally, switch losses and reverse recovery losses are computed. As the current escalates, the module's current imbalance and loss imbalance factors are graphically represented in Fig. 11. Owing to the enhanced distribution of parasitic resistance in Case 3, its current imbalance consistently outperforms the initial layout, corroborating the simulation outcomes from the prior section. At a conduction current of 1000 A, the IGBT current imbalance is mitigated from 5.87% to 3.66%, reflecting a 37.6% improvement. However, in Cases 2 and 4, the current sharing capability of the IGBTs has experienced significant degradation. Although the unevenness of IGBT switching loss slightly augments when the current exceeds 400 A, a detailed analysis of specific losses for each branch reveals a reduction in losses across all IGBT chips. At 1000 A, the total IGBT switching loss for Case 3 is 381.2 mJ, a decrease of 8.6% relative to the partial staggered layout, which contributes to a lower junction temperature. The same methodology is applied to assess the imbalance and loss of FRD chips, as depicted

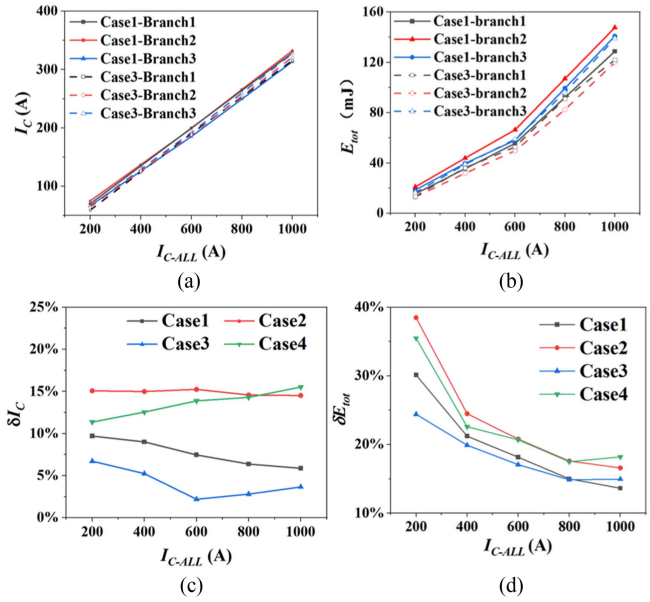


Fig. 11. Branch currents and losses for IGBT. (a) Branch currents. (b) Switch Losses of IGBT. (c) Imbalance of current sharing. (d) Imbalance of losses.

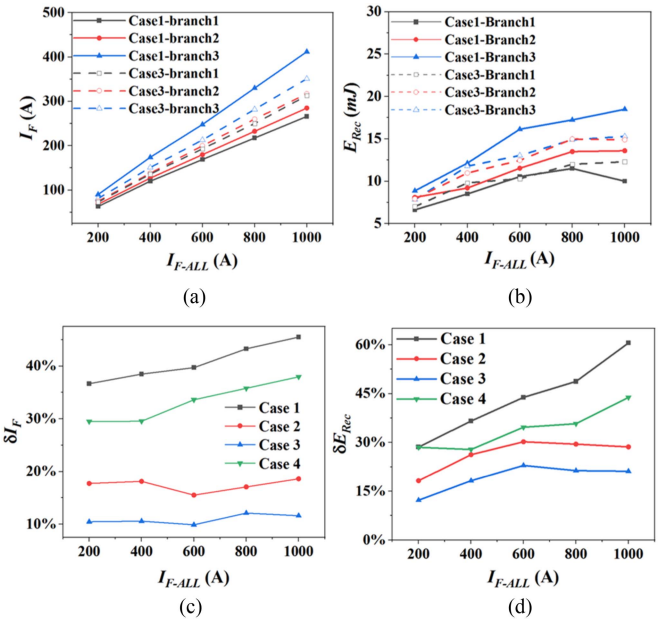


Fig. 12. Branch currents and losses for FRD. (a) Branch currents. (b) Reverse recovery losses. (c) Imbalance of current sharing. (d) Imbalance of reverse recovery losses.

in Fig. 12. The layout of Case 3 significantly enhances the FRD's current balancing capability, with the current imbalance diminishing from 45.5% to 11.6% at a total current of 1000 A, the maximum commutation difference from 146 A to 38 A, and the loss difference from 60.6% to 21.7%. Furthermore, Cases 2 and 4 have each effectively mitigated the disparities in FRD current and loss distribution, albeit to varying extents. Consequently, the junction temperature difference attributable to the disparity in reverse recovery loss is minimal, with the primary loss attributed to the FRD's conduction loss.

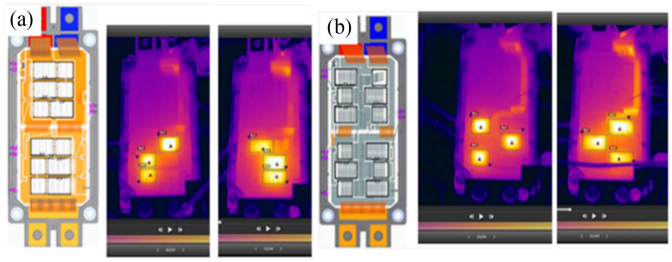


Fig. 13. Junction temperatures of FRD (left) and IGBT (right) for different layout of (a) Case 1 and (b) Case 3.

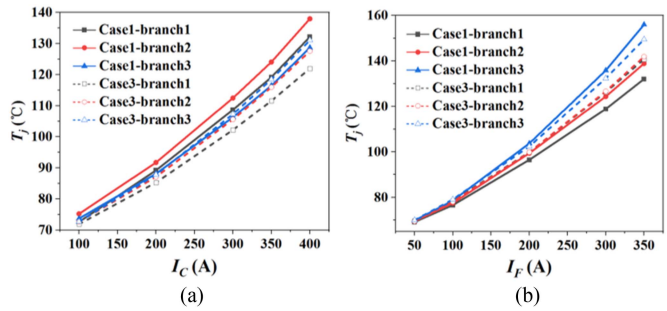


Fig. 14. Junction temperature changes with the current under PC conditions. (a) Temperature for IGBT chips. (b) Temperature for FRD chips.

V. Evaluation of Thermal Equilibrium

The objective of current sharing design is to ensure a uniform thermal distribution within the power module throughout its operation. Given the variability in load conditions, the composition of losses within the power module can vary significantly. Consequently, this section presents measurement of temperature distribution under both constant current and inverter conditions, with the goal of clarifying the effects of current imbalance on the thermal disparities among the junctions of parallel chips.

A. Steady-State Thermal Characteristics Evaluation

Under power cycling conditions, characterized by low switching frequencies in the power module, the static current equalization characteristics play a pivotal role in determining the temperature disparities among the module's branches. Consequently, the temperature distribution under constant current conditions can be analyzed to understand this effect. Currents of 350 A and 400 A are applied to the FRD and IGBT chips, respectively, to evaluate the impact of different chip layouts on the thermal equilibrium of the module. Infrared thermal imaging is employed to directly measure the junction temperatures of the chips, with the findings depicted in Fig. 13. As shown in Fig. 14, in the layout of Case 1, the FRD chips exhibit the highest junction temperature at the third branch, which aligns with the simulation and electrical test results indicating that the parasitic resistance of this branch is significantly lower than others, leading to increased current and, consequently, the highest junction temperature. Conversely, the IGBT chip with the highest junction temperature is located at the second branch, consistent with the conclusions from parasitic resistance and

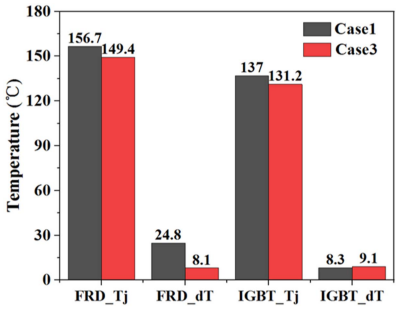


Fig. 15. Junction temperature and difference of chips under PC conditions.

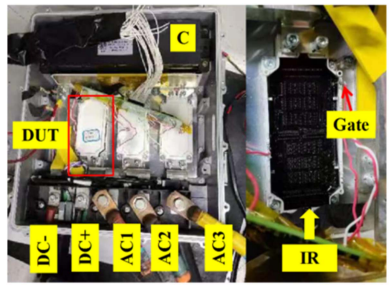
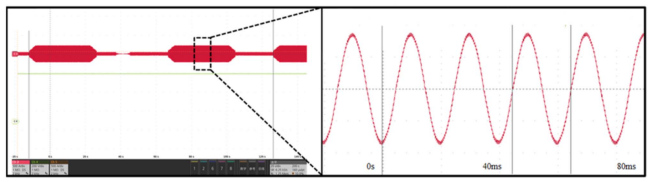
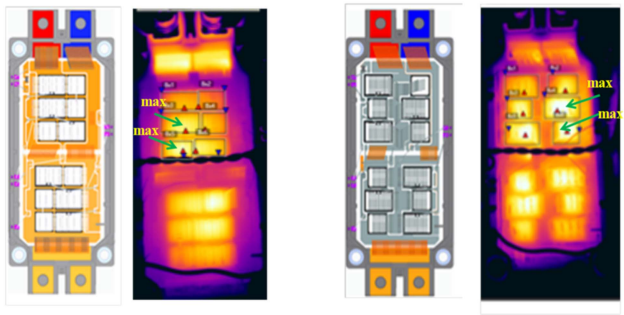


Fig. 16. Schematic diagram of the junction temperature test under inverter conditions.



(a) (b)

Fig. 17. Waveform of current output under inverter conditions.



(a) (b)

Fig. 18. Temperature distribution under inverter conditions. (a) Case 1. (b) Case 3.

double-pulse tests. In Case 3, the improved current sharing, due to the enhanced symmetry of parasitic resistance, leads to a substantial reduction in junction temperature differences under power cycling conditions.

The comprehensive statistical analysis of chip junction temperatures is presented in Fig. 15. It is evident that under a 350 A load, the temperature disparity among FRD chips in Case 1 is 24.8 °C, whereas in Case 3, this difference is significantly reduced to 8.1 °C, marking a reduction of over three times in chip junction temperature variation. This more equitable temperature distribution leads to a 7.3 °C decrease in the highest junction temperature for Case 3 compared to Case 1, under identical heat dissipation and load current conditions, which positively impacts the module's reliability and lifespan. Moreover, the variation in junction temperatures of IGBT chips between the two layouts remains minimal under constant current conditions, yet the highest junction temperature of the IGBT in the columnar layout is lowered by 5.8 °C. The column layout effectively mitigates the parasitic differences across individual branches, thereby enhancing the stability of multi-chip junction temperature disparities, particularly for FRD chips, with an improvement exceeding threefold. Additionally, it contributes to a reduction in maximum junction temperature of the module, further bolstering the reliability.

B. Dynamic Thermal Equilibrium Characteristic Evaluation

The DBC layout of Case 3 demonstrates considerable benefits in terms of chip temperature disparities and junction temperatures under constant current loading conditions. However, these conditions only provide a snapshot of the temperature distribution in a steady state.

Consequently, it is imperative to assess the junction temperature distribution under actual inverter operating conditions. The junction temperature testing platform, as illustrated in Fig. 16, features a three-phase, two-level inverter circuit. The module under test is coated with black paint to enhance thermal imaging, and an infrared thermal imaging camera is used to capture the surface junction temperatures of the chips. Pulsewidth modulation waveform modulation is applied to the input current, with the output single-phase current detailed in Fig. 17. To prevent excessively high junction temperatures, a multistage loading method is implemented, which alternates between large and small currents to create a cyclical loading pattern. The maximum equivalent current, as indicated in Fig. 17(b), is set at 400 A. Furthermore, the IGBT operates at a frequency of 6 kHz and a voltage of 400 V.

Fig. 18 presents the temperature distribution under inverter conditions for both the staggered layout and the upper and lower staggered layout. The junction temperature distribution for Case 1 is strikingly similar to that observed under power cycling conditions, with specific temperature values detailed in Figs. 19 and 20. The optimization of the DBC layout has led to a significant balancing of the junction temperatures. In Case 1, with an output of 400 A, the FRD chip junction temperature reaches 127.7 °C, with a maximum temperature difference of 14.2 °C and an imbalance degree of 11.6%. Furthermore, the temperature difference in Case 3 is only 5.8 °C, with an imbalance factor of 4.6%. The junction temperature test results are consistent with the parasitic parameter analysis and dynamic loss analysis. Additionally, taking into account the switching losses under inverter conditions, the total switching loss of the IGBT chips in Case 3 is significantly reduced, leading to a notable decrease in the IGBT junction temperature by 7.5 °C. However, the unevenness of the losses slightly increases, resulting in a

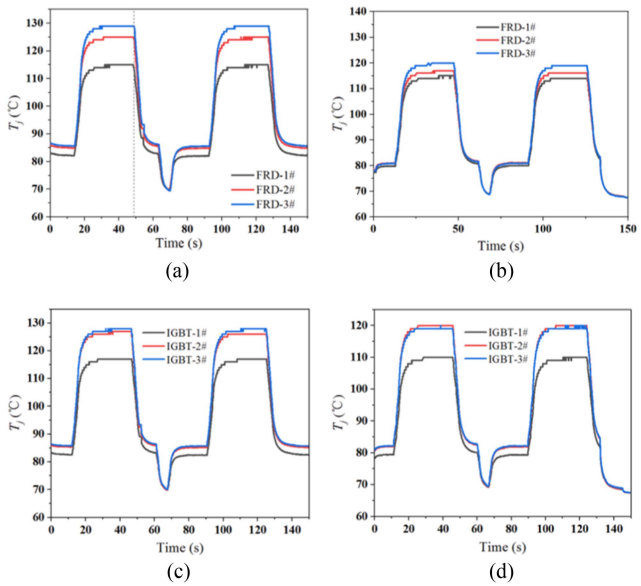


Fig. 19. Temperature rise of FRD and IGBT for (a), (c) Case 1 and (b), (d) Case 3.

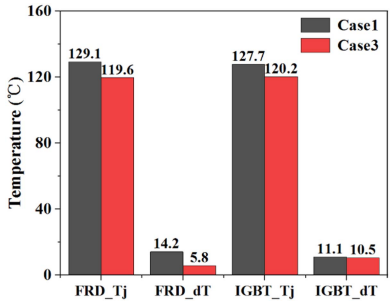


Fig. 20. Junction temperature and difference of chips under Inverter conditions.

junction temperature difference that is comparable to that of Case 1.

VI. Conclusion

In conclusion, this article proposes diverse chip layout structures for multichip parallel IGBT power modules. First, the parasitic balance of each chip is evaluated from the perspectives of DBC layout and current equalization groove design. The current distribution and dynamic losses of each chip are verified through double-pulse experiments, and the temperature distribution of the module under different operating conditions is compared. The bonding wire is identified as a significant source of parasitic parameters in module packaging, and the columnar layout effectively reduces parasitic resistance by approximating symmetrical bonding position distribution across branches. The parasitic imbalance factor for FRD can be reduced by 75.4%. The module with initial DBC layout lacks an optimal current sharing point, and for the sequential DBC layout, current sharing effects of IGBT and FRD change synchronously with the length of the current sharing groove. The design of the sharing groove can optimize the imbalance factor of IGBT parasitic parameters to 5.6% and that of FRD to 4.5%. Under constant current loading conditions, the junction temperature distribution of each chip branch strongly correlates with the parasitic and current imbalance, showing little association with switching losses. Under inverter conditions, the temperature distribution of FRD significantly improves, resulting in a substantial reduction in junction temperature. In summary, the optimized structure proposed in this article significantly enhances the current equalization capability of FRD chips without sacrificing the current equalization of IGBT chips. It can improve the temperature distribution of the module under multiple operating conditions and provide a solution to the current equalization problems faced by the industry.

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