Optimal Switching Pattern Control of the *CLLC* Resonant Converters in Dynamic Processes

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***Abstract*—The *CLLC* resonant converters are preferred for their high-power density and high efficiency. Nevertheless, their dynamic performance deteriorates due to the low impedance characteristic of the resonant tank near resonant frequency. This study proposes optimal switching patterns under specified peak resonant current conditions to enable rapid and smooth dynamic transitions. Building on this, a seamless, synergetic control strategy is developed for integration with the widely used proportional-integral controllers. The efficacy of this methodology is validated on a 2-kW *CLLC* resonant converter prototype, demonstrating zero inrush current and approximately ∼100% increase in the speed of dynamic response compared to existing techniques, across both step load changes and output voltage reference changes. Remarkably, the proposed methodology maintains high performance despite significant electrical component parameter variances, obviating the necessity for supplementary sensors.**

***Index Terms*—*CLLC* resonant converters, dynamic process, optimal switching patterns, zero inrush current.**

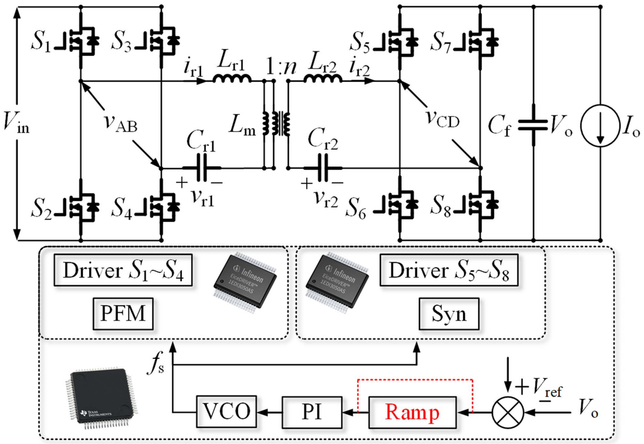

Fig. 1. Topology and typical PFM control of *CLLC* resonant converters.

I. Introduction

THE *CLLC* resonant converters find extensive application in various fields such as data centers [1], [2], [3], dc transformers [4], [5], [6], battery chargers [7], [8], [9], [10], and energy storage systems [11], [12], [13], attributed to their bidirectional power flow capability, inherent zero voltage switching (ZVS) characteristic, and galvanic isolation.

Zung et al. [14] elaborated on the operational mechanics and steady-state analysis of *CLLC* resonant converters, highlighting their significance in steady-state efficiency. On the other hand, dynamic performance is crucial for ensuring stable operation under variable loads, prompt response to transient conditions, and adaptability to a wide spectrum of applications, thereby playing a pivotal role in the overall efficiency, reliability, and lifespan of power electronic systems.

A typical schematic of an output voltage regulated *CLLC* resonant converter is illustrated in Fig. 1, featuring eight power MOSFETs S_1–S_8, resonant inductors and capacitors (L_{r1}, C_{r1} on the primary side and L_{r2}, C_{r2} on the secondary side), a transformer with turn ratio n, and an excitation inductance denoted as L_m. The prevalent control strategy employs pulse frequency modulation (PFM) combined with a proportional-integral (PI) controller, where the discrepancy between the output voltage V_o and the reference voltage V_{ref} is processed by the PI controller. To mitigate abrupt step changes in V_{ref}, a ramp function may be employed, facilitating a smoother transition. A voltage-controlled oscillator (VCO) converts the voltage error into a frequency signal, which is then dispatched to driver circuits on both primary and secondary sides to maintain synchronous rectification through controlled phase alignment of secondary side power MOSFETs [15], [16].

The dynamic performance of *CLLC* resonant converters tends to degrade near the resonant frequency due to the low impedance characteristic of resonant tank within conventional PI controller framework, leading to a tradeoff between regulation duration and resonant current and voltage spikes. To mitigate peak resonant

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TABLE I
CHARACTERISTIC COMPARISON OF DIFFERENT METHODS

	Advantage	Disadvantage
Trajectory control [18], [19], [20]	1) Straightforward, 2) Does not require additional sensors.	1) Complex control. 2) Limited to step load dynamics consideration.
Time-domain model-based method [9], [21], [23]	1) Addresses all potential operational conditions in PFM and PSM. 2) Accounts for both load step change and output voltage dynamics.	Fails to achieve the fastest output voltage step change during dynamic processes.
Constant current control method [22]	Enhances dynamic response in step load change scenarios.	1) Necessitates additional sensors. 2) Limited to step load dynamics consideration.
This work	1) Achieves the maximum output voltage increment under resonant current limit. 2) Does not require additional sensors.	1) Complex control. 2) Slightly performance degrades with significant electrical component parameter mismatches.

currents, a conservative PI parameter setting is often adopted, which invariably extends the regulation period.

A review of methodologies addressing this challenge is summarized in Table I, including early state plane analysis of resonant converters [17], multistep trajectory control for the *LLC* resonant converters [18], [19], [20], and constant resonant current limiting techniques [21]. Enhancements in dynamic performance have been achieved through methods such as sliding mode control [22], constant current control based on state trajectory analysis, and dynamic transition techniques combining PFM with phase shift modulation (PSM) [23].

Previous methodologies predominantly concentrate on the dynamics of load step changes, neglecting variations in output voltage. Moreover, the enhancement of dynamic performance typically necessitates additional sensors for measuring resonant voltages and currents. In practice, resonant parameters are subject to tolerances, necessitating a robust control strategy, particularly in the absence of supplementary sensors for monitoring high-frequency resonant components.

To address this deficiency, this article introduces an approach for achieving a swift and smooth dynamic transition in *CLLC* resonant converters within a specified resonant current range. Following an in-depth steady-state analysis and output voltage increment examination, this study compares the performance of traditional PI controllers, PI controllers with ramp function, and the proposed optimal switching patterns under a defined peak resonant current criterion. An integrated synergetic control algorithm designed for seamless incorporation into existing PI controllers is also presented. The preceding analysis has been empirically substantiated through experimentation with a 2-kW *CLLC* resonant converter prototype. The advantages conferred by the proposed methodology are delineated as follows.

1) Facilitates an increased dynamic under a predefined resonant current limit for both step load variations and output voltage reference adjustments.
2) Eliminates inrush resonant current throughout the dynamic phase, enhancing system robustness.
3) Demonstrates seamless compatibility with the prevalent PI controller architectures, ensuring straightforward adoption in existing frameworks.
4) Delivers consistent performance, albeit moderate, in scenarios characterized by significant mismatches in the electrical parameters of resonant components.

This concise presentation underscores the method efficacy in improving dynamic performance and system reliability, while also highlighting areas of potential performance variability due to component mismatches. The rest of this article is organized as follows. Section II presents a detailed examination of the steady-state analysis alongside the investigation of output voltage variations during dynamic conditions. In Section III, an in-depth analysis of the dynamic behaviors associated with the PI controller, both with and without ramp modifications, is conducted. The determination of optimal switching patterns under a specified peak resonant current threshold is undertaken. The experimental results are discussed in Section IV. Finally, Section V concludes this article.

II. EQUIVALENT CIRCUIT DERIVATION AND ANALYSIS

The literature highlighted in [24] demonstrates that an asymmetric *CLLC* resonant tank can be converted into a symmetric configuration through the reconfiguration of electrical parameters. Given the symmetric nature of the *CLLC* resonant converter, our subsequent analysis focuses on the forward power transfer. In symmetric *CLLC* resonant converters, specific relationships are established, such as $L_{\mathrm{r1}} = n^2 L_{\mathrm{r2}}$, and $C_{\mathrm{r2}} = n^2 C_{\mathrm{r1}}$, and the inductor ratio k is defined as $k = L_{\mathrm{m}}/L_{\mathrm{r1}}$. The input voltage and output voltage of the *CLLC* system are denoted as V_{in} and V_{o}, respectively, with the reflected output voltage expressed as $V_{\mathrm{o}}' = V_{\mathrm{o}}/n$. The voltage gain M of the *CLLC* is defined as $M = V_{\mathrm{o}}'/V_{\mathrm{in}}$. The load is modeled as a constant current source I_{o}, while the primary and secondary resonant currents are labeled i_{r1} and i_{r2}, respectively. The excitation current is denoted as i_{m}. The voltages across the primary and secondary resonant capacitors are represented as v_{r1} and v_{r2}, respectively. Additionally, the voltages across the ac terminals of the primary and secondary full-bridge circuits are denoted as v_{AB} and v_{CD}, respectively.

A. *Operation Stages in Steady-State Operation*

The equivalent circuit of the *CLLC* resonant tank is depicted in Fig. 2. Typically, the secondary bridge operates in synchronized rectifier mode. In the case of a PFM modulated *CLLC*, both the input and output voltages of the resonant tank manifest as square waves. The equivalent switch S_0 is employed to indicate the output connection status. Specifically, when $S_0 = 1$, $v_{\mathrm{CD}} = V_{\mathrm{o}}$, S_5 and S_8 conduct; When $S_0 = 1$, $v_{\mathrm{CD}} = -V_{\mathrm{o}}$, S_6 and S_7 conduct; When $S_0 = 0$, S_6–S_8 are all cutoff. The steady state operation of the *CLLC* can be categorized into six stages within half switching cycles based on the values of v_{AB}, v_{CD}, and S_0.

To streamline the analysis, normalization is employed, and the base values are specified as

$$V_{\mathrm{Base}} = V_{\mathrm{in}}, Z_{\mathrm{Base}} = \sqrt{\frac{L_{\mathrm{r1}}}{C_{\mathrm{r1}}}}, I_{\mathrm{Base}} = \frac{V_{\mathrm{Base}}}{Z_{\mathrm{Base}}}$$

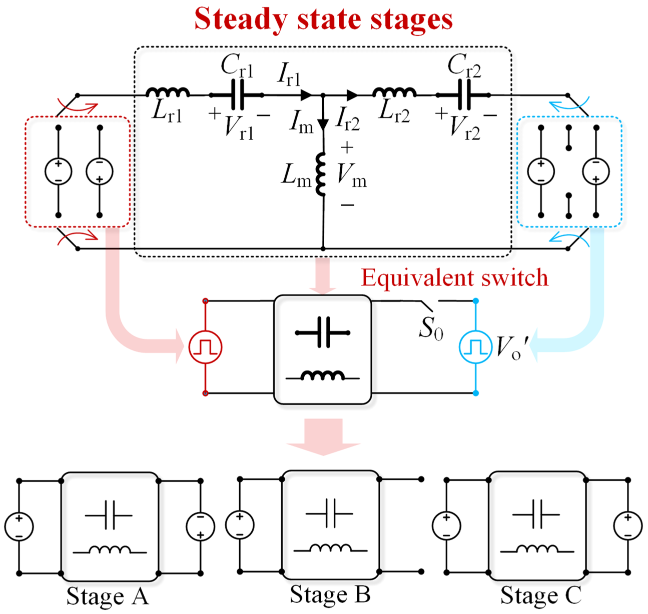

Fig. 2. Steady state equivalent circuit of the *CLLC* resonant tank, and three stages in one positive half switching cycle.

$$f_{\mathrm{Base}}=\frac{1}{2\pi\sqrt{L_{\mathrm{r1}}C_{\mathrm{r1}}}},\theta_{\mathrm{Base}}=2\pi f_{\mathrm{Base}}t. \tag{1}$$

Capital letters signify these normalized variables, with all electrical variables being time-dependent functions of θ.

Regarding stages A and C, we can derive the following set of constant coefficient original differential equations (ODEs):

$$\begin{cases} k\left(I'_{\mathrm{r1X}}(\theta)-I'_{\mathrm{r2X}}(\theta)\right)+I'_{\mathrm{r1X}}(\theta)+V_{\mathrm{r1X}}(\theta)=1\\ k\left(I'_{\mathrm{r1X}}(\theta)-I'_{\mathrm{r2X}}(\theta)\right)-I'_{\mathrm{r2X}}(\theta)-V_{\mathrm{r2X}}(\theta)=\{-M,M\}\\ I_{\mathrm{r1X}}(\theta)=V'_{\mathrm{r1X}}(\theta)\\ I_{\mathrm{r2X}}(\theta)=V'_{\mathrm{r2X}}(\theta)\end{cases} \tag{2}$$

and the general solution is given as

$$\begin{bmatrix} I_{\mathrm{r1X}}(\theta)\\ I_{\mathrm{r2X}}(\theta)\\ I_{\mathrm{mX}}(\theta)\\ V_{\mathrm{r1X}}(\theta)\\ V_{\mathrm{r2X}}(\theta)\end{bmatrix}=\mathbf{A}_{\mathrm{X}}\begin{bmatrix}\cos(\theta)\\ \sin(\theta)\\ \cos(k_1\theta)\\ \sin(k_1\theta)\end{bmatrix}+\begin{bmatrix}0\\0\\0\\1\\ \mp M\end{bmatrix} \tag{3}$$

$$\mathbf{A}_{\mathrm{X}}=$$

$$\begin{bmatrix} \frac{c_{1\mathrm{X}}+c_{2\mathrm{X}}}{2} & -\frac{c_{3\mathrm{X}}+c_{4\mathrm{X}}}{2} & \frac{c_{1\mathrm{X}}-c_{2\mathrm{X}}}{2} & \frac{k_1(c_{4\mathrm{X}}-c_{3\mathrm{X}})}{2}\\ \frac{c_{1\mathrm{X}}+c_{2\mathrm{X}}}{2} & -\frac{c_{3\mathrm{X}}+c_{4\mathrm{X}}}{2} & \frac{c_{2\mathrm{X}}-c_{1\mathrm{X}}}{2} & \frac{k_1(c_{3\mathrm{X}}-c_{4\mathrm{X}})}{2}\\ 0 & 0 & \frac{c_{1\mathrm{X}}-c_{2\mathrm{X}}}{2} & \frac{-k_1(c_{3\mathrm{X}}+c_{4\mathrm{X}})}{2}\\ \frac{c_{3\mathrm{X}}+c_{4\mathrm{X}}}{2} & \frac{c_{1\mathrm{X}}+c_{2\mathrm{X}}}{2} & \frac{k_1(c_{3\mathrm{X}}-c_{4\mathrm{X}})}{2} & \frac{c_{1\mathrm{X}}-c_{2\mathrm{X}}}{2k_1}\\ \frac{c_{3\mathrm{X}}+c_{4\mathrm{X}}}{2} & \frac{c_{1\mathrm{X}}+c_{2\mathrm{X}}}{2} & \frac{k_1(c_{4\mathrm{X}}-c_{3\mathrm{X}})}{2} & \frac{c_{2\mathrm{X}}-c_{1\mathrm{X}}}{2k_1}\end{bmatrix}. \tag{4}$$

In (3) and (4), each electrical variable incorporates two resonant frequencies, and there are four coefficients $c_{1\mathrm{X}}$–$c_{4\mathrm{X}}$ (X = A or C) to be determined.

Stage B differs from stages A/C as the output side constitutes an open circuit, resulting in only one resonant frequency in the resonant tank. The general solution for stage B is provided as

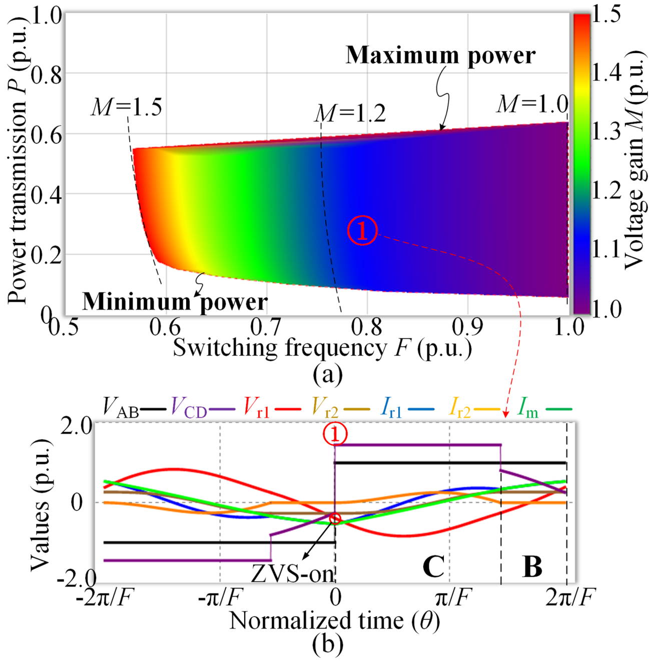

Fig. 3. (a) Two-dimensional density plot of the relation interplay among F, P, and M in CB sequence of the *CLLC* resonant converters, where the dashed lines illustrate the contour lines of voltage gain M. (b) Typical waveform in sequence CB.

$$\begin{bmatrix} I_{\mathrm{r1B}}(\theta)\\ I_{\mathrm{r2B}}(\theta)\\ I_{\mathrm{mB}}(\theta)\\ V_{\mathrm{r1B}}(\theta)\\ V_{\mathrm{r2B}}(\theta)\end{bmatrix}=\begin{bmatrix} c_{1\mathrm{B}} & -c_{2\mathrm{B}}\\ 0 & 0\\ c_{1\mathrm{B}} & -c_{2\mathrm{B}}\\ c_{2\mathrm{B}} & -c_{1\mathrm{B}}\\ 0 & 0\end{bmatrix}\begin{bmatrix}\cos(k_2\theta)\\ \sin(k_2\theta)\end{bmatrix}+\begin{bmatrix}0\\0\\0\\1\\ V_{\mathrm{r2B}}(0)\end{bmatrix} \tag{5}$$

where $c_{1\mathrm{B}}$ and $c_{2\mathrm{B}}$ are two coefficients to be determined, and $V_{\mathrm{r2B}}(0)$ is the initial value of the secondary side resonant voltage.

The frequency coefficients k_1 and k_2 are given as

$$k_1=\sqrt{\frac{1}{1+2k}},\quad k_2=\sqrt{\frac{1}{1+k}}. \tag{6}$$

Each stage has its constraint conditions. As for stages A–C, the constraint condition can be expressed as

$$\forall\theta\in[0,\theta_{\mathrm{A}}]:I_{\mathrm{r1A}}(\theta)\le I_{\mathrm{mA}}(\theta)\leftrightarrow I_{\mathrm{r2A}}(\theta)\le 0 \tag{7}$$

$$\forall\theta\in[0,\theta_{\mathrm{B}}]:\left|\left(k_2^2-1\right)\left(V_{\mathrm{r1B}}(\theta)-1\right)-V_{\mathrm{r2B}}(\theta)\right|\le M \tag{8}$$

$$\forall\theta\in[0,\theta_{\mathrm{C}}]:I_{\mathrm{r1C}}(\theta)\ge I_{\mathrm{mC}}(\theta)\leftrightarrow I_{\mathrm{r2C}}(\theta)\ge 0. \tag{9}$$

The operation sequence of the *CLLC* resonant converter within a half-switching cycle is delineated through a concatenation of various stages. The typical operation sequences of *CLLC* resonant converters, as outlined in PFM, include C, CB, BCB, CBA, CA, and AC [24], [25], [26]. Within these, the CB sequence is often favored due to its extensive range of power transmission and voltage regulation, inherent ZVS on capability, and the simplicity of integrating synchronous rectification. The interplay among F, P, and M in CB sequence is illustrated in Fig. 3. This sequence is demarcated by boundaries of maximum and minimum power. In Fig. 3(a), dashed lines illustrate the

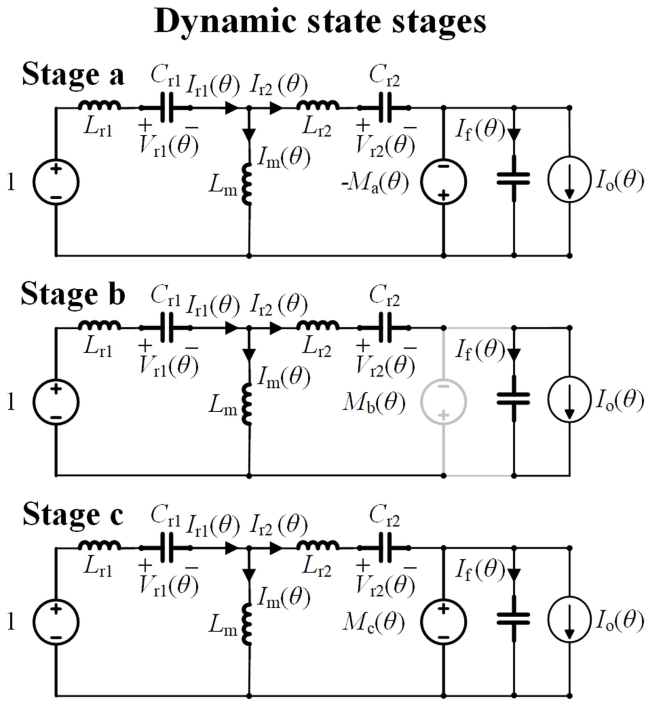

Fig. 4. Equivalent circuits transitioning from stage a to stage c in dynamic processes.

contour lines of voltage gain *M*. Fig. 3(b) presents four representative waveforms, labeled 1 through 4, where the black, purple, red, brown, blue, orange, and green lines correspond to V_{AB}, V_{CD}, V_{r1}, V_{r2}, I_{r1}, I_{r2}, and I_m, respectively.

The steady-state operational behavior of the *CLLC* resonant converter is encapsulated by an implicit function $\boldsymbol{f}(.) = \boldsymbol{f}(k, F, M, P) = 0$. During the positive half-cycle of the switching period, the terminal values of each resonant variable are the inverse of their initial values, establishing a symmetrical operational framework [27], [28].

B. Output Voltage Increment in Dynamic Processes

During the dynamic process, the voltage gain *M* manifests as a time-variant function, symbolized by θ. Regrettably, a closed-form expression for the electrical variables under these conditions remains elusive. To surmount this challenge, a simplification approach is adopted, predicated on the premise that the time constant of the resonant tank (ordinarily within μs range) is markedly less than the time constant of the output capacitor (customarily spanning in ms range). This assumption permits the presumption that the output voltage remains stable throughout a single switching cycle. In the dynamic sequence, corresponding to stages A–C, the equivalent circuits transitioning from stage a to stage c are delineated in Fig. 4. The voltage gains in different stages are represented as $M_a(\theta) \sim M_c(\theta)$, while the output current source is denoted as $I_o(\theta)$.

Taking stage c as an illustrative case, the relationship between $I_o(\theta)$ and $M_c(\theta)$ can be expressed as

$$I_o(\theta) = gM_c(\theta). \tag{10}$$

The energy transfer leads to an incremental output voltage dM_c, which can be expressed as

$$\begin{aligned} dM_c &= \\ &\int_0^{\theta_c} c\left(I_{r2C}(\theta) - gM_c(\theta)\right) d\theta \approx \int_0^{\theta_c} c\left(I_{r2C}(\theta) - gM\right) d\theta \\ &= \frac{c}{2} \\ &\left(\begin{array}{l} (c_{3C} + c_{4C})\cos(\theta_c) + (c_{1C} + c_{2C})\sin(\theta_c) \\ -(c_{3C} - c_{4C})\cos(k_1\theta_c) - k_1(c_{1C} - c_{2C})\sin(k_1\theta_c) \\ -2(c_{4C} + gM\theta_c) \end{array}\right) \end{aligned} \tag{11}$$

where *c* and *g* are the output capacitor and load coefficients, respectively. A higher value of *c* indicates a smaller output capacitor, while a higher value of *g* indicates a heavier load.

The expressions for the output voltage increments in stages a and b are provided as

$$\begin{aligned} dM_a &= \int_0^{\theta_a} c\left(-I_{r2a}(\theta) - gM_a(\theta)\right) d\theta \\ &\approx \int_0^{\theta_a} c\left(-I_{r2a}(\theta) - gM\right) d\theta \\ &= \frac{c}{2} \\ &\left(\begin{array}{l} -(c_{3A} + c_{4A})\cos(\theta_a) - (c_{1A} + c_{2A})\sin(\theta_a) \\ +(c_{3A} - c_{4A})\cos(k_1\theta_a) + k_1(c_{1A} - c_{2A})\sin(k_1\theta_a) \\ +2(c_{4A} - gM\theta_a) \end{array}\right) \end{aligned}$$

$$dM_b = \int_0^{\theta_b} c\left(-gM_b(\theta)\right) d\theta \approx -cgM\theta_b. \tag{12}$$

Within a single switching cycle, the increment in output voltage, symbolized as dM, is constituted by the sum of dM_a, dM_b, and dM_c. Given the direct proportionality of dM_a, dM_b, and dM_c to the output capacitor coefficient *c*, it consequently follows that dM also exhibits a proportional relationship to *c*.

For a *CLLC* resonant converter with $k = 6$, the interrelation among dM and M, g, I_{Peak} is depicted in Fig. 5. The dashed line within the figure represents $dM = 0$. At a certain I_{Peak}, a condition where $dM > 0$ indicates the output capacitor is in the process of charging, whereas $dM < 0$ denotes its discharging phase. The value of dM escalates with an increase in I_{Peak} but diminishes with a higher *g*. Under a no-load scenario, wherein $g = 0$, dM maintains a constant value, showing no dependency on *M*.

In conclusion, the dynamic operational behavior of the *CLLC* resonant converter can be encapsulated by an implicit function: $\boldsymbol{g}(.) = \boldsymbol{g}(k, F, M, g, c) = 0$. The numerical resolution of $\boldsymbol{g}(.) = 0$ facilitates the determination of both dM and I_{Peak}, providing insights into the converter performance under dynamic conditions.

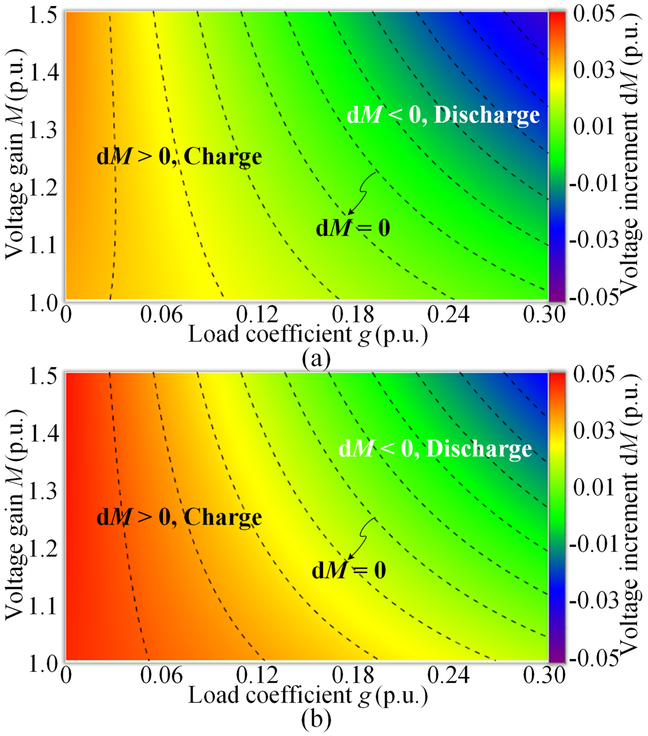

Fig. 5. Interrelation among output voltage increment dM, voltage gain M, load coefficient g, and peak resonant current I_{Peak} for a *CLLC* resonant converter with inductor ratio $k = 6$. (a) $I_{\mathrm{Peak}} = 0.6$. (b) $I_{\mathrm{Peak}} = 0.8$.

III. Optimal Switching Patterns Derivation

A. Description of the Dynamics Process

When the input voltage of the *CLLC* resonant converter remains constant, the dynamic processes can primarily be categorized into load dynamics (indicated by step changes in the load coefficient g) and output voltage dynamics (reflected by step changes in the output voltage reference M_{ref}). It is pertinent to observe that each data point in Fig. 5 is associated with a distinct switching frequency F. As for a given $k = 6$, and $c = 0.03$, the relation of load coefficient g, voltage gain M, I_{Peak}, and F are depicted in Fig. 6(a), where the shaded red, green, and blue regions denote three cases with $g = 0.20$, $M = 1.2$, and $I_{\mathrm{Peak}} = 0.6$. In Fig. 6(b), where the load resistance is a constant, a higher M corresponds to a higher I_{Peak}. In Fig. 6(c) when M is determined, I_{Peak} increases with the increase of g. However, the variation of F is very narrow. On comparison of Fig. 6(c) and (d), it can be inferred that I_{Peak} is almost linearly proportional to g when M is a constant. This indicates that the *CLLC* resonant converter is insensitive to load step change. Upon a load step increase, I_{Peak} linearly rises, yet the control variable (switching frequency F) exhibits minimal variation. In contrast, F demonstrates sensitivity to the variations in both M and g, suggesting that the *CLLC* resonant converter exhibits greater sensitivity during output voltage dynamic processes.

The methodology for deriving the switching pattern during dynamic processes is outlined in Fig. 7. Initially, key parameters such as the inductor ratio k, output capacitor coefficient c, and

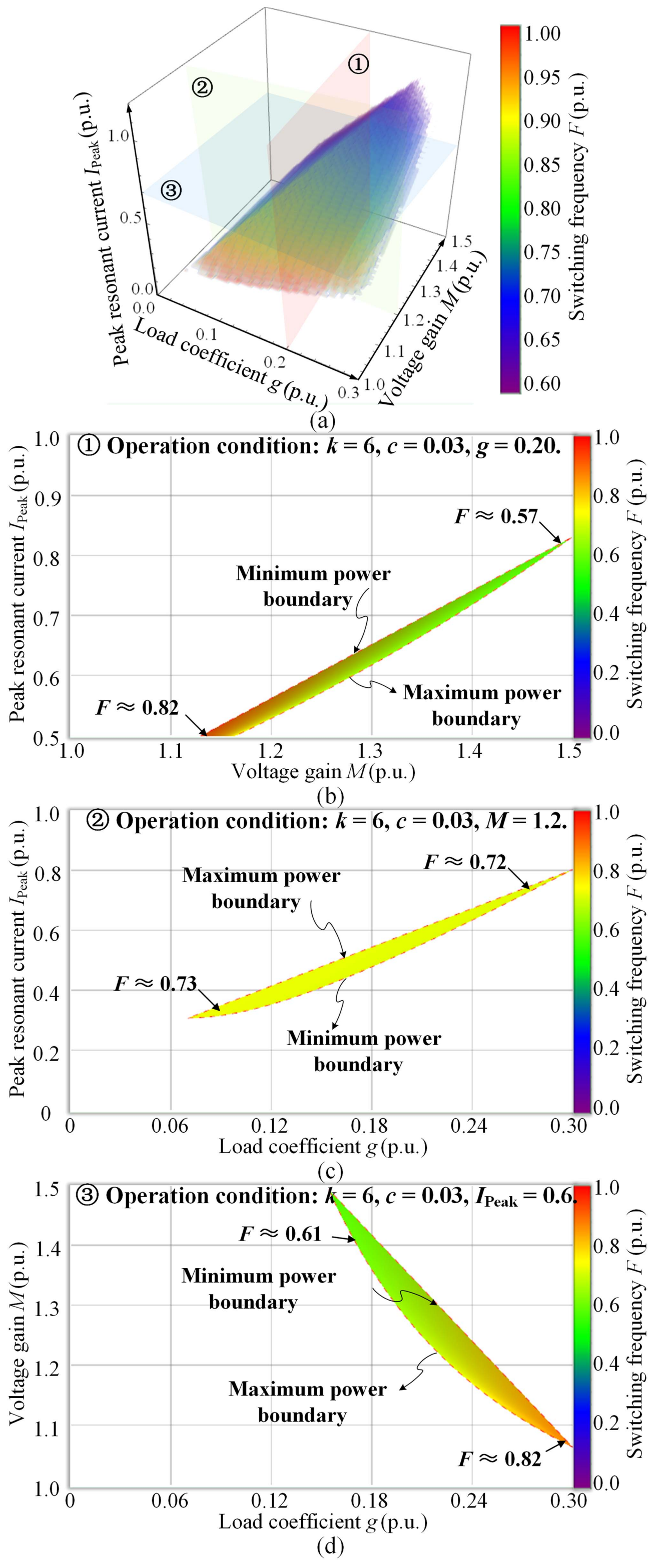

Fig. 6. (a) The Relation of g, M, I_{Peak}, and F for a *CLLC* resonant converter with $k = 6$, $c = 0.03$. (b) Two-dimensional density plot elucidating the correlations between F, M, and I_{Peak} when $g = 0.20$. (c) Two-dimensional density plot elucidating the correlations between F, g, and I_{Peak} when $M = 1.2$. (d) Two-dimensional density plot elucidating the correlations between F, g, and M when $I_{\mathrm{Peak}} = 0.6$.

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Switching Patterns with Constraints in Dynamic Process
    Electrical parameter normalization: $k$, $c$, $V_{Base}$, $I_{Base}$, $Z_{Base}$, $f_{Base}$.
    Initialization: $M \leftarrow M_{Init}$, $g \leftarrow g_{Init}$.
    Determine the operation sequence;
    Solving ODEs in sequence CB with constraints via (2)~(5);
    Check the operation conditions in stage C and B;
    $I_{r10} \leftarrow -I_{r1}(\theta_b)$, $I_{r20} \leftarrow -I_{r2}(\theta_b)$, $V_{r10} \leftarrow -V_{r1}(\theta_b)$, $V_{r20} \leftarrow -V_{r2}(\theta_b)$.
repeat
    Operation condition: $M_{ref}$, $g$.
    // Iterative solving ODEs in sequence CB until $M$ reaches $M_{ref}$
    Check the operation conditions;
    // Save the end electrical qualities
    $I_{r10} \leftarrow -I_{r1}(\theta_b)$, $I_{r20} \leftarrow -I_{r2}(\theta_b)$, $V_{r10} \leftarrow -V_{r1}(\theta_b)$, $V_{r20} \leftarrow -V_{r2}(\theta_b)$.
    //Calculate $dM$ via (10)~(12);
    $dM = dM_c + dM_b$, $M \leftarrow M + dM$.
    Record the switching frequency $F$ and the voltage gain $M$.
until $M = M_{ref}$
Output :
    1) The switching frequency trajectory ($F_1$, $F_2$,..., $F_N$).
    2) The output voltage trajectory ($M_1$, $M_2$,..., $M_N$).
    Input: ($k$, $c$, $g$, $I_{Peak}$, $M_{Init}$, $M_{ref}$)
    Output: ({$F_1$, $M_1$}, {$F_2$, $M_2$},..,{$F_N$, $M_N$})
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Fig. 7. Flowchart of deriving switching patterns during dynamic processes.

the base values are established based on the specifications of the *CLLC* resonant tank. Subsequently, given an initial condition characterized by an initial voltage gain M_{Init} and an initial load coefficient g_{Init}, the initial steady-state operation data of the converter is ascertained by solving the ODEs in CB sequence. This involves verifying constraint conditions and preserving the terminal values of resonant variables as the initial conditions for the subsequent switching cycle. In scenarios where there is a change in M_{ref} or g, mathematical representation of the ODEs undergoes modification. During the iterative computation phase, the output voltage increment, dM is determined following the resolution of the ODEs. Subsequently, the switching frequency F and the voltage gain M are recorded until M reaches M_{ref}. The culmination of this process yields the switching frequency trajectory $(F_1, F_2, \ldots, F_{\text{N}})$, as well as the output voltage trajectory $(M_1, M_2, \ldots, M_{\text{N}})$, facilitating comprehensive analysis and optimization of the converter dynamic performance.

After executing the diagram in Fig. 7, the trajectory ({F_1, M_1}, {F_2, M_2}, .., {F_{N}, M_{N}}) corresponds to specific operating conditions (k, c, g, I_{Peak}, M_{Init}, M_{ref}) is obtained. When operating conditions change, the trajectory changes as well. To prepare training data, the process in Fig. 7 is iteratively executed with the variables k, c, g, I_{Peak} M_{Init}, and M_{ref}. The ranges for these variables are: $k = [2{:}1{:}10]$, $c = [0.01{:}0.01{:}0.1]$, $g = [0{:}0.01{:}0.1]$, $I_{\text{Peak}} = [0.4{:}0.1{:}1.4]$, $M_{\text{Init}} = [1.0{:}0.05{:}1.6]$, and $M_{\text{ref}} = [1.0{:}0.01{:}\max(M_{\text{Init}}, 2.0)]$. This data preparation process takes around 7.3 h to iteratively solve the ODEs.

For artificial neural network (ANN) training, the data structure is modified. For real-time execution, the input data should be the sampled or calculated values, and the output data should be the switching frequency. Thus, the input data is (k, c, g, I_{Peak}, M), and the output data is the switching frequency f_{s}. This restructured dataset, consisting of 967 508 data points, is created by modifying the *F*/*M* pairs in the switching sequence.

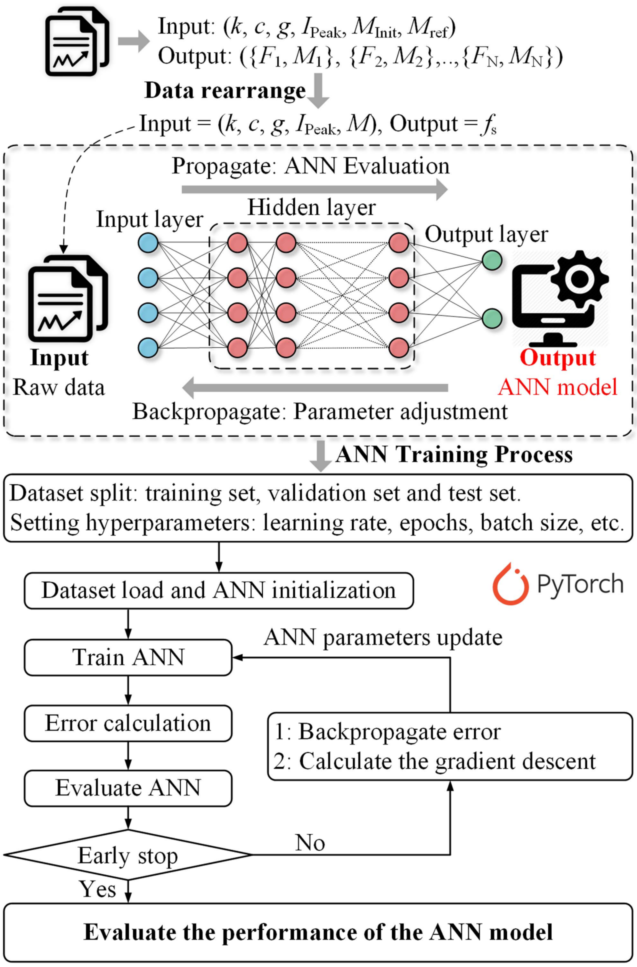


Fig. 8. Data reconstruction and ANN training process.

The training process of the ANN is shown in Fig. 8. The original dataset is shuffled and split into three sets: 70% for training, 20% for testing, and 10% for validation. The Adam optimizer with an initial learning rate of 0.01 is used. Training occurs over 1000 epochs, with the learning rate reduced by a factor of 10 every 100 epochs. The batch size is set to 64, and the model is trained using the PyTorch framework [29].

First, the dataset is loaded, and the ANN is initialized with weights and biases randomized using Gaussian initialization to achieve zero mean and controlled variance. The ANN consists of input, hidden, and output layers. Data is normalized with min-max normalization to ensure values are within the range [0, 1]. Each hidden layer uses the tanh activation function. The difference between ANN predictions and actual outputs is calculated as the error, with mean square error used as the loss function. The error is backpropagated to update the weights and biases through gradient descent. This process is repeated for the predefined number of epochs or until convergence. Validation is used to prevent overfitting, and the test set assesses final model performance [30].

Increasing the number of layers and neurons can enhance prediction accuracy but also increases computation time. Considering the problem size and available computational resources on a digital signal processor (DSP), a single-layer ANN with 12

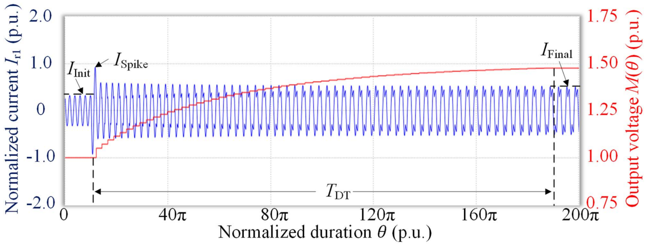


Fig. 9. Typical waveforms during the dynamic process of the PI controller.

neurons is used for this multivariable fitting problem. The mean absolute percentage error on the test set is 0.13%, demonstrating high predictive accuracy.

B. Dynamic Process in PI Controller

The typical waveforms observed during the dynamic process of the PI controller are illustrated in Fig. 9, where the red and blue lines represent $I_{\rm r1}$ and M, respectively. The steady-state peak resonant current is indicated as $I_{\rm Init}$, and the magnitude of the resonant current spike is labeled as $I_{\rm Spike}$. The normalized dynamic transition duration is expressed as $T_{\rm DT}$.

As for a PI controller based *CLLC* resonant converter, where the output voltage $V_{\rm o}$ serves as the feedback variable, and the switching frequency $f_{\rm s}$ is derived as

$$\begin{cases} e(k) = V_{\rm o}(k) - V_{\rm oref} \\ \Delta f_{\rm s}(k) = k_{\rm p}(e(k) - e(k-1)) + k_{\rm i} e(k) \\ f_{\rm s}(k) = f_{\rm s}(k-1) + \Delta f_{\rm s}(k) \end{cases}$$

$$\Rightarrow \begin{cases} M(k) = M(k-1) + {\rm d}M \\ e(k) = M(k) - M_{\rm ref} \\ F(k) = F(k-1) + k'_{\rm p}(e(k) - e(k-1)) + k'_{\rm i} e(k) \end{cases} \tag{13}$$

where $k_{\rm p}$, $k_{\rm i}$ are the control parameters of the converter, and $k'_{\rm p}$, $k'_{\rm i}$ are the corresponding normalized control parameters.

By applying (13) in the iterative computation outlined in the flowchart, the cycle-by-cycle operational waveforms for the *CLLC* resonant tank are derived. Illustratively, considering a step change in the output voltage reference, the dynamic process is influenced by factors such as $k'_{\rm p}$, $k'_{\rm i}$, $M_{\rm Init}$, $M_{\rm ref}$, g, and c. Fig. 10 showcases typical resonant waveforms along with variations in the normalized switching frequency F, and the output voltage M. From this analysis, several key insights emerge.

1) The occurrence of a resonant current spike during the dynamic process is a common phenomenon under a traditional PI controller configuration. To mitigate the amplitude of this spike, it is advisable to fine-tune the PI controller parameters according to the specific operational conditions.
2) In lighter load conditions, the resonant current spike can be diminished within identical operational contexts.
3) The resonant current spike $I_{\rm Spike}$ typically manifests only during the initial switching cycles of the dynamic process.

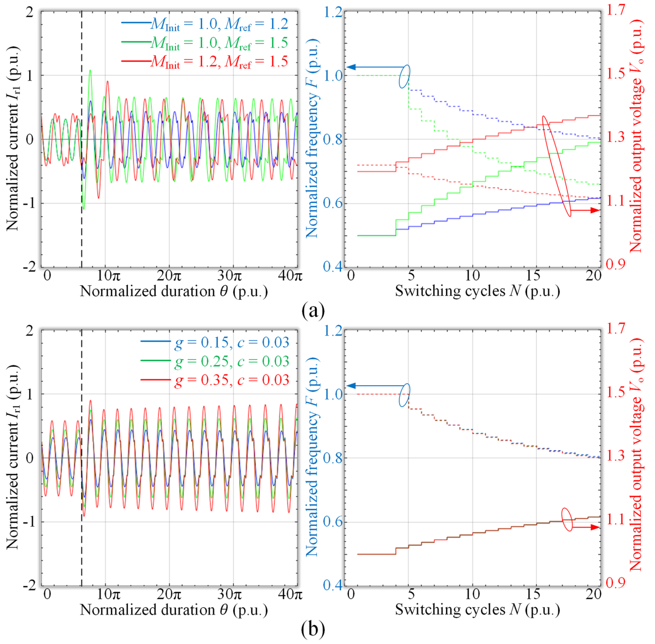


Fig. 10. Typical resonant waveforms of the conventional PI controller along with variations in F, and M in the dynamic process. (a) Impact of $M_{\rm Init}$ and $M_{\rm ref}$. (b) Impact of g.

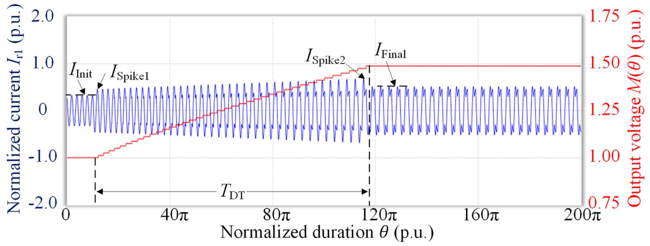


Fig. 11. Typical waveforms during the dynamic process of the PI controller with a ramp.

C. Dynamic Process in PI Controller With Ramp

To mitigate $I_{\rm Spike}$ while concurrently achieving a reduced $T_{\rm DT}$, employing a ramp during an output voltage reference step change presents a logical approach [c.f., Fig. 1]. Fig. 11 illustrates the typical waveforms during the dynamic process with a PI controller with a ramp function. Under these circumstances, the voltage gain follows a ramp profile, leading to the occurrence of two distinct resonant current spikes ($I_{\rm Spike1}$ and $I_{\rm Spike2}$). When compared with a standard PI controller setup, the implementation of a ramp results in significant reductions in both $I_{\rm Spike}$ and $T_{\rm DT}$, demonstrating the effectiveness of this strategy in enhancing the dynamic response of the system.

The switching frequency $f_{\rm s}$ in this condition is calculated as

$$\begin{cases} e(k) = V_{\rm o}(k) - V_{\rm oref}(k) \\ \Delta f_{\rm s}(k) = k_{\rm p}(e(k) - e(k-1)) + k_{\rm i} e(k) \\ V_{\rm oref}(k) = V_{\rm oref}(k-1) + dV_{\rm oref} \\ f_{\rm s}(k) = f_{\rm s}(k-1) + \Delta f_{\rm s}(k) \end{cases}$$

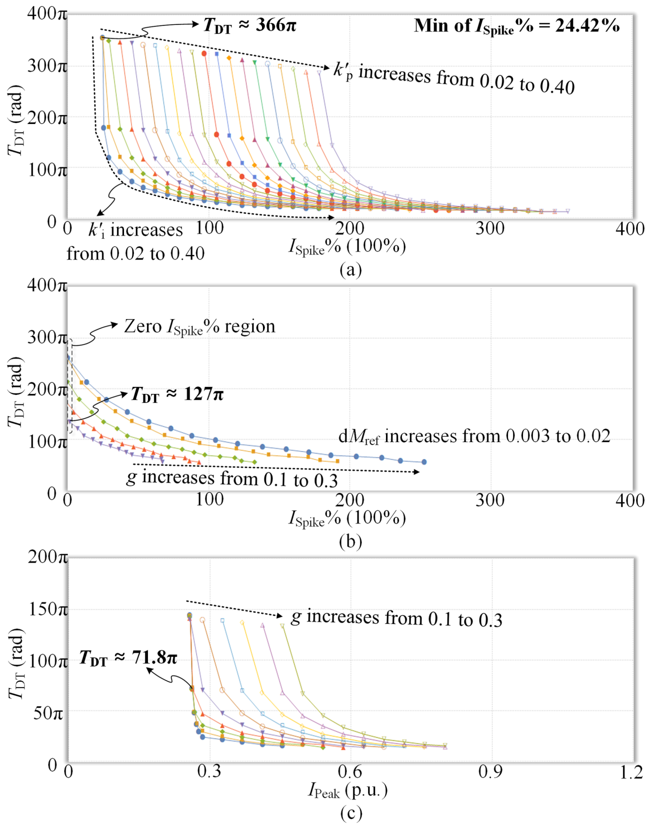


Fig. 12. Resonant current spike versus the total dynamic transition. (a) PI controller scenario when $I_{\mathrm{Peak}} = 0.25$ and $g = 0.1$. (b) PI controller with ramp scenario when $I_{\mathrm{Peak}} = 0.25$. (c) Proposed method.

$$\Rightarrow \begin{cases} M(k) = M(k-1) + \mathrm{d}M \\ e(k) = M(k) - M_{\mathrm{ref}}(k) \\ M_{\mathrm{ref}}(k) = M_{\mathrm{ref}}(k-1) + dM_{\mathrm{ref}} \\ F(k) = F(k-1) + k'_{\mathrm{p}}(e(k) - e(k-1)) + k'_{\mathrm{i}}e(k). \end{cases} \tag{14}$$

When k'_{p}, k'_{i}, and $\mathrm{d}M_{\mathrm{ref}}$ are well tuned to ensure the output voltage tracks the output voltage reference, (14) can be simplified to

$$M(k) = M(k-1) + \mathrm{d}M = M_{\mathrm{ref}}(k-1) + dM_{\mathrm{ref}}. \tag{15}$$

The corresponding $F(k)$ can be solved from $\boldsymbol{g}(.) = 0$.

Fig. 12 shows the resonant current spike versus total dynamic transition for the PI controller and PI controller with ramp under different conditions. In this figure, the x-axis represents the normalized current spike $I_{\mathrm{Spike}}\%$, and the y-axis represents the total dynamic transition duration T_{DT}. When conservative PI parameters (i.e., small values of k'_{p} and k'_{i}) are selected, $I_{\mathrm{Spike}}\%$ can be reduced, but this results in an increased T_{DT}. The trends of k'_{p} and k'_{i} are shown as different lines in these figures. Compared to k'_{p}, k'_{i} can achieve a reduced T_{DT} for a given $I_{\mathrm{Spike}}\%$. The minimum $I_{\mathrm{Spike}}\%$ observed, when k'_{p} and k'_{i} range from 0.02 to 0.40, is 24.42%, indicating that PI controllers are unable to achieve a smooth transition without resonant current spikes.

For PI controllers with a ramp, three parameters need to be adjusted: k'_{p}, k'_{i}, and $\mathrm{d}M_{\mathrm{ref}}$. In this scenario, larger values of k'_{p} and k'_{i} can be chosen when an appropriate value of $\mathrm{d}M_{\mathrm{ref}}$ is selected. Fig. 12(b) shows the trends of $\mathrm{d}M_{\mathrm{ref}}$ under different load conditions with k'_{p} and k'_{i} both set to 0.10. There is a region with zero $I_{\mathrm{Spike}}\%$ for each operating condition. When $\mathrm{d}M_{\mathrm{ref}}$ is smaller than a critical value, $I_{\mathrm{Spike}}\%$ becomes zero, indicating the absence of resonant current spikes. Further reduction in $\mathrm{d}M_{\mathrm{ref}}$ only increases T_{DT}.

Since the proposed method effectively eliminates current spikes, the x-axis in Fig. 12(c) represents the peak current I_{Peak}. In this case, T_{DT} is a function of both I_{Peak} and the load condition g. A higher peak current and a lighter load result in a shorter T_{DT}, though the relationship is nonlinear. Three typical comparison cases are highlighted where $I_{\mathrm{Peak}} = 0.25$ and $g = 0.1$, with their corresponding T_{DT} indicated. For the PI controller method, $T_{\mathrm{DT}} \approx 366\pi$ is needed to achieve a relatively low $I_{\mathrm{Spike}}\%$. With PI controllers using the ramp method, T_{DT} in the zero $I_{\mathrm{Spike}}\%$ region when $g = 0.1$ is approximately 127π. In contrast, the proposed method achieves $T_{\mathrm{DT}} \approx 71.8\pi$ under the same operating conditions. This comparison demonstrates that the proposed method outperforms the other two methods in terms of T_{DT} under the same conditions and constraints.

D. Optimal Switching Patterns

Analysis from Figs. 9–11 reveals that the PI controller alone is insufficient for a smooth dynamic transition devoid of resonant current spikes, primarily due to the lack of control over the resonant current. By integrating a peak resonant current limitation within each switching cycle, both the output voltage increment dM and the corresponding switching frequency F can be accurately determined. Fig. 13 showcases typical resonant waveforms alongside variations in F and M, illustrating that with a predefined I_{Peak}, the transition process can be effectively managed to prevent resonant current spikes. To adhere to the peak resonant current constraint, it emerges that the switching frequency F depends on a set of parameters (k, I_{Peak}, M, g, c).

E. Synergetic Control and Implementation

The core algorithm of this methodology is outlined in Fig. 14, where the control diagram is segmented into the steady-state control part (illustrated in black) and the transient control part (depicted in red). $V_{\mathrm{o}}(k)$, $V_{\mathrm{ref}}(k)$, and $I_{\mathrm{o}}(k)$ represent the kth step sampled output voltage, reference output voltage, and output current, respectively. V_{oerr}, and I_{oerr} denote the predefined output voltage error and output current error thresholds. In a steady-state condition, characterized by $(|V_{\mathrm{o}}(k) - V_{\mathrm{ref}}(k)| < V_{\mathrm{oerr}})$ && $(|I_{\mathrm{o}}(k) - I_{\mathrm{o}}(k-1)| < I_{\mathrm{oerr}})$, only the output voltage V_{o} is sampled and compared against V_{ref}. The error is sent to a PI controller and a VCO, the output signal of the VCO is the switching frequency f_{s}. According to the PFM modulation and synchronous rectification control, the driver signals for S_1–S_4 in the primary inverter bridge and S_5–S_8 in the secondary synchronous rectification bridge are obtained. When the steady-state condition is not satisfied, the switching frequency of the next cycle is calculated via the programmed ANN. Subsequently,

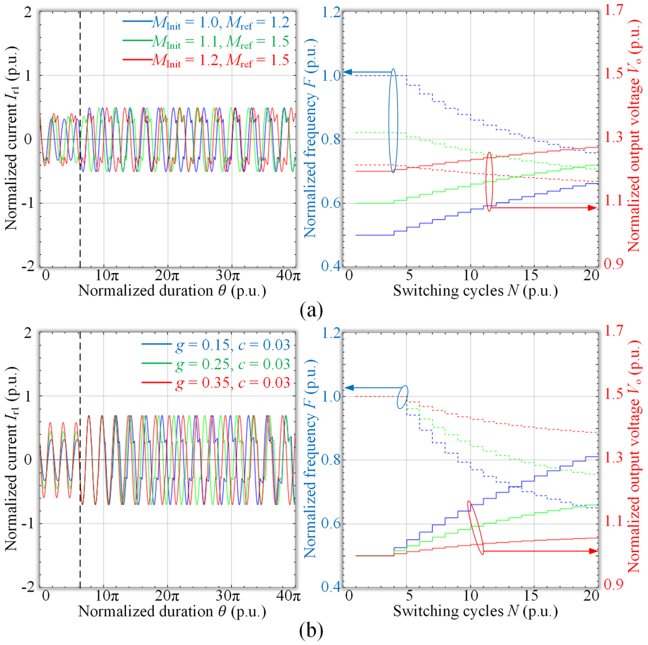


Fig. 13. Typical resonant waveforms of the proposed optimal switching patterns along with variations in F, and M in the dynamic process. (a) Impact of M_{Init} and M_{ref}. (b) Impact of g.

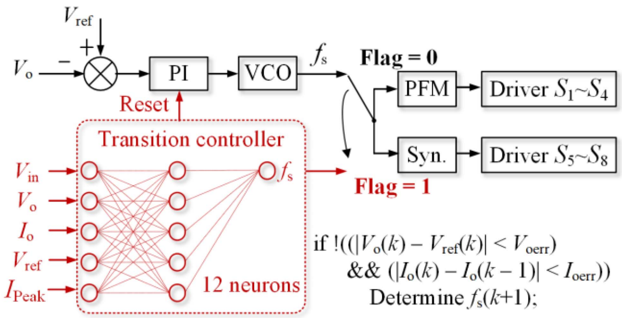


Fig. 14. Core algorithm of the proposed methodology implemented in the DSP, including the steady-state control part as well as the transient control part. A single-layer 12-neuron ANN is utilized in the transition controller to determine the switching frequency $f_{\mathrm{s}}(k+1)$ in the next switching cycle.

the active and shadow enhanced pulsewidth modulation registers are adjusted in alignment with this computation. The transition process concludes once the steady-state condition is reestablished. Thereafter, the PI controller undergoes a reset, and the default output frequency is aligned with the final switching frequency to preclude any abrupt changes in switching frequency, ensuring a smooth transition back to steady-state operation.

Empirically, V_{oerr} and I_{oerr} should be set to small values, typically around 1% or 2% of the rated value. Larger values indicate a prematurely terminated transition process. While discrepancies between V_{ref} and V_{o} increase the input to the steady-state PI controller, the initial output of the PI controller inherits the final switching frequency of the transition controller, preventing abrupt frequency changes. Although large values of V_{oerr} and I_{oerr} may slow the transition, they do not cause resonant current or voltage spikes, nor do they lead to instability.

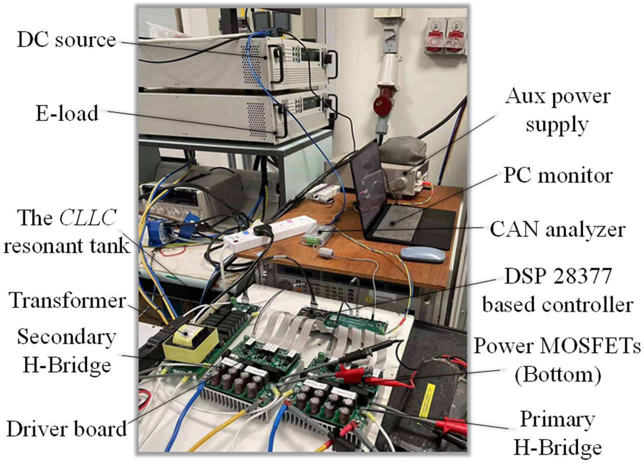


Fig. 15. Experimental prototype of the 2-kW *CLLC* resonant converter.

TABLE II
SPECIFICATION OF THE EXPERIMENTAL PROTOTYPE

Component	Part number	Parameters
MOSFETs	C3M0021120K	1.2-kV, 21-mΩ
MCU	TMS320F28377D	Digital signal processer
Dc capacitors	EKXG401ELL330ML20S F862BZ564K310ZV054	33-μF, 4 series, 2 parallel. 560-nF 4 series.
Resonant capacitors	BFC238350473	47-nF, 550-V, MMKP
Resonant inductors	B82559B3222A027, B82559A6472A024	4.7-μH and 2.2-μH extra inductors
Transformer	18T/12T, 600 strands Litz wire, EE70 core	$L_{\mathrm{lk}} \approx 7.3$-$\mu$H, $L_{\mathrm{m}} \approx 64.7$-$\mu$H

The implemented 12-neuron ANN requires 19 additions and 87 multiplications per control cycle, taking 10.26 μs. Although this significantly increases the computational burden compared to the PI controller or PI controllers with a ramp, which require fewer than 10 float32 multiplications per cycle, it remains manageable. Given the converter resonant frequency of 83.9 kHz, even in the worst-case scenario where the switching frequency matches the resonant frequency, the control cycle is still shorter than the switching cycle. Therefore, real-time cycle-by-cycle implementation of the 12-neuron ANN is feasible.

IV. EXPERIMENTAL VERIFICATION

Fig. 15 illustrates the experimental prototype and testbed. The experimental assessment of the proposed methodologies utilized a 2-kW, 480 V input voltage *CLLC* resonant converter prototype, with the electrical parameter specifications delineated in Table II. The design specification of the converter is based on time domain analysis. The specifications of the *CLLC* resonant converter is given as $V_{\mathrm{in}} = 480$ V, 160 V$< V_{\mathrm{o}} < 480$ V, $n = 3/2$, 60 kHz$< f_{\mathrm{s}} <$150 kHz. The design goal is to achieve a power loss minimization, and the detailed design processes are given in [28]. The transformer turn ratio results in a rated output voltage of 320 V at the designated resonant frequency point. The leakage and excitation inductances of the transformer are ascertained by measuring the open/short circuit impedance with

TABLE III
OPERATION CONDITIONS IN DIFFERENT CASES

Case	Output voltage reference V_{ref}	Load resistor R_{L}	Peak resonant current I_{Peak} (A)
Case 1	320 V→448 V M: 1.0→1.4	10 kΩ P_{o}: 10 W→23 W	8
Case 2	480 V→400 V M: 1.5→1.0	150 Ω P_{o}: 1.5 kW→1.0 kW	8
Case 3	400 V	10 kΩ→100 Ω P_{o}: 16 W→1.6 kW	8
Case 4*	320 V→448 V M: 1.0→1.4	10 kΩ P_{o}: 10 W→23 W	8

* In this case, the transition controller ANN model is retrained with an 50% increased of excitation inductance ($L_{\mathrm{m}} = 100\ \mu$H). However, the experimental prototype hold the actual $L_{\mathrm{m}} = 64.7\ \mu$H excitation inductance.

a frequency analyzer. To align with the resonant frequency, 6 and 13 47 nF MMKP film capacitors are connected in parallel on the primary and secondary sides, respectively. Additionally, resonant inductors of 4.7 μH and 2.2 μH are incorporated on the primary and secondary sides, setting the resonant frequency at 83.9 kHz and achieving near symmetry in the *CLLC* resonant tank configuration.

In the experimental section, the performance of the proposed method is benchmarked against four cases: 1) the conventional PI controller approach, 2) the PI controller with a ramp, 3) the self disturbance rejection control based on [31], [32], and 4) the proposed method under both output voltage reference step change and load step change scenarios. For fair comparisons, all tests are conducted using the same hardware and software configurations. At the hardware level, the cutoff frequency for the voltage sampling signals is set to 1 kHz, while for the current sampling signals, it is set to 10 kHz. At the software level, a four-bit moving average digital filter is applied to the sampled signals, resulting in very clean input variables (V_{in}, V_{o}, and I_{o}) with minimal electrical noise. The electrical parameters for these experiments are summarized in Table III. An ITECH IT6012B power source is employed as the input voltage source, and another unit of the same model served as the electrical load in constant load mode.

A. *Output Voltage Reference Step Change*

In Case 1, the load resistor is $R_{\mathrm{L}} = 10\,\mathrm{k}\Omega$, simulating a no-load condition, the reference output voltage V_{ref} is adjusted from an initial value of 320 V to 448 V, equivalently altering the voltage gain from $M = 1.0$ to $M = 1.4$. The performance comparisons are illustrated in Fig. 16. For the conventional PI controller, parameters are set to $k'_{\mathrm{p}} = 0.02$ and $k'_{\mathrm{i}} = 0.02$, determined through empirical fine-tuning based on the analysis in Fig. 12. Peak resonant current spikes are observed at 14 A for $i_{\mathrm{r}1}$ and 19 A for $i_{\mathrm{r}2}$ at the onset of the step change in V_{ref}, with the total voltage regulation time, $T_{\mathrm{VR}} = 2.6$ ms. By incorporating a ramp with a 3-V increment per switching cycle (through trial-and-error), based on identical PI control parameters, a smoother transition is achieved with the ramp-based PI controller, reducing T_{VR} to 860 μs. As for the linear active disturbance rejection control (LADRC), the unknown dynamic system can be treated as a

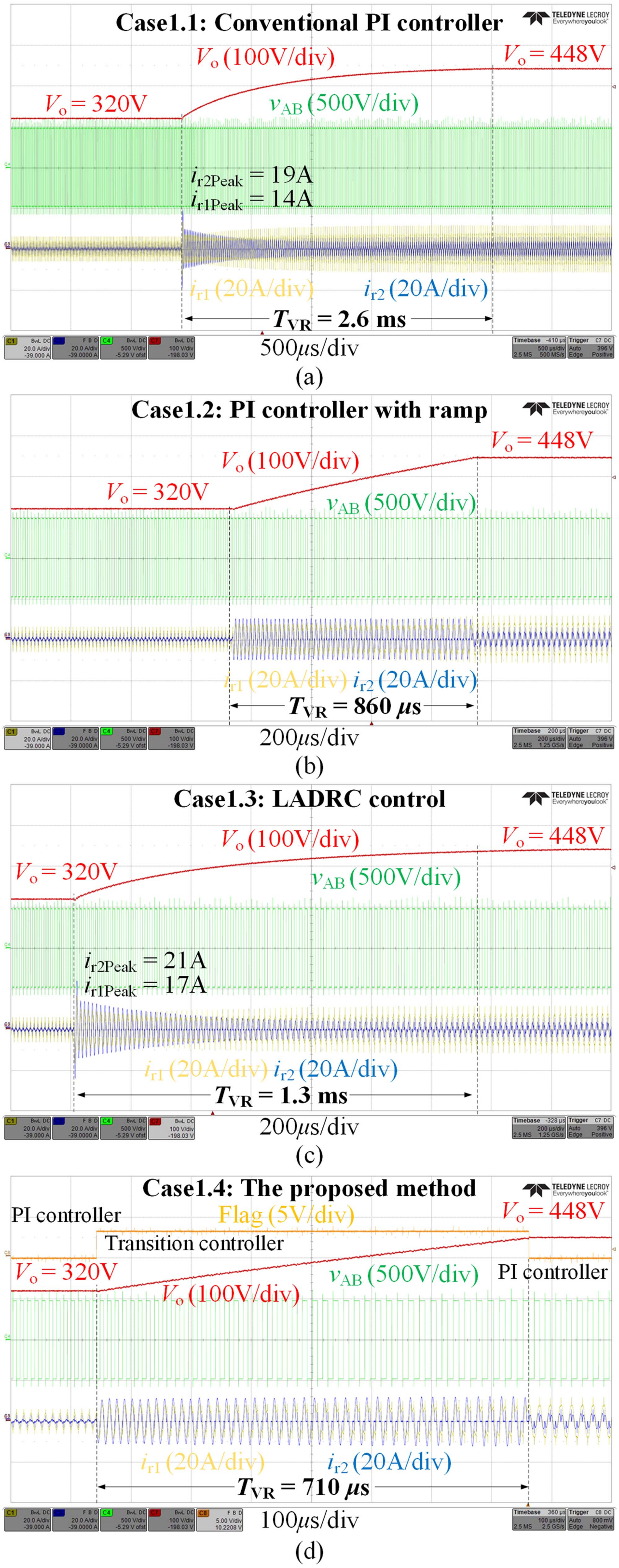


Fig. 16. Operation waveforms and comparisons in case 1. (a) Case1.1: Conventional PI controller. (b) Case1.2: PI controller with ramp. (c) Case1.3: LADRC control method. (d) Case1.4: The proposed method.

cascaded integration system, allowing for a simple proportional-derivative (PD) control. In the experiment, the PD control is discretized, and the bandwidth is set as with a $\omega_c = 500$ Hz (1 kπ rad), determined empirically through trial and error. The dynamic transition duration is observed to be 1.3 ms, which is half that of the PI controller method. However, since peak resonant current information is not included in the LADRC control diagram, the resonant current spikes are measured at $i_{\rm r1Peak} = 17$ A, $i_{\rm r2Peak} = 21$ A. The amplitudes of these spikes are only slightly increased compared to the PI controller, indicating that LADRC performs better than the conventional PI controller in dynamic processes. The proposed method utilized a general-purpose input/output Flag to signify the control algorithm operational state, transitioning between modes and achieving a $T_{\rm VR}$ of 710 μs with a predefined peak resonant current of 8 A, after which the final switching frequency is set as the initial for the PI controller.

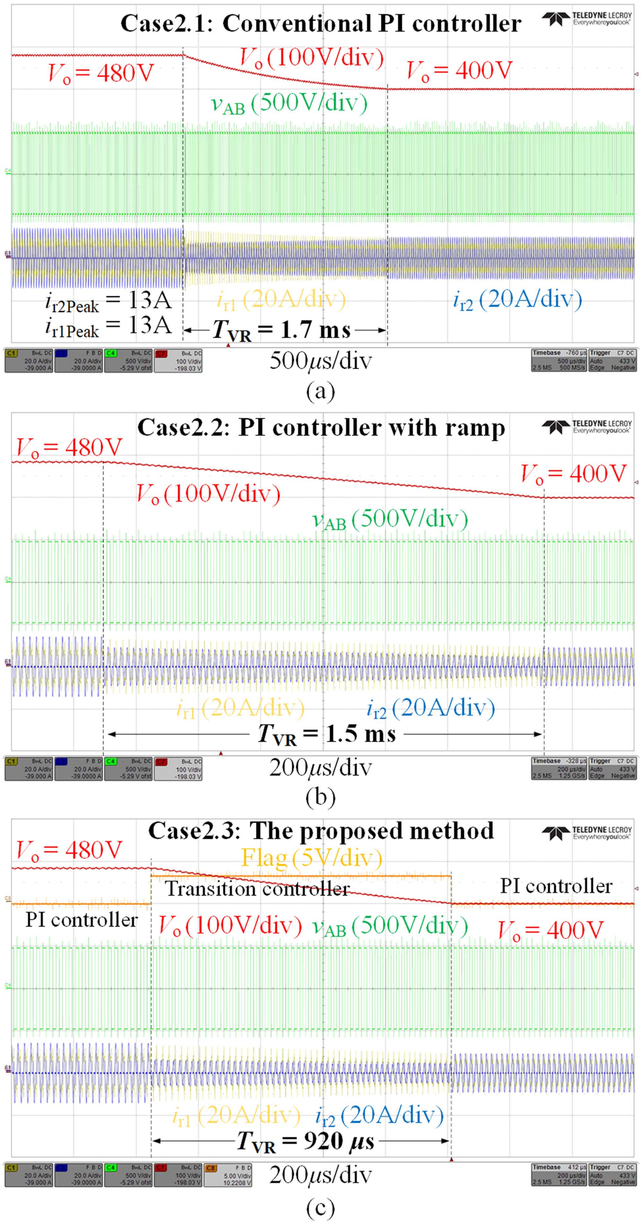
Case 2 explored an output voltage step-down scenario, with performance comparisons shown in Fig. 17, where similar outcomes are observed. The proposed method demonstrated a capability for smooth (zero inrush current) and rapid response (approximately +100% increased speed) in both output voltage reference step-up and step-down changes, significantly reducing transition time compared to the conventional PI controller, both with and without ramp function, and eliminating the need for trial-and-error adjustments. Upon specifying the peak resonant current, the proposed method efficiently operates within this constraint, showcasing its effectiveness and efficiency.

B. Load Step Change

During the load step change scenario, $R_{\rm L}$ is adjusted from 10 kΩ to 100 Ω, with the output voltage reference maintained at 400 V. The comparative performance of the three methods is illustrated in Fig. 18. To diminish disturbances in the sampling signals, a 4-bit moving average filter is employed in both the output voltage and current sampling programs. This introduces a delay ($T_{\rm sag} = 4$ switching cycles) in the control diagram across all scenarios, leading to a maximum voltage sag $V_{\rm osag} = 10$ V. Reducing the averaging bit count can decrease both $T_{\rm sag}$ and $V_{\rm osag}$; however, this reduction comes at the expense of diminished steady-state performance.

In the case of the PI controller, the total load regulation time $T_{\rm LR}$ is measured at 310 μs, with peak resonant current spikes recorded at 15 A for $i_{\rm r1}$ and 20 A for $i_{\rm r2}$. Incorporating a 1-V per switching cycle ramp (also through trial-and-error method) into the PI controller mitigated the resonant current spikes but resulted in an increased $T_{\rm LR}$ to 460 μs. The proposed method achieved a $T_{\rm LR}$ of 300 μs under a peak resonant current of 8 A. It is noteworthy that, compared to output voltage regulation time, the load regulation time is significantly shorter due to the smaller variations in switching frequency, as detailed in Fig. 6.

When the input voltage is reduced to 360 V, similar load dynamic tests (Case3.4 and 3.5) are conducted with the output voltage reference set to 340 V ($M = 1.41$). The comparison waveforms between the conventional PI controller and the proposed method are shown in Fig. 19. With the PI controller, resonant current spikes are observed at $i_{\rm r1Peak} = 16$ A, $i_{\rm r2Peak} = 22$ A. In contrast, the proposed algorithm limits the resonant currents to steady-state values, preventing current spikes under different operating conditions.



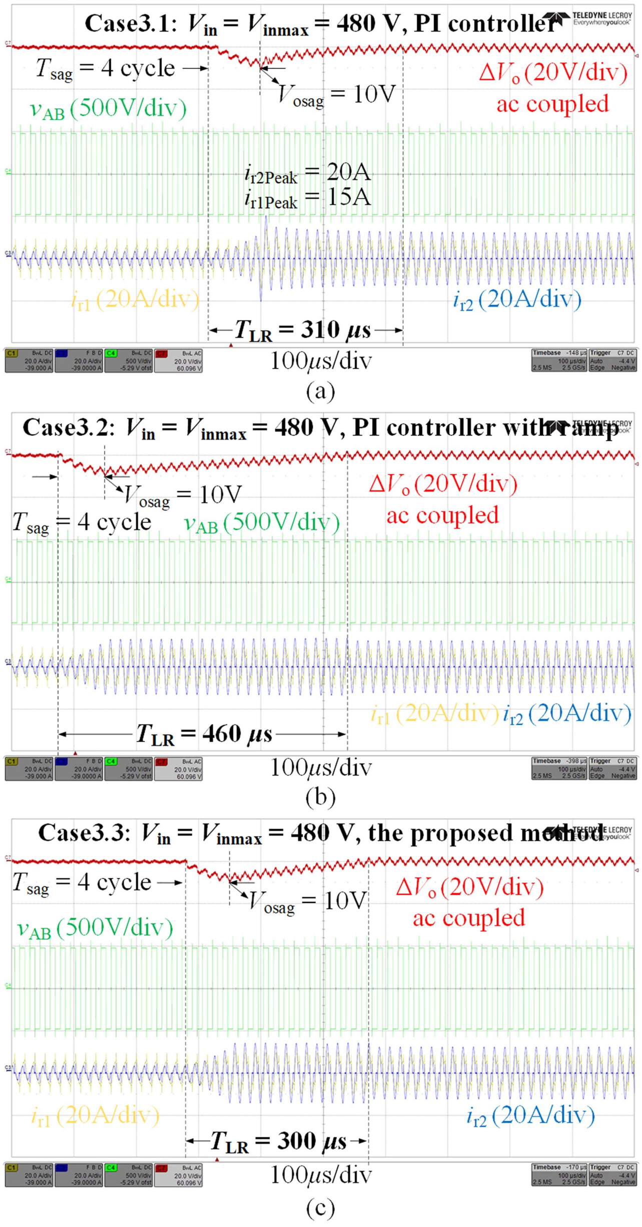
(a)

(b)

(c)

Fig. 17. Operation waveforms and comparisons in case 2. (a) Case2.1: Conventional PI controller. (b) Case2.2: PI controller with ramp. (c) Case2.3: The proposed method.

Fig. 20 presents a comprehensive comparison of Case1, illustrating the theoretical relationships between the conventional PI control method, the PI control with a ramp, and the proposed method with red, blue, and green dotted lines, respectively. Correspondingly, the experimental outcomes for Case1 are indicated by stars in red, blue, and green, denoting each method performance. Decreasing the PI parameters or the rate of change $dM_{\rm ref}/dt$ has been observed to decrease $I_{\rm Peak}$, albeit at the expense of an elongated $T_{\rm DT}$. Notably, the proposed method achieves the lowest $T_{\rm DT}$ for any specified $I_{\rm Peak}$, indicating



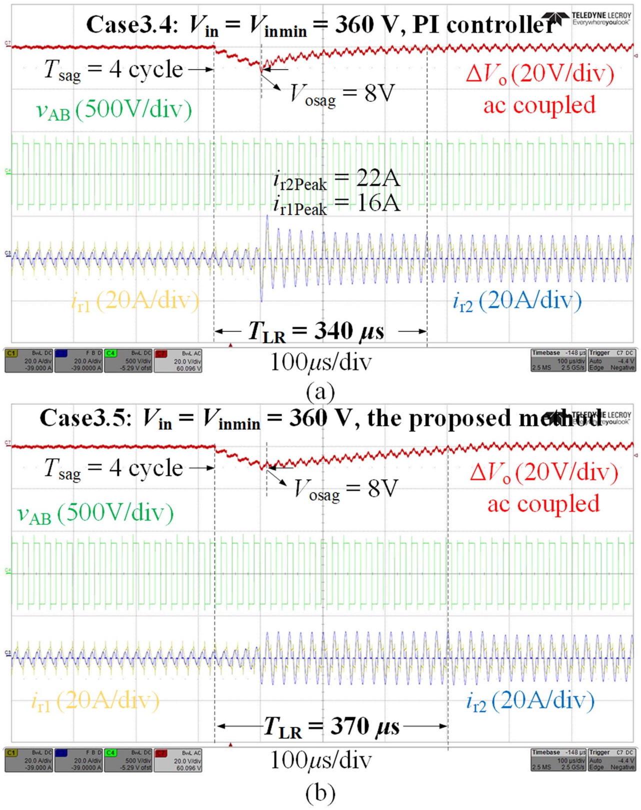
(a)

(b)

(c)

Fig. 18. Operation waveforms and comparisons in case 3 when $V_{\rm in} = V_{\rm inmax} = 480$ V. (a) Case3.1: Conventional PI controller. (b) Case3.2: PI controller with ramp. (c) Case3.3: The proposed method.

its superiority in performance. The experimental results are in substantial concordance with the theoretical predictions, underscoring the validity of the proposed method.



(a)

(b)

Fig. 19. Operation waveforms and comparisons in case 3 when $V_{\rm in} = V_{\rm inmin} = 360$ V. (a) Case3.4: Conventional PI controller. (b) Case3.5: The proposed method.

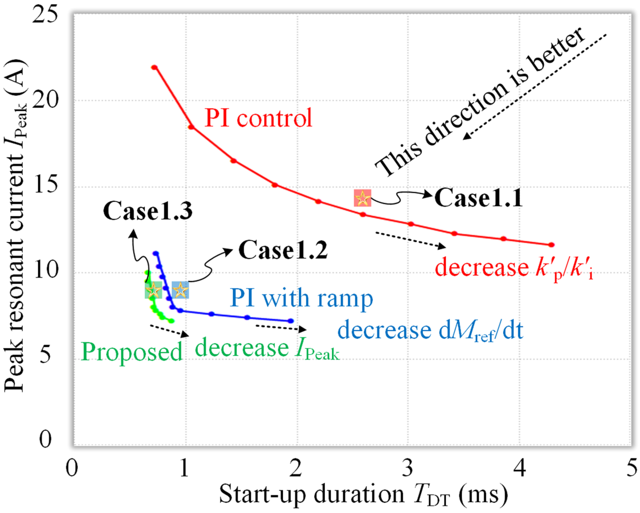


Fig. 20. Comprehensive comparison of different methods in Case1.

C. *Parameter Mismatch Conditions*

The proposed method relies exclusively on $V_{\rm in}$, $V_{\rm o}$, and $I_{\rm o}$. Due to the limitation of the analogy-digital-converter in the utilized DSP, the sampling frequency (also equals switching frequency) is inadequate for capturing the resonant currents and voltages at the switching frequency level. Consequently, the effectiveness of the transition controller is heavily dependent on precise values of the electrical parameters, like $L_{\rm r1}$, $C_{\rm r1}$, $L_{\rm r2}$, $C_{\rm r2}$, $L_{\rm m}$, n, and $C_{\rm f}$. Prior to the activation of the algorithm, it is imperative to accurately specify these parameters within the transition controller ANN. Deviations in these electrical parameters can result in discrepancies in the ANN output.

Variations in $L_{\rm r1}$, $C_{\rm r1}$, $L_{\rm r2}$, $C_{\rm r2}$ can lead to shifts in the resonant frequency, while changes in $L_{\rm m}$ influence the switching frequency range during output voltage regulation. The transformer turn ratio n impacts the output voltage, and the output capacitor

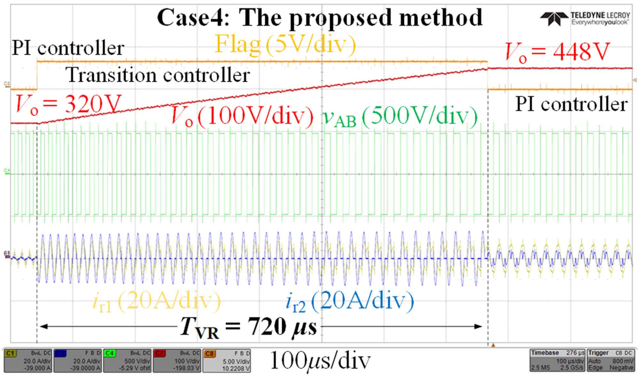


Fig. 21. Operation waveforms and comparisons in case 4.

TABLE IV
COMPARISON OF THE NUMBER OF SENSORS

Control methods	Required sensors
Trajectory control [18], [19], [20]	Input/output voltage, output current, resonant current and resonant voltage.
[21]	Input/output voltage, output current, secondary side resonant current.
[23]	Input/output voltage, Input/output current*.
Slide mode control [22]	Input/output voltage†.
Charge control [33]	Input/output voltage, output current, resonant voltage.
This work	Input/output voltage, output current*†.

*Resonant current control is not implemented.

†Maintaining CC mode operation is challenging.

*†Robust to potential parameter mismatches. Resonant current is controlled without sensors. Improves dynamic transition through real-time control.

TABLE V
COMPARISON AMONG DIFFERENT CONTROL METHODS

Control methods	Additional sensors	Control complexity	Resonant current control	Dynamic performance
Trajectory control	Required*	Complex†	No	Fast
Time-domain model-based method	Not required	Easy	No	Slow
Constant current control method	Required	Complex	No	Medium
This work	Not required	Complex	Yes	Fastest*†

*Theoretically, resonant current and capacitor voltages are required, but these values can be derived if the converter operating conditions and precise resonant tank parameters are known.

†These methods often require substantial look-up tables, making real-time implementation challenging.

*†The proposed method achieves the maximum output voltage increment under given peak resonant current conditions.

C_f plays a crucial role in determining the regulation time, particularly under output voltage reference step change conditions. It is advised that electrical parameters be measured using an impedance analyzer prior to prototype fabrication. Initial open-loop tests are recommended to establish the relationship between switching frequency, voltage gain, and output power.

To examine the effects of resonant parameter mismatches, an adjustment is made where $L_m = 100\ \mu$H, representing a 50% increase from its actual value, followed by retraining of the transition controller ANN. The operational scenario in Case 4 mirrors that of Case 1 and the experimental waveforms are depicted in Fig. 21. The comparison between Cases 1 and 4 reveals that a smooth transition remains achievable, albeit with a minor increase in transition time. Similar outcomes are observed with other types of parameter mismatches, with the actual peak resonant current experiencing approximately ±5% variation in response to ±20% variation in resonant capacitance. Considering ±5% tolerance of the used BFC238350473 capacitor, the impact on peak resonant current is minimal.

D. Comparison Analysis

A comprehensive comparison of the proposed method with previous methods, including both hardware and software levels, is summarized in Tables IV and V.

Input and output voltage sensors are essential for controlling a converter with a voltage closed loop. When output current control is required, an output current sensor is also necessary. For state trajectory methods such as those in [18], [19], and [20], resonant current and capacitor voltages are theoretically required. However, these values can be derived if the converter operating conditions and precise resonant tank parameters are known. These methods use inverse triangular functions to calculate the switching frequency, often necessitating substantial look-up tables, which make real-time implementation challenging. Typically, trajectory control refreshes the control signals every 5–20 switching cycles, reducing dynamic performance.

In [21], the secondary side resonant current is sensed to accelerate dynamic transitions. In [23], all input/output voltage/current signals are sampled, and the converter operates in PFM and PSM modes, but resonant current control is not implemented, leaving room for dynamic improvement. Slide mode control in [22] does not use output current sensors. Although dynamic performance improves during load step changes, maintaining constant current (CC) mode operation is challenging. Charge control in [33] with a 240 W *LLC* prototype samples resonant voltage for the inner loop, achieving a faster response compared to voltage mode control.

In summary, time-domain model-based methods do not require additional sensors and have straightforward control algorithms but exhibit slow dynamic performance. The constant current control method samples the resonant current, speeding up dynamic performance at the cost of increased control complexity.

The proposed method senses input/output voltage and output current, requiring knowledge of the resonant tank electrical parameters. Despite potential parameter mismatches, the method is robust and maintains performance with slight reductions. By setting a predefined peak resonant current, the proposed method achieves the maximum output voltage increment through real-time, cycle-by-cycle control, resulting in the fastest dynamic performance among the different control methods under a given resonant current limit.

The shortcomings of the proposed method are summarized as follows.

1) Precise dynamic control requires accurate values for all electrical parameters.
2) Nonlinear and nonideal factors, such as parasitic components and converter deadtime, are not considered, affecting model accuracy.
3) Real-time implementation on high-frequency (> 300 kHz) *CLLC* resonant converters is challenging due to DSP calculation resource limits.

V. CONCLUSION

This article introduces optimal switching patterns predicated on designated peak resonant current conditions to facilitate swift and seamless dynamic transitions with zero inrush current. Extending from this foundation, a cohesive, synergetic control strategy is devised for amalgamation with the extensively employed PI controllers. The validity of this approach is corroborated through its application on a 2-kW *CLLC* resonant converter prototype, evidencing a roughly 100% enhancement in dynamic response speed relative to conventional methods, encompassing both step load change and output voltage reference step change. Notably, the proposed methodology sustains superior performance amidst considerable variances in electrical component parameters, obviating the necessity for supplementary sensors.

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