Letters

Novel SVPWM Update Strategy to Solve Calculation Delay in PMSM Driver

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***Abstract*—PWM output delay caused by calculation is widely presented in permanent magnet synchronous motor drive systems, which reduces control performance, accuracy, and stability. This article proposes a novel enhanced SVPWM update strategy, which is easy to implement and achieves completely delay-free output. Compared to traditional methods, this approach is simpler to compute, does not rely on motor parameters, and does not require an increase in sampling frequency. The effectiveness and superiority of the proposed algorithm are verified through comparative experiments.**

***Index Terms*—Calculation delay, permanent magnet synchronous motor (PMSM), SVPWM.**

I. Introduction

THE control of permanent magnet synchronous motor (PMSM) is primarily implemented by digital systems, involving links, such as signal acquisition and processing, algorithms calculation, etc. [1]. These links inevitably result in the delay of PWM updating and ultimately lead to the reduction of control performance and stability [2], [3]. From the perspective of vector modulation, this delay can be described in Fig. 1(a). To eliminate it, several approaches have been proposed, summarized as follows.

Method I—Prediction (PR)-based compensation: Predicting the next cycle's current based on the PMSM model can equivalently eliminate the impact of one-beat delay [4], [5]. Nevertheless, due to the variation of system parameters, PR error occurs, and it is described in Fig. 1(b). To reduce reliance on model parameters, the current's predicted value is obtained by considering the constant current slope over a short period and employing multiple sampling and linear PR [6], [7]. Despite its robustness to system parameters, PR error still exists due to the hardware filtering circuits and switching noise from power tubes [8].

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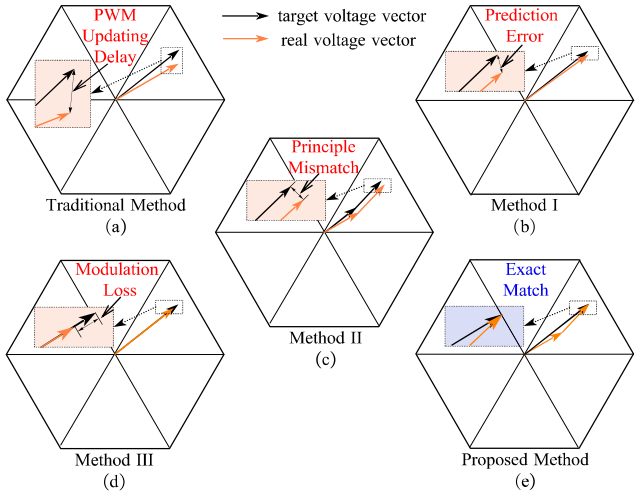

Fig. 1. Comparison of the proposed none-delay SVPWM update strategy with existing delay elimination methods from the perspective of vector modulation. (a) Traditional method. (b) Method I. (c) Method II. (d) Method III. (e) Proposed method.

Method II—Increasing sampling and update frequency: Increasing the sampling frequency offers a direct means to decrease digital delay. For instance, sampling current and updating PWM at both the beginning and midpoint of the PWM cycle effectively reduce delays [9]. In addition, implementing multiple sampling and multiple updates of PWM commands can further reduce delay [10], [11]. While these approaches enhance control performance, the increased frequency of PWM command calculation imposes a greater hardware burden. In addition, although the delay can be reduced, it cannot be completely eliminated, as shown in Fig. 1(c).

Method III—Real-time updating: The high computational power of chips enables rapid completion of field-oriented control (FOC) calculations and simultaneous updating of PWM duty cycles within a single control cycle, thereby eliminating delays. For instance, utilizing advanced computing chips, such as FPGA, or employing simple control algorithms can reduce calculation delays to just a few microseconds, with PWM commands being updated immediately after calculation [12], [13]. However, this approach may incur increased hardware costs and potentially result in a certain degree of modulation ratio loss, as illustrated in Fig. 1(d). Although the drawbacks

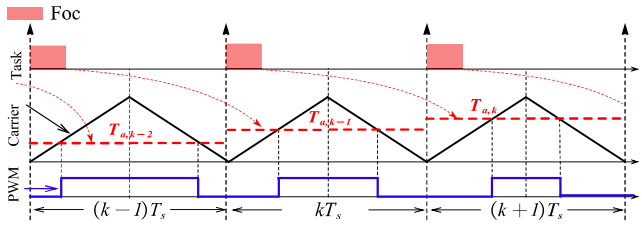

Fig. 2. Time sequence of the traditional SVPWM update strategy.

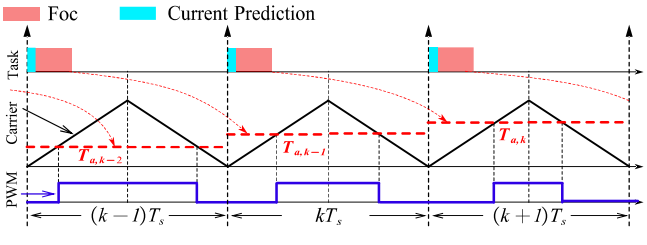

Fig. 3. Time sequence of Method I.

of modulation ratio loss can be mitigated by utilizing improved real-time updating [14], [15], [16], these methods require modification (MD) of current sampling points and complex decision rules, limiting their applicability.

This article presents a novel strategy to eliminate delay and its updating principle to achieve exact match with target voltage vector is simply described in Fig. 1(e). This method can completely eliminate delays, is independent of model parameters and computational power, does not require additional sampling times, and incurs no modulation ratio loss.

II. Proposed SVPWM Update Strategy

A. Time Sequence Analysis of Existing Methods

Traditionally, the PMSM operates with the FOC algorithm, and its time sequence diagram is shown in Fig. 2, where T_s is the PWM period. The PWM generator works at the one-sided edge update mode and uploads the duty reference at the beginning of each PWM period. At the beginning of the k period, the current sample is triggered and then the FOC algorithm is conducted, giving the duty reference $[T_{a,k}, T_{b,k}, T_{c,k}]$. Nevertheless, the time spent on sampling and calculation cannot be ignored, and the ideal duty reference $[T_{a,k}, T_{b,k}, T_{c,k}]$ desired for the k period is delayed to act on the $(k+1)$ period.

Similarly, Methods I–III mentioned in the introduction can be visually represented by time sequence diagrams, as shown in Figs. 3 –5.

From Fig. 3–5, it is clearly seen that Method I predicts the current for the next cycle, and the accuracy of the PR determines the compensation effect. Method II performs two calculations and updates within one period, reducing delay errors but doubling additional calculations. The value calculated by Method III is updated in the current period, but it is required that the FOC calculation be fast enough; otherwise, modulation loss will be introduced.

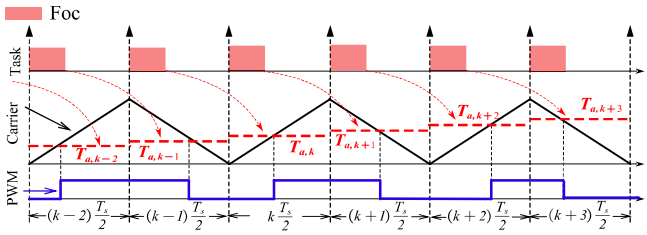

Fig. 4. Time sequence of Method II.

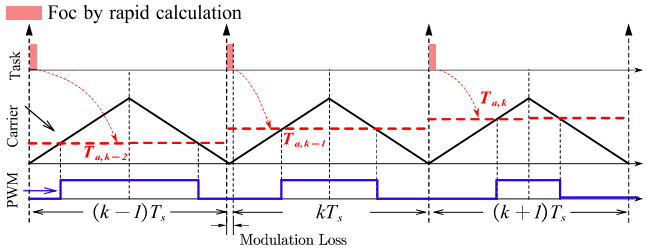

Fig. 5. Time sequence of Method III.

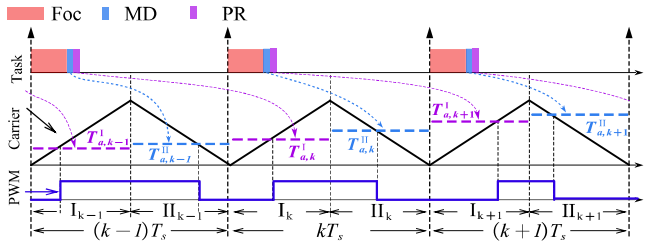

Fig. 6. Time sequence of the proposed SVPWM update strategy.

B. Principle of the Proposed Method

To eliminate this delay, this article proposes a novel method, and its time sequence is shown in Fig. 6. The PWM generator of MCU works at the two-sided edge update mode and one PWM period is divided into two stages, I_k and II_k. $[T^{\mathrm{I}}_{a,k}, T^{\mathrm{I}}_{b,k}, T^{\mathrm{I}}_{c,k}]$ is the rising duty reference in I_k stage (loaded at the beginning of the k period), and $[T^{\mathrm{II}}_{a,k}, T^{\mathrm{II}}_{b,k}, T^{\mathrm{II}}_{c,k}]$ is the falling duty reference in II_k stage (loaded at the middle of the k period). $[T^{\mathrm{I}}_{a,k}, T^{\mathrm{I}}_{b,k}, T^{\mathrm{I}}_{c,k}]$ and $[T^{\mathrm{II}}_{a,k}, T^{\mathrm{II}}_{b,k}, T^{\mathrm{II}}_{c,k}]$ are calculated in the (k-1) period's PR and k period's MD part, respectively.

a) Calculation of $[T^{\mathrm{I}}_{a,k}, T^{\mathrm{I}}_{b,k}, T^{\mathrm{I}}_{c,k}]$ by PR: The calculation of $[T^{\mathrm{I}}_{a,k}, T^{\mathrm{I}}_{b,k}, T^{\mathrm{I}}_{c,k}]$ is performed in the PR part of the (k-1) period. Based on the output voltage vector of the last three periods, the predictive k period's output vector $\hat{\boldsymbol{U}}_k$ ($\hat{U}_{\alpha,k}$ and $\hat{U}_{\beta,k}$) is obtained by the second-order Lagrange interpolation method:

$$\begin{aligned}\hat{U}_{\alpha,k} &= L_2(U_{\alpha,k-1}, U_{\alpha,k-2}, U_{\alpha,k-3})\\ \hat{U}_{\beta,k} &= L_2(U_{\beta,k-1}, U_{\beta,k-2}, U_{\beta,k-3}).\end{aligned} \tag{1}$$

where, $L_2(.)$ is a second-order Lagrange operator. Then, $[T^{\mathrm{I}}_{a,k}, T^{\mathrm{I}}_{b,k}, T^{\mathrm{I}}_{c,k}]$ is calculated as:

$$[T^{\mathrm{I}}_{a,k}, T^{\mathrm{I}}_{b,k}, T^{\mathrm{I}}_{c,k}] = f_{SVPWM}(\hat{U}_{\alpha,k}, \hat{U}_{\beta,k}) \tag{2}$$

where $f_{SVPWM}(\cdot)$ is the SVPWM modulation operator. The purpose of this PR is to align the direction of the output vector $\hat{\boldsymbol{U}}_k$ as close as possible to the target output vector $\boldsymbol{U}_k$ in stage I_k, which forms the basis to adjust the actual output vector to $\boldsymbol{U}_k$ by $\boldsymbol{U}'_k$ in II_k.

Remark 1: In Method I, a detailed motor model is required, and the PR results directly determine the compensation effect. In proposed method, the PR merely provides a basis for subsequent MD, and the accuracy of the PR does not play a decisive role.

b) Calculation of $[T^{II}_{a,k}, T^{II}_{b,k}, T^{II}_{c,k}]$ by MD: The calculation of $[T^{\mathrm{II}}_{a,k}, T^{\mathrm{II}}_{b,k}, T^{\mathrm{II}}_{c,k}]$ is performed in the MD part of the k period. In stage II_k, the target output vector $\boldsymbol{U}_k$ ($U_{\alpha,k}$ and $U_{\beta,k}$) is realized completely in the k period by the correction vector $\boldsymbol{U}'_k$ ($U'_{\alpha,k}$ and $U'_{\beta,k}$), which achieves none delay.

From the analysis of the volt second characteristics, in I_k, $0.5T_s\hat{\boldsymbol{U}}_k$ has been realized. Therefore, for the remaining II_k stage, the output vector $\boldsymbol{U}'_k$ satisfies

$$0.5T_s\hat{\boldsymbol{U}}_k + 0.5T_s\boldsymbol{U}'_k = T_s\boldsymbol{U}_k \tag{3}$$

then

$$\begin{cases} U'_{\alpha,k} = 2U_{\alpha,k} - \hat{U}_{\alpha,k} \\ U'_{\beta,k} = 2U_{\beta,k} - \hat{U}_{\beta,k}. \end{cases} \tag{4}$$

Hence, the duty reference for the II_kstage is calculated by

$$[T^{\mathrm{II}}_{a,k}, T^{\mathrm{II}}_{b,k}, T^{\mathrm{II}}_{c,k}] = f_{\mathrm{SVPWM}}(2U_{\alpha,k} - \hat{U}_{\alpha,k}, 2U_{\beta,k} - \hat{U}_{\beta,k}). \tag{5}$$

Remark 2: The algebraic operations in (1) and (2) are simple and negligible in calculation time. Therefore, the additional computation load of the proposed algorithm is roughly equivalent to one SVPWM, which is significantly less than the whole FOC of Method II.

C. Universality Analysis of Proposed Method

Based on the above analysis, it is evident that there are two necessary conditions for implementing this algorithm.

1) The original control algorithm and the proposed correction calculation must be completed within half a PWM cycle. With the advancement of electronic technology, this is achievable for most MCUs and FPGAs nowadays. If the calculation time exceeds $T_s/2$, it may result in incomplete correction.
2) Support for asymmetric PWM output mode is required. FPGAs can flexibly achieve this, and currently, most MCUs also support asymmetric output. For other MCUs that only support symmetric PWM output, approximate asymmetric output can be achieved by setting interrupt request when the count register equals 0 and reaches its maximum value. The timing for this is shown in Fig. 7.

Therefore, most of MCUs currently available can apply this algorithm, demonstrating a high level of universality.

Remark 3: The computation time constraint of the proposed method is less stringent than those of other methods. In [9] and [16], the requirements for computation time are $0.25T_s$ and a value that less than $T_s/12$, respectively.

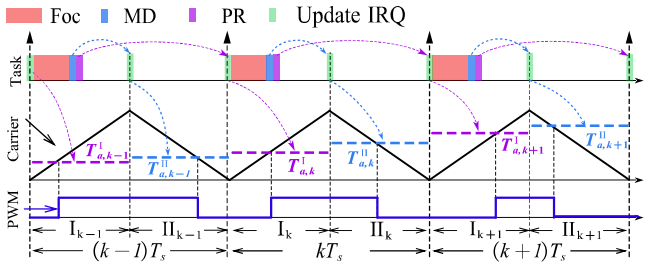

Fig. 7. Time sequence of the proposed SVPWM update strategy with MCUs supporting symmetric PWM output.

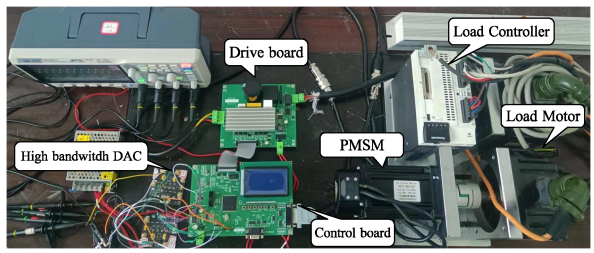

Fig. 8. Experimental platform.

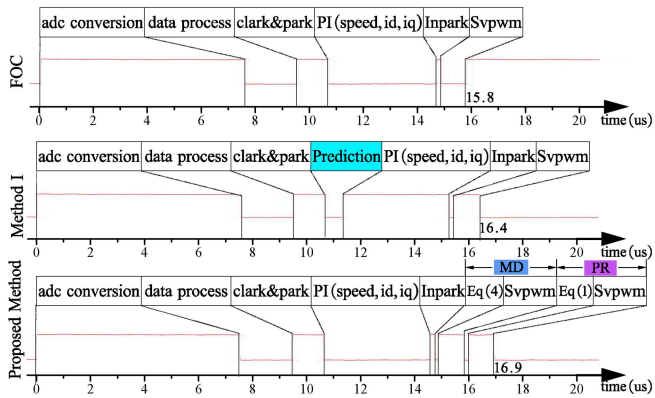

Fig. 9. Calculation time of FOC, method I, and proposed method.

III. Experimental Results

The experimental verification is conducted using an experimental platform based on DSP TMS320F28335. An intelligent power module, FSBB30CH60C, is used as the voltage source inverter. The PMSM motor used in the experiment has a rated voltage of ac 220 V, a rated current of 3 A, a rated speed of 3000 r/min, pole pairs of 4, a resistance of 0.9 Ω, and an inductance of 6.55 mH. The frequencies of PWM, current sampling, and current loop control are 10 KHz, while the frequency of speed loop control is 1 KHz. The experimental platform is shown in Fig. 8.

The detailed settings of the PWM generator in this controller are as follows: the EPWM part of DSP adopts a left and right asymmetric output strategy, the correction part is stored in the CMPA register, and the PR part is stored in the CMPB register. They are updated to the shadow register at the middle and beginning of the period, respectively.

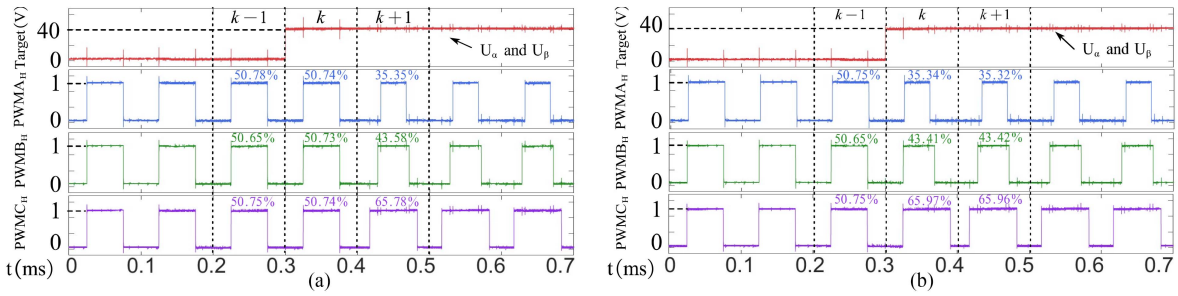

Fig. 10. Switching waveform of the three-phase upper bridge arm when U_α and U_β both turns from 0 to 40 V. (a) Traditional SVPWM strategy. (b) Proposed SVPWM strategy.

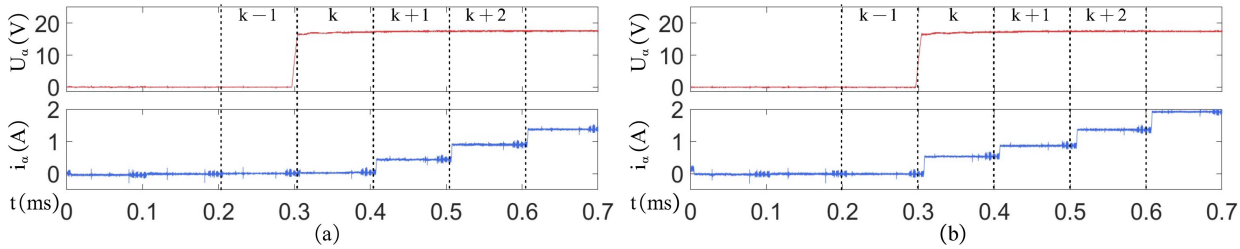

Fig. 11. Waveform of i_α when U_α changes from 0 to 17.3 V. (a) Traditional SVPWM strategy. (b) Proposed SVPWM strategy.

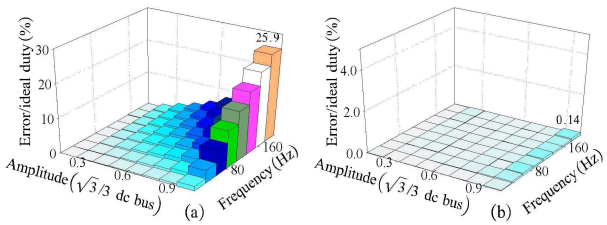

Fig. 12. Average duty cycle error under various operating conditions. (a) Traditional method (GPIO2). (b) Proposed method (GPIO4).

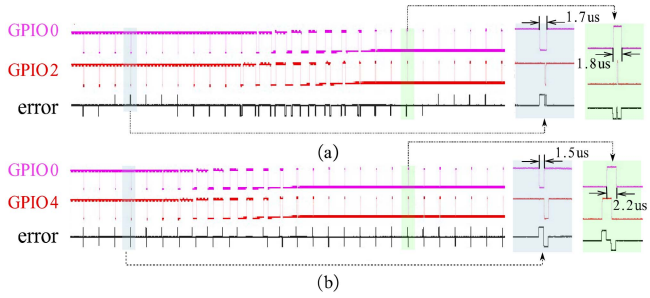

Fig. 13. Detailed implementation of duty cycle when amplitude is $\sqrt{3}/3$ DC bus voltage and frequency is 200 Hz. (a) Traditional method. (b) Proposed method.

A. Comparison of Calculation Time

A toggle GPIO-level operation is inserted into the program to measure the execution time of each algorithm, and the results are shown in Fig. 9. The calculation times of FOC, PR method, and proposed method are 15.8, 16.4, and 16.9 μs, respectively. The calculation time of proposed method increases by 1.1 μs compared to that of FOC, accounting for 7.0% of the execution time, which is considered a small computational complexity.

B. Validation of Delay Elimination

To directly demonstrate that the proposed SVPWM update strategy indeed eliminates one-cycle delay, two experiments are conducted.

The first experiment conducts a comparison from the perspective of PWM duty. Fig. 10(a) and (b), respectively, shows the upper bridge switch waveforms of the traditional algorithm and the proposed algorithm. In the k period, target alpha–beta axis voltage U_α and U_β change from 0 to 40 V, respectively. The desired duty of three phase can be calculated as 35.35%,43.57%, and 65.78%, respectively. In Fig. 10(a), the traditional method realizes the desired duty in the $k+1$ period. On the contrary, the proposed method realizes the desired duty in the k period in Fig. 10(b), which completely cancels the delay.

The second experiment conducts comparison from the perspective of current waveform. Fig. 11(a) and (b), respectively, shows the alpha-axis current waveforms of the traditional algorithm and the proposed algorithm. In the k period, the target voltage U_α transits from 0 to 17.3 V. In Fig. 11(a), the current change at the $k+1$ period. However, the current change at the k period in Fig. 11(b). This comparison also demonstrates that the proposed method completely eliminates computational delays.

C. Discussion in Duty Cycle Range

This experiment implements the command of a rotating voltage vector with the frequency ranging from 0 to 200 Hz and the amplitude from 0 to $\sqrt{3}/3$ dc bus voltage. This duty setup covers the whole undermodulation region, and the maximum frequency is set according to the motor's rated electrical speed, ensuring the test results are generalizable. In the DSP, three strategies are executed simultaneously, with pins GPIO0, GPIO2, and GPIO4 outputting their respective PWM signals.

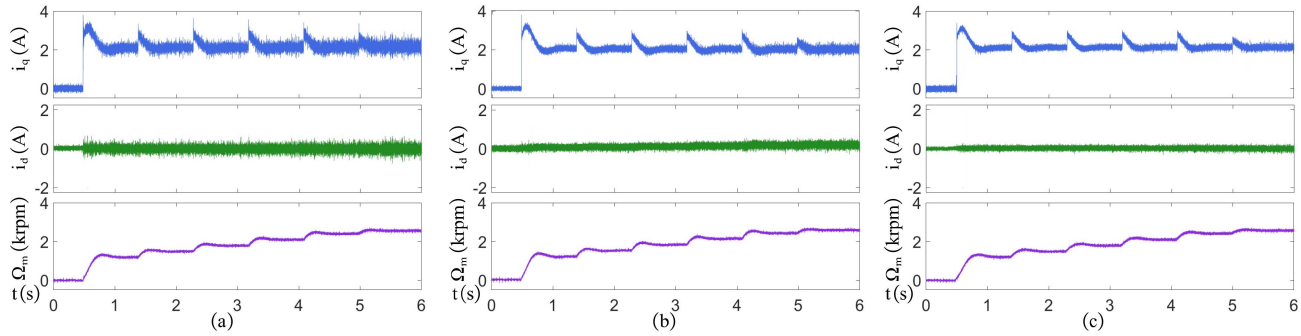

Fig. 14. Waveforms of *dq*-axis current and speed under steady-state and transient conditions. (a)Traditional method. (b) Predictive based delay elimination strategy. (c) Proposed strategy.

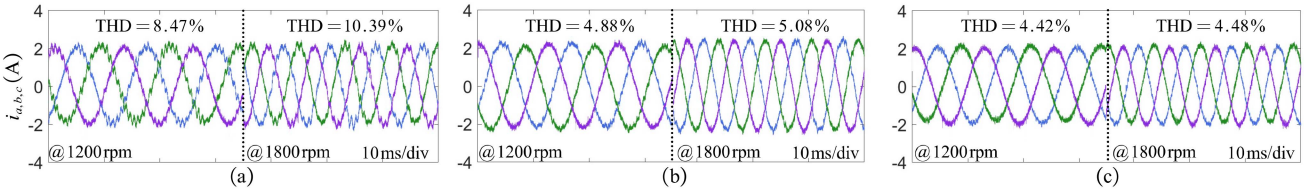

Fig. 15. Current waveform of three phases when motor runs at 1200 and 1800 r/min with a load of 1.2N·m. (a) Traditional strategy. (b) Predictive based delay elimination strategy. (c) Proposed strategy.

1) *GPIO0:* PWM signal of phase A's upper bridge using the traditional SVPWM update strategy.
2) *GPIO2:* Same as GPIO0, but with a one-period command delay.
3) *GPIO4:* PWM signal of phase A's upper bridge using the proposed SVPWM update strategy, with a one-period command delay.

With the one-period delay in GPIO2 and GPIO4, GPIO0 serves as the ideal, no-delay signal. By measuring and analyzing the duty errors between GPIO0 and GPIO2, and between GPIO0 and GPIO4, the deviation from the ideal duty cycle for both methods can be determined. The results are shown in Fig. 12.

From Fig. 12, it is evident that the duty loss of the traditional method (GPIO2) is significant, with the highest loss reaching up to 25.9%. In contrast, the proposed method (GPIO4) shows very low duty losses across its entire operational range, with a maximum loss of only 0.14%. The duty cycles at the points of maximum error for both methods are shown in Fig. 13.

Fig. 13 shows that under the traditional method (GPIO2), errors are unidirectionally distributed locally, whereas the duty cycle errors of proposed method (GPIO4) are bidirectionally distributed across each cycle. As a result, nearly every cycle with the proposed method achieves practical duty cycles that closely align with ideal values, including those near 0% and 100% duty cycles, as marked in Fig. 13.

D. Comparison of Control Performance

To demonstrate the control performance advantages of the proposed SVPWM strategy, this section compares three methods: the traditional strategy (without delay elimination), a predictive-based delay elimination strategy, and the proposed strategy. The load is 1.2 N·m.

TABLE I
STEADY-STATE STANDARD DEVIATION OF THE *D*-AXIS CURRENT (A)

Strategy \ Speed(rpm)	1200	1500	1800	2100	2400	2550
Traditional method	0.116	0.112	0.119	0.120	0.136	0.152
Predictive method	0.069	0.073	0.071	0.074	0.079	0.088
Proposed method	0.058	0.057	0.058	0.057	0.062	0.065

The first experiment compares the steady-state and transient fluctuations of speed and current among the three methods at different speeds, as shown in Fig. 14. The motor's target speed starts from 0 and sequentially jumps to 1200, 1500, 1800, 2100, and 2400 r/min, eventually reaching 2550 r/min, with time intervals between each jump ensuring system stability. From Fig. 14(a), it is observed that using the traditional strategy without delay elimination results in a significant ripple in the *dq*-axis currents. Comparing Fig. 14(a) with (b), it is evident that employing the predictive strategy to eliminate delay leads to a noticeable improvement in current ripple. However, it introduces new issues, and the *d*-axis current shows a significant positive offset, exacerbating with increasing speed. Analysis suggests that higher speeds significantly magnify adverse effects caused by parameter mismatches in the predictive strategy. Comparing Fig. 14(a)–(c), it is apparent that the proposed strategy, independent of system parameters, not only markedly improves the current ripple but also introduces no new issues. On the other hand, the steady-state standard deviations of the *dq*-axis currents are recorded, as shown in Tables I and II. It can be observed that the proposed method achieves the minimum current fluctuations.

In the second experiment, as shown in Fig. 15, comparisons of the three-phase current waveforms are conducted at 1200 and 1800 r/min. In Fig. 15(a), without delay elimination, the

TABLE II
STEADY-STATE STANDARD DEVIATION OF THE Q-AXIS CURRENT (A)

Strategy \ Speed(rpm)	1200	1500	1800	2100	2400	2550
Traditional method	0.128	0.131	0.129	0.138	0.151	0.156
Predictive method	0.061	0.068	0.069	0.070	0.077	0.087
Proposed method	0.058	0.059	0.061	0.062	0.066	0.068

total harmonic distortion (THD) of three-phase currents at these speeds are 8.47% and 10.39%, respectively. In Fig. 15(b), utilizing the predictive method to eliminate delay reduces THD to 4.88% and 5.08%, respectively. In Fig. 15(c), the proposed strategy further reduces THD to 4.42% and 4.48%, indicating better performance in optimizing distortion caused by delay.

Based on the two experiment results, it can be concluded that the proposed algorithm effectively reduces current noise and distortion caused by delay. Moreover, compared with predictive-based delay elimination methods, the algorithm maintains consistent performance regardless of parameter variations or changes in speed, demonstrating strong robustness.

IV. CONCLUSION

This article proposes an improved none-delay SVPWM update strategy, and its superiority is verified by comparative experiments. Different from other delay compensation strategies, this method eliminates output (calculation) delay in principle and does not require any model parameters, making it easy to implement. In addition, this method is not only applicable to PMSM drivers but also to any three-phase ac system, achieving significant control performance improvement, thus having strong universality and derivability.

REFERENCES

[1] H. Zhang, W. Liu, Z. Chen, and N. Jiao, "An overall system delay compensation method for IPMSM sensorless drives in rail transit applications," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1316–1329, Feb. 2021.

[2] C. Gong, Y. Hu, J. Gao, Y. Wang, and L. Yan, "An improved delay-suppressed sliding-mode observer for sensorless vector-controlled PMSM," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5913–5923, Jul. 2020.

[3] H. Zhang, X. Wang, Y. He, D. Pan, and X. Ruan, "A compensation method to eliminate the impact of time delay on capacitor-current active damping," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 7512–7516, Jul. 2022.

[4] X. Luo, A. Shen, Q. Tang, J. Liu, and J. Xu, "Two-step continuous-control set model predictive current control strategy for SPMSM sensorless drives," *IEEE Trans. Energy Convers.*, vol. 36, no. 2, pp. 1110–1120, Jun. 2021.

[5] X. Zhang, G. H. B. Foo, T. Jiao, T. Ngo, and C. H. T. Lee, "A simplified deadbeat based predictive torque control for three-level simplified neutral point clamped inverter fed IPMSM drives using SVM," *IEEE Trans. Energy Convers.*, vol. 34, no. 4, pp. 1906–1916, Dec. 2019.

[6] J. Gao, C. Gong, W. Li, and J. Liu, "Novel compensation strategy for calculation delay of finite control set model predictive current control in PMSM," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5816–5819, Jul. 2020.

[7] V. Repecho, D. Biel, and A. Arias, "Fixed switching period discrete-time sliding mode current control of a PMSM," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2039–2048, Mar. 2018.

[8] Q. Zeng and L. Chang, "An advanced SVPWM-based predictive current controller for three-phase inverters in distributed generation systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1235–1246, Mar. 2008.

[9] Z. Lin, X. Ruan, H. Zhang, and L. Wu, "A generalized real-time computation method with dual-sampling mode to eliminate the computation delay in digitally controlled inverters," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5186–5195, May 2022.

[10] X. Zhang, P. Chen, C. Yu, F. Li, H. T. Do, and R. Cao, "Study of a current control strategy based on multisampling for high-power grid-connected inverters with an LCL filter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5023–5034, Jul. 2017.

[11] H. Fujita, "A single-phase active filter using an H-bridge PWM converter with a sampling frequency quadruple of the switching frequency," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 934–941, Apr. 2009.

[12] L. Rovere, A. Formentini, and P. Zanchetta, "FPGA implementation of a novel oversampling deadbeat controller for PMSM drives," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3731–3741, May 2019.

[13] M. Hu et al., "Fast current control without computational delay by minimizing update latency," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12207–12212, Nov. 2021.

[14] J. Ma, X. Wang, F. Blaabjerg, and W. Song, "Real-time calculation method for single-phase multilevel converters based on phase-shifted carrier pulsewidth modulation," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 3043–3050.

[15] J. Ma, X. Wang, F. Blaabjerg, W. Song, S. Wang, and T. Liu, "Real-time calculation method for single-phase cascaded H-bridge inverters based on phase-shifted carrier pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 977–987, Jan. 2020.

[16] M. Li, J. Liu, M. Xiao, and E. Xie, "A real-time calculation PWM strategy that can eliminate one beat delay for PMSM driving," *IEEE Trans. Energy Convers.*, vol. 39, no. 2, pp. 1230–1244, Jun. 2024.