

# Monte Carlo Statistical Tolerance Analysis of a Parallel-Plate Multichip Power Module

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**Abstract**—A Monte Carlo statistical tolerance analysis is conducted on a parallel-plate, wirebond-less multichip power module (MCPM) to analyze the planarity across modules with post interconnects and identify which parts in the assembly contribute the most variation. Power electronics packaging has migrated from wirebonds to post interconnects that allow for vertical, parallel-plate modules, improving power density, reducing power loop inductances, and enabling double-sided cooled modules. Demonstrations of MCPMs of this structure have been limited in the number of die. This is a substantial gap in literature since as the number of die in parallel increases, the number of post interconnects and bondlines scale, resulting in more variation across component heights and reducing the yield and probability of connecting every interconnect. Different tolerance analyses are discussed and analyzed for the assembly of the MCPM, and a Monte Carlo statistical tolerance analysis is conducted to quantify the maximum height mismatch across the module and identify, which components introduce the most variation. Three MCPMs are fabricated using the statistical tolerance analysis, targeting components to reduce the maximum height mismatch. The 13 kV, six-die module is successfully characterized and is the first functional module of its kind.

**Index Terms**—Monte Carlo, multichip power module, nano-silver sintering, post interconnects, silicon carbide, statistical tolerance analysis.

## I. INTRODUCTION

POWER electronics has shifted from the long-standing use of silicon (Si) devices to exploring the capabilities that wide-bandgap (WBG) devices can offer [1], [2]. WBG devices have allowed for miniaturization and performance developments in electric transportation [3], [4], renewable energy [5], [6], and grid connection [7], [8]. The packaging of these devices proves challenging as traditional packaging schemes for Si,

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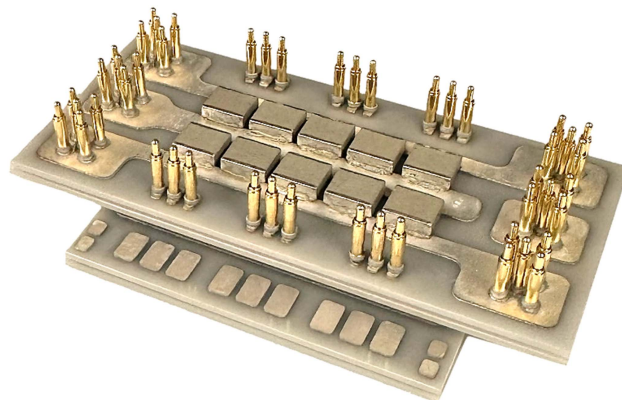


Fig. 1. Parallel-plate, wirebond-less, 13 kV SiC half-bridge MCPM designed in [13] and using advanced packaging techniques in [14].

when applied to SiC devices, have limited the ability of SiC to meet the demands of the previously noted applications.

Wirebond interconnects have been a long-standing technology in Si packaging due to their cost-effective, mature manufacturing processes, and flexibility [9]. For medium-voltage SiC modules, this technology introduces significant challenges, such as large footprints for lateral bonding that reduce power densities and contribute to the commutation loop inductance [10], [11]. The high power loop inductances can be detrimental to medium-voltage SiC switching characteristics [12].

The advancements of SiC devices have been accompanied by the advancement in more appropriate packaging schemes, applied to the module in Fig. 1. Packaging engineers have increasingly replaced wirebonds with ribbons, clips, and double-sided interconnect bonding to improve reliability for WBG devices [15]. The use of post interconnects from the die to the substrate instead of wirebonds enables parallel-plate power modules (see Fig. 2) with high power densities, low power loop inductances, improved coefficient of thermal expansion matching [13], and better thermal performance due to the ability for double sided cooling [16], [17]. Additionally, bonding with nano-silver (Ag) paste instead of multiple solder alloys of descending reflow temperatures allows for the construction of complicated module structures in multiple steps without limiting the high-temperature performance [13], [18], [19].

The package structure now adopted for SiC devices mainly utilizes this parallel-plate vertical structure (see Fig. 3), where the die is bonded to the bottom substrate or printed circuit board (PCB), several posts or clips are bonded to the top side

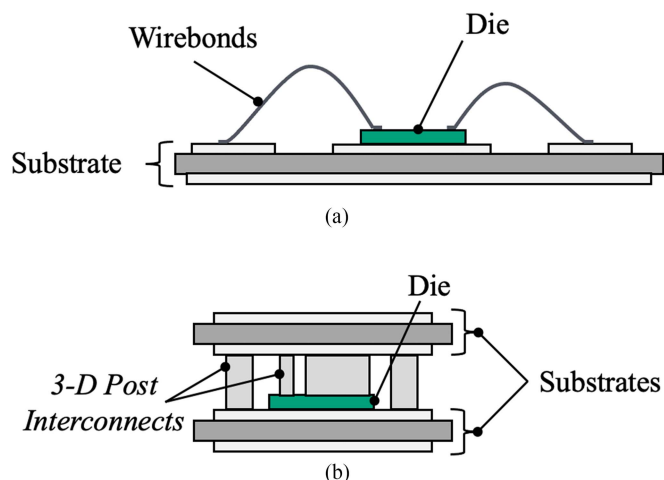


Fig. 2. (a) Wirebonded interconnects for lateral bonding, versus (b) post interconnects for vertical bonding.

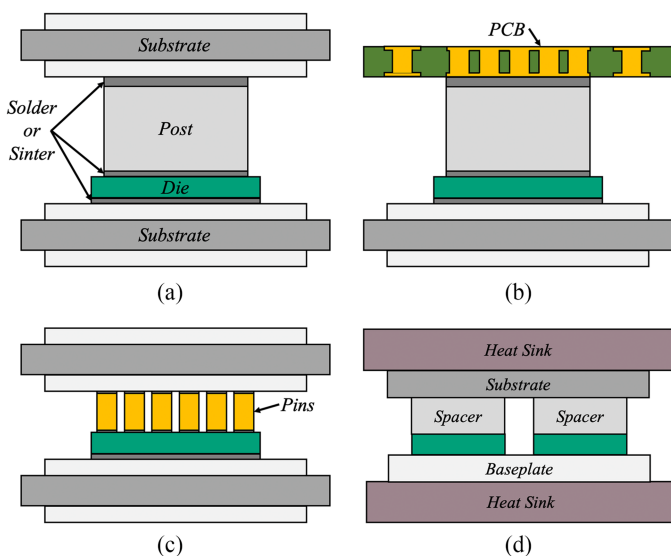


Fig. 3. Different parallel-plate modules across literature and industry, fabricated using (a) post interconnects with substrates, (b) post interconnects with substrates and PCBs, (c) pin interconnects with substrates or PCBs, and (d) spacers with pressure contacts (press-pack style).

of the die, and the topside of the post is then bonded to the top substrate or PCB [16], [17], [20], [21], [22], [23], [24], [25], [26]. The wet bondline is typically nano-Ag paste or solder. The post interconnects/spacers/clips vary from copper (Cu) [27], [28], molybdenum (Mo) [13], [16], [23], [24], and Cu-Mo alloy [21], each for accommodating the thermomechanical stresses based on different module designs and materials [29]. These modules have been demonstrated as IGBTs [22], rectifiers [17], phase-leg inverters [22], half-bridge configurations [13], [16], [30], and full bridges [24] across research. Within the industry, various modules with this structure have been developed, from Siemens [31], ABB [32], ON semiconductor [33], Infineon [34], and Delphi [35]. It is noted that these modules vary between SiC and Si, and the voltage ratings are less than 3.3 kV.

Connecting devices in parallel within the power module improves the current rating and power density while reducing control complexity and safety at the converter level [12],

[36], [37], [38], but the fabrication process for multichip power modules (MCPMs) proves challenging. The combination of warpage from large substrates [39], [40], machined post height tolerances, and sinter bondline thickness variations increases the difficulty in achieving planarity across all post interconnects. As an MCPM is fabricated, these variations compound at every layer, resulting in a considerable variation for the final bondline to absorb [18]. These variations only become worse with more die in parallel. From the demonstrated modules following this parallel-plate, structure many have been limited in the number of die or post interconnections and the voltage ratings compared to the module in [13].

Out of five previous attempts to fabricate the module in [13], none have resulted in a module with all devices connected and operable. The modules had an average of 49% of devices connected, and of the devices that were connected, 0% had bonds less than 10 m $\Omega$ , 45.8% were between 10 m $\Omega$  and 1 k $\Omega$ , and 22% were greater than 6.5 k $\Omega$ . The scope of this work defines a functional module as all posts being connected, and the devices are deemed operable if their bonds connecting to the terminals are less than 10 m $\Omega$ .

Others are trying to use this structure for the performance advantages previously noted, but it is challenging in terms of manufacturability and tolerancing when scaling the number of die. Outside of this work, from [41], a press-pack MCPM with a parallel-plate structure and post interconnects had issues with even pressure applied across the module. Not all the devices were successfully connected in the module because of height tolerancing errors of the components. Another press-pack MCPM was conceptually designed to operate with 30 devices; however, the demonstration of devices was derated by 80% [42].

A double-sided cooled half-bridge with post interconnects and sintered bonds rated for 1600 A and 32 die per switch position (64 total) from [43] uses a similar structure to this MCPM to meet a power loop inductance requirement of 1 nH, something that cannot be achieved with a wirebonded module. The work noted that the challenges of the fabrication were height differences to connect the posts to the top substrate and noted height tolerances from the components below the posts added to the height mismatch. Not one module fabricated could connect all die, thus, static characterization was performed to only 8% of the rated current, and double-pulse tests were performed at 25% of the rated current because many posts were disconnected from the top substrate, leaving many die per switch position useless.

For parallel-plate MCPMs, the variations in the parts and unsuccessful fabrication point to a tolerance issue. Tightening component tolerances, while a valid solution, may increase tooling and inspection costs while negatively impacting individual component yield. Utilizing a statistical approach to tolerance analysis for the MCPM quantifies the impact of the individual component tolerance distributions. The insights: 1) enable targeted efforts to improve the tolerance of a specific component/process rather than a holistic approach, and 2) inform redistribution of the tolerance allocation to components that are more cost-effectively controlled. The improved tolerance robustness allows parallel-plate MCPMs to scale to higher power levels, with more die in parallel without compromising yield.

Tolerance analysis methods are applied widely across manufacturing and engineering. Many tolerance analyses have targeted the gaps between components that must mate for proper operation, such as gear teeth [44] and flange gaps when assembling the towers of wind turbines [45]. The Monte Carlo has also been utilized in circuit design optimization and component sensitivity [46], [47], [48]. Within power electronics, a handful of tolerance analyses have been conducted comparing the benefits of statistical analyses, specifically the Monte Carlo simulation, over worst-case analyses [49]. This includes the assembly of QFN packages to minimize lead pullback [50] and delamination [51], proper tolerances for assembly of PCB daughter cards [52], alignment tolerances of press-fit pins on PCBs to motors [53], and vertical fabrication of package-on-package low-voltage modules [54]. The Monte Carlo simulation has been a staple in reliability analyses regarding the thermal and thermomechanical performance of heat sinks [55], thermal cycling and lifetime [56], solder bond stress and lifetime performance [57], and die characteristics to improve electrothermal performance of paralleled devices [58]. It has also been used to optimize thermal reliability designs of MCPMs [59]. These statistical analyses have been used across power electronics and manufacturing assemblies to improve yield but have yet to be applied to the next-generation structure of power module packaging assemblies.

Since the future of packaging is shifting to parallel-plate structures, it is vital to conduct a statistical tolerance analysis to identify which components are bottlenecks for the yield of MCPMs to accelerate adoption into wide-scale manufacturing. This is the first statistical tolerance analysis done to analyze the variation in sinter bond thicknesses and quantify the variation for each component in the MCPM.

## II. MOTIVATION FOR A STATISTICAL TOLERANCE ANALYSIS USING A MONTE CARLO SIMULATION

Tolerance analysis methods are commonly used to quantify the variation in a part or its assembly. Different categories of analysis include the dimensions of study (one-dimensional (1-D), 2-D, or 3-D) and the type (worst-case or statistical). These analyses are often applied to each part population to quantify variance between different manufactured lots, but they are also applied to stacked assemblies where tolerances accrue on each other [49]. The half-bridge parallel-plate MCPM in Fig. 4 is an example of a stacked assembly; however, no literature on applied tolerance analysis could be found. The following sections will discuss the different types of tolerance analyses and which to apply to fabricating this parallel-plate MCPM.

### A. Worst-Case Tolerance Analysis

The flaw of designing assemblies based on worst-case tolerances is that constraints are based on two specific cases (the minimum and maximum possible heights of each component) that are statistically very rare [60], [61]. This produces assemblies that are overengineered for the majority of cases. Additionally, if the resulting tolerance range is too large, no insights are gained to inform targeted error reduction and a holistic approach is required to improve the assembly. The result is increased

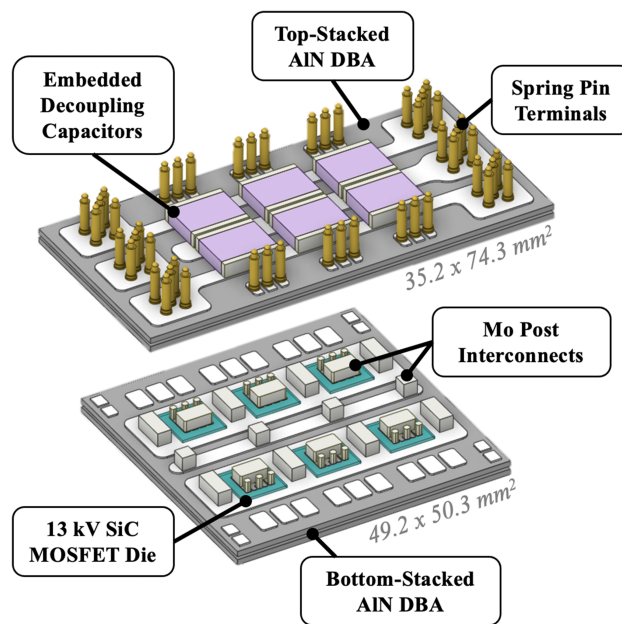


Fig. 4. Half-bridge MCPM from [13], detailing the number of components contributing to the variation of heights when assembling the parallel-plate module.

manufacturing cost, lead times, and potentially lower yield [50], [53], [62].

### B. Linear Statistical Tolerance Analysis

Linear statistical analysis improves on worst-case analysis by 1) including information on the probability of occurrence, and 2) allowing 2-D and 3-D tolerance analysis via analytical and algebraic expressions [49], [63], [64]. Statistical-based tolerance analyses allow for insightful judgments on process modifications as compared to a worst-case analysis. Linear statistical analysis is conducted using a root sum squares (RSS) method, representing the variation distribution for each part within an assembly included in the tolerance stack-up. This begins with a histogram, which represents the frequency a data point occurs. A distribution is then fit to the histogram to represent the part height population trend [65]. Using the distribution created from a population of measured parts, a probability density function (PDF) is generated. A PDF represents the prospect of a particular part occurring and is fit to a histogram of measured parts [49], [65]. The tolerances generated from the PDF are more representative of physical parts and are typically less restrictive than the extreme tolerances generated from worst-case analysis. Using RSS, every part within the assembly has a tolerance modeled by a distribution instead of solely the minimum and maximum values [66].

A key limitation of linear tolerance analysis, such as the RSS method, is the assumption that components are normally distributed across the tolerance range with a mean at the nominal value, which is typically untrue for manufactured parts. As a result, batch-to-batch variation, which manifests as overlapping normal distributions, and offsets (i.e., mean is not equal to the

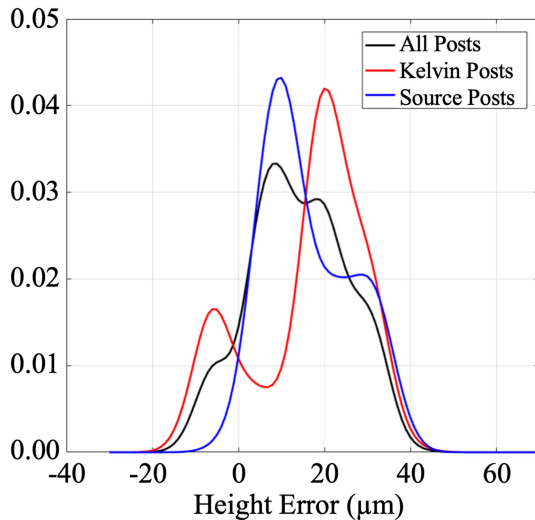


Fig. 5. Probability density function of the measured posts in the MCPM exhibiting non-normal behavior.

nominal values) cannot be represented and included in the analysis as their distributions are not normal. Fig. 5 shows the measured tolerance density functions for different post interconnects in the MCPM. The posts were specified to the manufacturer with a  $\pm 50 \mu\text{m}$  tolerance and are plotted as a height error from their desired height. Not only is the true variation much less than the specified tolerance, but the distribution is not normal, indicating the mean is skewed from the desired height error of  $0 \mu\text{m}$  from the manufactured height. Many manufacturing processes result in non-normal and shifted tolerance distributions, meaning linear statistical analysis is unsatisfactory [49], [61].

### C. Monte Carlo Nonlinear Statistical Tolerance Analysis

Monte Carlo nonlinear analysis builds on the backing of linear analysis but adds the ability to utilize arbitrary tolerance distributions and complex relationships between tolerances that do not follow normal distributions [67], [68]. A Monte Carlo simulation models the probability of tolerance outcomes from an assembly using random sampling of part distributions [49], [50], [69]. This allows for a better representation of tolerance distributions from manufacturing assemblies [70]. The Monte Carlo simulation for the statistical tolerance analysis leverages pieces of the linear tolerance analysis such as the histogram, distribution, and PDF generation, and can be conducted as follows [49], [70].

- 1) Identify the critical dimension to evaluate.
- 2) Obtain a histogram and distribution of measured parts.
- 3) Create a PDF for the distribution of each part.
- 4) Randomly sample each distribution the number of times the part occurs in the assembly and generate a new histogram from the samples (the Monte Carlo step).
- 5) Fit a new distribution to the histogram created from the Monte Carlo and create a PDF from that distribution.
- 6) Integrate the PDF to obtain the cumulative density function (CDF). The CDF demonstrates the probability of an outcome being less than or equal to a certain value.

While Monte Carlo analysis is the most demanding of all the techniques discussed, thus far, it represents the most comprehensive method for modeling and understanding the nuances of component tolerances distributions and, thus, was chosen as the appropriate statistical tolerance analysis method to analyze the gap from the posts to the top substrate that needs to be filled in these parallel-plate MCPMs.

## III. STATISTICAL TOLERANCE ANALYSIS: MONTE CARLO SIMULATION FOR A PARALLEL-PLATE STRUCTURE MULTICHIP POWER MODULE

The Monte Carlo simulation method for statistical tolerance analyses is chosen to solve for the probability of the maximum height mismatch across the Mo posts that the top substrate will solder to in the MCPM. The Monte Carlo process represented in Fig. 6 follows the procedure from Section II-A, but is specified for the MCPM tolerance analysis. The stacking of the following parts represents the critical dimension in the MCPM in Fig. 7: substrates, sinter bonds, die, and posts. Each part of the assembly will have measurements taken, distributions created, and PDFs generated from 10 000 samples, allowing for a robust distribution that proved convergence.

### A. Generating Component Distributions

Component distributions were generated using on-hand inventory. In total, 35 screen-printed and 66 hand-dipped sinter bonds, 27 die, 63 midplane posts, 105 DBA posts, 134 source posts, and 308 kelvin-source/gate posts were measured. A Mitutoyo Digimatic micrometer, with a resolution of  $1 \mu\text{m}$ , was used to measure all the posts. Both the hand-dipped and screen-printed sinter bonds were measured by sintering posts to a glass slide. The glass slide was premeasured along with the posts, and the thickness of the sintered bond was calculated. The die were measured using the Bruker DekTak stylus profilometer, which has a resolution of  $200 \text{ nm}$ .

Once every component was measured, a histogram is created, representing the height error from the nominal value. Using the height error instead of the nominal immediately allows tolerances to add to a net relative mismatch. Components deviating from their nominal can still yield the goal of minimum mismatch when paired with components that deviate in the opposite direction. A distribution is then fit to the histogram. Two different distributions are created since there are two types of sinter bonds (hand-dipped and screen-printed).

Within the hand-dipped distribution are further subdistributions to account for different-sized posts having unique bondline variations. Every post type has a different distribution since each post type is machined in different manners. Finally, a distribution is generated for the 13 kV SiC die. No accurate distribution representative of the population can be created for the substrates since only five samples were taken. After analyzing the distributions, the best-fit distribution was a Kernel distribution. They are often applied to data from manufacturing processes that are nonlinear [71], [72]. An example of the unique part distributions is shown in Fig. 8, while the detailed distributions are in Fig. 9

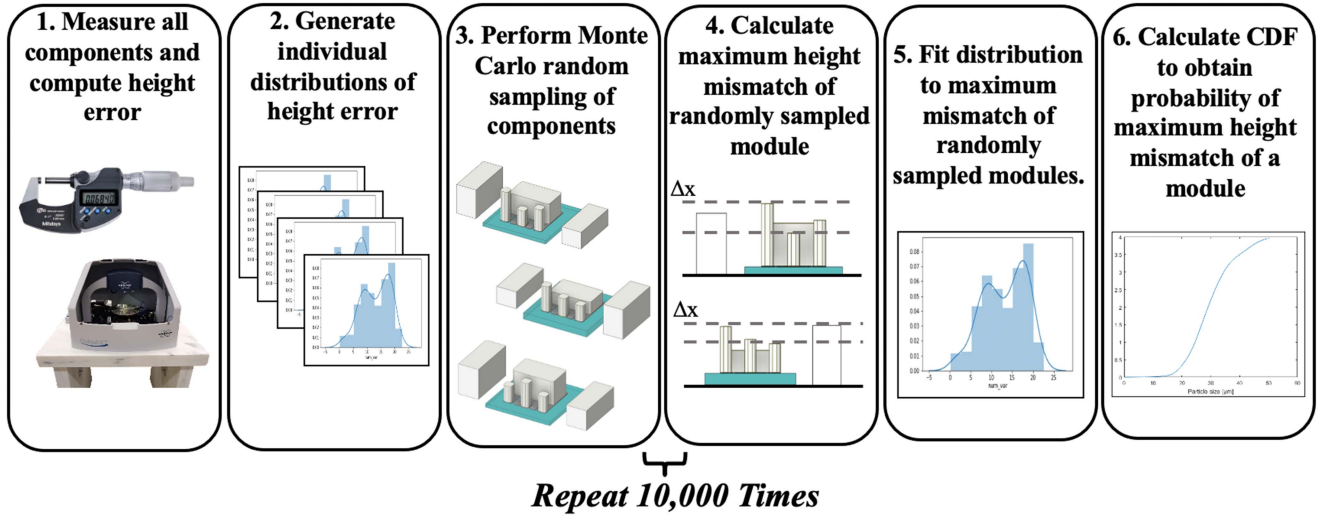


Fig. 6. Monte Carlo simulation process applied to an MCPM to quantify the maximum height mismatch from the variation of part tolerances on the assembly.

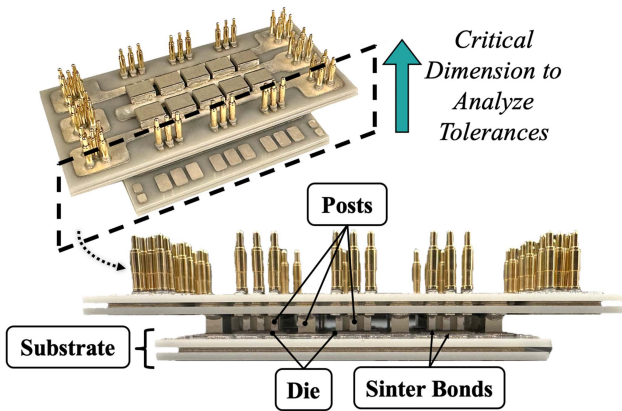


Fig. 7. Critical dimensions and parts to conduct the statistical tolerance analysis for the MCPM.

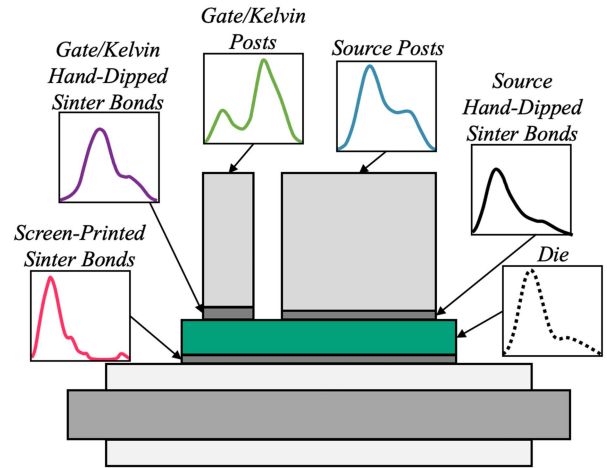


Fig. 8. Representative figure of part distributions generated from measuring each component in the MCPM stack-up based on the critical dimension.

for all of the different post interconnects, Fig. 10 for the different sinter bonds corresponding to how they are dispensed for each post interconnect and die, and Fig. 11 for the die used in the MCPM.

To ensure a representative sample size of each component and validate the distributions generated, a confidence interval analysis was performed. The confidence interval analysis indicates a percentage of confidence that the true mean of the population falls within the range of samples measured [73]. This method has been used to validate that the distributions created from sampled data can be representative of the population for future analyses and decisions, notably in power electronics reliability studies [74], [75], [76], [77]. Table I shows the mean, the standard deviation, and a 95% confidence interval for where the population mean will fall in each of the component distributions. Since each sample mean fell within one standard deviation of the 95% confidence interval, this is a high enough certainty to move forward and feel confident the sample accurately represented the population.

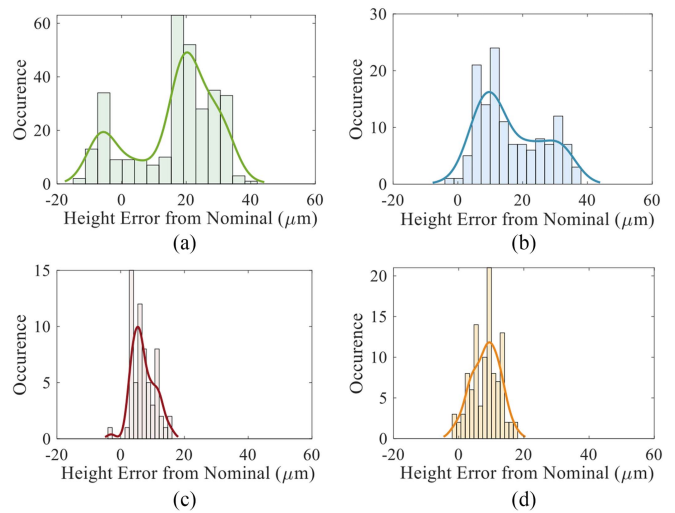


Fig. 9. Post distributions of (a) kelvin and gate posts, (b) source posts, (c) midplane posts, and (d) DBA posts.

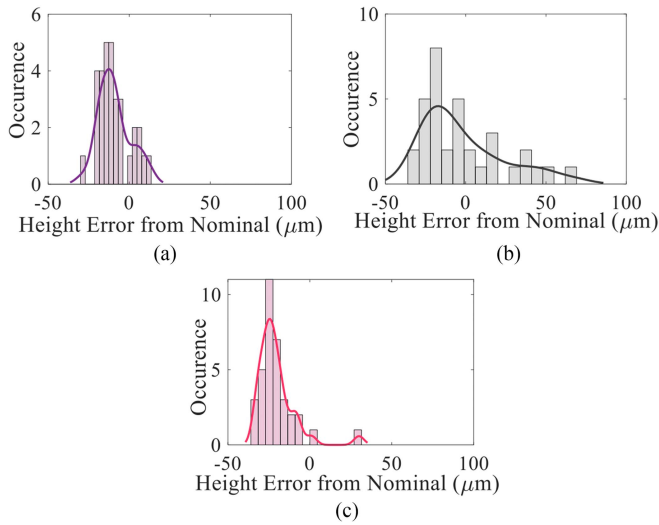


Fig. 10. Sinter bond distributions of (a) kelvin and gate post hand-dipped sinter bonds, (b) source post hand-dipped sinter bonds, and (c) midplane post, DBA post, and die screen-printed sinter bonds.

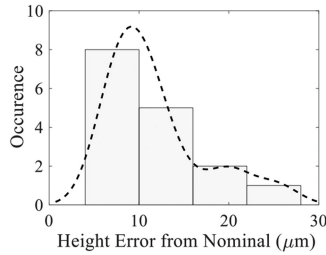


Fig. 11. 13 kV SiC Die distribution.

TABLE I  
CONFIDENCE INTERVAL ANALYSIS OF COMPONENT DISTRIBUTIONS

Component	Mean ( $\mu\text{m}$ )	Standard Deviation ( $\mu\text{m}$ )	95% Confidence Interval ( $\mu\text{m}$ )
Die	11.81	5.48	[9.13,14.58]
Screen-Printed Sinter Bonds	-20.43	11.82	[-24.34,-16.51]
Kelvin Hand-Dipped Sinter Bonds	-9.28	9.85	[-12.69,-5.86]
Source Hand-Dipped Sinter Bonds	-1.62	25.96	[-10.35,7.11]
Gate/Kelvin Posts	16.28	12.83	[14.85,17.72]
Source Posts	16.29	9.91	[14.61,17.97]
Midplane Posts	7.11	3.65	[6.21,8.01]
DBA Posts	8.30	4.27	[7.48,9.11]

B. Building the Monte Carlo Simulation

An example of the Monte Carlo simulation for six different post locations in the module is shown in Fig. 12. The locations consider four posts on one die as well as the two other posts located on the substrate. The unique distributions for each component in Fig. 12 feed into the Monte Carlo simulation. The simulation randomly samples each distribution for each occurrence of a part in the MPCM.

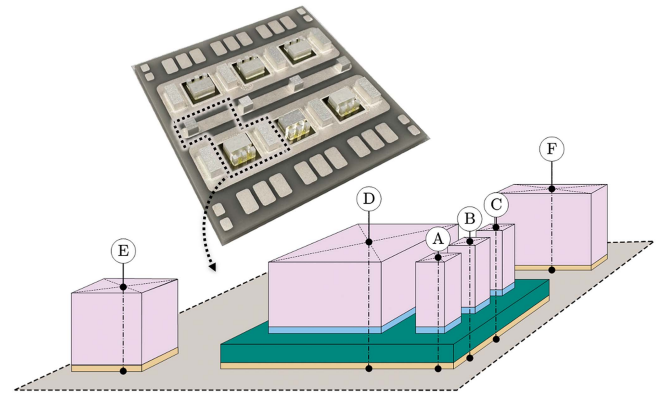


Fig. 12. Monte Carlo simulation process demonstration for six different post locations on the MPCM. The component distributions are represented in Fig. 13, corresponding to the screen-printed sinter bond (yellow), the die (green), the hand-dipped sinter bond (light blue), and the posts (light pink).

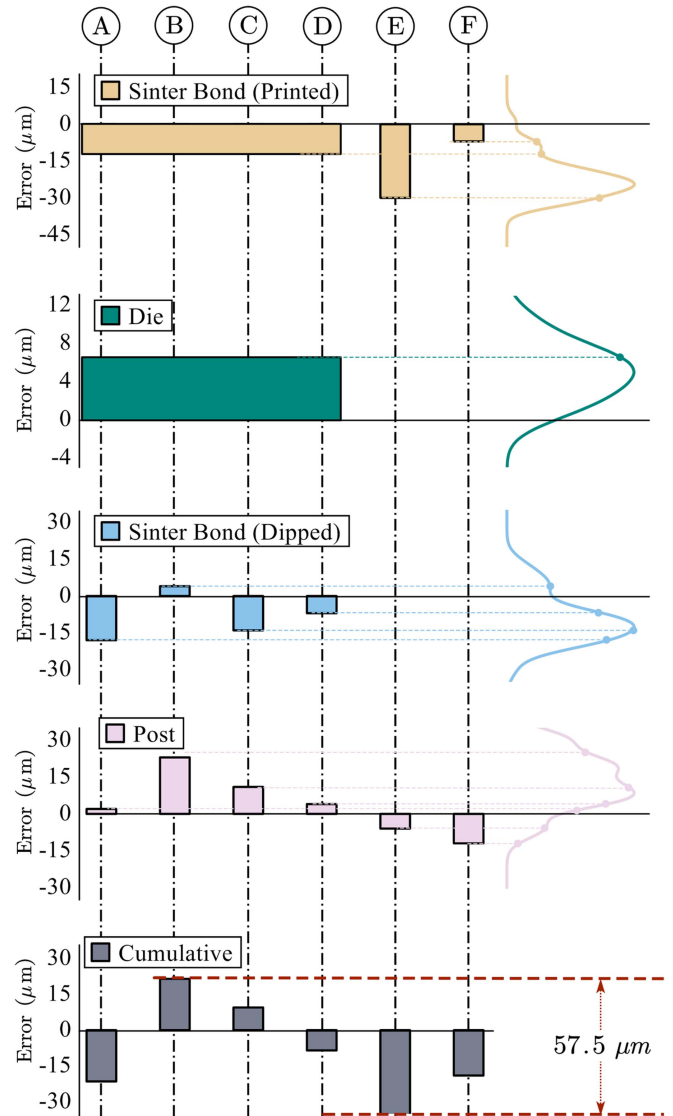


Fig. 13. Randomly sampling part distributions based on the fabrication of the MPCM for the components represented in Fig. 12 and calculating the maximum height mismatch at each location.

TABLE II  
NUMBER OF COMPONENTS SAMPLED FOR EACH MODULE ANALYZED IN THE MONTE CARLO

	Single-Die	Two-Die Module	MCPM
Screen-Printed Sinter Bonds	0	6	18
Die	1	2	6
Hand-Dipped Sinter Bonds	4	8	24
Kelvin Posts	2	4	12
Gate Posts	1	2	6
Source Posts	1	2	6
Midplane Posts	0	2	4
DBA Posts	0	4	8

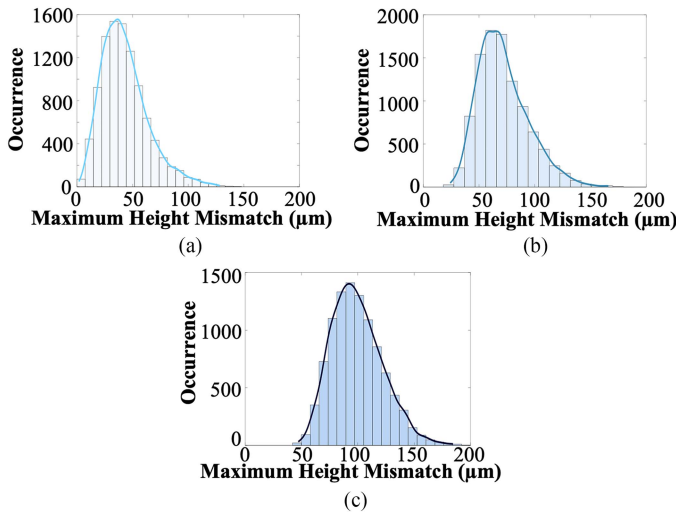


Fig. 14. Monte Carlo distributions for (a) a single die, (b) a two-die module, and (c) an MCPM.

For the partial module image in Fig. 12, three screen-printed sinter bonds, one die, four hand-dipped sinter bonds, two kelvin posts, one gate post, one source post, one midplane post, and one DBA post are sampled from their distributions in Fig. 13. Given the samples, their accrued height mismatch is calculated at each point noted in Fig. 12. The maximum height mismatch across the module is measured, resulting in the largest possible gap for the solder to fill (for this example,  $57.5 \mu\text{m}$ ). The number of components for each type of module case is shown in Table II, highlighting the MCPM in the fourth column. This sampling process is repeated 10 000 times for the number of components noted in Table II to simulate the fabrication of 10 000 modules in order to build a robust distribution that ensured convergence of the results [69]. This Monte Carlo simulation was conducted for multiple cases: a single die, a two-die module, and the MCPM, and the resulting distributions for each are shown in Fig. 14, increasing in height mismatch from a single-die module to the MCPM.

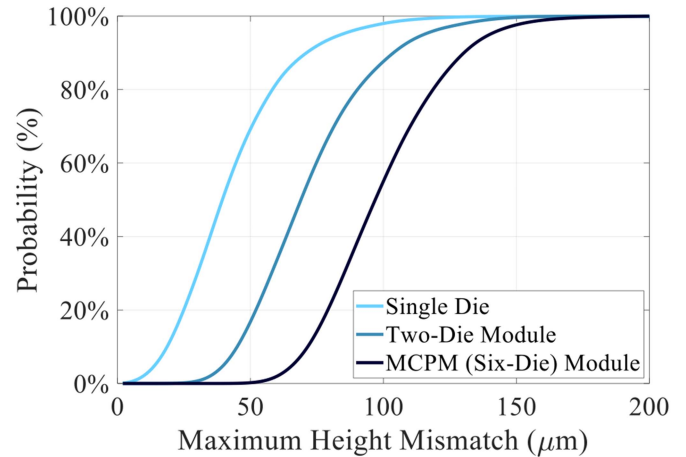


Fig. 15. Cdfs representing the probability of achieving a particular maximum height mismatch for a single die, a two-die module, and an MCPM plotted from left to right.

### C. Results From the Monte Carlo Simulation

The cdfs plotted in Fig. 15 show a positive trend between the number of die in a module and the maximum height mismatch across that module. It is impossible to achieve  $0 \mu\text{m}$  of a mismatch for an MCPM, and only 55% likely of achieving a height mismatch of less than  $100 \mu\text{m}$ . Previous work was able to fabricate twelve two-die modules without any missing post-to-substrate bonds. In contrast, five previous attempts at fabricating the MCPM have resulted in no successful modules. This indicates that the CDF generated for the two-die module has a low enough mismatch to connect all the posts successfully. In contrast, the CDF of the MCPM indicates that the possible height mismatches are too significant to fabricate functional modules.

From this analysis, the yield discussion is based on engineering knowledge and inferences made from the CDF. The CDF does not directly indicate a yield percentage but only the probability of achieving a particular height mismatch across a module, which significantly impacts the yield and successful connection of every post across the MCPM. One beneficial study of these results would target the components that contribute the most to the maximum height mismatch, how much it contributed, and propose solutions to reduce the mismatch from said component. A better understanding of these relations will be explored in the following section.

## IV. IDENTIFYING CONTROL VARIABLES IN THE MULTICHIP POWER MODULE USING ANOVA AND TUKEY'S ANALYSIS

Controllable variables are components of an assembly stack-up that most impact the maximum height mismatch and are targeted for mismatch reduction. Statistical experiments done in this manner have demonstrated improved yield when applied to manufacturing procedures [65, pp. 540–545], [65, p. 549]. An ANOVA analysis compares the means of different treatments (the components) to see if they are statistically different from the response (the maximum height mismatch). However, it only identifies that a difference exists, not which specific treatments are statistically different. By using Tukey's honestly significant

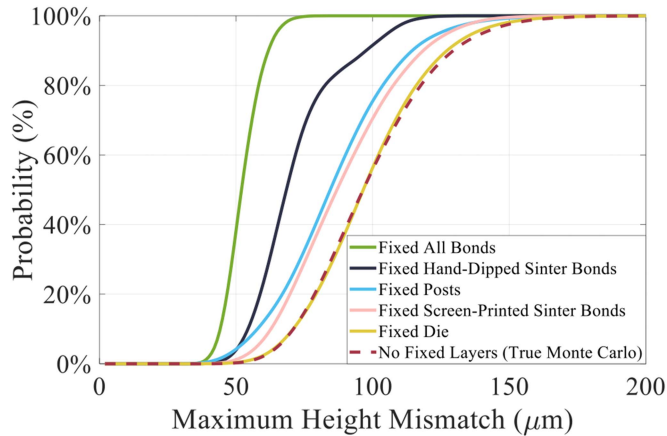


Fig. 16. Cdfs representing the probability of achieving a particular maximum height mismatch when fixing different layers to zero mismatch, including all bonds (green), hand-dipped sinter bonds (navy), posts (light blue), screen-printed sinter bonds (pink), die (yellow), and the true random Monte Carlo (dashed red), plotted from left to right.

TABLE III  
MULTICHIP POWER MODULE ANOVA RESULTS FROM DIFFERENT FIXED HEIGHT MISMATCHES

Source	Treatments	Error	C. Total
Degrees of Freedom	5	59994	59999
Sum of Squares	2844.98	2871.37	5719.35
Mean Square	568.995	0.048	
F Ratio	11888.5		
Prob > F	0		

difference (HSD), the output of the ANOVA results can then be analyzed further, and the statistically different treatments can be identified [79].

Fixing each component in the MCPM to zero mismatch is a different treatment, and the response is the maximum height mismatch across the MCPM. The Monte Carlo Simulation developed in Section III is done six times, fixing a different component to zero mismatch each time during the sampling of 10 000 modules. The cdfs from each Monte Carlo simulation are shown in Fig. 16. Visually, the CDF indicates different treatments have statistically different means, but the ANOVA and Tukey's must be completed for statistical analysis.

As shown from the ANOVA results in Table III, the p-value returned is less than 0.05, and the large F-statistic means a statistical difference between treatments exists. From Tukey's analysis in Table IV, an ordered letters report identifies that every treatment except for the die is statistically different from the true Monte Carlo simulation, meaning each component except the die can impact the maximum height mismatch. The magnitude of impact from each fixed layer is quantified by the distance the mean is from the control mean. Fig. 16 provides visual evidence of which components to target, and when analyzing the means in Table IV, the three most impactful treatments are: 1) hand-dipped sinter bonds, 2) posts, and 3) screen-printed sinter bonds. Using this analysis, three modules will be fabricated to reduce the maximum height mismatch and improve the yield of these MCPMs by successfully fabricating functional modules,

TABLE IV  
TUKEY'S HSD ORDERED LETTERS REPORT FROM DIFFERENT FIXED HEIGHT MISMATCHES

Treatment					Mean	P-Value
CONTROL: No Fixed Layers (True Monte Carlo)	A				4.5675	NA
Fixed Die	A				4.4207	0.55
Fixed Posts		B			4.5623	$2.07 \cdot 10^{-8}$
Fixed Hand-Dipped Sinter Bonds			C		4.2393	$2.07 \cdot 10^{-8}$
Fixed Screen-Printed Sinter Bonds				D	4.4597	$2.07 \cdot 10^{-8}$
Fixed All Sinter Bonds				E	3.9447	$2.07 \cdot 10^{-8}$

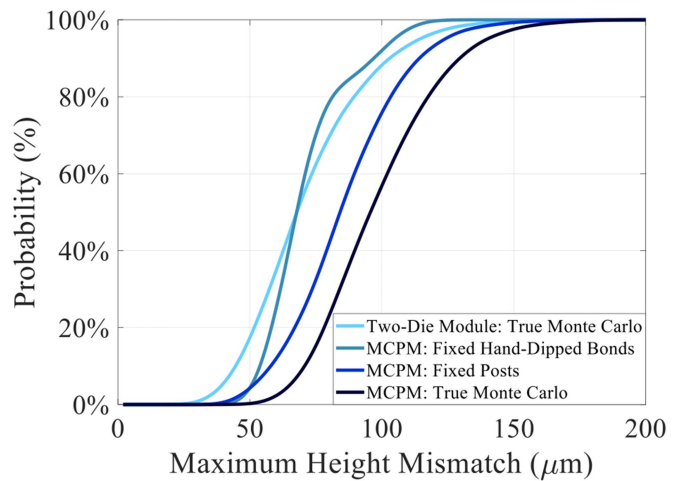


Fig. 17. Cdfs representing the probability of achieving a maximum height mismatch for the two-die module true Monte Carlo, MCPM with fixed hand-dipped sinter bonds, MCPM with fixed posts, and MCPM true Monte Carlo.

which as previously stated, in the scope of this work, a functional module has all posts connected and the devices are deemed operable if their bonds connecting to the terminals are less than 10 m $\Omega$ .

## V. MODULE FABRICATION USING THE STATISTICAL TOLERANCE ANALYSIS

The results from the statistical tolerance analysis demonstrate that the successful fabrication of the MCPM is not trivial. The variation from the additional die in parallel, thus, additional posts and sinter bonds, compound on each other during fabrication. To fabricate the MCPMs, the statistical tolerance analysis is used to inform fabrication decisions to reduce the maximum height mismatch using the cdfs shown in Fig. 17. Historically, the two-die module has been fabricated with 100% yield of all posts connected from twelve attempts. This is due to the lower height mismatch, as the CDF shows, compared to the MCPM. It is used as a benchmark to indicate how effective fixing different components for the MCPM can be to result in a functional module.

The sinter bonds, specifically hand-dipped, result in the lowest mismatched when fixed. However, this would require replacing

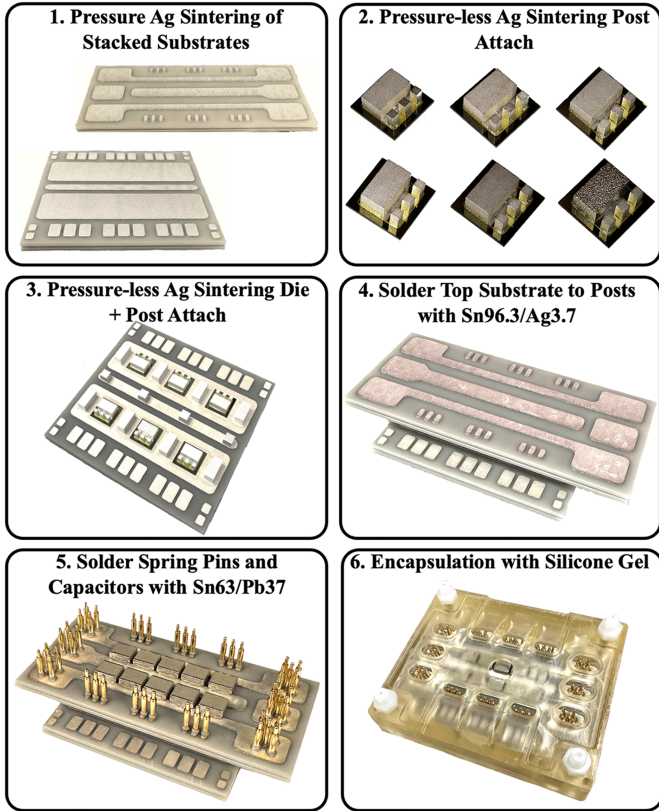


Fig. 18. Fabrication of the MCPM using fixed post heights from the statistical tolerance analysis.

the hand-dipped sinter bonds with a more controlled bondline like sinter preform [80]. Since this required more analysis and there are limited 13 kV die, it was decided to fix the post heights to the least possible mismatch ( $15 \mu\text{m}$ ). This option is more straightforward and is the second most effective method from the ANOVA and Tukey's HSD analysis in the previous section. The CDF in Fig. 17 also indicates it is an effective method for reducing the maximum height mismatch.

The module is fabricated accordingly in Fig. 18, described in [13] and [14] with more detail in terms of the module design and advanced packaging techniques used. Every post for each device was electrically connected to the terminals, with bonds measuring resistances less than  $10 \text{ m}\Omega$ , and an average bond resistance of  $4.15 \text{ m}\Omega$ . From the fabrication attempts before this statistical tolerance analysis, the modules had an average of 49% of the devices being connected, and of the devices that were connected, 0% measured bonds less than  $10 \text{ m}\Omega$ . The MCPM fabricated in this work has 100% of devices connected with these criteria.

## VI. MULTICHIP POWER MODULE ELECTRICAL CHARACTERIZATION

The SiC devices used in fabricating the MCPM are 13 kV, 5 A MOSFETs from the National Institute of Advanced Industrial Science and Technology. Once fabricated, the module is connected to the Keysight Agilent B1505A curve tracer. The forward characteristics are detailed in Fig. 19 for the high-side

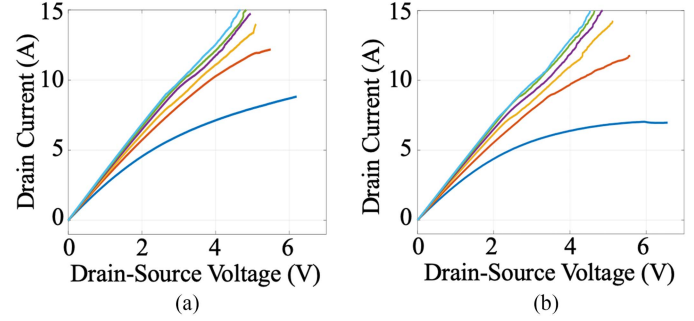


Fig. 19. Forward characteristics of the (a) high-side MOSFETs and (b) low-side MOSFETs in the MCPM.

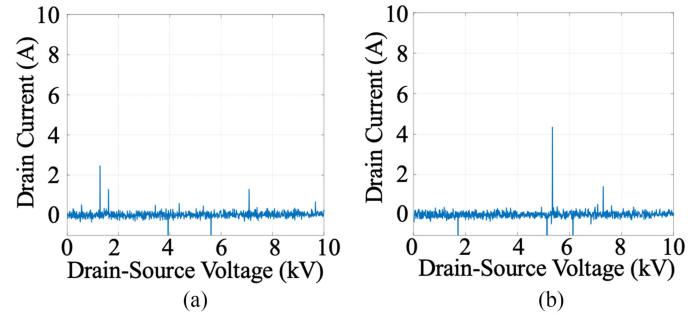


Fig. 20. Blocking voltage versus leakage current of the (a) high-side MOSFETs and (b) low-side MOSFETs in the MCPM, limited to 10 kV by the curve tracer.

and low-side SiC MOSFETs, indicating healthy operation and that every device is successfully connected to supply the rated 15 A of three devices in parallel. The blocking voltage versus leakage current for both the high-side and low-side devices is in Fig. 20, and both devices exhibit no drain leakage current up to 10 kV, limited by the maximum voltage rating of the curve tracer.

Five previous fabrication attempts of this MCPM have resulted in zero successfully fabricated modules from the criteria of every device connected and operable. The statistical tolerance analysis developed in this work resulted in a statistical conclusion for the low yield of functional modules. The ANOVA and Tukey's analysis information targeted, which components introduce the most mismatch. Using this, the module fabrication was informed and controlled, reducing the mismatch and resulting in the first functional MCPM of this kind. While this analysis resulted in the successful fabrication of this module design, the Monte Carlo simulation can be easily applied to many different power modules using these standard components and structures. Additionally, the analysis can be extrapolated to generate further knowledge to inform the packaging and design decisions for this MCPM.

## VII. DISCUSSION ON FURTHER APPLICATIONS FOR THE MONTE CARLO SIMULATION IN MULTICHIP POWER MODULES

The statistical analysis applied to this MCPM enables an investigation into the different sources of error in the assembly and identifies cost effective means of addressing them. This section will expand on the application of the analysis both with and beyond this module.

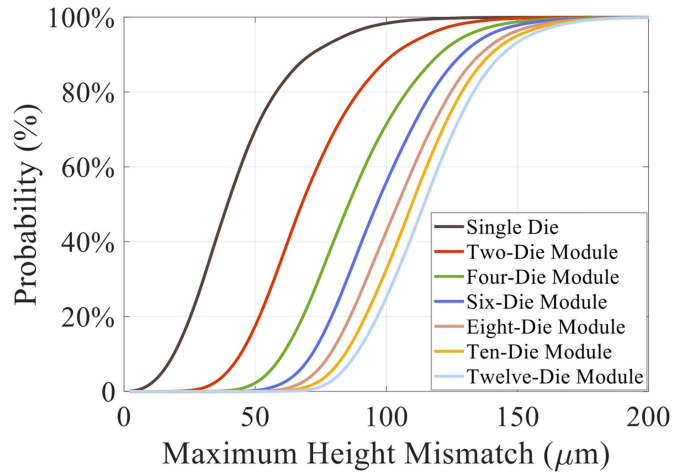


Fig. 21. Cdfs of the maximum height mismatch, scaling from a single die to a twelve-die module (from left to right).

Fig. 21 showcases the challenges associated with increasing the number of die in an MCPM beyond this six-die module. Even though the component tolerance distributions remain identical, the higher number of components increases the likelihood of using components at the ends of the tolerance distribution, increasing the maximum height mismatch. The CDF plateaus as the number of die increase, indicating that continued sampling of components means the extent of the phenomenon has been captured. However, this does not imply that the severity of height mismatch concerns will subside. This statistical tolerance analysis is required to identify solutions and inform engineers when evaluating the scalability of a module to theoretical modules with more die in parallel.

The Monte Carlo analysis in this work was used to identify components with large variations and eliminate the variation to observe the impact on fabricating a functional MCPM. While this component-based method proved effective, the Monte Carlo points to a process modification that will further reduce the maximum height mismatch in Fig. 16: fixing the hand-dipped sinter bonds by using Ag preform. The predried Ag preform eliminates nearly all variation in the bondline. When analyzing the maximum mismatch of increasing die in parallel when replacing the sinter bonds with preform, the probability of achieving 100  $\mu\text{m}$  of mismatch increases from 25.1% to 82.1% (see Fig. 22).

Another modification that the Monte Carlo suggests involves the module structure. The parts in this structure can only be designed to certain tolerances, and their warpage is inevitable. Designing out components with large variations can aid in shifting the CDFs to the left, while allowing components with larger tolerance ranges more flexibility in their distributions. One example could be exchanging a substrate, which results in large variations from machining, to a simpler contact that can be specified on the order of microns. Another would be to introduce compliance in the stack-up, such as less-rigid posts that can aid in absorbing geometric variations [20]. The component and process modifications are fabrication decisions that can be made after the design of the power module, but the structure change

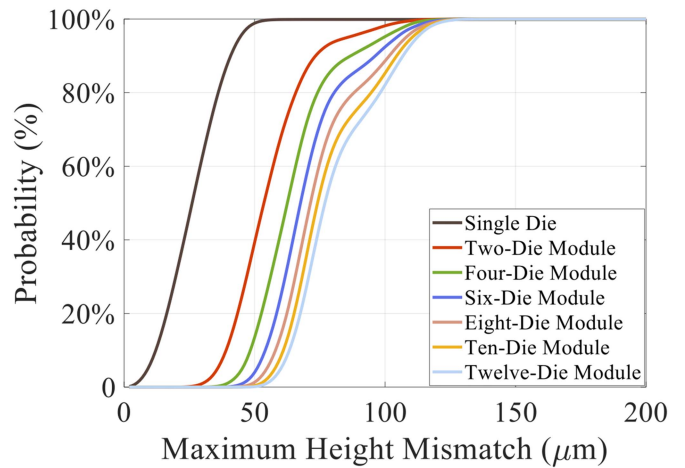


Fig. 22. Cdfs of the maximum height mismatch, scaling from a single die to a twelve-die module (from left to right) when using Ag preform instead of nano-Ag paste for the sinter bonds.

would need to be considered in the initial design stages of an MCPM.

Beyond this module, two different parallel-plate modules were noted in Section I that experienced fabrication tolerance challenges [41], [43]. Since these modules use similar components (post interconnects and sinter bonds), the result of this analysis can be extrapolated to their components and processes to improve yield. This study also informs the packaging field of critical components that impact yield when creating future designs of modules with many die in parallel.

The statistical tolerance analysis was leveraged in this article to identify which component to target, but that is not the only question the Monte Carlo simulation answers. This work sheds light on the following:

- 1) how much do you need to improve the height tolerance to achieve working and connected bonds;
- 2) are there other components that impact the height mismatch that are easier to target;
- 3) what components do not need a process modification based on statistical evidence.

Statistical analysis gives sensitivity when scaling technology and how much it needs to be improved. Overall, applying trusted statistical analysis techniques to parallel-plate MCPMs to answer the previous questions provides a framework and new insights into known scalability and manufacturing problems that future packaging engineers can leverage to improve the module design process.

## VIII. CONCLUSION

The parallel-plate module has become paramount in future power module packaging designs. As the number of die and post interconnects increases in the module, the fabrication becomes more challenging as the assembly complexities grow. This results in low yield or derated modules. Tolerance analyses commonly address low-yield challenges from assembling many parts with varying tolerances. A Monte Carlo simulation was constructed by measuring the variation of each

part used to fabricate the MCPM, then randomly sampling each component to build an MCPM 10 000 times to create a distribution.

The statistical tolerance analysis answered critical questions for the fabrication of parallel-plate MCPMs: 1) what about the fabrication of these MCPMs results in low yield, 2) what parts in the assembly contribute the most to the height mismatch across an MCPM, and 3) how much that height tolerance needs to improve to fabricate functional modules. From analyzing the CDF of the MCPM compared to a two-die module and a single die, the maximum mismatch is much higher, given the accrued variation of parts. The ANOVA and Tukey's analysis identified potential solutions: reduce the variation between hand-dipped sinter bonds and the posts.

The post height variation was reduced to less than 15  $\mu\text{m}$ , and three MCPMs were successfully fabricated with every post and device successfully connected and the bonds less than 10  $\text{m}\Omega$ , indicating that the maximum height mismatch had been reduced and every device was deemed operable. This is the first successful electrical characterization of this module type, and its success is due to the statistical analysis provided by the Monte Carlo, ANOVA, and Tukey's HSD by identifying components that had the most control in reducing the mismatch. This analysis can scale beyond this module to analyze the tolerance impacts of other parallel-plate modules with similar structures.

While fixing the post heights reduced the maximum height mismatch, the statistical tolerance analysis indicated that the hand-dipped sinter bonds introduced the most variation. Future work can include analyzing stamp-transferred, pressure-assisted sintering of Ag preform. A distribution can be created of the more controlled bonding method, and the impact on the maximum height mismatch can be analyzed. This analysis can be used and easily scaled for other modules using this parallel-plate structure to address the manufacturing and yield concerns and inform packaging techniques and processes beyond this particular module structure.

## REFERENCES

- [1] C. D. Fuentes, S. Kouro, and S. Bernet, "Comparison of 1700-V SiC-MOSFET and Si-IGBT modules under identical test setup conditions," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7765–7775, Nov./Dec. 2019, doi: [10.1109/TIA.2019.2934713](https://doi.org/10.1109/TIA.2019.2934713).
- [2] R. A. Wood and T. E. Salem, "Application study of the benefits for using silicon-carbide versus silicon in power modules," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 2499–2505, doi: [10.1109/APEC.2012.6166173](https://doi.org/10.1109/APEC.2012.6166173).
- [3] A. Vicenzutti, D. Bosich, G. Giadrossi, and G. Sulligoi, "The role of voltage controls in modern all-electric ships: Toward the all electric ship," *IEEE Electr. Mag.*, vol. 3, no. 2, pp. 49–65, Jun. 2015, doi: [10.1109/MELE.2015.2413437](https://doi.org/10.1109/MELE.2015.2413437).
- [4] L. C. G. Freitas, M. G. Simoes, and P. P. Praça, "Power electronics converters for on-board electric power systems," *Energies*, vol. 16, no. 9, Jan. 2023, Art. no. 3771, doi: [10.3390/en16093771](https://doi.org/10.3390/en16093771).
- [5] E. Bouchetob, B. Nadji, and I. Mahdi, "Efficiency comparison of silicon and silicon carbide MOSFETs in a PV system application," in *Proc. Int. Conf. Adv. Electron., Control Commun. Syst.*, Mar. 2023, pp. 1–6, doi: [10.1109/ICAEECS56710.2023.10104789](https://doi.org/10.1109/ICAEECS56710.2023.10104789).
- [6] I. Kortazar, I. Larrababal, and P. Friedrichs, "Analysis of hybrid modules with silicon carbide diodes, comparison with full silicon devices and the impact in wind applications," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Sep. 2016, pp. 1–9, doi: [10.1109/EPE.2016.7695491](https://doi.org/10.1109/EPE.2016.7695491).
- [7] X. Ding, F. Chen, M. Du, H. Guo, and S. Ren, "Effects of silicon carbide MOSFETs on the efficiency and power quality of a microgrid-connected inverter," *Appl. Energy*, vol. 201, pp. 270–283, Sep. 2017, doi: [10.1016/j.apenergy.2016.10.011](https://doi.org/10.1016/j.apenergy.2016.10.011).
- [8] S. M. S. H. Rafin, R. Ahmed, and O. A. Mohammed, "Wide band gap semiconductor devices for power electronic converters," in *Proc. 4th Int. Symp. 3-D Power Electron. Integration Manuf.*, Feb. 2023, pp. 1–8, doi: [10.1109/3D-PEIM55914.2023.10052586](https://doi.org/10.1109/3D-PEIM55914.2023.10052586).
- [9] S. Seal and H. A. Mantooh, "High performance silicon carbide power packaging—Past trends, present practices, and future directions," *Energies*, vol. 10, no. 3, Mar. 2017, Art. no. 341, doi: [10.3390/en10030341](https://doi.org/10.3390/en10030341).
- [10] B. Passmore et al., "The next generation of high voltage (10 kV) silicon carbide power modules," in *Proc. IEEE 4th Workshop Wide Bandgap Electron. Devices Appl.*, Nov. 2016, pp. 1–4, doi: [10.1109/WIPDA.2016.7799900](https://doi.org/10.1109/WIPDA.2016.7799900).
- [11] M. K. Das et al., "10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 2689–2692, doi: [10.1109/ECCE.2011.6064129](https://doi.org/10.1109/ECCE.2011.6064129).
- [12] R. Wu, L. Smirnova, H. Wang, F. Iannuzzo, and F. Blaabjerg, "Comprehensive investigation on current imbalance among parallel chips inside MW-scale IGBT power modules," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, Jun. 2015, pp. 850–856, doi: [10.1109/ICPE.2015.7167881](https://doi.org/10.1109/ICPE.2015.7167881).
- [13] C. DiMarino et al., "Design of a novel, high-density, high-speed 10 kV SiC MOSFET module," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2017, pp. 4003–4010, doi: [10.1109/ECCE.2017.8096699](https://doi.org/10.1109/ECCE.2017.8096699).
- [14] D. Lester, M. Cairnie, and C. DiMarino, "Fabrication refinements and evaluation of a wirebond-less multi-chip power module with 13 kV SiC devices," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, May 2023, pp. 1–8, doi: [10.30420/566091072](https://doi.org/10.30420/566091072).
- [15] L. Wang, W. Wang, R. J. E. Huetting, G. Rietveld, and J. A. Ferreira, "Review of topside interconnections for wide bandgap power semiconductor packaging," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 472–490, Jan. 2023, doi: [10.1109/TPEL.2022.3200469](https://doi.org/10.1109/TPEL.2022.3200469).
- [16] M. Cairnie and C. DiMarino, "10 kV SiC MOSFET power module with double-sided jet-impingement cooling," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2023, pp. 336–343, doi: [10.1109/APEC43580.2023.10131433](https://doi.org/10.1109/APEC43580.2023.10131433).
- [17] Z. Zhang et al., "Packaging of a 10-kV double-side cooled silicon carbide diode module with thin substrates coated by a nonlinear resistive polymer-nanoparticle composite," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14462–14470, Dec. 2022, doi: [10.1109/TPEL.2022.3190303](https://doi.org/10.1109/TPEL.2022.3190303).
- [18] L. Gao et al., "Nano-silver pressureless sintering technology in power module packaging," in *Proc. IEEE Int. Conf. Mechatronics Automat.*, Aug. 2022, pp. 1452–1456, doi: [10.1109/ICMA54519.2022.9856054](https://doi.org/10.1109/ICMA54519.2022.9856054).
- [19] X. Zhao et al., "Flexible epoxy-resin substrate based 1.2 kV SiC half bridge module with ultra-low parasitics and high functionality," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2017, pp. 4011–4018, doi: [10.1109/ECCE.2017.8096700](https://doi.org/10.1109/ECCE.2017.8096700).
- [20] C. Ding, H. Liu, K. D. T. Ngo, R. Burgos, and G.-Q. Lu, "A double-side cooled SiC MOSFET power module with sintered-silver interposers: I-design, simulation, fabrication, and performance characterization," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11672–11680, Oct. 2021, doi: [10.1109/TPEL.2021.3070326](https://doi.org/10.1109/TPEL.2021.3070326).
- [21] X. Liu, Z. Wu, Y. Yan, Y. Kang, and C. Chen, "A novel double-sided cooling inverter leg for high power density EV based on customized SiC power module," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2020, pp. 3151–3154, doi: [10.1109/ECCE44975.2020.9235332](https://doi.org/10.1109/ECCE44975.2020.9235332).
- [22] Z. Liang, P. Ning, F. Wang, and L. Marlino, "A phase-leg power module packaged with optimized planar interconnections and integrated double-sided cooling," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 443–450, Sep. 2014, doi: [10.1109/JESTPE.2014.2312292](https://doi.org/10.1109/JESTPE.2014.2312292).
- [23] M. Wang et al., "Reliability improvement of a double-sided IGBT module by lowering stress gradient using molybdenum buffers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1637–1648, Sep. 2019, doi: [10.1109/JESTPE.2019.2920254](https://doi.org/10.1109/JESTPE.2019.2920254).
- [24] J. Knoll, J. Miranda-Santos, X. Chen, C. DiMarino, and Q. Li, "1.2 kV SiC MOSFET full-bridge power module with integrated gate driver and coupled inductor," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2022, pp. 1–7, doi: [10.1109/ECCE50734.2022.9947473](https://doi.org/10.1109/ECCE50734.2022.9947473).
- [25] "Review of packaging schemes for power module | IEEE Journals & Magazine | IEEE Xplore." Accessed: Jun. 5, 2024. [Online]. Available: [https://ieeexplore-ieee-org.ezproxy.lib.vt.edu/abstract/document/8869891?casa\\_token=1208T5chQvoAAAAA:c5kdGagkML28QixLd2g9zXNwZe79QS52nSeYGEvjlrUWw05VVMSw9HHVKRPuCEBtuctPmzg](https://ieeexplore-ieee-org.ezproxy.lib.vt.edu/abstract/document/8869891?casa_token=1208T5chQvoAAAAA:c5kdGagkML28QixLd2g9zXNwZe79QS52nSeYGEvjlrUWw05VVMSw9HHVKRPuCEBtuctPmzg)

- [26] Z. Zhang et al., "Package design and analysis of a 20-kV double-sided silicon carbide diode module with polymer nanocomposite field-grading coating," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 14, no. 5, pp. 776–783, May 2024, doi: [10.1109/TCPMT.2024.3381090](https://doi.org/10.1109/TCPMT.2024.3381090).
- [27] M. Cairnie, J. Gersh, and C. DiMarino, "Thermal and thermomechanical analysis of a 10 kV SiC MOSFET package with double-sided cooling," in *Proc. IEEE 8th Workshop Wide Bandgap Power Devices Appl.*, Nov. 2021, pp. 394–399, doi: [10.1109/WIPDA49284.2021.9645075](https://doi.org/10.1109/WIPDA49284.2021.9645075).
- [28] C.-K. Liu et al., "Double-sided cooling SiC power module packaging for industrial motor driving system," in *Proc. 15th Int. Microsystems, Packag., Assem. Circuits Technol. Conf.*, Oct. 2020, pp. 105–108, doi: [10.1109/IM-PACT50485.2020.9268577](https://doi.org/10.1109/IM-PACT50485.2020.9268577).
- [29] B. P. Singh, S. S. Ghahfarokhi, K. Kostov, H.-P. Nee, and S. Norrga, "Analysis of the thermo-mechanical performance of double-sided cooled power modules," in *Proc. 25th Int. Conf. Thermal, Mech. Multi-Phys. Simul. Experiments Microelectronics Microsystems*, Apr. 2024, pp. 1–8, doi: [10.1109/EuroSimE60745.2024.10491556](https://doi.org/10.1109/EuroSimE60745.2024.10491556).
- [30] "A double-sided cooled power module with embedded decoupling capacitors | IEEE Journals & Magazine | IEEE Xplore." Accessed: Jun. 5, 2024. [Online]. Available: <https://ieeexplore-ieee-org.ezproxy.lib.vt.edu/document/10378702>
- [31] K. Weidner, M. Kaspar, and N. Seliger, "Planar interconnect technology for power module system integration," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2012, pp. 1–5.
- [32] S. Kicin et al., "Low-voltage AC drive based on double-sided cooled IGBT press-pack modules," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2140–2146, Nov./Dec. 2012, doi: [10.1109/TIA.2012.2226552](https://doi.org/10.1109/TIA.2012.2226552).
- [33] "Automotive 750 V, 800 A dual side cooling half-bridge power module," ON Semiconductor, 2019. [Online]. Available: <https://www.onsemi.com/products/power-modules/igbt-modules/nvg800a7514dsc>
- [34] A. Grassmann et al., "Double sided cooled module concept for high power density in HEV applications," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, May 2015, pp. 1–7.
- [35] M. Anwar, S. M. N. Hasan, M. Teimor, M. Korich, and M. B. Hayes, "Development of a power dense and environmentally robust traction power inverter for the second-generatio chevrolet VOLT extended-range EV," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 6006–6013, doi: [10.1109/ECCE.2015.7310502](https://doi.org/10.1109/ECCE.2015.7310502).
- [36] N. Rajagopal, C. DiMarino, R. Burgos, I. Cvetkovic, and M. Shawky, "Design of a high-density integrated power electronics building block (iPEBB) based on 1.7 kV SiC MOSFETs on a common substrate," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Jun. 2021, pp. 1–8, doi: [10.1109/APEC42165.2021.9487167](https://doi.org/10.1109/APEC42165.2021.9487167).
- [37] T. Yin, L. Lin, C. Xu, D. Zhu, and K. Jing, "A hybrid modular multilevel converter comprising SiC MOSFET and Si IGBT with its specialized modulation and voltage balancing scheme," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11272–11282, Nov. 2022, doi: [10.1109/TIE.2021.3118372](https://doi.org/10.1109/TIE.2021.3118372).
- [38] S. Moevic et al., "Power cell design and assessment methodology based on a high-current 10-kV SiC MOSFET half-bridge module," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 3916–3935, Aug. 2021, doi: [10.1109/JESTPE.2020.2995386](https://doi.org/10.1109/JESTPE.2020.2995386).
- [39] B. Mouawad, C. Di Marino, J. Li, R. Skuriat, and M. Johnson, "Packaging technology for a highly integrated 10kV SiC MOSFET module." Aug. 2018. Accessed: Apr. 18, 2023. [Online]. Available: <https://nottingham-repository.worktribe.com/index.php/output/1062739/packaging-technology-for-a-highly-integrated-10kv-sic-mosfet-module>
- [40] T. Anzai et al., "Warpage evaluation of high-temperature sandwich-structured power module for SiC power semiconductor devices," *J. Microelectronics Electron. Packag.*, vol. 12, no. 3, pp. 153–160, Jul. 2015, doi: [10.4071/imaps.464](https://doi.org/10.4071/imaps.464).
- [41] R. Simpson, A. Plumpton, M. Varley, C. Tonner, P. Taylor, and X. Dai, "Press-pack IGBTs for HVDC and FACTS," *CSEE J. Power Energy Syst.*, vol. 3, no. 3, pp. 302–310, Sep. 2017, doi: [10.17775/CSEEJPES.2016.01740](https://doi.org/10.17775/CSEEJPES.2016.01740).
- [42] E. Deng, Z. Zhao, Q. Xin, J. Zhang, and Y. Huang, "Analysis on the difference of the characteristic between high power IGBT modules and press pack IGBTs," *Microelectronics Rel.*, vol. 78, pp. 25–37, Nov. 2017, doi: [10.1016/j.microrel.2017.07.095](https://doi.org/10.1016/j.microrel.2017.07.095).
- [43] A. Mantooth, "Silicon carbide power modules for medium voltage applications task #BP6-power America module challenge," presented at the PowerAmerica, North Carolina State University, Aug. 3, 2022.
- [44] J. Bruyère, J.-Y. Dantan, R. Bigot, and P. Martin, "Statistical tolerance analysis of bevel gear by tooth contact analysis and Monte Carlo simulation," *Mechanism Mach. Theory*, vol. 42, no. 10, pp. 1326–1351, Oct. 2007, doi: [10.1016/j.mechmachtheory.2006.11.003](https://doi.org/10.1016/j.mechmachtheory.2006.11.003).
- [45] A. Buchholz and M. Seidel, "Gap height prediction for bolted ring flange connections based on measurements," *Steel Construction*, vol. 16, no. 2, pp. 114–126, May 2023, doi: [10.1002/stco.202200019](https://doi.org/10.1002/stco.202200019).
- [46] M. Merrett et al., "Modelling circuit performance variations due to statistical variability: Monte Carlo static timing analysis," in *Proc. Des., Automat. Test Europe*, Mar. 2011, pp. 1–4, doi: [10.1109/DATE.2011.5763329](https://doi.org/10.1109/DATE.2011.5763329).
- [47] N. Chhabria, A. Jaiprakash, K. R. Motwani, and R. Srinivasan, "RLC circuit simulation and Monte Carlo analysis in MATLAB," in *Proc. Int. Conf. Commun. Electron. Syst.*, Oct. 2016, pp. 1–6, doi: [10.1109/CESYS.2016.7889890](https://doi.org/10.1109/CESYS.2016.7889890).
- [48] J. Gajda and T. Sidor, "Using Monte Carlo analysis for practical investigation of sensitivity of electronic converters in respect to component tolerances," *Elect. Eng.*, vol. 2, pp. 297–302, May 2012, doi: [10.5923/j.eee.20120205.09](https://doi.org/10.5923/j.eee.20120205.09).
- [49] Z. Shen, G. Ameta, J. J. Shah, and J. K. Davidson, "A comparative study of tolerance analysis methods," *J. Comput. Inf. Sci. Eng.*, vol. 5, no. 3, pp. 247–256, May 2005, doi: [10.1115/1.1979509](https://doi.org/10.1115/1.1979509).
- [50] J. S. Talledo, P. A. Cabading Jr, and R. A. Real, "Automotive package lead pullback elimination using Monte Carlo analysis for determining leadframe and blade design," *J. Eng. Res. Rep.*, vol. 20, no. 3, pp. 97–107, 2021.
- [51] T. S. Tong, J. Kumar, and M. M. D. Kanan, "A study and investigation on processes inducing delamination in QFN package using statistical analysis," in *Proc. 31st IEEE/CPMT Int. Electron. Manuf. Technol. Symp.*, Nov. 2006, pp. 381–389, doi: [10.1109/IEMT.2006.4456483](https://doi.org/10.1109/IEMT.2006.4456483).
- [52] J. Guilford, M. Sethi, and J. Turner, "Worst case and statistical tolerance analysis of the daughter card assembly," in *Proc. Int. Comput. Eng. Conf. Expo., Amer. Soc. Mech. Engineers Digit. Collection*, Mar. 2021, pp. 343–350, doi: [10.1115/CIE1992-0042](https://doi.org/10.1115/CIE1992-0042).
- [53] M. Drienovsky, A. Davidescu, and D. Rozputniak, "Tolerance analysis of an over-constrained assembly with press-fit solderless electric contact pins," in *New Advances in Mechanisms, Mechanical Transmissions and Robotics*, E.-C. Lovasz, I. Maniu, I. Doroftei, M. Ivanescu, and C.-M. Gruescu, Eds., in *Mechanisms and Machine Science*. Berlin, Germany: Springer, 2021, pp. 324–337, doi: [10.1007/978-3-030-60076-1\\_29](https://doi.org/10.1007/978-3-030-60076-1_29).
- [54] C. C. Tee and S. Soh, "Innovative solutions for package on package test," in *Proc. 5th Asia Symp. Qual. Electron. Des.*, Aug. 2013, pp. 161–166, doi: [10.1109/ASQED.2013.6643580](https://doi.org/10.1109/ASQED.2013.6643580).
- [55] C. W. Han, S. C. Sung, and K. M. Choi, "Statistical analysis of the thermal performance and reliability in the heat sink with heat pipes for the power electronics module," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 12, no. 1, pp. 59–68, Jan. 2022, doi: [10.1109/TCPMT.2021.3129212](https://doi.org/10.1109/TCPMT.2021.3129212).
- [56] M. Novak, A. Sangwongwanich, and F. Blaabjerg, "Monte Carlo-based reliability estimation methods for power devices in power electronics systems," *IEEE Open J. Power Electron.*, vol. 2, pp. 523–534, Sep. 2021, doi: [10.1109/OJPEL.2021.3116070](https://doi.org/10.1109/OJPEL.2021.3116070).
- [57] B. Hu et al., "Failure and reliability analysis of a SiC power module based on stress comparison to a Si device," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 4, pp. 727–737, Dec. 2017, doi: [10.1109/TDMR.2017.2766692](https://doi.org/10.1109/TDMR.2017.2766692).
- [58] A. Borghese et al., "Statistical analysis of the electrothermal imbalances of mismatched parallel SiC power MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1527–1538, Sep. 2019, doi: [10.1109/JESTPE.2019.2924735](https://doi.org/10.1109/JESTPE.2019.2924735).
- [59] X. Huang, J. Hu, Y. Ge, L. Guo, K. Han, and J. Zhang, "Automatic optimization system for heat source layout of multi-chip components based on multi-software integration," *Appl. Sci.*, vol. 14, no. 11, Jan. 2024, Art. no. 4577, doi: [10.3390/app14114577](https://doi.org/10.3390/app14114577).
- [60] F. Bennis, P. Castagliola, and L. Pino, "Statistical analysis of geometrical tolerances: A case study," *Qual. Eng.*, vol. 17, no. 3, pp. 419–427, Jul. 2005, doi: [10.1081/QEN-200059875](https://doi.org/10.1081/QEN-200059875).
- [61] H. Peng and Z. Peng, "A practical method for redesigning statistical tolerances using Monte Carlo simulation," in *Proc 9th Int. Conf. Mech. Aerosp. Eng.*, Jul. 2018, pp. 213–218, doi: [10.1109/ICMAE.2018.8467654](https://doi.org/10.1109/ICMAE.2018.8467654).
- [62] Y. S. Hong and T. C. Chang, "A comprehensive review of tolerancing research," *Int. J. Prod. Res.*, vol. 40, no. 11, pp. 2425–2459, Jan. 2002, doi: [10.1080/00207540210128242](https://doi.org/10.1080/00207540210128242).
- [63] A. K. Sahani, P. K. Jain, S. C. Sharma, and J. K. Bajpai, "Design verification through tolerance stack up analysis of mechanical assembly and least cost tolerance allocation," *Procedia Mater. Sci.*, vol. 6, pp. 284–295, Jan. 2014, doi: [10.1016/j.mspro.2014.07.036](https://doi.org/10.1016/j.mspro.2014.07.036).

- [64] Y.-T. Tsai, K.-H. Lin, and C.-S. Chen, "A study of tolerance allocation and stack-up analysis to improve the assembly precision of an injection mold," *J. Chin. Inst. Eng.*, vol. 46, no. 5, pp. 479–489, Jul. 2023, doi: [10.1080/02533839.2023.2204883](https://doi.org/10.1080/02533839.2023.2204883).
- [65] D. C. Montgomery and G. C. Runger, *Applied Statistics and Probability for Engineers*. Hoboken, NJ, USA: Wiley, 2010.
- [66] D. Shringi and K. Purohit, "Analysis of new non traditional tolerance stack up conditions," *Int. J. Eng. Res. Appl.*, vol. 3, pp. 1419–1424, 2013.
- [67] R. Y. Rubinstein and D. P. Kroese, *Simulation and the Monte Carlo Method*. Hoboken, NJ, USA: Wiley, 2016.
- [68] F. James, "Monte Carlo theory and practice," *Rep. Prog. Phys.*, vol. 43, no. 9, Sep. 1980, Art. no. 1145, doi: [10.1088/0034-4885/43/9/002](https://doi.org/10.1088/0034-4885/43/9/002).
- [69] G. Q. Chen and J. W. Zhao, "Application and implementation of Monte Carlo method in mechanical engineering," *Appl. Mech. Mater.*, vol. 26–28, pp. 925–930, 2010, doi: [10.4028/www.scientific.net/AMM.26-28.925](https://doi.org/10.4028/www.scientific.net/AMM.26-28.925).
- [70] H. Yan, X. Wu, and J. Yang, "Application of Monte Carlo method in tolerance analysis," *Procedia CIRP*, vol. 27, pp. 281–285, Jan. 2015, doi: [10.1016/j.procir.2015.04.079](https://doi.org/10.1016/j.procir.2015.04.079).
- [71] A. AlBahar, I. Kim, and X. Yue, "A robust asymmetric kernel function for bayesian optimization, with application to image defect detection in manufacturing systems," *IEEE Trans. Automat. Sci. Eng.*, vol. 19, no. 4, pp. 3222–3233, Oct. 2022, doi: [10.1109/TASE.2021.3114157](https://doi.org/10.1109/TASE.2021.3114157).
- [72] E. Goka, P. Beaurepaire, L. Homri, and J.-Y. Dantan, "Probabilistic-based approach using Kernel Density Estimation for gap modeling in a statistical tolerance analysis," *Mech. Mach. Theory*, vol. 139, pp. 294–309, Sep. 2019, doi: [10.1016/j.mechmachtheory.2019.04.020](https://doi.org/10.1016/j.mechmachtheory.2019.04.020).
- [73] M. Smithson, *Confidence Intervals*. Newbury Park, CA, USA: Sage, 2003.
- [74] "Confidence interval estimation of apparent residential load with PV system based on just-in-time modeling | IEEE conference publication | IEEE Xplore." Accessed: Jun. 4, 2024. [Online]. Available: <https://ieeexplore.ieee.org.ezproxy.lib.vt.edu/document/8980670>
- [75] N. Yan, H. Zhao, X. Pan, G. Ma, and S. Ma, "Study on the cluster selection method of echelon utilization power battery based on confidence interval estimation," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 8, Nov. 2021, Art. no. 9000804, doi: [10.1109/TASC.2021.3107831](https://doi.org/10.1109/TASC.2021.3107831).
- [76] H. Wang and F. Blaabjerg, "Power electronics reliability: State of the art and outlook," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 6476–6493, Dec. 2021, doi: [10.1109/JESTPE.2020.3037161](https://doi.org/10.1109/JESTPE.2020.3037161).
- [77] F. Blaabjerg, H. Wang, I. Vernica, B. Liu, and P. Davari, "Reliability of power electronic systems for EV/HEV applications," *Proc. IEEE*, vol. 109, no. 6, pp. 1060–1076, Jun. 2021, doi: [10.1109/JPROC.2020.3031041](https://doi.org/10.1109/JPROC.2020.3031041).
- [78] B. Ramos Barbero, J. Pérez Azcona, and J. González Pérez, "A tolerance analysis and optimization methodology. The combined use of 3D CAT, a dimensional hierarchization matrix and an optimization algorithm," *Int. J. Adv. Manuf. Technol.*, vol. 81, no. 1, pp. 371–385, Oct. 2015, doi: [10.1007/s00170-015-7068-4](https://doi.org/10.1007/s00170-015-7068-4).
- [79] J. W. Tukey, "The philosophy of multiple comparisons," *Stat. Sci.*, vol. 6, no. 1, pp. 100–116, 1991.
- [80] J. Gersh, C. DiMarino, D. DeVoto, P. Paret, J. Major, and S. Gage, "Evaluation of low-pressure-sintered multi-layer substrates for medium-voltage SiC power modules," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Jun. 2021, pp. 20–26, doi: [10.1109/APEC42165.2021.9487244](https://doi.org/10.1109/APEC42165.2021.9487244).



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