Miniaturized Current Shunt With High Bandwidth and Low Parasitics for High-Integrated Applications: Electro-Thermal Considerations and Co-Design

Yulei Wang, *Student Member, IEEE*, Jiakun Gong, Mingrui Zou, Liang Wang, Yiming Gong, Chaoqiang Jiang, *Senior Member, IEEE*, and Zheng Zeng, *Member, IEEE*

***Abstract*—The development of current sensors for wide-bandgap (WBG) applications consistently emphasizes high bandwidth, minimal invasiveness, and integration. Despite the meticulous design that enables current shunts to achieve excellent performance with high bandwidth and low parasitics, their inherent bulkiness remains a significant challenge for their integration into high-integrated applications that depend on the high switching speeds of WBG power devices. This study thoroughly investigates and uncovers the tradeoff faced by traditional current shunts in balancing miniaturization and high bandwidth. Building upon this understanding, the miniaturized current shunt (MiniShunt) concept is introduced to overcome inherent limitations and achieve both high performance and compact size. To realize this concept, a physical implementation that involves the high-density stacking of multiple coupled transmission lines is presented. Additionally, a thermal network model specifically for the proposed MiniShunt configuration is developed and a comprehensive thermal analysis methodology for the current shunts is established. By applying this methodology to finite element analysis, the thermal safe operating area for the MiniShunt can be determined, further providing valuable insights into its maximum static power dissipation and maximum energy loss. These findings contribute to the development of a highly compact 9 × 9-mm, 100-mΩ current shunt with an ultrahigh bandwidth of 3 GHz, near-zero parasitic inductance, and a maximum energy loss of 2.0 J at a reference temperature rise limit of 20 °C. Extensive experiments conducted in both the frequency and time domains serve to further validate the advantages of the MiniShunt in terms of its miniaturization, integration, ultrafast response, and low invasiveness for future high-integrated power electronics applications.**

***Index Terms*—Current sensor, high bandwidth, integration, impedance matching, miniaturization, safe operating area (SOA), thermal analysis, wide-bandgap (WBG) device.**

I. Introduction

DYNAMIC testing plays a vital role in the effective application of power semiconductor devices in diverse scenarios [1], [2]. It serves as a fundamental foundation for parasitic evaluation, loss estimation, thermal design, and lifetime assessment in advanced packaging development and power converter design [3], [4].

With the transition of power semiconductor devices from silicon to wide-bandgap (WBG) materials, packaging strategies are continuously evolving to achieve reduced sizes and lower inductance [5]. This evolution has led to an increased demand for current sensing technologies that offer higher bandwidth, lower invasiveness, and smaller form factors, in line with the advancements in next-generation packaging technologies, cf. Fig. 1. Additionally, to meet the requirements of future high-density power converter designs driven by the fast switching speeds of WBG devices [6], the development of current sensors also focuses on achieving high performance and integration [7].

In terms of performance, the rapid switching speeds of WBG power devices are approaching the theoretical limits of current sensors, as illustrated in Fig. 2. Therefore, to accurately capture the switching transients, the measurement bandwidth of sensors for silicon carbide metal-oxide-semiconductor field-effect transistors should exceed 100 MHz, while for gallium nitride (GaN) high-electron-mobility transistors (HEMTs), it should surpass 500 MHz [8].

Among various current sensors, the current transformer can achieve a bandwidth up to 250 MHz. Nonetheless, its large and bulky size imposes significant limitations on its utilization in WBG measurements. Commercial Rogowski coil (RC) has a maximum bandwidth of 50 MHz, and the system bandwidth can be further improved by reducing the number of winding turns [9] or implementing the postcharacteristic compensation [10], [11]. Furthermore, transmission line RC has emerged as a novel concept, successfully demonstrating its potential for achieving an ultrahigh bandwidth that exceeds 3 GHz [12]. However,

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Yulei Wang is with the State Key Laboratory of Power Transmission Equipment Technology, School of Electrical Engineering, Chongqing University, Chongqing 400044, China, and also with the McMaster Automotive Resource Centre, McMaster University, Hamilton, ON L8P 0A6, Canada (e-mail: yulei_wang@cqu.edu.cn).

Jiakun Gong, Mingrui Zou, Liang Wang, Yiming Gong, and Zheng Zeng are with the State Key Laboratory of Power Transmission Equipment Technology, School of Electrical Engineering, Chongqing University, Chongqing 400044, China (e-mail: gonjiakun@cqu.edu.cn; zoumingrui@cqu.edu.cn; wangliang-edu@cqu.edu.cn; gongyiming@cqu.edu.cn; zengerzheng@cqu.edu.cn).

Chaoqiang Jiang is with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong (e-mail: chjiang@cityu.edu.hk).

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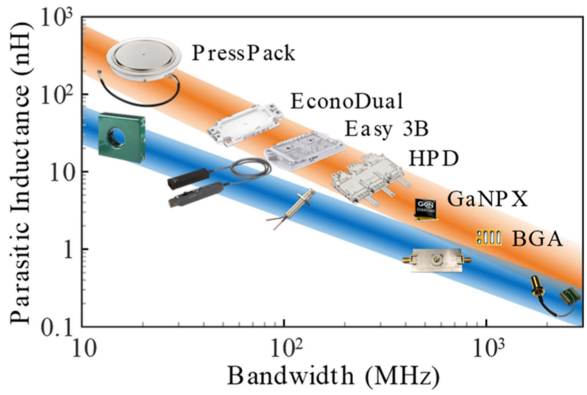

Fig. 1. Development trend of packaging scheme and current sensing technology for power semiconductor device.

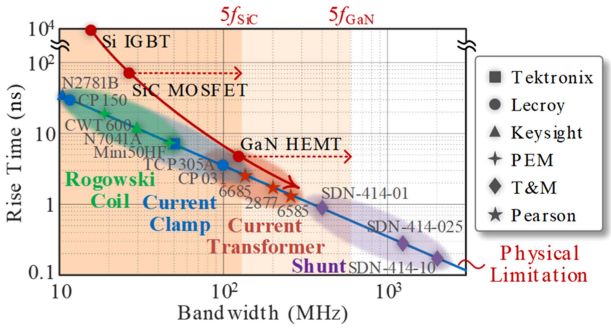

Fig. 2. State of the art of commercial current sensors for WBG power devices.

in addition to the fundamental bandwidth performance, the comprehensive performance design of the RC is gaining more attention due to concerns regarding its inability to measure direct current and its susceptibility to interference in certain scenarios. Therefore, it is essential to design and optimize the RC in a targeted manner, considering the specific requirements of different application scenarios. Striking a suitable tradeoff between bandwidth, interference resistance, low drift, and minimal droop error is of utmost importance. For instance, addressing issues such as transient common-mode interference caused by ultrahigh dv/dt exhibited by WBG devices [13], minimizing droop distortion arising from the limited low-frequency measurement capability of the RC [14], [15], and mitigating dc operating point drift resulting from the absence of dc measurement capability in the RC, which can further lead to continuous charging of subsequent integrating capacitors and larger drift errors [16].

In contrast, the current shunt presents an attractive option for the dynamic current testing in further WBG applications, such as medium voltage [13], [17], and ultrahigh speed [8], [18], [20]. This is primarily due to its inherent dc measurement capability, coupled with its ultrahigh bandwidth potential and robust anti-interference capability. The commercial coaxial shunts from T&M are widely employed for the characterization of switching currents. However, extensive field measurements have revealed substantial performance degradation in these shunts, displaying significant deviations from their intended nominal values [8], [19], [20], [21], [22]. As a response, an advanced surface mount device (SMD) based coaxial shunt configuration is proposed and verified to have the potential for GHz bandwidth [18], [23]. Additionally, the incorporation of a multicurrent loop and active compensation network further enhances the bandwidth of the current shunt, extending it into the GHz range [20]. Nevertheless, the approaches mentioned above for extending bandwidth and reducing inductance have predominantly relied on experiences, trial and error, or compensation, lacking a precise and quantitative design methodology. To address this issue, Wang et al. [8] provided further insights, revealing that a current shunt is always accompanied by a typical transmission line configuration, and the theoretical upper limit of its performance is solely reliant on the fulfillment of the impedance matching condition. Consequently, the impedance matching shunt (IM-Shunt) has emerged as a highly promising solution for the dynamic testing of the WBG device, showcasing exceptional performance capabilities with a bandwidth exceeding 3 GHz and a minimal parasitic inductance below 0.1 nH. However, achieving the impedance matching design criteria requires a tradeoff that involves sacrificing the overall size of the IM-Shunt, which poses a significant limitation to its integration into various power electronics applications.

In terms of integration, the mutual inductance-based RC has gained widespread use as an integrated solution, particularly for integrated current monitoring and ultrafast protection in WBG applications [13], [24]. Moreover, several sensors incorporating current monitoring cells that are directly integrated with the die chip have been developed, utilizing hybrid sensing principles such as the combination of Hall sensor and RC [25], [26], [27]. However, these sensors typically have a maximum bandwidth ranging from a few to tens of MHz, which is considerably lower than the requirements for the dynamic current characterization of the WBG device.

The analysis presented above reveals that high-performance current shunts are typically bulky, whereas easily integrated current sensing methods often lack the sufficient bandwidth. To meet the requirements of integrated high-performance dynamic current characterization for advanced packaging developments and next-generation highly-compact power converter designs, there still remains an unresolved challenge for a comprehensive, quantified, and accurate design methodology for miniaturized high-performance current shunts.

Aiming to fulfill these research gaps, a novel concept known as miniaturized current shunt (MiniShunt) is introduced as a solution to overcome the inherent bulkiness typically associated with conventional IM-Shunts.

The rest of this article is organized as follows. Section II delves into the design criteria of IM-Shunts, shedding light on the tradeoff between compact size and high bandwidth. Drawing upon this understanding, the MiniShunt concept is introduced as a solution to overcome this tradeoff, accompanied by a physical implementation that aims to push the boundaries of performance design. Furthermore, a comprehensive thermal analysis methodology is established to empower the practical applications of current shunts, offering valuable insights into critical parameters such as maximum static power dissipation, safe operating region, and maximum energy loss. In Section III,

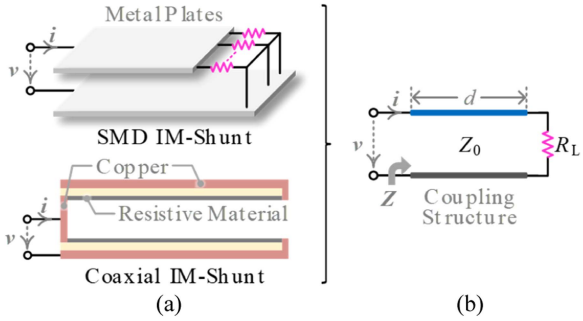

Fig. 3. IM-Shunts [8]. (a) Typical physical configuration of SMD and coaxial IM-Shunts. (b) Equivalent transmission line model.

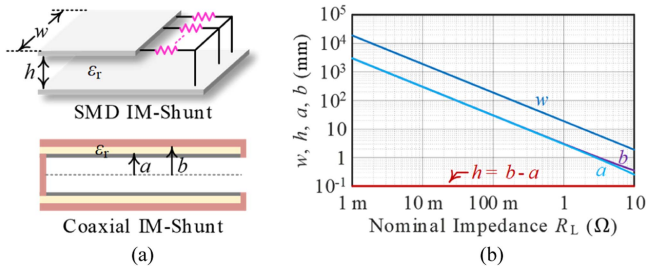

Fig. 4. Tradeoff between nominal impedance R_L and physical dimensions of IM-Shunts on the premise of impedance matching-oriented ultrahigh bandwidth. (a) Physical structure of IM-Shunts. (b) Effect of R_L on physical dimensions of IM-Shunts under insulating substrate thickness (h and $b-a$) of 0.1 mm.

extensive experimental validation in both the frequency and time domains confirms the exceptional performance of the developed MiniShunt. Finally, Section IV concludes this article.

II. Model and Design of Miniaturized Current Shunt for High-Integrated Power Electronics: Electrical and Thermal Perspectives

A. Typical Configuration and Design Difficulty of IM-Shunt

Fig. 3(a) illustrates two primary types of IM-Shunts, i.e., SMD and coaxial IM-Shunts. Both of these types are characterized by the presence of a coupled structure and a resistive load R_L. When combined, these components collectively form a typical transmission line configuration, as depicted in Fig. 3(b).

The input impedance of IM-Shunt $\boldsymbol{Z}$ can be expressed as [28]

$$\boldsymbol{Z} = \frac{\boldsymbol{v}}{\boldsymbol{i}} = Z_0 \frac{R_L + \mathrm{j}Z_0 \tan(2\pi d/\lambda)}{Z_0 + \mathrm{j}R_L \tan(2\pi d/\lambda)} \tag{1}$$

where $\boldsymbol{i}$ and $\boldsymbol{v}$ denote the measured current flowing through the IM-Shunt and the resulting voltage signal, respectively. R_L is the resistive load, also referred to as the nominal impedance, of the IM-Shunt. Z_0 corresponds to the characteristic impedance, also known as the design impedance, of the coupled structure in the IM-Shunt, and is determined by the dimensions of the coupled structure, requiring careful calculation and design to achieve impedance matching, i.e., $Z_0 = R_L$. d and λ stand for the geometric length of the coupled structure and the wavelength of input current signals, respectively. Building upon the foundation of $Z_0 = R_L$, the geometric-electrical design criteria for SMD and coaxial IM-Shunts are derived and can be expressed as [8]

$$\underline{\text{SMD}}: \frac{h}{w} = \frac{\sqrt{\varepsilon_r}}{377} R_L, \ \underline{\text{Coaxial}}: \frac{b}{a} = \exp\left(\frac{2\pi\sqrt{\varepsilon_r}}{377} R_L\right) \tag{2}$$

where h and w represent the substrate thickness and signal trace width of the SMD IM-Shunt, respectively. a and b refer to the outer diameter of the resistive layer and the inner diameter of the copper layer of the coaxial IM-Shunt, respectively. Additionally, ε_r denotes the relative permittivity of the insulating substrate layer.

The variation of the physical dimension of the coupled structure with respect to the nominal impedance R_L is calculated utilizing (2) and plotted in Fig. 4(b). The results clearly highlight the inherent design limitation arising from the tradeoff between small size and low impedance. In other words, achieving low impedance requires sacrificing the physical space occupied. For instance, when considering a 1-Ω IM-Shunt, the SMD type just needs a trace width w of 18 mm, but this requirement soars to 180 mm for a 100-mΩ IM-Shunt. Consequently, the miniaturization of low-impedance IM-Shunts poses a significant design challenge, emphasizing the necessity to explore more advanced configurations to overcome this inherent limitation.

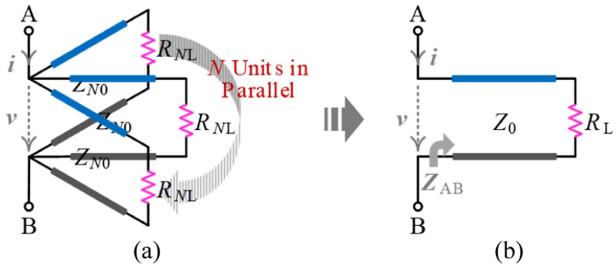

Fig. 5. Concept of MiniShunt. (a) Multiple transmission line units in parallel. (b) Equivalent single transmission line.

B. Concept Definition and Design Criteria of Proposed MiniShunt

To address the aforementioned limitation, the concept of the MiniShunt is proposed. This concept entails the arrangement of multiple coupled transmission line units in parallel within a confined space, with the goal of optimizing the space utilization while maintaining a small nominal impedance, on the premise of ensuring the impedance matching design condition.

The theoretical support of the proposed MiniShunt concept is shown in Fig. 5. Similar to (1), the input impedance of the paralleled transmission line unit $\boldsymbol{Z}_N$ in Fig. 5(a) can be written as

$$\boldsymbol{Z}_N = Z_{N0} \frac{R_{NL} + \mathrm{j}Z_{N0} \tan(2\pi d/\lambda)}{Z_{N0} + \mathrm{j}R_{NL} \tan(2\pi d/\lambda)} \tag{3}$$

where Z_{N0} and R_{NL} stand for the characteristic impedance and resistive load of the transmission line unit, respectively. N represents the number of transmission line units interconnected in parallel to construct a MiniShunt. In this context, the input

impedance of the MiniShunt, denoted as $\boldsymbol{Z}_{\mathrm{AB}}$, can be computed as

$$\begin{aligned}\boldsymbol{Z}_{\mathrm{AB}} &= \frac{1}{N}\boldsymbol{Z}_N = \frac{1}{N}Z_{N0}\frac{R_{NL}+\mathrm{j}Z_{N0}\tan(2\pi d/\lambda)}{Z_{N0}+\mathrm{j}R_{NL}\tan(2\pi d/\lambda)}\\ &= (Z_{N0}/N)\frac{(R_{NL}/N)+\mathrm{j}(Z_{N0}/N)\tan(2\pi d/\lambda)}{(Z_{N0}/N)+\mathrm{j}(R_{NL}/N)\tan(2\pi d/\lambda)}\\ &= Z_0\frac{R_{\mathrm{L}}+\mathrm{j}Z_0\tan(2\pi d/\lambda)}{Z_0+\mathrm{j}R_{\mathrm{L}}\tan(2\pi d/\lambda)} \qquad (4)\end{aligned}$$

where Z_0 and R_{L} denote the characteristic impedance and resistive load of the equivalent single transmission line depicted in Fig. 5(b), respectively, and can be mathematically expressed as

$$Z_0 = Z_{N0}/N,\ R_{\mathrm{L}} = R_{NL}/N. \qquad (5)$$

Upon examining (5), it becomes apparent that N identical transmission line units connected in parallel can be substituted by a single transmission line with a characteristic impedance and resistive load that are $1/N$ of the original values. Aligned with the design criteria of the IM-Shunt, for the equivalent single transmission line to attain impedance matching, it is necessary for each unit to adhere to the following derived design criteria:

$$\{Z_0 = R_{\mathrm{L}}\} \Rightarrow \{Z_{N0} = R_{NL}\} \Rightarrow \{Z_{N0} = NR_{\mathrm{L}}\}. \qquad (6)$$

As evident from (6), the parallel connection of the identical impedance-matching transmission lines, i.e., $Z_{N0} = R_{NL}$, ensures the continuous satisfaction of the matching condition of the equivalent single transmission line, i.e., $Z_0 = R_{\mathrm{L}}$. At this stage, the design difficulty shifts from achieving $Z_0 = R_{\mathrm{L}}$ to $Z_{N0} = NR_{\mathrm{L}}$.

In short, the key to achieving a low-impedance IM-Shunt lies in parallelizing multiple high-impedance matching structures. As the impedance of these matching structures increases, the overall size of the system decreases accordingly, cf. Fig. 4. This theoretical foundation paves the way for the development of a miniaturized current shunt that excels in high performance.

C. Physical Implementation and Laminated Design of MiniShunt

To validate the proposed MiniShunt concept, a physical implementation based on it is presented in Fig. 6, where a multilayer PCB is utilized to stack multiple coupled structures with identical controlled impedance within a restricted space.

The physical implementation of the MiniShunt can be mainly divided into two parts. Part ① represents the external interactive structure depicted in Fig. 6(a), which comprises the top and bottom layers, where the bottom layer facilitates the inflow and outflow of the measured current, and the top layer transmits the induced voltage signal to the oscilloscope. Part ② corresponds to the interior n layers consisting of $n/2$ signal-ground (S-G) coupled pairs, as shown in Fig. 6(c). This part also refers to the specific transmission line unit that demands meticulous design.

To aid in comprehension, a sectional view of the physical implementation is presented in Fig. 7(a). Additionally, for a better understanding of the operating principle of the proposed MiniShunt, a step-by-step decomposition and accompanying

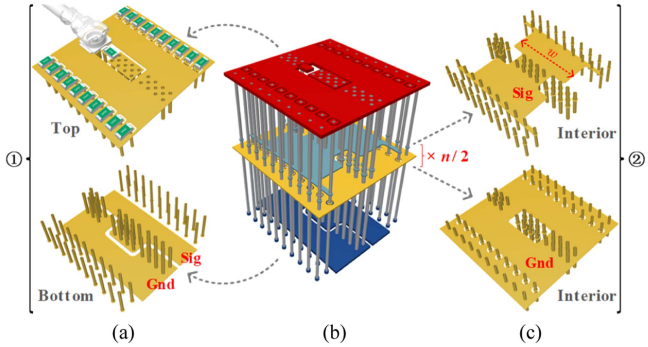

Fig. 6. Physical implementation of proposed MiniShunt. (a) Top and bottom layers. (b) Overall interconnection structure. (c) Interior n layers consisting of $n/2$ signal-ground (S-G) coupled pairs.

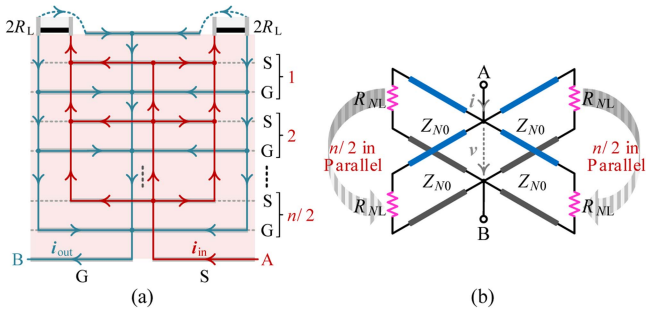

Fig. 7. Laminated configuration of proposed MiniShunt. (a) Sectional view of PCB lamination. (b) Equivalent transmission line model.

explanations are provided for the multilayer PCB structure depicted in Fig. 6 and the interior commutation loops shown in Fig. 7(a). These are illustrated in Fig. 8.

Fig. 8(a): The measured current enters the MiniShunt from the bottom layer. Fig. 8(b): The current signal reaches the interior $n/2$ signal layers and propagates simultaneously in both left and right directions. Fig. 8(c): The current signal from the signal layers reaches the load resistor. Due to the careful design of the signal layers, their overall equivalent wave impedance matches the load impedance, ensuring no signal reflection. This results in a broadband voltage signal across the load resistor. Fig. 8(d): The signal flowing through the load resistor returns through the interior ground layers. Fig. 8(e): The measured current signal finally exits the MiniShunt from the bottom layer, completing the measurement.

It is important to highlight that Fig. 7(a) illustrates a typical stripline transmission line configuration, where each signal layer is associated with upper and lower ground layers. In this setup, the electromagnetic field generated by the signal layer is completely confined within the two ground layers [28], facilitating effective decoupling between adjacent signal layers. This configuration forms the basis for the MiniShunt concept, which allows for the implementation of a parallel transmission line without mutual coupling among the individual units, i.e., Figs. 5 and 7(b).

Through the detailed explanation of the operating principle of MiniShunt as described above, the $n/2$ S-G pairs can be first equivalent to $n/2$ transmission line units connected in parallel.

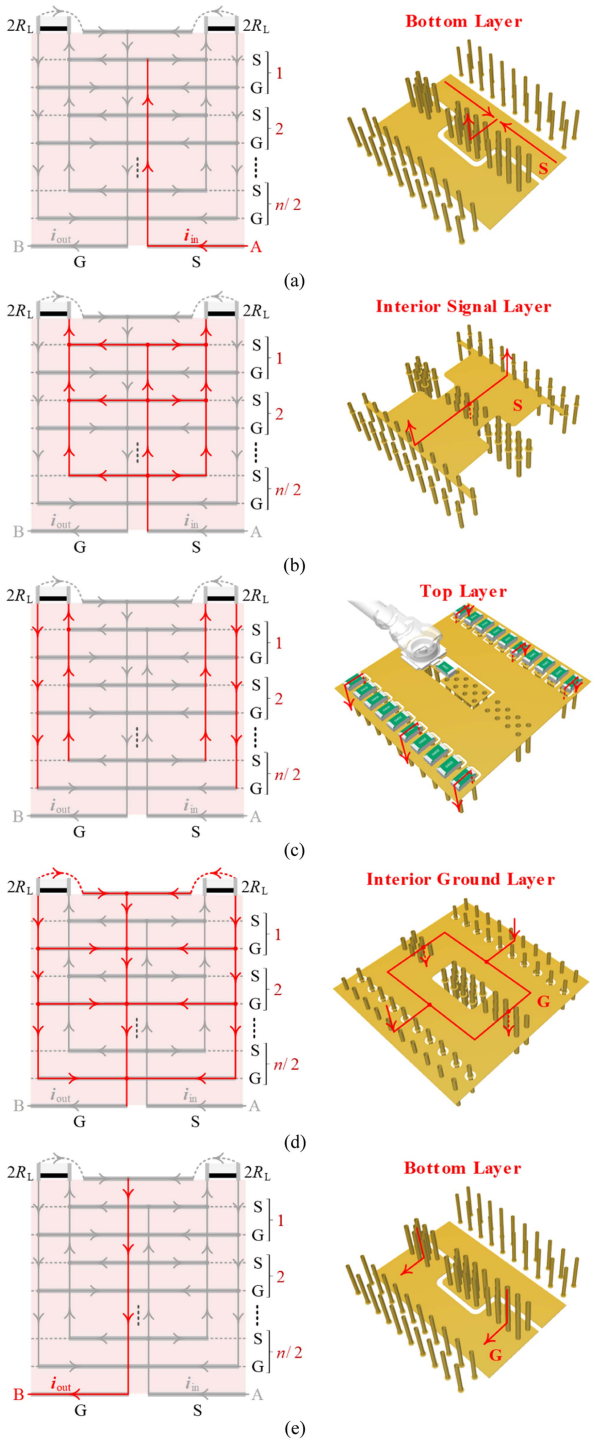

Fig. 8. Step-by-step breakdown of operating principle of proposed MiniShunt.

Second, thanks to the symmetrical design of the physical implementation, the total number of parallel connections for the transmission line units, i.e., N, is ultimately equal to n. This can be visually grasped and comprehended more vividly through the equivalent circuit model presented in Fig. 7(b).

In this case, according to (6), the design impedance for each unit Z_{N0} can be determined through

$$\{N = n\} \Rightarrow \{Z_{N0} = nR_{\mathrm{L}}\}. \tag{7}$$

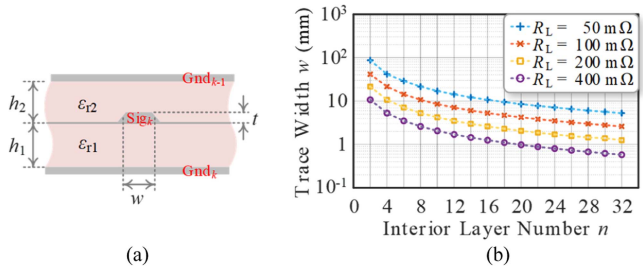

Fig. 9. Laminated design of proposed MiniShunt. (a) Schematic diagram of used stripline model. (b) Calculated trace width w versus layer number n under fixed R_{L}.

TABLE I
LAMINATED PARAMETERS OF EMPLOYED STRIPLINE MODEL

Parameters	Value	Parameters	Value
Sub. 1 Height (h_1)	99 μm	Sub. 2 Height (h_2)	104 μm
Sub. 1 Dielectric (ε_{r1})	4.11	Sub.2 Dielectric (ε_{r2})	4.31
Trace Thickness (t)	15 μm		

The precise calculation and design of Z_{N0} is performed using the PCB transmission line field solver, Polar Si9000. To accurately represent the laminated configuration of the signal trace shown in Figs. 6(b) and 7(a), the "Offset Stripline 1B1A" [29] configuration is chosen for the simulation and calculation, as shown in Fig. 9(a), where Sig$_k$ and Gnd$_k$ ($1 \leq k \leq n/2$) make up the kth S-G pair in Fig. 7(a), while Gnd$_{k-1}$ indicates the grounding layer of the (k-1)th S-G pair. h_1 and h_2 stand for the height of the substrate 1 and 2, respectively. ε_{r1} and ε_{r2} represent the dielectric constant of the substrate 1 and 2, respectively. t is the trace thickness. w refers to the trace width, as graphically demonstrated in Fig. 6(c). In the case of the fixed laminated parameters, i.e., h_1, h_2, ε_{r1}, ε_{r2}, and t, Z_{N0} directly impacts the value of w, and these two variables exhibit a negative correlation. As evident from (7), the introduction of n leads to an increase in Z_{N0}, thereby effectively reducing the required w.

The specific laminated parameters of the stripline model utilized in this article are provided in Table I. Notably, various board factories may adopt distinct PCB materials and processes, leading to variations in the laminated parameters. Hence, it is essential to adjust the values in Table I accordingly.

To examine the impact of layer number n on the overall size, the fixed nominal impedance R_{L} is considered, and n is varied from 2 to 32. The corresponding Z_{N0} values can then be obtained using (7). Based on these values, w is calculated by Table I and Si9000. The results are summarized in Fig. 9(b).

It is evident that increasing the value of n can significantly decrease the size of MiniShunt, and the utilization of multiple layers can reduce the design complexity by an order of magnitude or even more. To be more specific, considering a constraint of $w < 10$ mm, the minimum values of n required to achieve different design goals for R_{L} are determined. For a goal of 400 mΩ, $n = 4$ is sufficient. However, for a more stringent goal of 100 mΩ, n should be at least 10. Furthermore, for an even more demanding goal of 50 mΩ, a value of n up to 18 is just enough.

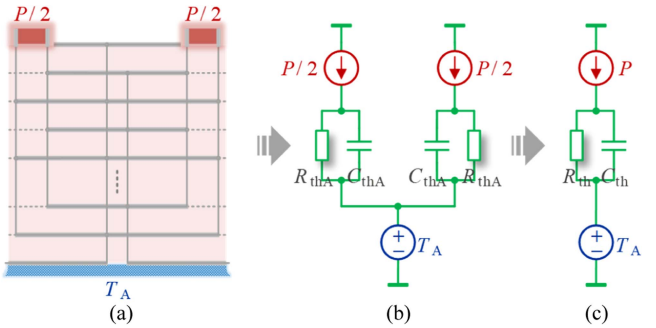

Fig. 10. (a) Actual physical model. (b) Equivalent thermal network model with dual heat sources. (c) Simplified thermal network model with single heat source for MiniShunt.

D. Thermal Design Considerations of MiniShunt

1) Thermal Network Model of MiniShunt: The total power dissipation generated after the current flows through the MiniShunt is denoted as P. Due to the complete symmetry of the MiniShunt, it can be considered as a dual heat source configuration, as illustrated in Fig. 10(a).

After the MiniShunt is soldered onto the PCB, its actual size is much smaller than both the application circuit and the 35 × 35-mm air-cooled heatsink on the backside [30]. Therefore, it can be assumed that the bottom surface of the MiniShunt remains at the ambient temperature T_A throughout.

Due to the presence of numerous vias in the central region of the MiniShunt, as shown in Fig. 8, directly connecting to the bottom layer of the PCB for efficient heat dissipation, it minimizes the coupling effects between heat sources on the left and right sides. Therefore, for the sake of simplification, it is assumed that the thermal coupling effect between the two heat sources is weak and can be neglected in the analysis.

Based on the aforementioned assumptions and the physical model depicted in Fig. 10(a), the equivalent thermal network model shown in Fig. 10(b) can be derived. In this model, R_{thA} and C_{thA} represent thermal resistance and thermal capacitance observed by a single heat source, respectively.

It should be noted that due to the involvement of vias and multilayer structures, the actual thermal network model is much more complex. However, in order to provide concise and valuable thermal analysis, a simplified approach is taken here, treating the multilayer PCB as a whole and approximating it as a first-order system with thermal resistance and capacitance in parallel. More accurate thermal network modeling, thermal performance analysis, and thermal capability improvements would be a focus of ongoing research, optimization, and enhancement of the MiniShunt.

Based on Fig. 10(b), the temperature rise ΔT of a single heat source under power dissipation $P/2$ can be expressed as

$$\Delta T = \frac{P}{2}\boldsymbol{Z}_{\mathrm{thA}} = \frac{P}{2}\frac{R_{\mathrm{thA}}}{R_{\mathrm{thA}}C_{\mathrm{thA}}s+1}. \tag{8}$$

Notably, $\boldsymbol{Z}_{\mathrm{thA}}$ is not easy to use or compute since it corresponds to the thermal impedance of the heat source to the environment under $P/2$ power dissipation. However, our primary interest lies in understanding the overall impact of the heat source on MiniShunt under P power dissipation, as it better aligns with typical usage scenarios.

From (8), further deduction can be made to obtain

$$\Delta T = \frac{P}{2}\boldsymbol{Z}_{\mathrm{thA}} = \frac{P}{2}\frac{R_{\mathrm{thA}}}{R_{\mathrm{thA}}C_{\mathrm{thA}}s+1} = P\frac{R_{\mathrm{thA}}/2}{(R_{\mathrm{thA}}/2)(2C_{\mathrm{thA}})s+1}$$
$$= P\frac{R_{\mathrm{th}}}{R_{\mathrm{th}}C_{\mathrm{th}}s+1} = P\boldsymbol{Z}_{\mathrm{th}} \tag{9}$$

where R_{th} and C_{th} can be, respectively, expressed as

$$R_{\mathrm{th}} = \frac{1}{2}R_{\mathrm{thA}},\ C_{\mathrm{th}} = 2C_{\mathrm{thA}}. \tag{10}$$

Equation (9) provides clear guidance that the new thermal impedance, $\boldsymbol{Z}_{\mathrm{th}}$, can exhibit a same physical process under power dissipation of P as the impedance $\boldsymbol{Z}_{\mathrm{thA}}$ under the power dissipation of $P/2$. Therefore, $\boldsymbol{Z}_{\mathrm{th}}$ is defined as the equivalent thermal impedance of the MiniShunt under a single heat source power dissipation P, as shown in Fig. 10(c).

Note that Fig. 10(c) does not depict a one-to-one physical model. It merely serves as a simplified equivalent model designed to facilitate the analysis and computation of the actual thermal effects of the MiniShunt.

2) Theoretical Foundation for Thermal Analysis of Mini Shunt: Based on Fig. 10(c) and (9), $\boldsymbol{Z}_{\mathrm{th}}$ can be expressed as

$$\boldsymbol{Z}_{\mathrm{th}} = \frac{R_{\mathrm{th}}}{R_{\mathrm{th}}C_{\mathrm{th}}s+1}. \tag{11}$$

From (11), the time-domain unit step response of MiniShunt with the addition of a heat source P can be written as

$$Z_{\mathrm{th}} = R_{\mathrm{th}}\left(1-\mathrm{e}^{-t/\tau}\right) \tag{12}$$

where $\tau = R_{\mathrm{th}}C_{\mathrm{th}}$ is the thermal time constant of the MiniShunt.

Furthermore, the time response of the temperature rise ΔT can be expressed as

$$\Delta T = PZ_{\mathrm{th}} = PR_{\mathrm{th}}\left(1-\mathrm{e}^{-t/\tau}\right). \tag{13}$$

It is defined that the maximum allowable temperature rise of the MiniShunt is ΔT_{m}. If, under a power dissipation P, the temperature rise process is completed within a time interval t_{c}, this process can be represented according to (13) as

$$\Delta T_{\mathrm{m}} = PR_{\mathrm{th}}\left(1-\mathrm{e}^{-t_{\mathrm{c}}/\tau}\right). \tag{14}$$

Fig. 11 provides a clear visualization of the process described by (14). It can be observed that when applying a higher power P_1 or P_2, the MiniShunt reaches the specified maximum temperature rise ΔT_{m} within the time intervals $t_{\mathrm{c}1}$ and $t_{\mathrm{c}2}$, respectively. At time of 3τ – 4τ, thermal equilibrium is reached, and the temperature differences with the environment are $\Delta T_1 = P_1R_{\mathrm{th}}$ and $\Delta T_2 = P_2R_{\mathrm{th}}$, respectively.

Notably, from Fig. 11, it is also evident that the applicability of (14) can be visually observed. Specifically, the discussed scenario here is that the steady-state temperature rise caused by P should be sufficient to exceed ΔT_{m}, e.g., P_1 and P_2, which can be expressed as

$$\{P > P_0\} \Rightarrow \{P > \Delta T_{\mathrm{m}}/R_{\mathrm{th}}\} \tag{15}$$

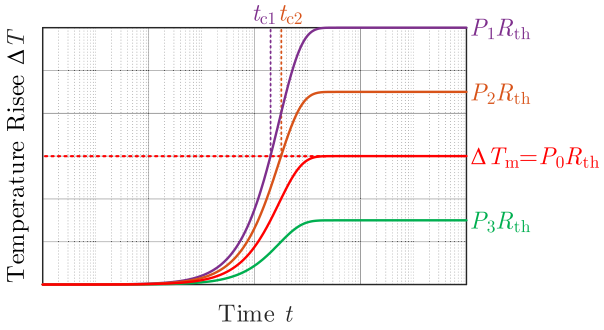

Fig. 11. Temperature rise ΔT over time t for MiniShunt at different levels of power dissipation P.

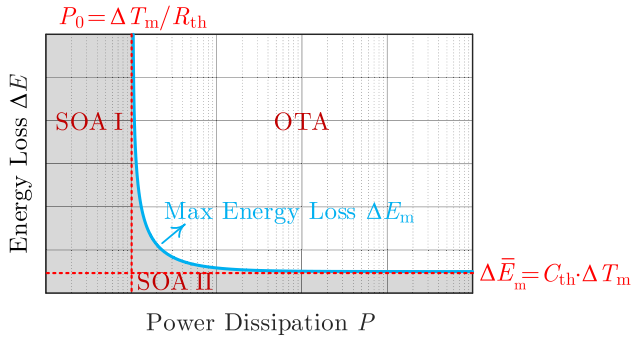

Fig. 12. Maximum energy dissipation ΔE_m determined by power dissipation P.

where P_0 is defined as the maximum static power dissipation indicator of the MiniShunt, representing the power dissipation at which the static temperature rise precisely reaches ΔT_m. Thus, for any $P < P_0$, such as P_3, the resulting steady-state temperature rise will not exceed ΔT_m. This indicates that the MiniShunt can operate continuously for extended periods under these power levels.

Next, we will discuss the maximum energy loss ΔE_m for the MiniShunt. This parameter informs us that the duration of applying higher power dissipation P should not exceed t_c. Exceeding this limit would result in a temperature rise that surpasses ΔT_m, posing the risk of overtemperature conditions.

Therefore, to calculate ΔE_m, it is necessary to know the value of t_c corresponding to specific P. By carefully observing (14), it can be noted that R_{th} and τ are known constants for a fixed design. Thus, for any given ΔT_m, t_c is solely dependent on P and can be deduced as

$$t_c = -\tau \ln\left(1 - \frac{\Delta T_m}{R_{th}P}\right) = -R_{th}C_{th} \ln\left(1 - \frac{\Delta T_m}{R_{th}P}\right). \quad (16)$$

Combining Fig. 11 and (16), the energy generated by a specific P during the t_c duration is defined as the acceptable maximum energy loss ΔE_m, and it can be expressed as

$$\Delta E_m = Pt_c = -R_{th}C_{th}P \ln\left(1 - \frac{\Delta T_m}{R_{th}P}\right). \quad (17)$$

Once again, it is important to note and clarify that the range of values for P is defined by (15).

Based on (17), the variation of ΔE_m with respect to P can be plotted, as shown in Fig. 12, where safe operating area (SOA) and OTA are defined as the safe operating area and the overtemperature area of the MiniShunt, respectively.

The lower-left region of the ΔE_m curve ensures that the temperature rise does not exceed ΔT_m, and is, therefore, labeled as the SOA. Conversely, the upper-right portion of the ΔE_m curve leads to a steady-state temperature rise surpassing ΔT_m, earning the label of OTA.

Additionally, the SOA can be further classified into SOA I and SOA II, depending on whether P exceeds $P_0 = \Delta T_m / R_{th}$. SOA I signifies that at this stage, P is sufficiently low for the MiniShunt's heat dissipation capacity to handle, allowing for continuous power dissipation and making it suitable for prolonged operation in the circuit. SOA II indicates that with higher P, the MiniShunt's heat dissipation capacity falls short, leading to a rapid temperature increase. Therefore, to maintain safety, the operating time must be limited to not exceed t_c to prevent the temperature rise from exceeding ΔT_m, as depicted in Fig. 11 for visual clarity.

Furthermore, from Fig. 12, it can be observed that the ΔE_m curve is a monotonically decreasing function within the range of $P > P_0$. Therefore, as the most conservative estimate, $\Delta \bar{E}_m$ is defined as

$$\Delta \bar{E}_m = \lim_{P\to\infty} \Delta E_m = \lim_{P\to\infty} \left[-R_{th}C_{th}P \ln\left(1 - \frac{\Delta T_m}{R_{th}P}\right)\right] = C_{th} \cdot \Delta T_m. \quad (18)$$

By examining (18), it becomes apparent that the ΔE_m curve is entirely situated above $\Delta \bar{E}_m$. As a result, $\Delta \bar{E}_m$ enables users to guarantee the utmost thermal stability and safe operation margin of the MiniShunt by solely considering this parameter value.

In summary, this section provides two standards for the max energy loss specification, namely ΔE_m in (17) and $\Delta \bar{E}_m$ in (18). Their advantages and disadvantages are summarized as follows.

ΔE_m: *Advantage*: Fully utilizes the testing capability at lower power levels. *Disadvantage*: Inconvenient to use, as it varies with the actual power dissipation and, thus, requires referencing a specific table for different dissipation levels.

$\Delta \bar{E}_m$: *Advantage*: Ensures absolute safety. *Disadvantage*: Sacrifices certain testing capability for low power levels.

3) Thermal Simulation Analysis of MiniShunt: To maximize the heat dissipation capability of MiniShunt, copper-filled via technology is employed for all the vias used. Taking the example of an $n = 16$ configuration MiniShunt with dimensions of $9 \times 9 \times 2$ mm, a total of 20 parallel-connected 0402 chip resistors [31] are utilized.

In the finite element analysis conducted using the COMSOL Multiphysics, the MiniShunt is set up with thermal insulation in all regions except for the bottom surface, which is maintained at a fixed temperature of 30 °C. This configuration simulates the favorable heat dissipation conditions on the MiniShunt's bottom surface after it is soldered onto the PCB, as described in Section II-D1). The temperature distribution of the MiniShunt

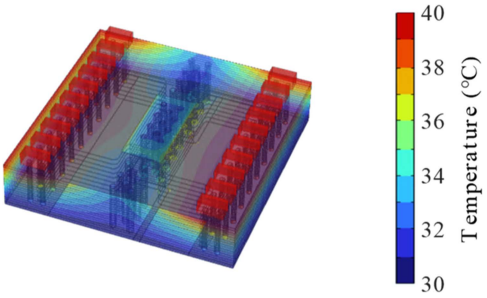

Fig. 13. Thermal equilibrium temperature profile of $n = 16$ MiniShunt at 4-W total power dissipation.

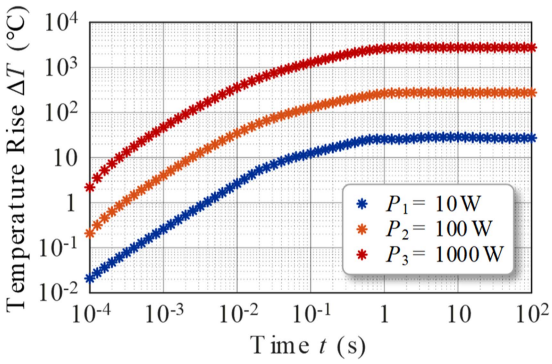

Fig. 14. Simulated temperature rise ΔT over time for MiniShunt at different levels of power dissipation P.

after reaching thermal equilibrium at a total power dissipation of 4 W is depicted in Fig. 13.

From Fig. 13, it is clear that the heat is mainly conducted from vias to the bottom layer, emphasizing the crucial role of the vias in improving the overall heat dissipation capacity of the MiniShunt. Moreover, the large number of vias in the central region of the MiniShunt, directly connecting to the bottom layer for the heat dissipation, contributes to a certain level of thermal decoupling between two heat sources on the left and right sides.

To further obtain the thermal performance parameters of MiniShunt and ultimately determine its maximum energy loss, simulations are conducted at power levels of 10 W, 100 W, and 1000 W. The resulting temperature rise over time is illustrated in Fig. 14. Additionally, by utilizing (13), the time response of thermal impedance can be obtained and is depicted in Fig. 15.

Fig. 15 reveals that the simulation curves of the thermal impedance response do not perfectly align with a first-order response. It is important to recognize that the complexity of the actual physical model of MiniShunt, which includes multiple layers and vias, making accurate thermal modeling a challenge. Relying solely on a first-order thermal network model may not accurately depict the actual thermal response of the MiniShunt. However, as an approximation to obtain essential thermal performance parameters, it still holds value and provides useful reference information.

By conducting nonlinear least squares fitting on the simulated thermal impedance response curves in Fig. 15, employing (12) as the form, the thermal impedance response equations for the

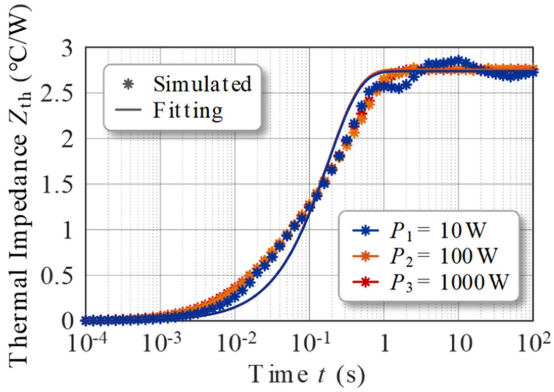

Fig. 15. Simulated and fitting thermal impedance $Z_{\rm th}$ over time for MiniShunt at different levels of power dissipation P.

MiniShunt at corresponding power levels can be expressed as

$$\begin{aligned} &\underline{P_1 = 10\text{W}}\text{: } Z_{\rm th1} = 2.738\left(1 - \mathrm{e}^{-t/0.1778}\right) \\ &\underline{P_2 = 100\text{W}}\text{: } Z_{\rm th2} = 2.752\left(1 - \mathrm{e}^{-t/0.1773}\right) \\ &\underline{P_3 = 1000\text{W}}\text{: } Z_{\rm th3} = 2.758\left(1 - \mathrm{e}^{-t/0.1786}\right). \end{aligned} \tag{19}$$

According to (19), the thermal resistance of the MiniShunt can be determined as $R_{\rm th} \approx 2.75$ °C/W, the time constant as $\tau \approx 0.18$ s, and further calculation yields the thermal capacitance as $C_{\rm th} = \tau/R_{\rm th} \approx 0.065$ J/°C.

According to (15), the maximum static power dissipation of the MiniShunt can be determined as $P_0 = \Delta T_{\rm m}/R_{\rm th} = \Delta T_{\rm m}/2.75$. Referring to (17), the maximum energy loss index I, $\Delta E_{\rm m}$, for the MiniShunt can be given by

$$\Delta E_{\rm m} = -0.18P \ln\left(1 - \frac{\Delta T_{\rm m}}{2.75P}\right),\ P > \frac{\Delta T_{\rm m}}{2.75}. \tag{20}$$

Based on (18), the maximum energy loss index II, $\Delta \bar{E}_{\rm m}$, for the MiniShunt can be calculated as $\Delta \bar{E}_{\rm m} = C_{\rm th} \cdot \Delta T_{\rm m} = 0.065 \Delta T_{\rm m}$.

It is evident that the permissible temperature rise $\Delta T_{\rm m}$ has a direct impact on three crucial thermal parameters: P_0, $\Delta E_{\rm m}$, and $\Delta \bar{E}_{\rm m}$. In practice, the temperature of the bottom surface $T_{\rm A}$ is influenced by the surrounding environment. As a result, the available margin for $\Delta T_{\rm m}$ should differ depending on specific application scenarios. The upcoming discussion will explore the factors to consider when determining the range of $\Delta T_{\rm m}$.

Taking into account the operating temperature range of -55 to $+155$ °C specified for 0402 chip resistors [31] and allowing for a certain operating margin, at a bottom surface temperature $T_{\rm A}$ of 25 °C, the maximum temperature rise $\Delta T_{\rm m}$ should not exceed 80 °C. For cases where $T_{\rm A}$ is higher than 25 °C, $\Delta T_{\rm m}$ should be reduced accordingly to avoid the MiniShunt entering the OTA. Considering the temperature coefficient of resistors as $\alpha = \pm 100$ ppm/°C, a temperature increase of 80 °C would result in a maximum variation in resistance of $\pm 0.8\%$, which remains within an acceptable range.

The typical thermal performance parameters for a 16-layer configuration MiniShunt are summarized in Table II.

TABLE II
SIMULATED THERMAL PERFORMANCE PARAMETERS OF $N = 16$ MINISHUNT

Parameters	Symbol	Value
Thermal Resistance	R_{th}	2.75 °C/W
Thermal Capacitance	C_{th}	0.065 J/°C
Thermal Time Constant	τ	0.18 s
Temperature Coefficient	α	±100 ppm/°C
Allowable Temperature Rise	ΔT_{m}	0 – 80°C
Max Static Power Dissipation	P_0	$\Delta T_{\text{m}}/2.75$
Max Safe Energy Loss	$\Delta \bar{E}_{\text{m}}$	$0.065\Delta T_{\text{m}}$

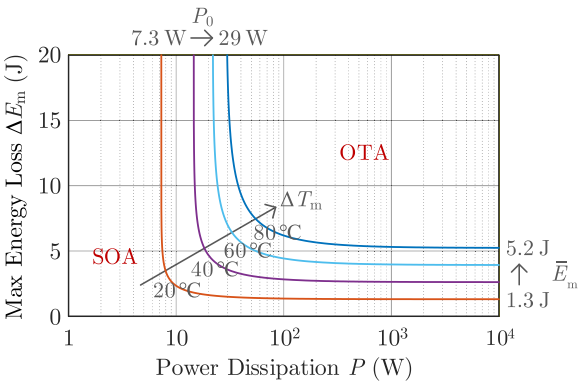

Fig. 16. P_0, $\Delta \bar{E}_{\text{m}}$ and SOA for $n = 16$ configuration MiniShunt with increasing allowable ΔT_{m} limits from 20 °C to 80 °C.

By utilizing (20), the SOA and OTA for MiniShunt can be plotted against the temperature rise ΔT_{m}, as shown in Fig. 16. It is evident that as the temperature rise limit expands from 20 °C to 80 °C, the P_0, $\Delta \bar{E}_{\text{m}}$, and SOA experience notable increases. This highlights the significance of efficient heat dissipation for the current shunts in order to maintain a larger margin of ΔT_{m}, particularly during high-power operations.

To gain a deeper understanding of the thermal parameters listed in Table II, let's consider a 100-mΩ MiniShunt as an example for reference. Assuming a ΔT_{m} limit of 20 °C, it can be calculated that P_0 is equal to 7.3 W. Consequently, the continuous conduction current through the MiniShunt in the circuit should not exceed 8.5 A. Additionally, the calculated value of $\Delta \bar{E}_{\text{m}}$ is 1.3 J. If we consider a higher conduction current of $I = 100$ A, resulting in a power dissipation of $P = 1$ kW, the recommended operating time, t_{c}, should not exceed 1.3 ms. Notably, this value is over four orders of magnitude larger than the typical switching times of WBG devices, which are usually in the range of tens or even several nanoseconds. This observation indicates that the MiniShunt has an ample amount of time to capture and restore the switching current transients of WBG power devices.

Based on the analysis and discussion in this section, it can be concluded that the current shunts are primarily designed for the precise characterization of high-speed transient currents while having limited capacity for continuous operation at high power levels. In order to achieve continuous power testing capability, precision power shunt resistors [32] may be a preferable option, although it comes at the cost of sacrificing high-frequency bandwidth and parasitic performance. This represents a tradeoff between different requirements.

(a) (b) (c)

Fig. 17. Frequency characteristics measurement of MiniShunt. (a) Test rig. (b) Experimental prototype. (c) Measurement principle based on $\boldsymbol{S}_{21}$ shunt-through.

TABLE III
DESIGN PARAMETERS OF MINISHUNT PROTOTYPES

Parameters	Value	Parameters	Value
Unit Design Impedance (Z_{N0})	1.6 Ω	Trace Width (w)	5.28 mm
Nominal Impedance 1 (R_{L1})	800 mΩ	Layer Number 1 (n_1)	2
Nominal Impedance 2 (R_{L2})	100 mΩ	Layer Number 2 (n_2)	16
Nominal Impedance 3 (R_{L3})	50 mΩ	Layer Number 3 (n_3)	16

III. EXPERIMENTAL VALIDATIONS AND ANALYSES

The development of three MiniShunt prototypes, MiniShunt-80, MiniShunt-10, and MiniShunt-05, is showcased in Fig. 17(b). These MiniShunts have a same dimension of 9 × 9 × 2 mm and possess nominal resistances of 800 mΩ, 100 mΩ, and 50 mΩ, respectively.

To validate the effectiveness of the proposed MiniShunt concept and physical implementation methodology, the unit design impedance Z_{N0} is set at 1.6 Ω, w can be further identified as 5.28 mm. For the MiniShunt-80, with R_{L1} of 800 mΩ, the corresponding n_1 can be calculated as 2 utilizing (7). In contrast, as the R_{L2} of the MiniShunt-10 decreases to 100 mΩ, the corresponding n_2 increases to 16.

Both the MiniShunt-80 and MiniShunt-10 mentioned earlier fulfill the design criteria outlined in (7). However, it is important to consider a counterexample, MiniShunt-05, which fails to meet the design criteria. MiniShunt-05 maintains the same number of layers as MiniShunt-10, with $n_3 = 16$, but reduces the nominal impedance R_{L3} to 50 mΩ. In this case, $Z_{N0} > n_3 R_{\text{L3}}$, which violates the impedance matching condition. Consequently, internal signal reflection is expected to occur within the MiniShunt-05, leading to a significant degradation in its bandwidth performance.

The detailed design parameters for these three MiniShunts are summarized in Table III.

A. Frequency Characteristics Calibration

In Fig. 17(a), the frequency properties of the developed three MiniShunts are calibrated by measuring the forward transfer coefficient $\boldsymbol{S}_{21}$ using the vector network analyzer (VNA) Agilent E5061B with a frequency measurement range of 3 GHz.

The further impedance analysis, including the measurement of the input impedance $|\boldsymbol{Z}_{\text{AB}}|$ and the calculation of the series parasitic inductance L_{s}, is automatically performed by the VNA E5061B, utilizing the port 1–2 shunt connection and following the $\boldsymbol{S}_{21}$ shunt-through measurement principle displayed in Fig. 17(c).

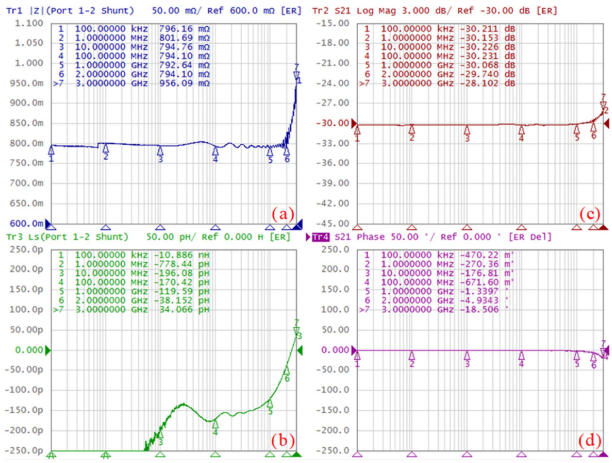

Fig. 18. Frequency characteristics (100 kHz – 3 GHz) of MiniShunt-80. (a) Input impedance. (b) Parasitic inductance. (c) Forward gain response. (d) Forward phase response.

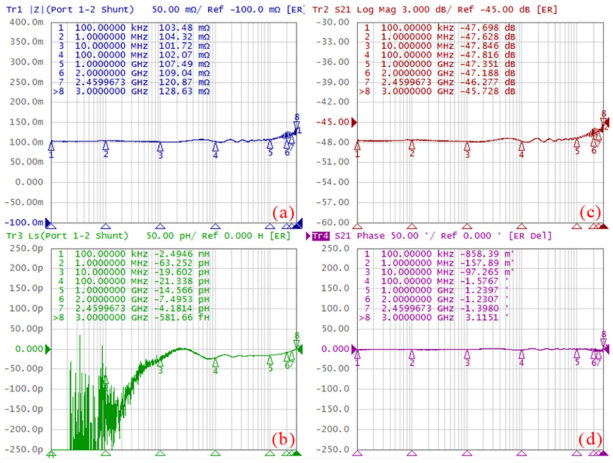

Fig. 19. Frequency characteristics (100 kHz – 3 GHz) of MiniShunt-10. (a) Input impedance. (b) Parasitic inductance. (c) Forward gain response. (d) Forward phase response.

Fig. 18 displays the calibration results of the MiniShunt-80 using the VNA E5061B. Observing Fig. 18(c) and (d), it is evident that the design criteria outlined in (7) are met, leading to a bandwidth for the MiniShunt-80 that exceeds 3 GHz.

Fig. 18(a) provides additional insight, revealing that the input impedance of MiniShunt-80 maintains a level of approximately 800 mΩ within the 2 GHz range. However, as the frequency extends to 3 GHz, its input impedance experiences an increase, reaching around 950 mΩ. In the range of 2 GHz, the series parasitic inductance is calibrated with a negative value, indicating a capacitive behavior. As the frequency crosses the zero point and becomes positive, the inductance gradually increases with frequency. It reaches approximately 34 pH at 3 GHz, as demonstrated in Fig. 18(b).

Fig. 19 depicts the calibration results of the MiniShunt-10 employing the E5061B. Undoubtedly, by satisfying the design criteria specified in (7), it is achievable to significantly decrease the input impedance of the MiniShunt-10 from 800 mΩ to 100 mΩ, by increasing the layer number from 2 to 16. Importantly, such an adjustment ensures the MiniShunt-10 retains its exceptional bandwidth and minimal parasitic performance.

Fig. 19(c) and (d) displays the forward gain and phase characteristics of the MiniShunt-10, respectively. It is worth noting that the MiniShunt-10 retains a bandwidth exceeding 3 GHz, with its phase characteristics remaining nearly constant at 0° within this frequency range. At 3 GHz, there is only a slight phase advancement of approximately 3°.

Fig. 19(a) and (b) illustrates the input characteristics of the MiniShunt-10. By satisfying impedance matching condition, the signal reflection within the MiniShunt-10 is minimized, resulting in minimal variations in input impedance and minimal parasitic inductance. As a result, the MiniShunt-10 maintains a consistent input impedance of 100 mΩ across a wide frequency range. At 3 GHz, the input impedance experiences the highest distortion, reaching approximately 129 mΩ.

Furthermore, within the 3-GHz measurement range, the parasitic inductance remains negative, indicating the absence of significant inductance characteristics. The near-zero inductance value of the MiniShunt-10 effectively reduces interference to the circuit under test (CUT). When combined with its compact size and high bandwidth, these characteristics work together to facilitate the implementation of a compact, ultrafast, and minimally invasive current measurement solution.

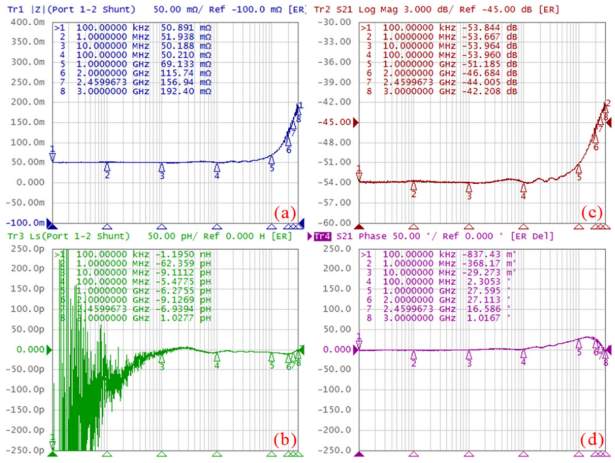

Fig. 20. Frequency characteristics (100 kHz – 3 GHz) of MiniShunt-05. (a) Input impedance. (b) Parasitic inductance. (c) Forward gain response. (d) Forward phase response.

Fig. 20 exhibits the calibration results of the MiniShunt-05 with the E5061B. Compared to the MiniShunt-10, the reduction of R_L disrupts the impedance matching condition, leading to a severe distortion in the high-frequency characteristics. This is evident in Fig. 20(c), where the bandwidth is significantly reduced from 3.14 GHz to 1.00 GHz. Additionally, the phase characteristics also exhibit a noticeable distortion, with a maximum phase lead distortion of approximately 33° observed at 1.5 GHz, as displayed in Fig. 20(d).

Fig. 20(a) illustrates the input impedance characteristics of the MiniShunt-05. Owing to internal signal reflection, its input impedance begins at 50 mΩ and experiences a rapid increase at

TABLE IV
PERFORMANCE PARAMETERS SUMMARY OF DEVELOPED MINISHUNTS

MiniShunt	Dimensions	Impedance	Bandwidth	Inductance L_s @ ≤ 3 GHz
MiniShunt-80	9×9×2 mm	800 mΩ	3.00 GHz	34 pH
MiniShunt-10	9×9×2 mm	100 mΩ	3.00 GHz	0 pH
MiniShunt-05	9×9×2 mm	50 mΩ	1.00 GHz	8 pH

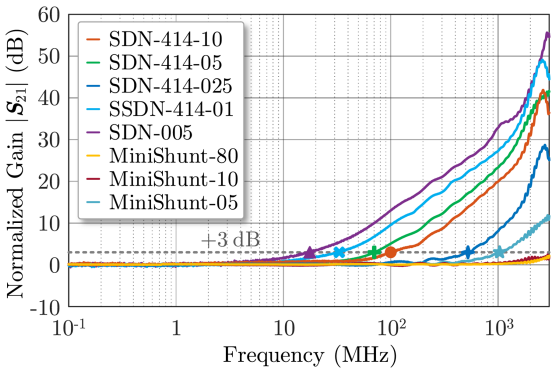

Fig. 21. Normalized forward gain comparison between developed MiniShunts and state-of-the-art commercial T&M coaxial current shunts.

TABLE V
T&M COAXIAL SHUNTS FOR EVALUATION AND COMPARISON

Part No.	Nominal Impedance	Measurement Bandwidth	Parasitic Inductance	Max Energy Loss
SDN-414-10	100 mΩ	0.10 GHz	5.6 nH	1.0 J
SDN-414-05	50 mΩ	0.07 GHz	6.8 nH	2.0 J
SDN-414-025	25 mΩ	0.50 GHz	3.6 nH	3.0 J
SSDN-414-01	10 mΩ	0.03 GHz	7.3 nH	6.0 J
SDN-005	5 mΩ	0.02 GHz	8.7 nH	3.0 J

1 GHz. By the time 3 GHz is reached, the input impedance has nearly quadrupled, reaching approximately 192 mΩ.

Fig. 20(b) illustrates the input series inductance of the MiniShunt-05. The measurement of series inductance reveals noticeable low-frequency noise, primarily caused by the very small resistance value of the MiniShunt-05. However, as the frequency increases, the noise diminishes rapidly, and the maximum value of the parasitic inductance, which is 8 pH, is observed at 28 MHz.

To facilitate a clearer and more intuitive comparison, the essential performance parameters of the three MiniShunt prototypes are presented in Table IV. It is important to emphasize once again that the measured series inductance L_s of the MiniShunt-10 within the 3 GHz range is negative, cf. Fig. 19(b), indicating equivalent capacitive properties. Therefore, for ease of comparison, its parasitic inductance is designated as "0 pH @ $\leq$ 3 GHz" in this context.

Finally, the forward gain characteristics of various commonly used coaxial shunts from T&M are evaluated and compared with MiniShunts. The results are summarized in Fig. 21 and Table V. It is evident that the sizes of the T&M coaxial shunts are considerably larger than those of the MiniShunts, which poses a hindrance to their effective applications in integrated designs with WBG power devices.

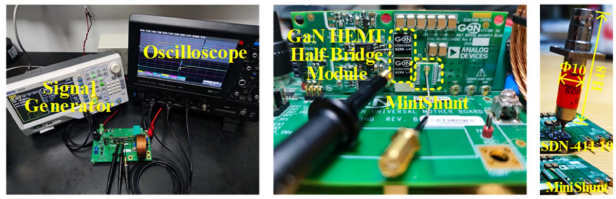

Fig. 22. Comprehensive performance verification based on DPT. (a) DPT test rig. (b) Half-bridge module with GaN E-HEMT GS66508B. (c) SDN-414-10 and MiniShunt-10 mounted onto PCB.

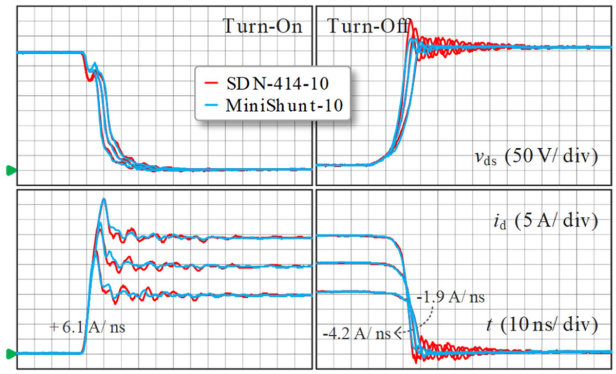

Fig. 23. Drain current i_d measured with SDN-414-10 and MiniShunt-10 at fixed V_{dc} of 400 V and varying I_d of 20 A, 30 A, and 40 A.

Furthermore, T&M coaxial shunts experience significant performance degradation at high frequencies beyond 10 MHz, leading to noticeable differences between their calibrated parameters, such as bandwidth and parasitic inductance, and their nominal values. Similar findings can be found in [19], [20], [21], and [22], providing additional references on this matter. As a result, these limitations make mainstream T&M coaxial shunts inadequate for fulfilling the demands of high-speed, miniaturized, integrated, and low-invasive measurements required for the dynamic characterization in power electronics applications that utilize ultrafast WBG power devices.

It is worth noting that even though T&M coaxial shunts have larger dimensions, their maximum energy loss is comparable to MiniShunts. This is primarily because T&M coaxial shunts rely on natural convection for heat dissipation, as depicted in Fig. 22(c), and do not require active cooling measures. In contrast, MiniShunts necessitate additional forced cooling at the bottom layer during operation to maintain a stable temperature and prevent them from entering the OTA.

B. Comprehensive Performance Verification Based on DPT

The MiniShunt-10 is further compared with the state-of-the-art commercial coaxial shunt SDN-414-10 listed in Table V by virtue of the GaN HEMT-based double pulse test (DPT), as depicted in Fig. 22, at a fixed V_{dc} of 400 V and varying I_d of 20 A, 30 A, and 40 A. The DPT incorporates the employment of oscilloscope Lecroy 715Zi (1.5 GHz, 20 GS/s) and GaN E-HEMT GS66508B (650 V, 30 A). Experimental results are given in Fig. 23.

TABLE VI
LOOP INDUCTANCE CALCULATED BY MINISHUNT-10 AND SDN-414-10

I_d	Turn-Off di_d/dt	L_{loop} Mini	L_{loop} SDN	L_c	$L_{loop}-L_c$ Mini	$L_{loop}-L_c$ SDN
20 A	−1.9 A/ns	8.87 nH	17.73 nH	8.17 nH	+0.7 nH	+9.6 nH
30 A	−2.7 A/ns	9.97 nH	22.42 nH		+1.8 nH	+14.3 nH
40 A	−4.2 A/ns	6.73 nH	21.87 nH		−1.4 nH	+13.7 nH

In order to achieve the best heat dissipation performance, the bottom layer of the MiniShunt is directly soldered to the PCB of the half-bridge module, as shown in Fig. 22(b). The PCB of the module is equipped with a thermal pad on its bottom side to enhance heat dissipation. Heat is transferred to the bottom side of the PCB using thermal vias and copper planes. For further detailed information regarding the specific connection details between the MiniShunt and CUT, please refer to [30].

Fig. 22(c) clearly illustrate that the MiniShunt-10, measuring $9 \times 9 \times 2$ mm, closely resembles the GS66508B with a dimension of $7 \times 8.4 \times 0.5$ mm. Compared to the bulky SDN-414-10 measuring $\Phi 10 \times$ H48 mm, the MiniShunt-10's compact size facilitates its effortless integration into a GaN HEMT half-bridge module.

Upon careful observation of Fig. 23, it becomes evident that as I_d increases, the magnitude of di_d/dt remains relatively constant at +6.1 A/ns during the i_d rising edge, while exhibits an increase during the i_d falling edge. Consequently, as a result of the significantly larger L_s of the SDN-414-10 compared to the MiniShunt-10, distinct and consistent voltage undershoots are observed at the v_{ds} falling edge, while hazardous and soaring voltage overshoots can be seen at the v_{ds} rising edge.

The loop inductance of CUT, denoted as L_{loop}, can typically be calculated by the di_d/dt during the switching phases, and can be represented as

$$\Delta v_{ds} = -L_{loop}\frac{di_d}{dt} \tag{21}$$

where Δv_{ds} represents the voltage undershoot during the turn-on phase or the voltage overshoot during the turn-OFF phase. The L_{loop} is primarily composed of two parts: the inherent loop inductance without the inclusion of the current shunt, denoted as L_c, and the additional inductance introduced by the current shunt, denoted as L_s. The value of L_c for the half-bridge module shown in Fig. 22(b) has been calibrated using the VNA E5061B and determined to be 8.17 nH.

The calculation results for loop inductance are compiled in Table VI. The MiniShunt-10, with its remarkably low series inductance, exhibits a calculated L_{loop} value that closely aligns with the VNA calibrated value of L_c. This serves as evidence that the MiniShunt-10 minimizes its impact on the CUT, establishing a robust basis for accurately capturing the authentic switching transients of WBG devices.

Upon closer analysis of the i_d waveforms, it can be observed that the MiniShunt-10 demonstrates significantly reduced oscillations and exhibits faster, smoother responses compared to its SDN-414-10 counterpart. These observations emphasize the outstanding performance of the MiniShunt-10, specifically its ultrahigh measurement bandwidth and near-zero inductance.

(a) (b)

Fig. 24. Steady-state thermal test. (a) Heat dissipation settings. (b) Temperature measurement settings.

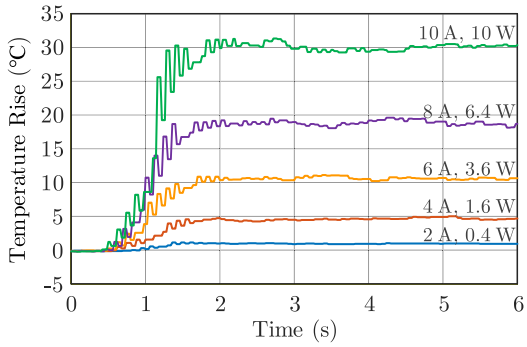

Fig. 25. Temperature rise of the top surface resistors of MiniShunt-10 relative to the bottom surface at different conduction currents ranging from 2 A to 10 A, and different power dissipation levels ranging from 0.4 W to 10 W.

This exceptional performance empowers the MiniShunt-10 to precisely capture and restore the ultrafast switching transients of WBG devices.

C. Thermal Performance Verification Through Steady-State and Impulse Testing

1) Steady-State Test: Building upon the test setup illustrated in Fig. 24, a 35 × 35-mm copper Pin-Fin heatsink was attached to the bottom side of the half-bridge module, accompanied by the forced-air cooling [30]. The conduction current and total power dissipation were varied to examine different scenarios. Thermocouples were utilized to measure the temperatures of the top-layer SMD resistors and the bottom layer of MiniShunt-10. Subsequently, the temperature difference was calculated, and the summarized findings are presented in Fig. 25.

Based on the information provided in Fig. 25, the MiniShunt-10 can be characterized by an approximate equivalent thermal resistance, R_{th}, of 3.02 °C/W, a thermal time constant, τ, of approximately 0.30 s, and an equivalent thermal capacitance, C_{th}, of around 0.099 J/°C. Utilizing these values, further calculations can be conducted to determine the values of P_0 and $\Delta\bar{E}_m$, which are given by $\Delta T_m/3.02$ and $0.099\Delta T_m$, respectively. The thermal parameters obtained from both experimental and simulation data are summarized in Table VII.

Upon observation, it is noted that the experimental results show slightly higher values in comparison to the simulation results. This can be attributed to the difficulty in accurately measuring the temperature of the MiniShunt's bottom surface

TABLE VII
THERMAL PARAMETERS OBTAINED THROUGH SIMULATION AND EXPERIMENT

–	R_{th}	C_{th}	τ	P_0	$\Delta\bar{E}_m$
Simulation	2.75 °C/W	0.065 J/°C	0.18 s	ΔT_m/2.75	0.065ΔT_m
Experiment	3.02 °C/W	0.099 J/°C	0.30 s	ΔT_m/3.02	0.099ΔT_m

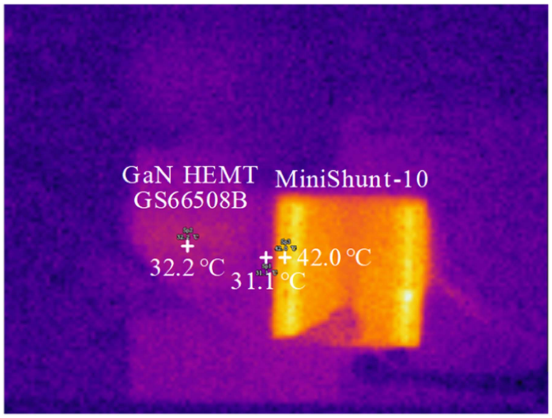

Fig. 26. Thermal image of MiniShunt-10 at the steady-state condition with a conduction current of 6 A and a total power dissipation of 3.6 W.

while ensuring optimal electrical and thermal contact between the MiniShunt and the CUT. Instead, measurements were taken in locations very adjacent to the MiniShunt's bottom surface, resulting in an increased thermal path length in the actual measurements. Consequently, thermal resistance and thermal capacitance may appear slightly larger. However, overall, the experimental results closely align with the simulation results, thereby validating the effectiveness of the simulation model. This model can serve as a starting point for further thermal design of the MiniShunt in conjunction with specific CUTs and testing conditions.

Fig. 26 showcases the thermal image of the MiniShunt-10 operating under a conduction current of 6 A and a total power dissipation of 3.6 W. Similar results can be compared with the simulated steady-state thermal distribution presented in Fig. 13.

It is crucial to highlight that in practical applications, when the MiniShunt is soldered onto the CUT, the temperature of the bottom layer can be influenced by the surrounding environment. Hence, it is imperative to perform a thorough thermal analysis, considering the basic thermal parameters of the MiniShunt, and taking into account the specific testing scenarios and circuit configurations. This analysis will help establish a reasonable ΔT_m limit, enabling the further determination of effective values for P_0, $\Delta\bar{E}_m$, and thermal SOA, cf. Fig. 16, ultimately achieving an optimal electro-thermal testing performance.

2) Impulse Test: To verify the high-power testing capability of the MiniShunt, a short-duration high-current impulse testing was conducted. It is essential to understand that the impulse testing differs from thermal performance testing. Thermal performance focuses on the system's ability to dissipate heat generated by a specific power dissipation, ensuring that the overall temperature rise remains within specified limits. On the other hand, the impulse testing assesses whether the resistor packaging itself can withstand the high power for a brief period. Put simply, if the resistor can effectively handle the instantaneous high power, then further consideration is given to the thermal changes. Otherwise, the resistor may sustain damage, resulting in variations in effective resistance. If this damage accumulates over time, it can eventually lead to failure.

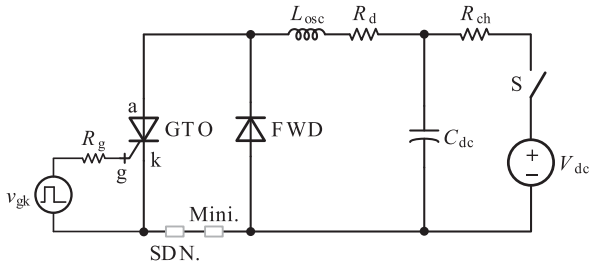

Fig. 27. Principle and configuration of high-current impulse generating circuit.

Fig. 27 demonstrates the principle of high-current impulse testing using the gate turn-OFF thyristor (GTO). Prior to the test initiation, switch S is activated to charge the bus capacitor C_{dc} to the bus voltage V_{dc}, following which S is opened. The stored energy in C_{dc} is harnessed to generate a single high-current pulse, where the amplitude of the current pulse is regulated by the magnitude of V_{dc}. The GTO maintains a fixed turn-on time of 2 μs, and the outcomes of the test are depicted in Fig. 28.

In this case, we initially estimate the temperature rise during short-duration high-current impulses. For the MiniShunt-025 with a nominal resistance value of 25 mΩ, if a sinusoidal current with a half-wave amplitude of 1 kA passes through it, the total energy dissipation within 2 μs is only 25 mJ. By using $\Delta\bar{E}_m = C_{th}\cdot\Delta T_m$, the instantaneous temperature rise of the upper SMD resistors relative to the bottom surface is only 0.25 °C. Similarly, for the MiniShunt-01 with a resistance value of 10 mΩ, the energy dissipation is 10 mJ, resulting in an instantaneous temperature rise of 0.1 °C. Therefore, from a thermal perspective, short-duration high-current pulses do not significantly affect the measurement capability of MiniShunt. However, at this point, the limitation shifts to the resistor's ability to withstand the pulsed power, which is related to the resistor's packaging.

To be more specific, a single 0402-packaging resistor can tolerate a pulsed power of around 50 W for 2 μs [31]. The MiniShunt incorporates 20 0402-packaging resistors connected in parallel, giving it a total 2-μs power tolerance of 1 kW. As a result, the MiniShunt-025 can withstand a sinusoidal current with a half-wave peak value of 282 A, while the MiniShunt-01 can handle up to 447 A. These values align with the test results shown in Fig. 28(b) and (c).

However, when the pulse amplitude exceeds the tolerance limit, it results in damage to the resistive layer inside the resistor, leading to the measurement errors that become increasingly prominent as the load current continues to rise. If the damage continues to accumulate, the resistor will eventually undergo complete failure, as depicted in Fig. 28(b).

If an 0805 resistor is used, the power tolerance can increase by nearly ten times compared to a single 0402 resistor, reaching 500 W [31]. This underscores the importance of wide-width resistor stripes in improving the tolerance to high-current impulses. Consequently, the design of next-generation

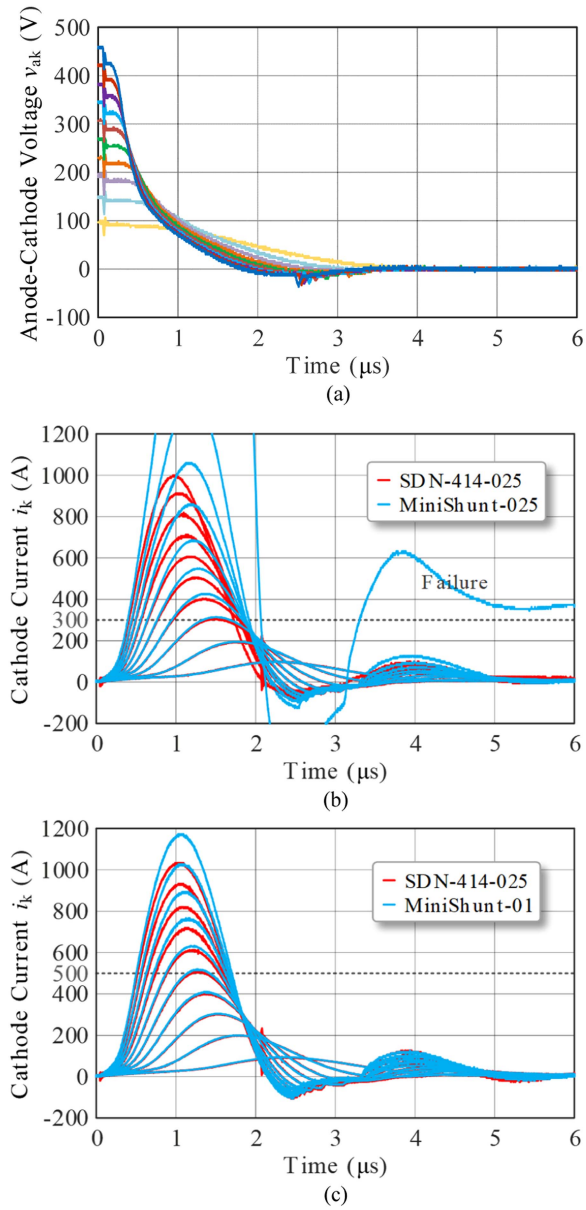

Fig. 28. Impulse test results at varying load current amplitude ranging from 100 A to 1 kA. (a) Anode-cathode voltage v_{ak}. (b) Cathode current i_k measured with SDN-414-025 and MiniShunt-025. (c) Cathode current i_k measured with SDN-414-025 and MiniShunt-01.

high-performance current shunts, which prioritizes high bandwidth, low parasitics, and resilience to high-current impulses, may incorporate the high-density stacking configuration of multiple coupled transmission lines based on the MiniShunt concept, as well as the terminal resistive load that includes the wide-width resistor stripes, as a replacement for the conventional approach of using multiple small resistors connected in parallel.

IV. Conclusion

This article introduces a novel MiniShunt concept for ultrafast, low-invasive, and high-integrated current measurements in the dynamic characterization of WBG power devices. Traditional IM-Shunts typically face the need to compromise their overall size to achieve low impedance, but this tradeoff can be effectively mitigated by stacking multiple coupled transmission line units within a limited space. On this basis, for a 100-mΩ design objective, as the interior layer number increases to 16, the required trace size experiences a significant reduction from the initial 180 mm by almost two orders of magnitude, reaching approximately 5 mm, which facilitates the effective realization of a remarkably compact 9 × 9-mm MiniShunt that still retains its exceptional electrical performance of a 3-GHz measurement bandwidth and a near-zero parasitic inductance. Thorough experiments conducted in both the frequency and time domains provide further confirmation of the benefits offered by the MiniShunt, including its compact size, integration capabilities, ultrafast response, and minimal invasiveness.

In addition, a comprehensive thermal analysis methodology is developed to facilitate the practical applications of current shunts. By utilizing the standard thermal response curve, the thermal resistance and thermal capacitance can be determined, enabling the further calculation of essential thermal parameters such as P_0 and $\Delta\bar{E}_m$ at a specified ΔT_m limit. These parameters not only provide the valuable guidance for both continuous and transient current testing of the current shunts but also serve as the foundation for establishing their thermal SOA. Furthermore, this thermal analysis methodology goes beyond current shunts and lays the theoretical groundwork for enhancing the transient thermal performance of common hotspots, such as power semiconductor devices in power modules.

Expanding the exploration of transient testing capabilities for current shunts to more extreme scenarios, further investigation is carried out. By subjecting the MiniShunt-025 and MiniShunt-01 to short-duration impulse testing with load current peaks of up to 1 kA, the significant impact of terminal resistor packaging on the current shunt's resilience against high-current impulses is unveiled. Therefore, it can be concluded that integrating the MiniShunt concept with wide-width resistor stripes at the terminals holds promise as an approach for developing future miniaturized, integrated, high-performance shunts capable of fast high-current transient testing.

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Yulei Wang (Student Member, IEEE) received the B.Sc. degree from China University of Mining and Technology, Xuzhou, China, in 2019, and the M.Sc. degree from Chongqing University, Chongqing, China, in 2023, both in electrical engineering. He is currently working toward the Ph.D. degree in electrical and computer engineering with McMaster University, Hamilton, ON, Canada.

His research interests include advanced packaging and industrial application of wide bandgap power devices.

Jiakun Gong received the B.Sc. degree in electrical engineering in 2022 from Chongqing University, Chongqing, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include advanced packaging and industrial application of wide bandgap power devices.

Mingrui Zou received the B.Sc. degree in electrical engineering from Kunming University of Science and Technology, Kunming, China, in 2020. He is currently working toward the Ph.D. degree in electrical engineering with Chongqing University, Chongqing, China.

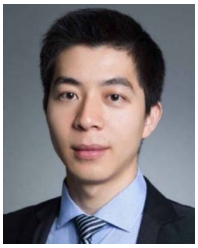
His research interests include advanced packaging and industrial application of wide bandgap power devices.

Liang Wang received the B.Sc. degree in electrical engineering from Chongqing University of Posts and Telecommunications, Xuzhou, China, in 2016, and the M.Sc. and Ph.D. degrees in electrical engineering from Chongqing University, Chongqing, China, in 2019 and 2024, respectively.

Since 2023, he has been a Visiting Student with the Department of Engineering, University of Cambridge, Cambridge, U.K. His research interests include advanced packaging and industrial application of wide bandgap power devices.

Yiming Gong received the B.Sc. degree in electrical engineering from Kunming University of Science and Technology, Kunming, China, in 2022. He is currently working toward the M.Sc. degree in electrical engineering with Chongqing University, Chongqing, China.

His research interests include advanced packaging and industrial application of wide bandgap power devices.



Chaoqiang Jiang (Senior Member, IEEE) received the B.Eng. and M.Eng. (first class hons.) degrees in electrical engineering and automation from Wuhan University, Wuhan, China, in 2012 and 2015, respectively, and the Ph.D. degree in electrical and electronic engineering from The University of Hong Kong, Hong Kong, in 2019.

He is currently an Assistant Professor with the Department of Electrical Engineering, faculty member with the State Key Laboratory of Terahertz and Millimeter Waves, City University of Hong Kong, Hong Kong. From 2019 to 2021, he was a Postdoctoral Research Associate with the University of Cambridge, U.K. Also, he has been affiliated with Clare Hall, University of Cambridge since 2021. In 2019, he was a Visiting Researcher with the Nanyang Technological University, Singapore. His research interests include power electronics, wireless power transfer, electric machines and drives, and electric vehicle technologies.

Dr. Jiang was the recipient of Gold Medals with Congratulations of the Jury in International Exhibition of Inventions of Geneva, Winner of CAPE Acorn Blue Sky Research Award at the University of Cambridge, Gold Medal in 3rd Asia Exhibition of Innovations and Inventions, Silver Award and Bronze Award in Shenzhen Qianhai Youth Innovation and Entrepreneurship Competition, and First Prize in the Interdisciplinary Research Competition at the University of Hong Kong. He is currently an Associate Editor of *IET Renewable Power Generation*, Guest Editor of *Energies, Electronics*, *Wireless Power Transfer*, IEEE OPEN JOURNAL OF VEHICULAR TECHNOLOGY.

Zheng Zeng (Member, IEEE) received the B.Sc. degree from Wuhan University, Wuhan, China, in 2009, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 2014, both in electrical engineering.

In 2014, he was with the School of Electrical Engineering, Chongqing University, Chongqing, China, where he was promoted to Associate Professor in 2017 and Full Professor in 2022. From 2018 to 2019, he was also a Research Fellow with School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. His research interests include advanced packaging for wide bandgap power device and grid-connected inverter for renewable energy integration.