Hysteresis Current Controller With Fixed Switching Frequency and Phase for Interleaved Converters

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***Abstract*—The changing switching frequency of the hysteresis current controlled (HCC) converter leads to difficult filter configuration and wide electromagnetic impact. Random current ripples from parallel HCC converters cannot be interleaved, and this limits the application in high-power conditions. To improve the EMI characteristics and reduce the filtering difficulty, this article proposes a double-loop hysteresis current controller to fix the switching frequency and phase. Specifically, the inner loop accurately fixes the switching frequency on the order of switching cycles through feeding forward the disturbances from the grid and the reference. The outer loop detects and fixes the switching phase by adjusting reference frequency. The double-loop structure is independent of the power control and takes effect by adjusting the hysteresis band width. Furthermore, by shifting the switching phase between parallel hysteresis current control (HCC) converters, the ripple of total current can be cancelled, which enables multiple interleaving of HCC converters. The improved HCC converter retains excellent dynamic and antidisturbance performance, laying the foundation for the usage of HCC in high-power condition. Finally, experimental results are provided to verify the effectiveness of the proposed method. Dynamic response and antidisturbance performance of the proposed HCC method are also tested. This article is accompanied by a video file demonstrating the effect of ripples interleaving of two parallel HCC converters.**

***Index Terms*—Hysteresis current control, parallel converters, ripple interleaving, switching phase control.**

I. Introduction

With the latest development of distributed generation technologies, grid-connected converters have a significant impact on the power quality of the grid. Different from the modulation methods based on triangular carrier comparison, such as sinusoidal pulsewidth modulation (PWM) or space vector PWM, hysteresis current control (HCC) generates switching signals in real-time through hysteresis comparison and logic judgment, providing stronger robustness and faster dynamic response [1], [2], [3], [4]. Under linear control with PWM, grid disturbances will cause fluctuations of output current by affecting working status of the loop. The increasingly complex grid environment also brings high-frequency resonance problems to the converter [5], [6], [7], [8]. But as nonlinear control, HCC enables the output current to follow the reference quickly and robustly without risk of overcurrent, while resisting disturbances from the grid. The special performance of HCC in high frequency stability, current limiting and harmonic resistance often meets the control requirements in harsh environments. Therefore, HCC is also widely used for applications such as active power filter (APF) and reactive power compensation that require high dynamic performance and reliability.

The most prominent disadvantage of HCC is that it cannot stabilize the switching frequency [9]. The changing switching frequency makes it difficult to choose filtering devices and switches, causes obvious current noise, and results in poor electromagnetic compatibility [10], [11], [12], [13], [14]. The changing frequency also causes the random changes in switching phase. When HCC converters are connected in parallel, the ripple of the total ac current swings randomly within the superimposed band of the converters. This increases the difficulty of filtering, deteriorates the power quality of point of common coupling (PCC) point, and causes uneven heating of the converters. The above shortcomings limit the application of HCC converters in parallel expansion when facing high power demand.

For fixing of the HCC switching frequency, a considerable amount of researches [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26] have been carried out. In [15], [16], [17], and [18], the frequency is fixed by calculating the hysteresis band width according to the HCC model. Though the influence from changing rate of the current reference is considered, the accuracy of the method is poor due to the control structure of open-loop calculating. In [19], [20], [21], [22], [23], and [24], the influence from operating delay on the switching frequency is considered and eliminated by finely adjusting the delay. But this method is still open-loop, and the accuracy of switching frequency is less improved. In [25] and [26], a frequency closed loop is introduced to control the switching frequency. But due to the neglect of the physical disturbances, there exists the steady-state error in the loop, resulting in poor frequency-fixing effect.

In addition to HCC, other nonlinear methods, such as sliding mode control (SMC) [27], [28], [29] and second order boundary

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control (BC2) [30], [31], can also provide excellent dynamic performance and achieve the goal of fixing switching frequency. But complexity of the two methods is much higher than HCC, and there exists risks of chattering [28], [31]. To fix the switching frequency, SMC relies on PWM or timing action [27], and steady-state error will be introduced.

Due to the insufficient accuracy of the switching frequency control in previous studies, the switching phase is in the random state, and no research on phase control has been carried out. As for the ripple interleaving of multiple machines in parallel, the current research focuses on the triangle carrier modulation methods such as sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) [32], [33], [34], which requires no additional switching phase detection and control. There is currently a lack of ripple interleaving for HCC converters.

In this article, a strategy for accurately fixing the HCC switching frequency and phase is proposed. The disturbances on the switching frequency from varying current reference, hysteresis band, grid voltage, and digital delay are modeled and analyzed. The frequency closed loop is designed to resist the influence from digital delay, and a feed-forward compensator is designed to compensate other physical disturbances. Based on the frequency loop, the outer phase loop is created to achieve the phase synchronization between the switching wave and the reference square wave. The detection of the switching phase is realized through a multiplication and counting algorithm. Finally, the accuracy of the frequency and phase loop, the ripple interleaving effect of two parallel-connected converters, and the antidisturbance ability of the proposed double loop are proved through experiments.

The rest of this article is organized as follows. Section II presents the HCC converter's switching model and the frequency loop. Section III shows the switching phase loop with a phase detector. The phase shifting and multiple realization of parallel HCC converters are also introduced. Section IV presents the environments of two parallel converters and the experimental results. Finally, Section V concludes this article.

II. Strategy of Fixing Switching Frequency

A. Modeling of Switching Frequency of HCC Converters

HCC has been used with a variety of converter types due to its quick dynamic response and outstanding antidisturbance performance. A typical grid-connected converter system is illustrated in Fig. 1. The grid impedance L_g and the grid side inductance L_f of the converter are combined and simplified into an inductor. The N line is dotted, indicating that that HCC can be applied to both three-wire and four-wire grids. Depending on the application conditions, the dc side of the converter may be equipped with various energy sources or loads. Or when applied in an APF, the dc devices can be ignored. The latter is also a typical application of HCC due to the dynamic performance requirements when compensating the harmonics.

The hysteresis comparator can limit the converter's output current to the band centered on the reference current by judging the difference between the reference current and the sampling

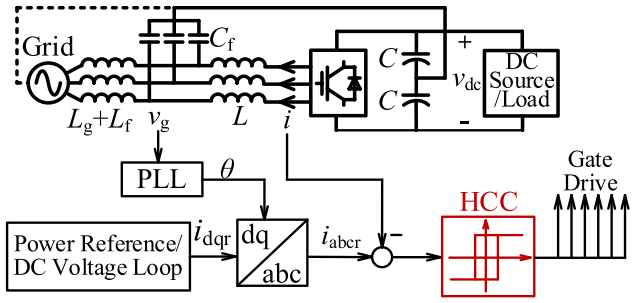

Fig. 1. Grid-connected HCC converter system.

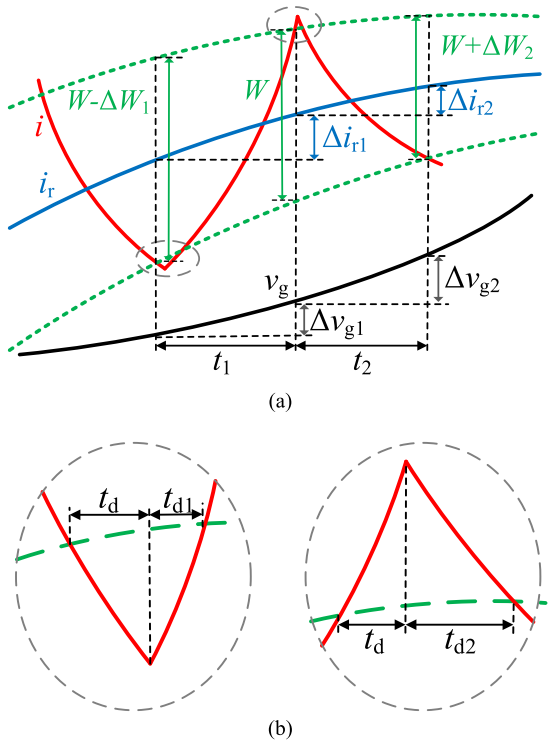

Fig. 2. Comparison model of the HCC controller considering that. (a) Grid voltage v_g, current reference i_r, and hysteresis band W change continuously. (b) Digital delay causes actual current to exceed hysteresis band limit.

value. Only one phase is analyzed due to the decoupling of the three-phase hysteresis comparison. Fig. 2 shows the comparison model in the HCC controller considering discrete digital delay as well as the influence of varying grid voltage, current reference and hysteresis band. In the model, the changes in hysteresis loop width are considered due to the possibility of improvement.

In Fig. 2(a), i_r stands for the current reference, v_g for the grid voltage, W for the changing hysteresis band, t_1 and t_2 for the turn-ON and turn-OFF time of the switch, Δi_{r1} and Δi_{r2} for the changes of i_r, and Δv_{g1} and Δv_{g2} for the changes of v_g, as well as ΔW_1 and ΔW_2 for the changes of W in those times.

In Fig. 2(b), the influence caused by the operation delay of the digital controller is partially enlarged. The delay comes from the discrete operation steps of the digital controller and switching dead times. The switching dead time is a fixed value, while the

turn-ON and turn-OFF delay caused by the discrete controller can be regarded as a random quantity whose mean value is half of the discrete step. The sum of the two can be approximately regarded as a constant digital delay t_{d}, so as to facilitate the calculation of the influence on the switching frequency. t_{d1} and t_{d2} represent the extra time it takes to correct the current exceeding the hysteresis band limit.

The change of the grid voltage will cause the ripple current flowing through L to be nonlinear. Let v_{g} be the grid voltage obtained from the PCC when the switch turns OFF, and let Δv_{g1} and Δv_{g2} be the variation of the grid voltage during the current rising time (t_1) and falling time (t_2). It is more accurate to incorporate the variation of grid voltage during the switching cycle into the model, while the model will become very complicated due to the nonlinear grid voltage. For accuracy and simplicity, Δv_{g1} and Δv_{g2} are linearized, and can be obtained according to the duty cycle from the grid voltage's total variation $\Delta v_{\mathrm{g}Ts}$ within switching period t_1+t_2

$$\begin{cases} \Delta v_{\mathrm{g1}} = (0.5 + v_{\mathrm{g}}/v_{\mathrm{dc}})\,\Delta v_{\mathrm{g}Ts} \\ \Delta v_{\mathrm{g2}} = (0.5 - v_{\mathrm{g}}/v_{\mathrm{dc}})\,\Delta v_{\mathrm{g}Ts} \end{cases}. \tag{1}$$

Linearized Δv_{g1} and Δv_{g2} simplifies the calculation of t_1 and t_2. After averaging, current equations for the filter inductor L during the whole switching cycle are shown as follows:

$$\begin{cases} L\frac{(W-\Delta W_1)/2+W/2+\Delta i_{\mathrm{r1}}}{t_1} = \frac{v_{\mathrm{dc}}}{2} - \left(v_{\mathrm{g}} - \frac{\Delta v_{\mathrm{g1}}}{2}\right) \\ L\frac{-W/2-(W+\Delta W_2)/2+\Delta i_{\mathrm{r2}}}{t_2} = -\frac{v_{\mathrm{dc}}}{2} - \left(v_{\mathrm{g}} + \frac{\Delta v_{\mathrm{g2}}}{2}\right). \end{cases} \tag{2}$$

In addition to the current rising and falling times within the band, the error time t_{e} caused by the digital delay t_{d} within one switching cycle is shown as

$$t_{\mathrm{d1}} = \frac{v_{\mathrm{dc}}/2 - v_{\mathrm{g}}}{v_{\mathrm{dc}}/2 + v_{\mathrm{g}}} t_{\mathrm{d}} \tag{3}$$

$$t_{\mathrm{d2}} = \frac{v_{\mathrm{dc}}/2 + v_{\mathrm{g}}}{v_{\mathrm{dc}}/2 - v_{\mathrm{g}}} t_{\mathrm{d}} \tag{4}$$

$$t_{\mathrm{e}} = 2t_{\mathrm{d}} + t_{\mathrm{d1}} + t_{\mathrm{d2}} = \frac{{v_{\mathrm{dc}}}^2}{(v_{\mathrm{dc}}/2)^2 - {v_{\mathrm{g}}}^2} t_{\mathrm{d}}. \tag{5}$$

In order to simplify the calculation, the idea of ignoring high-order quantities is used in the above process, which can effectively express the main components. That is, when calculating the influence of digital delay in (3)–(5), the changes of other physical quantities are ignored, and when calculating the influence caused by the change of various physical quantities in (1) and (2), the process of switching ON and OFF is regarded as ideal.

According to (2) and (5), the determinant of HCC converters' switching cycle T_{s} can be expressed as

$$\frac{1}{f} = T_{\mathrm{s}} = t_1 + t_2 + t_e = \frac{LWv_{\mathrm{dc}}^*}{(v_{\mathrm{dc}}^*/2)^2 - (v_{\mathrm{g}}^*)^2} + \frac{{v_{\mathrm{dc}}}^2 t_{\mathrm{d}}}{(v_{\mathrm{dc}}/2)^2 - (v_{\mathrm{g}})^2} \tag{6}$$

$$\begin{cases} v_{\mathrm{dc}}^* = v_{\mathrm{dc}} + \Delta v_{\mathrm{g}Ts}/2 \\ v_{\mathrm{g}}^* = v_{\mathrm{g}} + L\frac{\mathrm{d}i_{\mathrm{r}}}{\mathrm{d}t} - \frac{1}{2}L\frac{\mathrm{d}W}{\mathrm{d}t} - \frac{v_{\mathrm{g}}}{2v_{\mathrm{dc}}}\Delta v_{\mathrm{g}Ts}. \end{cases} \tag{7}$$

In (6), v_{dc}^* and v_{g}^* shown in (7) are the correction values of the dc voltage v_{dc} and the grid voltage v_{g} in consideration of changes in the physical quantities. Equation (6) also includes the switching cycle error t_{e} caused by the digital delay. It can be obtained from (5) that t_{e} changes periodically and obtains the maximum value at the peak and valley positions of the grid voltage.

Equation (6) establishes an accurate model of the switching frequency of HCC converters. Among the variables mentioned that affect switching frequency, it is necessary to evaluate the extent to which they affect the switching frequency. The most obvious factor is the periodically changing grid voltage v_{g}, as shown in (8), where V_{g} is the peak value of v_{g}, and other small quantities are ignored. (8) shows that the switching frequency changes greatly between the upper and lower limits during fundamental frequency cycle

$$\frac{(v_{\mathrm{dc}}/2)^2 - {V_{\mathrm{g}}}^2}{LWv_{\mathrm{dc}}} \le f_{v\mathrm{g}} = \frac{(v_{\mathrm{dc}}/2)^2 - {v_{\mathrm{g}}}^2}{LWv_{\mathrm{dc}}} \le \frac{v_{\mathrm{dc}}}{4LW}. \tag{8}$$

In order to separately analyze the influence of other physical quantities with small changes, the variation range of switching frequency is calculated using the idea of derivation of multivariate functions based on (6).

The influence of changing current command on switching frequency is shown in (9). The change rate of i_{r} depends on the working conditions. For example, when the APF is outputting harmonic current or the output mode of the converter changes suddenly, the impact Δf_i on the switching frequency may become very significant

$$\Delta f_i = -\frac{2v_{\mathrm{g}}}{v_{\mathrm{dc}}W} \cdot \frac{\mathrm{d}i_{\mathrm{r}}}{\mathrm{d}t}. \tag{9}$$

Equation (10) shows the effect of changing hysteresis band W on the switching frequency. Due to the limited variation range of W, the impact Δf_W is relatively small

$$\Delta f_W = \frac{v_{\mathrm{g}}}{v_{\mathrm{dc}}W} \cdot \frac{\mathrm{d}W}{\mathrm{d}t}. \tag{10}$$

There are two aspects of the impact on the change of HCC switching frequency from grid voltage. One is shown in (8), which is caused by the changes of v_{g} in power frequency. The other is caused by the change of v_{g} within one switching cycle, which causes the ripple current to be nonlinear. In (7), the first corresponds to v_{g}, and the second corresponds to $\Delta v_{\mathrm{g}Ts}$. The second influence on switching frequency $\Delta f_{\Delta v\mathrm{g}}$ is shown in (11). It can be found that $\Delta v_{\mathrm{g}Ts}$ causes little change in the switching frequency

$$\Delta f_{\Delta v\mathrm{g}} = \left(\frac{1}{8} + \frac{3{v_{\mathrm{g}}}^2}{2{v_{\mathrm{dc}}}^2}\right) \cdot \frac{\Delta v_{\mathrm{g}Ts}}{LW} = \left(\frac{1}{8} + \frac{3{v_{\mathrm{g}}}^2}{2{v_{\mathrm{dc}}}^2}\right) \frac{1}{LWf_s} \frac{\mathrm{d}v_{\mathrm{g}}}{\mathrm{d}t}. \tag{11}$$

The effect of digital delay on the change of the switching frequency is shown in (12). It can be estimated that the gain between the digital delay t_{d} and the switching frequency variation $\Delta f_{T\mathrm{d}}$ is relatively large, indicating that t_{d} has a significant impact on

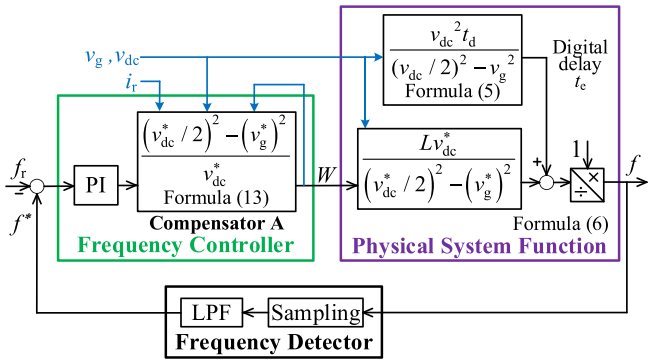

Fig. 3. Frequency loop to fix switching frequency.

the switching frequency

$$\Delta f_{Td} = -\frac{(v_{dc}/2)^2 - {v_g}^2}{(LW)^2} \cdot t_d. \tag{12}$$

For the sake of accuracy, the abovementioned influencing factors of switching frequency are quantitatively evaluated under the experimental condition in Section IV.

B. Strategy of Fixing Switching Frequency Based on the Compensated Frequency Loop

The traditional strategy of fixing the switching frequency of the HCC converter mainly calculates and adjusts the hysteresis band according to the relationship between the switching frequency and the grid voltage as well as the other variables. The accuracy of this method is poor because the digital delay, a factor that has a large impact on switching frequency, is ignored, and other variables may also be ignored due to the lack of model accuracy.

In order to fix the frequency more accurately, a frequency loop with feedforward that works by adjusting the hysteresis band is designed, as shown in Fig. 3.

There are two main ideas for designing the frequency loop: one is that the feedforward compensator can eliminate errors caused by grid voltage changes, current command changes, and hysteresis band changes, the other is that the closed-loop feedback can weaken the impact of digital delays. The closed loop can also weaken the errors caused by inaccuracy of sampling and model parameters during feedforward. The frequency detection is realized by timing the switching square wave, and a low-pass filter is added to remove the high-frequency components. The compensator A is designed, as given in (13), to reduce the impact of variations mentioned in (8)–(11). It is worth noting that the changing hysteresis band in (10) has little influence on the switching frequency, and can be omitted to save computing resources when calculating

$$\mathrm{A} = \frac{(v_{dc}^*/2)^2 - (v_g^*)^2}{v_{dc}^*}. \tag{13}$$

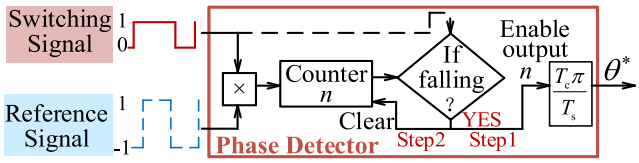

Fig. 4. Topology of phase detector.

The error and noise of the voltage sampling will affect the switching frequency through the feedforward path of compensator A. It has been proved in appendix that this influence is so small that it can be ignored.

The impact of digital delay on switching frequency cannot be offset by the feedforward compensator A, because in (6), the influence caused by digital delay and the effect of hysteresis band are two independent terms. However, in the model shown in Fig. 3, the error introduced by the digital delay, as the disturbance of the frequency loop, can be suppressed by the formation of the frequency closed loop. The transfer relationship of the switching frequency is analyzed according to Fig. 3, as shown in

$$(H_f(s)f - f_r) \cdot H_{PI}(s) \cdot L + t_e = 1/f \tag{14}$$

where $H_f(s)$ is the transfer function of the frequency detector, showing the low pass filter (LPF) characteristics of high cut-off frequency, and $H_{PI}(s)$ is the transfer function of the PI controller.

Solving (14), and using Taylor expansion to approximate and equivalent the calculation results, the transfer function of the switching frequency can be obtained

$$f^* = H_f(s)f = f_r - \frac{t_e}{LH_{PI}(s)}. \tag{15}$$

It can be seen from (15) and Fig. 3 that the existence of the feedforward compensator eliminates the influence of the grid voltage and current reference on the switching frequency. The disturbance t_e caused by the digital delay mainly contains dc component and the low frequency quantity from changing grid voltage. The high gain of PI controller in the low frequency band can greatly weaken the disturbance of the digital delay. These benefits demonstrate the necessity of introducing closed-loop for frequency control.

III. Strategy of Fixing Switching Phase

A. Phase Detection Method for the Switching Signals

Only fixed and controllable switching phase can lay the foundation for multiplexing of HCC converters, and the strategy of fixing switching frequency provides the basis for the control of phase. Only when the switching frequency is relatively fixed and stable, the switching phase can be measured rather than changing randomly. To detect and control the switching phase, the reference square wave is introduced and the phase detector is proposed to get the difference between switching wave and the reference.

The phase detection method presented in Fig. 4 runs in a discrete controller. Fig. 5 illustrates the principle of multiplier phase detector.

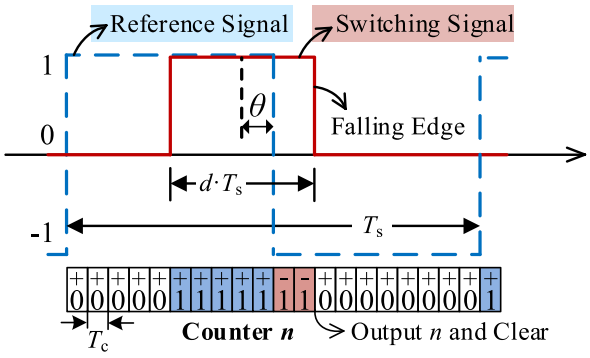

Fig. 5. Principle of phase detector.

In Figs. 4 and 5, the dotted square wave is the reference signal whose value varies between -1 and 1. Frequency of the wave is the same as the reference switching frequency f_r. The square wave with the solid line is the switch triggering command of the converter, and its value varies between 0 and 1. θ and $\theta*$ stands for the actual and measured switching phases, describing the phase difference between the center line of the switching wave and the falling edge of the reference wave. T_s stands for the switching period, T_c for the control period, and d for the duty cycle of switching square wave.

The two square waves are multiplied and accumulated in the discrete counter. If the falling edge of the switching wave is detected, the accumulated value n is output to get the phase $\theta*$ (Step1), and then it is cleared to 0 to start the next counting cycle. As can be seen from Fig. 5, the degree of asymmetry of the switching wave relative to the falling edge of the reference wave can be measured.

If the phase difference θ in Fig. 5 is large enough, it may not be accurately measured because the ON-state of switching wave is fully covered by 1 state or -1 state of the reference wave. With a change in the switching wave's duty cycle d, the functional relationship between the counter's output n and the switching phase θ is plotted in Fig. 6. The centrosymmetric graph in Fig. 6 can be separated into a linear region and two nonlinear regions. The width of the linear region changes with the duty cycle. When the switching phase θ is in the linear region, the slope of the function is maintained at T_s/T_c, which ensures that the phase detection result will not be affected by the duty cycle. This allows the phase of the switching wave to be accurately determined by

$$\theta^* = n \cdot T_c \pi / T_s. \tag{16}$$

When the switching phase θ is located in the nonlinear region, the phase detection result $\theta*$ obtained from (16) can reflect the lead or lag of switching phase, which is conducive to the control of the phase.

It is important to note that this phase detection method only requires a very tiny amount of calculation, and that when the switching phase is successfully controlled, the switching phase θ is typically in the linear region.

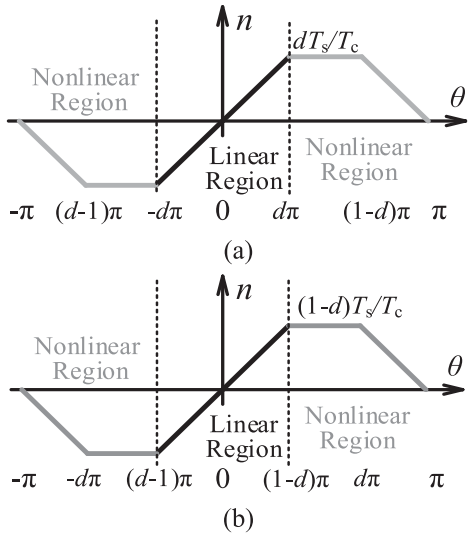

Fig. 6. Relationship between the input phase and the output of the counter when: (a) d $\leq$ 0.5 and (b) d $>$ 0.5.

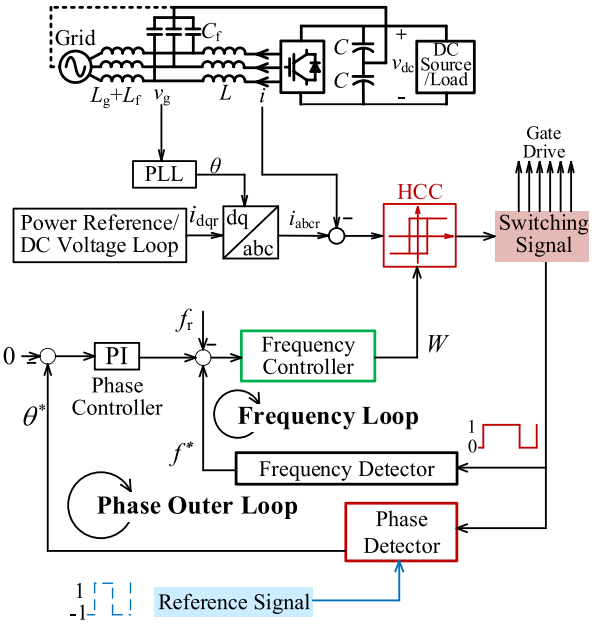

Fig. 7. Connection between the frequency control and phase control.

B. Strategy of Fixing Switching Phase Based on a Phase Outer Loop

Based on the frequency loop and phase detector, the method of phase control is designed, as shown in Fig. 7. When the phase control is working, the output of the PI controller is assigned as the additional frequency command of the frequency loop. Due to the integral relationship between the frequency and the phase, the switching phase can be corrected by fine-tuning the switching frequency. The details of double loop and phase correction are shown in Fig. 8.

As the inner loop, the control speed of the frequency loop needs to be set high. The gain of the PI controller is set to

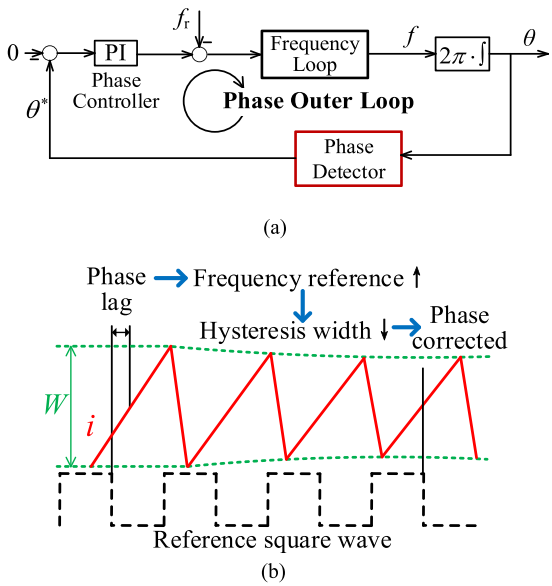

Fig. 8. Logic of the switching phase control. (a) Structure of the frequency loop and the phase loop. (b) The process of phase adjustment and correction.

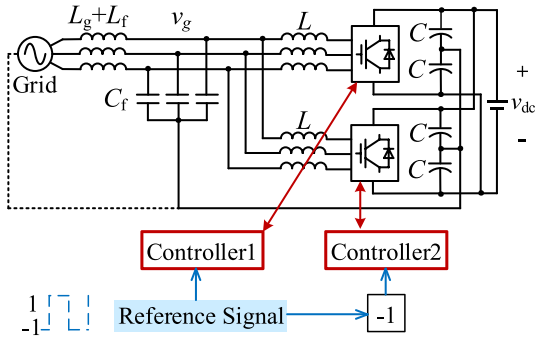

Fig. 9. Structure of two HCC converters in parallel.

a large value, resulting in a short response time. But for the phase loop, except setting the PI controller with lower gain, the integrator from the switching frequency f to the phase θ further depresses the bandwidth. This results in a much slower response speed of the phase outer loop than the frequency loop, forming a reasonable structure of double loop. Whenever the switching phase needs to be adjusted, the frequency loop works quickly to change the switching frequency, transferring the adjustment to the phase due to the integral effect.

Although the band width is changing to control the switching frequency and phase, it will not affect the performance of the converter during fundamental/harmonic current and power control. The response time of HCC is always within several switching cycles as long as the value of the band width is appropriate. Therefore, the amplitude limit is necessary for the frequency controller.

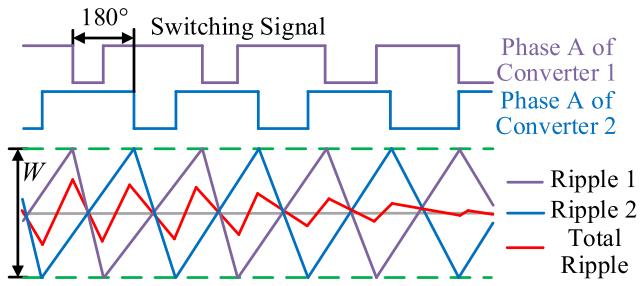

Fig. 10. Current ripple cancellation when the switching phases are controlled and interleaved.

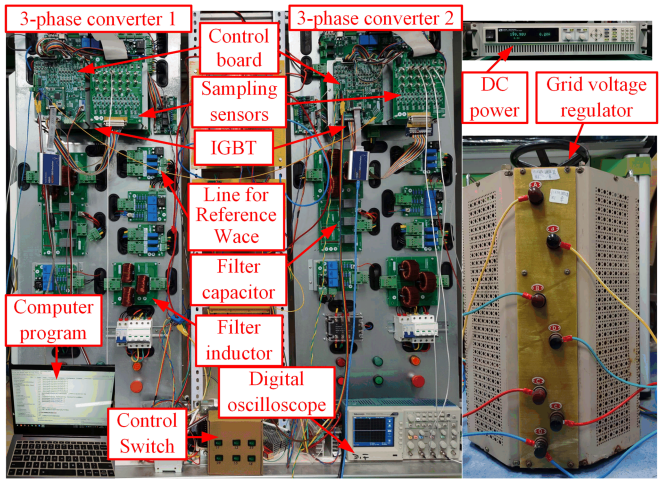

Fig. 11. Photograph of experimental system.

TABLE I
SYSTEM PARAMETERS

Definition	Symbol	Value
Rms line-to-line ac voltage	v_{grms}	73.5 V
Dc voltage	v_{dc}	200 V
Filter capacitance of dc side	C	1000 μF
Filter inductance of converter side	L	1200 μH
Filter capacitance of ac side	C_f	10 μF
Filter inductance of grid side	L_f	45 μH
Percentage impedance of grid voltage regulator	U_k%	5.40%
Rms line current of each converter	I_{rms}	1.0A – 8.5 A
Power level of the experiment	P	0.3–2.2 kW
Reference switching frequency	f_r	10 kHz
Sampling frequency	f_S	500 kHz
Hysteresis comparison period	T_c	2 μs
Dead time of switches	T_d	3.5 μs

TABLE II
INFLUENCE RANGE OF VARIABLES ON SWITCHING FREQUENCY

Disturbance variable	Disturbance symbol	Frequency changing range
Changing current reference in (9)[a]	di_r/dt	0.63 kHz
Changing hysteresis band in (10)	dW/dt	0.19 kHz
Changing grid voltage in (11)	Δv_{gTs}	0.27 kHz
Digital delay in (12)	t_d	2.23 kHz

[a] When the converter outputs a sinusoidal current stably.

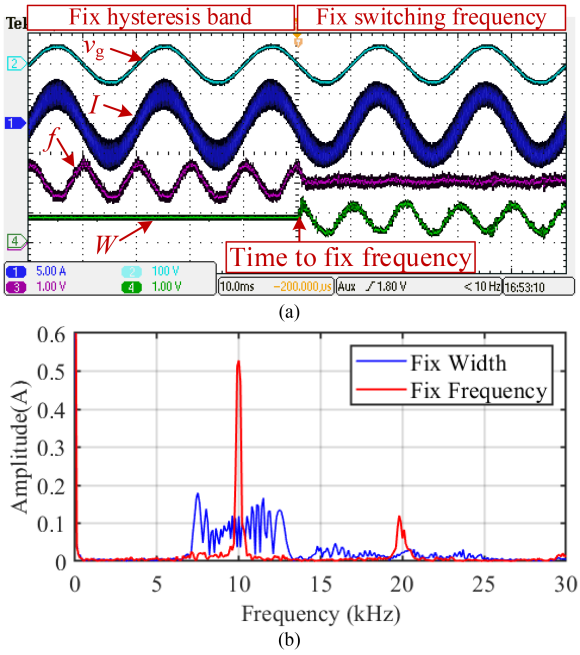

Fig. 12. HCC converter switches from fixing hysteresis band to fixing switching frequency. (a) Grid voltage v_g, output current I, switching frequency f (5 kHz/div), and hysteresis band W (1 A/div). (b) Frequency spectrum for I when fixing width and fixing frequency.

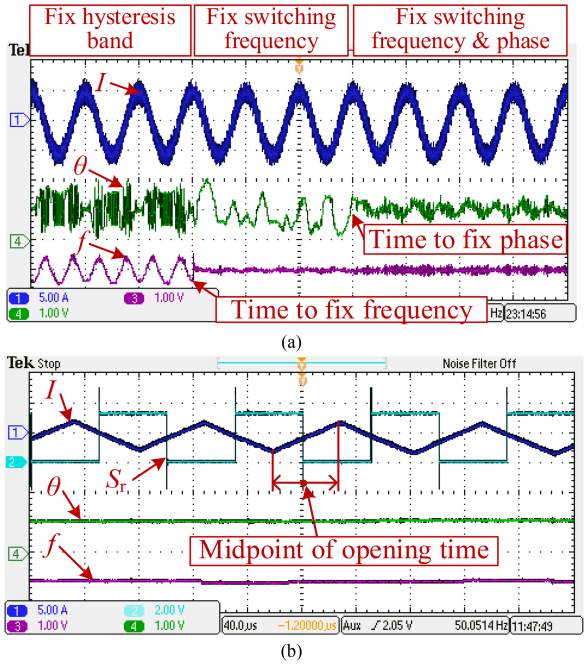

Fig. 13. HCC converter undergoes the three stages in sequence: fixing hysteresis band, fixing switching frequency, and fixing switching phase. (a) Output current I, phase detection result $\theta*$ (180°/div), and switching frequency f(5 kHz/div). (b) Partial enlarged view of the fixed phase, including the reference square wave S_r.

C. Ripple Cancellation of Parallel HCC Converters

Lots of researches on ripple interleaving and cancellation of paralleled converters based on SPWM has been done [27], [28], [29], and an example of two converters in parallel is shown in Fig. 9. Due to the superposition and cancellation of current ripples, parallel converters can share filter inductors L_f and capacitors C_f on the grid side to filter the ripple in the total current.

But for HCC converters in parallel, it is necessary to set *LCL* filters respectively to filter current ripples. Because when two HCC converters share the grid-side filters, as shown in Fig. 9, their current ripples are randomly superimposed, resulting in a large size of the required filter, serious electromagnetic interference, uneven heating, and noise problems.

The proposed double loops of the switching frequency and phase provide the basis for ripple control and cancellation. When two HCC converters are connected as Fig. 9, if providing the reference square wave with the same frequency and a 180° phase difference, the total current ripple will be weakened, and even be completely eliminated when the switching duty cycle is 0.5. As illustrated in Fig. 10, the harmonic frequency of the total current ripple is twice as high as the switching frequency. This makes it possible for parallel HCC converters to share the grid filters, and a smaller filter can be applied to handle the total ripple. Certainly, when 3 or more HCC converters are connected in parallel, ripple interleaving can also be achieved using the proposed strategy.

It is worth noting that the control of the switching frequency and phase of the HCC converter is achieved through adjusting the hysteresis band, which is independent of its power control. This indicates that the control of the switching frequency and phase will not be affected by the changes of the working state of the HCC converter, harmonic problems introduced by grid-side equipment and nonlinear loads, and stability problems caused by insufficient stability margins in the power loop. The corresponding influences from the above problems are accurately compensated by feedforward in the frequency loop. At the same time, the proposed loops will not affect the dynamic and steady-state performance of the HCC converter.

IV. Experimental Results and Discussion

The theory and control methods mentioned in the previous sections are validated experimentally. The experimental platform shown in Fig. 11 is built according to the topology in Fig. 9. The hardware parameters and working conditions in the experiments are listed in Table I. The changing ranges of the switching frequency caused by each physical quantity and digital delay shown in (9)–(12) under the experimental parameters are listed in Table II.

The two converters of three-phase four-wire topology share the same dc source with their neutrals connected. The grid voltage regulator connected to the grid on the primary side is used to provide ac voltage, and its leakage inductance is measured to be about 20 μH. The converters obtain the voltage phase at the filter capacitor through a phase-locked loop (PLL), and inject the pure active current with the peak value of I_p into the ac side.

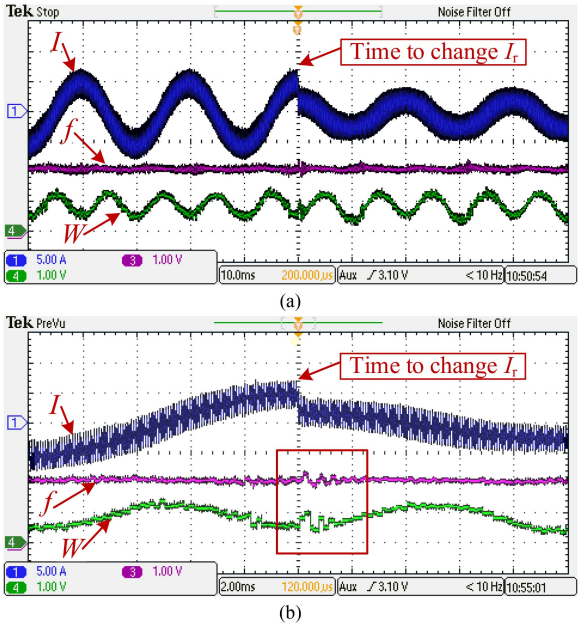

Fig. 14. Output current reference changes suddenly from 5 A to 3 A for the HCC converter with current reference feed-forward. (a) Output current I, switching frequency f (5 kHz/div) and hysteresis band W (1 A/div). (b) Partial enlarged view when the reference changes suddenly.

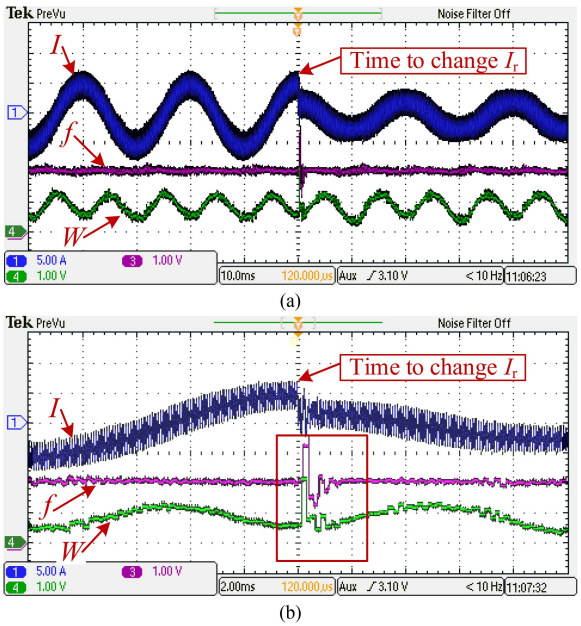

Fig. 15. Output current reference changes suddenly from 5 A to 3 A for the HCC converter without current reference feed-forward. (a) Output current I, switching frequency f (5 kHz/div) and hysteresis band W (1 A/div). (b) Partial enlarged view when the reference changes suddenly.

TI's DSP28377D is used for discrete digital control of the converter. Calculation of PLL, generation of current reference, control of the frequency loop and phase loop are executed in the 10 kHz control interruption. The interrupt frequency of the control law accelerator (CLA) in the DSP is set to 500 kHz, and the sampling conversion, switching frequency calculation,

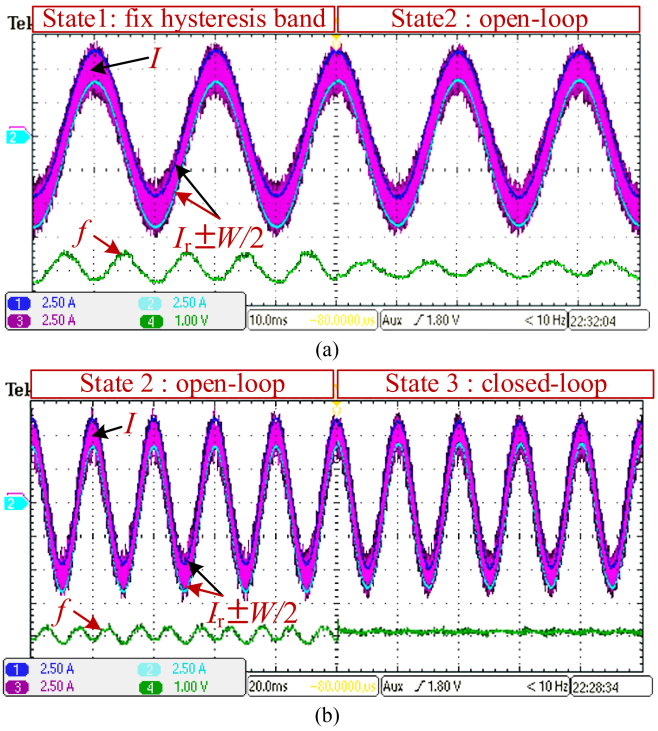

Fig. 16. Output current I, the upper and lower hysteresis sideband $I_r \pm W/2$ (2.5 A/div), switching frequency f (5 kHz/div) for. (a) Fixing hysteresis band (state 1) and open-loop fixing frequency (state 2). (b) State 2 and closed-loop fixing frequency (state 3).

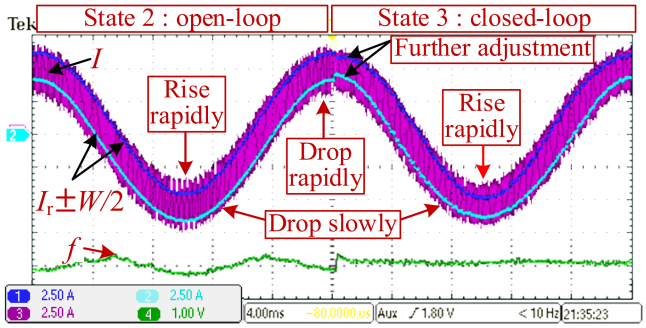

Fig. 17. Hysteresis comparison details when switching from open loop to closed loop for fixing switching frequency: output current I, the upper and lower hysteresis sideband $I_r \pm W/2$ (2.5 A/div), and switching frequency f (5 kHz/div).

switching phase detection, hysteresis comparison, and switching action are executed in the CLA. This means that for the converter with a switching period of 100 μs, the response time of the hysteresis comparison is less than 2 μs. When adding the dead time of the switching action, the turn-ON and turn-OFF delay t_d of the switches caused by the digital controller is about 4.5 μs totally.

In the experiment, it is necessary to provide reference square waves with the phase shift of 180° for the phase detectors of two converters. Set the converter 1 as the master to generate a reference square wave signal through the enhanced PWM module in the DSP chip. The other converter is set as a slave, and the reference signal is obtained from the converter 1 by

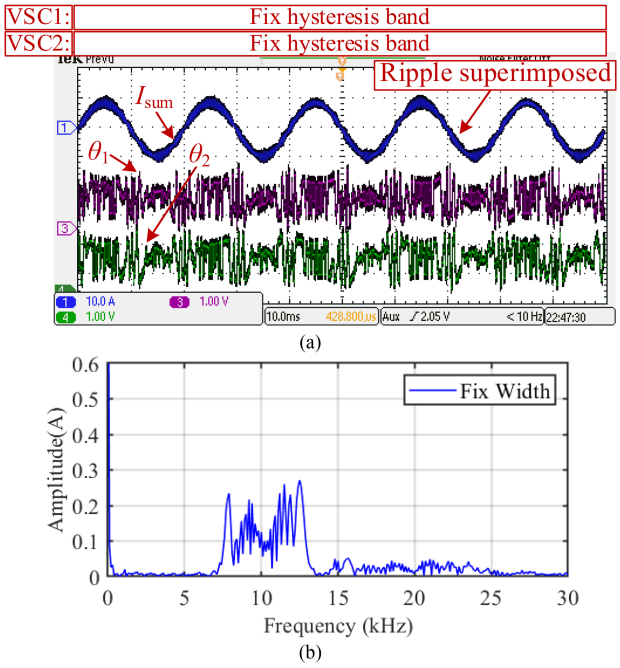

Fig. 18. Two converters fixing the hysteresis band are connected in parallel. (a) Total output ac current $I_{\rm sum}$, phase detection result for converter 1 (θ_1), and for converter 2 (θ_2) (180°/div). (b) Frequency spectrum for $I_{\rm sum}$.

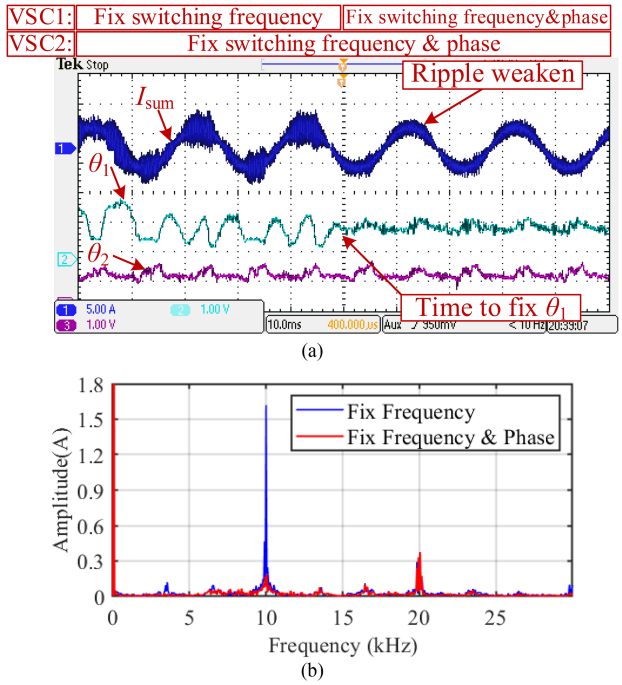

Fig. 19. Total power is 360 W. Two parallel HCC converters with fixed switching frequency are applied with the phase loop and ripple cancellation. (a) Total output ac current $I_{\rm sum}$, phase detection result θ_1 for converter 1 and θ_2 for converter 2 (180°/div). (b) Frequency spectrum for $I_{\rm sum}$ before and after the ripple cancellation.

means of wired connection. The phase shift is configured in the software of the slave converter. If more converters are connected to the parallel system, they can also be set as slaves and obtain the reference signal from converter 1, configuring corresponding phase shift angles, respectively.

Digital variables such as switching frequency f, hysteresis band W, and sidebands of the hysteresis in the experimental waveform are output by the digital analog converter of the DSP and displayed on the oscilloscope.

In Fig. 12, the effect of fixing the frequency is proved by switching the HCC converter from fixing hysteresis band W to applying the frequency loop. The hysteresis band starts to change and the switching frequency is fixed to 10 kHz.

Fig. 13(a) shows the detecting result of switching phase and frequency when the HCC converter undergoes the three stages in sequence: 1) fixing hysteresis band, 2) fixing switching frequency, and 3) fixing switching phase. When the band is fixed, the switching phase changes randomly. When the frequency is fixed, the change rate of the phase detection result is greatly reduced since the switching square wave is basically the same frequency as the reference wave, but the switching phase still changes randomly in the range.

When fixing the phase, the changing frequency reference caused by the phase loop leads to small fluctuations in the waveform of the frequency, but the switching phase is controlled near zero. Fig. 13(b) shows a detailed view of the fixed phase. When the phase is controlled to 0, the falling edge of $S_{\rm r}$ is located at the midpoint of the opening stage of I. This is consistent with the working principle of the phase detector in Fig. 5.

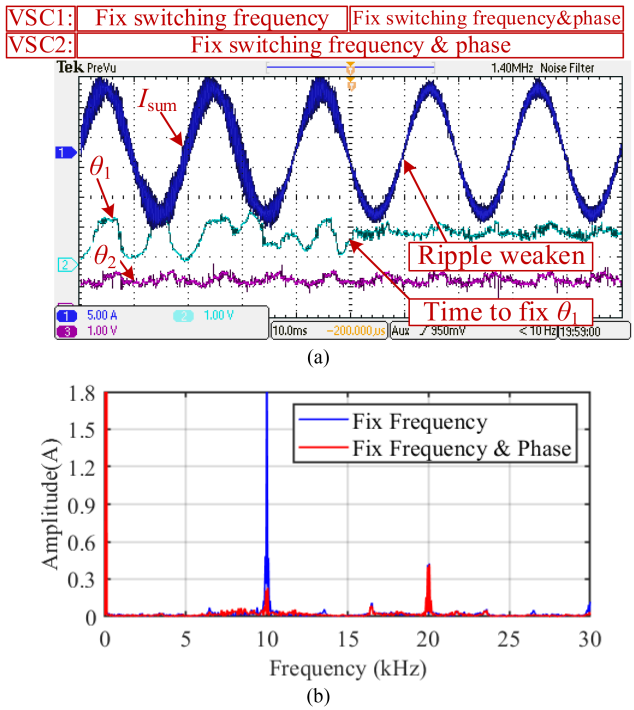

Fig. 20. Total power is 900 W. Two parallel HCC converters with fixed switching frequency are applied with the phase loop and ripple cancellation. (a) Total output ac current $I_{\rm sum}$, phase detection result θ_1 for converter 1 and θ_2 for converter 2 (180°/div). (b) Frequency spectrum for $I_{\rm sum}$ before and after the ripple cancellation.

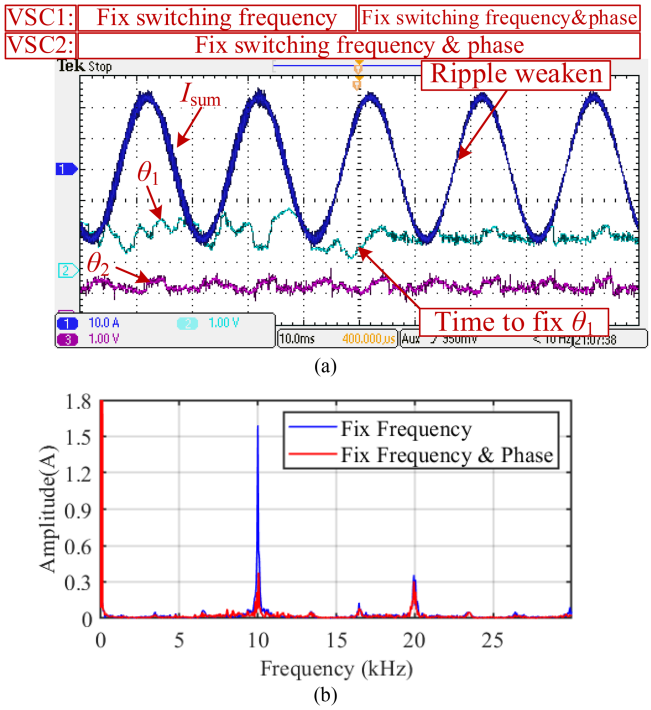

Fig. 21. Total power is 2160 W. Two parallel HCC converters with fixed switching frequency are applied with the phase loop and ripple cancellation. (a) Total output ac current $I_{\rm sum}$, phase detection result θ_1 for converter 1 and θ_2 for converter 2 (180°/div). (b) Frequency spectrum for $I_{\rm sum}$ before and after the ripple cancellation.

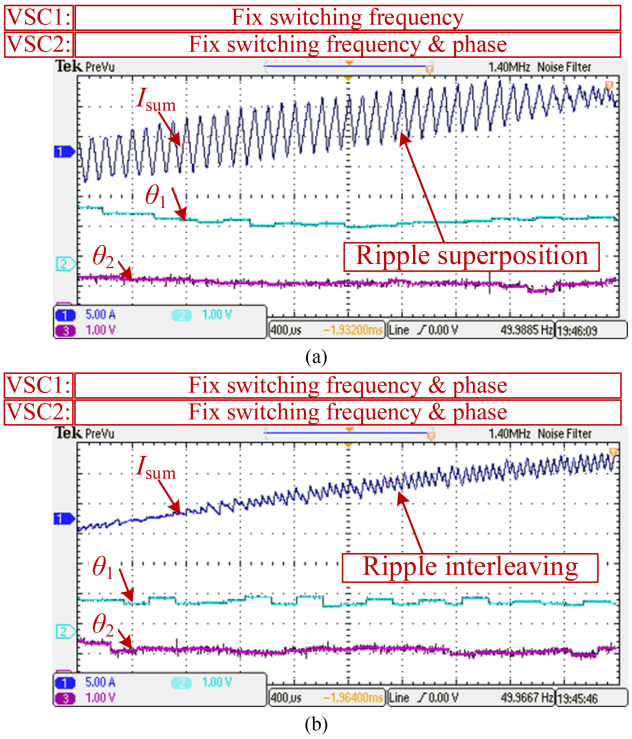

Fig. 22. Details of total ripple for parallel converters. (a) Converter2 fixes the switching frequency and phase and converter1 fixes the switching frequency. (b) Both converters fix the switching frequency and phase. The phase detection result $\theta 1$ is for converter 1 and $\theta 2$ for converter 2 (180°/div).

Figs. 14 and 15 show the sudden change of the current reference $I_{\rm r}$ when the HCC converter operates in the fixing frequency mode, where the feedforward of current reference is added to the compensator A in Fig. 14, but not in Fig. 15. The output current I follows the reference accurately within 2 ms, while for traditional current loop using SPWM, it often takes tens of milliseconds. This verifies the excellent dynamic performance of the HCC converter. In Fig. 15, when removing the feedforward of current reference, there is a short-term large fluctuation in f, indicating that the feed-forward of current reference is necessary under the condition of rapid changes in the output current.

Fig. 16(a) shows the hysteresis comparison process when the HCC converter switches from fixing hysteresis band to open-loop fixing the switching frequency. The open-loop method is to fix the output of the PI controller in Fig. 3 as a given value, and retain the feed-forward of multiple physical quantities to generate a variable loop width. In Fig. 16(b), the control switches from the open-loop control to the frequency closed-loop. It can be proved that the traditional open-loop control has a certain effect on limiting frequency fluctuations, but less effectively than the closed-loop control.

Fig. 17 shows the details when the converter switches from open-loop fixed-frequency control to closed-loop control. The output current is in the same phase as the grid voltage. While the digital delay is basically a constant value, rising slope of the current ripple is the largest near the minimum point of the grid voltage, resulting in the current ripple mostly exceeding the upper hysteresis sideband. Similarly, near the maximum of the grid voltage, the current ripple mostly exceeds the lower hysteresis sideband. It can be seen from the waveform that there is a large drop for f of these two positions under the open-loop control, which also corresponds to the coefficient of the digital delay in (5). But at the moment switched to the closed-loop control, the hysteresis loop width is further adjusted, thereby resisting the influence caused by the digital delay. The sampling delay causes the ripple to exceed the hysteresis band. This phenomenon is inherent and cannot be resisted by adjusting the band width. This will cause an error in the control of the switching frequency, as shown in (12). Fig. 17 shows the resistance effect of the frequency loop on the frequency error caused by sampling delay.

Fig. 18(a) shows the total ac current before the shared filters when two parallel converters are fixing the hysteresis band. The current ripples of the two converters are randomly superimposed and the total ripple changes randomly. Fig. 18(b) shows the switching frequency spectrum of the total current, and the range of the ripple is wide and distributed around 10 kHz. Fig. 19 shows the total current of two HCC converters paralleled before and after applying the ripple cancellation. Before the ripple cancellation, only converter 2 is in the state of fixing switching frequency and phase, while converter 1 is only fixing the frequency. The switching phase of converter 1 changes randomly, resulting in the random superimposition of current ripples. After applying the phase loop to converter 1 and setting the 180° phase shift, the ripples of the two converters can be offset. Fig. 19(b) shows that when the ripple cancellation is applied, the switching content of

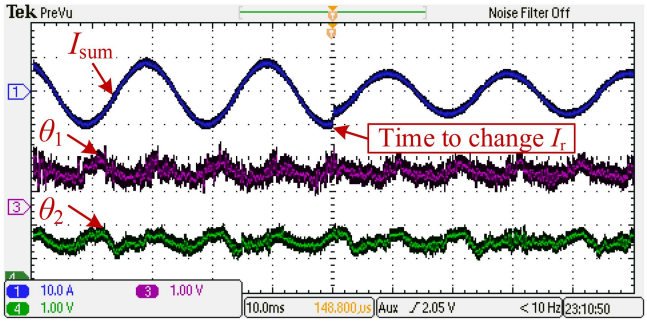

Fig. 23. Two parallel HCC converters applying the ripple cancellation, and output current of converter 1 changes suddenly from 5 A to 3 A. Total output ac current $I_{\rm sum}$, phase detection result for converter 1 (θ_1) and for converter 2 (θ_2) (180°/div).

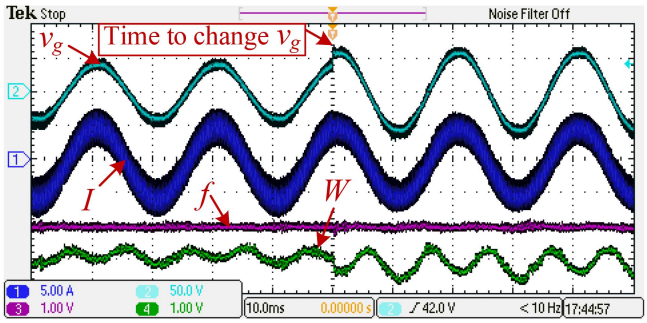

Fig. 24. Peak value of $v_{\rm g}$ changes suddenly from 40 V to 60 V when the HCC converter fixes switching frequency: grid voltage $v_{\rm g}$, output current I, switching frequency f (5 kHz/div), and hysteresis band W (1A/div).

the total ripple is greatly reduced, proving the effectiveness of the phase and frequency loop as well as the ripple cancellation. In order to show the effectiveness of switching phase and frequency control under different power, several experiments were carried out. The experimental powers corresponding to Figs. 19, 20, and 21 are 360 W, 900 W, and 2160 W, respectively.

The details of ripple superposition and interleaving are shown in Fig. 22.

Figs. 14 and 23, respectively, show the ability of the proposed frequency loop and phase loop to resist sudden changes in the output current. Similarly, Figs. 24 and 25, respectively, show the ability of the two loops to adapt to sudden changes in the grid voltage. The above experiments prove the excellent antidisturbance performance of the frequency loop and phase loop proposed in this paper. The essential reason is that these two loops belong to high-frequency additional control by adjusting the hysteresis band, and are independent of the power control of the converter.

V. Conclusion

In this article, a double-loop HCC controller with fixed switching frequency and phase for the grid-tied converters is proposed. By modeling the switching process as well as designing the feed-forward and feedback paths, the switching frequency is precisely fixed. The influences from changing grid

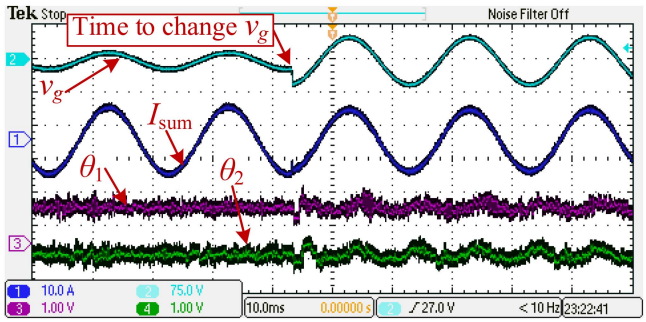

Fig. 25. Peak value of $v_{\rm g}$ changes suddenly from 20 V to 60 V when two parallel HCC converters apply the ripple cancellation: grid voltage $v_{\rm g}$, total output ac current $I_{\rm sum}$, phase detection result for converter 1 (θ_1), and for converter 2 (θ_2) (180°/div).

conditions and digital delay are offset. Additionally, the phase detector and the phase loop are designed, supporting phase shifting and ripples cancellation for parallel HCC converters. Using the controller, HCC converters almost obtain switching characteristics consistent with PWM, and interleaving of parallel HCC converters is realized. The effect has been tested through experiments. Fixed switching frequency and cancellation of the ripple improve the switching performance and save the filtering costs of HCC converters. This broadens the applications and power levels of HCC converters.

Appendix

The error and noise in voltage sampling will affect the fixing effect of the switching frequency through compensator A. Assume that the difference between the actual grid voltage and the sampled value $v_{\rm g}$ obtained in the digital controller is Δ_1, which is the sum of the sampling error and noise. For the dc voltage $v_{\rm dc}$, the error is assumed to be Δ_2. In a switching cycle, the variation of the grid voltage is $\Delta v_{\rm gTs}$, and the error from sampling is assumed to be Δ_3. In the worst case, $\Delta_3 \le 2\Delta_1$.

The error of correction values of the dc voltage $v_{\rm dc}^*$ and the grid voltage $v_{\rm g}^*$ can be obtained by recalculating (7) with the assumed sampling errors. They are shown in (A2) and (A4)

$$v_{\rm dc}^* + \Delta v_{\rm dc}^* = v_{\rm dc} + \Delta_2 + \frac{\Delta v_{\rm gTs} + \Delta_3}{2} = v_{\rm dc} + \frac{\Delta v_{\rm gTs}}{2} + \Delta_2 + \frac{\Delta_3}{2} \tag{A1}$$

$$\Rightarrow \Delta v_{\rm dc}^* = \Delta_2 + \frac{\Delta_3}{2} \tag{A2}$$

$$v_{\rm g}^* + \Delta v_{\rm g}^* = v_{\rm g} + \Delta_1 + L\frac{{\rm d}i_{\rm r}}{{\rm d}t} - \frac{1}{2}L\frac{{\rm d}W}{{\rm d}t} - \frac{v_{\rm g} + \Delta_1}{2(v_{\rm dc} + \Delta_2)}(\Delta v_{\rm gTs} + \Delta_3) = v_{\rm g} + L\frac{{\rm d}i_{\rm r}}{{\rm d}t} - \frac{1}{2}L\frac{{\rm d}W}{{\rm d}t} - \frac{v_{\rm g}}{2v_{\rm dc}}\Delta v_{\rm gTs}$$

$$+\Delta_1+\frac{v_{\mathrm{g}}\Delta v_{\mathrm{g}Ts}}{2v_{\mathrm{dc}}^2}\Delta_2-\frac{v_{\mathrm{g}}}{2v_{\mathrm{dc}}}\Delta_3-\frac{\Delta v_{\mathrm{g}Ts}}{2v_{\mathrm{dc}}}\Delta_1 \tag{A3}$$

$$\Rightarrow \Delta v_{\mathrm{g}}^*=\Delta_1-\frac{\Delta v_{\mathrm{g}Ts}}{2v_{\mathrm{dc}}}\Delta_1+\frac{v_{\mathrm{g}}\Delta v_{\mathrm{g}Ts}}{2v_{\mathrm{dc}}^2}\Delta_2-\frac{v_{\mathrm{g}}}{2v_{\mathrm{dc}}}\Delta_3. \tag{A4}$$

Similarly, with Δv_{dc}^* and Δv_{g}^*, (13) in the paper can be rederived as (A5). The method of calculating the derivative is used, and error of the compensator A is obtained and shown in (A6)

$$\begin{aligned}\mathrm{A}+\Delta\mathrm{A}&=\frac{\left(\frac{v_{\mathrm{dc}}^*+\Delta v_{\mathrm{dc}}^*}{2}\right)^2-\left(v_{\mathrm{g}}^*+\Delta v_{\mathrm{g}}^*\right)^2}{v_{\mathrm{dc}}^*+\Delta v_{\mathrm{dc}}^*}\\&=\frac{\left(\frac{v_{\mathrm{dc}}^*}{2}\right)^2+\frac{v_{\mathrm{dc}}^*}{2}\Delta v_{\mathrm{dc}}^*-\left(v_{\mathrm{g}}^*\right)^2-2v_{\mathrm{g}}^*\Delta v_{\mathrm{g}}^*}{v_{\mathrm{dc}}^*+\Delta v_{\mathrm{dc}}^*}\\&=\frac{\left(\frac{v_{\mathrm{dc}}^*}{2}\right)^2-\left(v_{\mathrm{g}}^*\right)^2}{v_{\mathrm{dc}}^*}-\frac{\left(\frac{v_{\mathrm{dc}}^*}{2}\right)^2-\left(v_{\mathrm{g}}^*\right)^2}{\left(v_{\mathrm{dc}}^*\right)^2}\Delta v_{\mathrm{dc}}^*\\&\quad+\frac{1}{2}\Delta v_{\mathrm{dc}}^*-2\frac{v_{\mathrm{g}}^*}{v_{\mathrm{dc}}^*}\Delta v_{\mathrm{g}}^*\end{aligned} \tag{A5}$$

$$\Rightarrow \Delta\mathrm{A}=\left[\frac{1}{4}+\left(\frac{v_{\mathrm{g}}^*}{v_{\mathrm{dc}}^*}\right)^2\right]\Delta v_{\mathrm{dc}}^*-2\frac{v_{\mathrm{g}}^*}{v_{\mathrm{dc}}^*}\Delta v_{\mathrm{g}}^*. \tag{A6}$$

Setting the output of the PI controller in Fig. 3 as $\mathrm{PI_{out}}$, the relationship between $\mathrm{PI_{out}}$ and switching frequency f can be obtained

$$\mathrm{PI_{out}}\cdot\mathrm{A}\cdot\frac{L}{\mathrm{A}}=\frac{1}{f}. \tag{A7}$$

Considering the sampling error ΔA in the feedforward compensator A, (A8) can be obtained

$$\mathrm{PI_{out}}(\mathrm{A}+\Delta\mathrm{A})\cdot\frac{L}{\mathrm{A}}=\frac{1}{f+\Delta f}. \tag{A8}$$

Combining (A7) and (A8), switching frequency error Δf caused by sampling errors and noises can be obtained

$$\Delta f=-f^2\cdot\mathrm{PI_{out}}\cdot\Delta\mathrm{A}\cdot\frac{L}{\mathrm{A}}=-f\cdot\frac{\Delta\mathrm{A}}{\mathrm{A}} \tag{A9}$$

$$\Rightarrow \frac{\Delta f}{f}==-\frac{\Delta\mathrm{A}}{\mathrm{A}}. \tag{A10}$$

It is worth noting that $\mathrm{PI_{out}}$ is regarded as a fixed number in the above calculation. However, due to the existence of frequency closed-loop, the value of $\mathrm{PI_{out}}$ will be feedbackly adjusted. Thus, the influence from ΔA on switching frequency will be reduced. To show the worst-case, the feedback regulation is ignored, so $\mathrm{PI_{out}}$ is regarded as invariant.

According to the experimental parameters in Table I, the potential influence from voltage sampling error and noise on switching frequency can be evaluated numerically. In this process, the proportion of voltage sampling deviation (errors add noises) is set to 5%. It is important to note that this value significantly exceeds the voltage sampling error and noise in real experimental system

$$\begin{cases}\Delta_1\le v_{\mathrm{g}}\cdot 5\%=3\mathrm{V}\\ \Delta_2\le v_{\mathrm{dc}}\cdot 5\%=10\mathrm{V}\\ \Delta_3\le\Delta_1\cdot 2=6\mathrm{V}\end{cases} \tag{A11}$$

$$\Rightarrow\begin{cases}\Delta {v_{\mathrm{dc}}}^*\le 13\mathrm{V}\\ \Delta {v_{\mathrm{g}}}^*\le 3.8977\mathrm{V}\end{cases} \tag{A12}$$

$$\Rightarrow \Delta\mathrm{A}\le 1.5903\mathrm{V}. \tag{A13}$$

Using (13), A$\ge$32 V can be obtained. Therefore, the frequency error can be obtained

$$\Delta f/f\le 4.72\%. \tag{A14}$$

The 4.72% error of frequency is convergent compared to the 5% sampling deviation. On the one hand, the actual voltage sampling deviation is much smaller than 5%. On the other hand, this error in the frequency loop can be accepted. Therefore, the sampling deviation has small influence on the switching frequency in the proposed method.

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