Fast Dynamic Control of Dual-Active-Bridge DC–DC Converter Based on an Adaptive Linear Extended State Observer

Hao Yin, Lingling Cao, Xianhao Zeng, K. H. Loo, and Chuan Sun

***Abstract*—Linear extended state observer (LESO) plays a critical role in ADRC's control performance. However, there exists a tradeoff between disturbance rejection and noise immunity for traditional linear ESO (TLESO). Compared to TLESO with similar bandwidth, phase-locking loop observer (PLLO) exhibits a better output tracking performance but weaker noise suppression capability. By combining the advantages of TLESO and PLLO, an adaptive LESO (ALESO) is proposed in this article, which utilizes TLESO in steady state and PLLO during transient state. The dynamic and noise-suppression performances of different observers are analyzed and compared systematically. The proposed ALESO inherits good dynamic response of PLLO and noise-suppression performance of TLESO, without using high bandwidth. It also possesses the advantages of simple structure, requiring few tuning parameters and ease of parameter tuning. To verify the feasibility and effectiveness of the proposed ALESO design, it is employed to a 500 W dual-active-bridge dc–dc converter for pulsed power applications. Experiments results show that, in comparison with TLESO, the proposed ALESO has resulted in 33.3%/37% and 60%/73.3% reductions in output voltage undershoot/overshoot and setting time, respectively, under load step-up/down. For steady-state performance, a noise level reduction of 76.3% is achieved compared to that resulting from PLLO.**

***Index Terms*—Adaptive linear extended state observer (ALESO), dual active bridge (DAB) dc–dc converter, phase-locking loop observer (PLLO), traditional linear extended state observer (TLESO).**

I. Introduction

THE power supply design for power pulsed loads (PPLs), such as active phased array radar transmitters, faces great challenges. Precise regulation of the output voltage is required, and the output voltage drop during the pulse period (1%–20%) must be small enough to ensure a good moving target indicator performance of the radar [1]. Typically, very large storage capacitors are connected at the output terminal. Bidirectional converters [2], [3], [4], [5], [6] are suggested to be paralleled to reduce the storage capacitance and increase the system power density. To ensure a small voltage drop and a well-regulated output voltage during the pulse cycle, the bidirectional converter must demonstrate a fast dynamic response in load power tracking and a good ability to suppress noise interference. Traditional proportional-integral (PI) controller in a single voltage loop cannot meet the requirements of fast response and good tracking accuracy over a wide range of operating conditions [7]. Dual loop control adds an inner current loop to improve system dynamic response [2]. A current reference feedforward control scheme is applied in a Buck/Boost converter to improve the current tracking ability [3], [4]. A systematic derivation of output impedance shaping methods is presented for a fuel-cell-battery-powered single-phase inverter system [5]. A comprehensive review of the active power decoupling control strategies is presented in [6]. A predictive current-mode controller is proposed in [8] by sampling the high-frequency transformer current and calculating a required control signal to track the current reference in one cycle, however, the prediction algorithm is dependent on the accuracy of the measured transformer's leakage inductance. The sliding mode control in [9] enables an efficient and fast tracking of the output voltage due to its insensitivity to parameter uncertainties and disturbances, but the inherent chattering phenomenon may deteriorate the system performance [10].

Active disturbance rejection control (ADRC) [11] has caught the attention of the industry because it is independent of model and has the advantage of high robustness and fast dynamic response. ADRC has been successfully applied in motion control [12], full-bridge dc–dc converter [13], etc. ADRC is also used in dual active bridge (DAB) converter to improve dynamic response [14], [15], [16], and it has been shown that the output impedance of DAB converter is significantly reduced and its performance is insensitive to system's parameter changes.

The extended or linear extended state observer (ESO / LESO) [17], which is used to estimate the total disturbances and uncertainties, plays a critical role in ADRC's control performance. The tracking performance can be improved by a higher bandwidth of LESO, but the output might be degraded by the

Received 6 March 2024; revised 14 June 2024 and 13 August 2024; accepted 22 August 2024. Date of publication 3 September 2024; date of current version 7 October 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 52007040 and in part by Key Laboratory of Reliability and Quality Consistency of Electronic Components, Ministry of Education (Harbin Institute of Technology). Recommended for publication by Associate Editor E. Babaei. *(Corresponding author: Lingling Cao.)*

Hao Yin, Lingling Cao, and Xianhao Zeng are with the School of Mechanical Engineering and Automation, Harbin Institute of Technology, Shenzhen 518000, China (e-mail: 21S153253@stu.hit.edu.cn; caolingling@hit.edu.cn; 23S153170@stu.hit.edu.cn).

K. H. Loo is with the Department of Electrical and Electronic Engineering, The Hong Kong Polytechnic University, Hong Kong, China (e-mail: kh.loo@polyu.edu.hk).

Chuan Sun is with the Department of Engineering Science and Faculty of Innovation Engineering, Macau University of Science and Technology, Macau 999078, China (e-mail: csun@must.edu.mo).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3454209.

Digital Object Identifier 10.1109/TPEL.2024.3454209

high-frequency measurement noises in the control loop. In addition, a higher observer bandwidth tends to lead to numerical problems in practical implementations. The reason is that the observer gain is proportional to the $(n+1)$ th power of its bandwidth, where n is the order of the system [18]. To resolve the tradeoff between the estimation speed/accuracy and noise suppression of the traditional LESO, different optimized observer designs have been proposed recently, which can be categorized into two groups: multiple-observer-based and single-observer-based.

In [19], [20], and [21], multiple observers are parallel or cascaded connected. The parallel multiple ESOs of different orders or different bandwidths are automatically selected with the objective of minimizing tracking error, which are applied in the high-speed precision motion stage [19]. In [20] and [21], the cascaded structure of LESO is less affected by noise due to the filtering effect of the front-end LESO. However, multiple observers are often coupled and parameters tuning is difficult.

For single-observer-based designs, the research work focuses on parametric optimization or structural optimization. Artificial neural network is used in [22] to determine the optimal observer gain and feedback control gain for the ADRC controller, so that the output voltage can be regulated quickly and accurately under all working conditions. However, a large amount of training data and training time is needed. In [23], based on the duty cycle signal, the system control gain is adapted in real-time to deal with the switch fault uncertainty. Further, the system gain is adaptively optimized by introducing an additional regulation law so that time-varying disturbances can be estimated accurately [24]. Instead of adjusting the control gain, the closed-loop bandwidth and the observer's bandwidth are adaptively adjusted based on the position error and observation error, respectively [25]. A high-order ESO is used to enhance the antidisturbance ability, but the noise immunity is weakened [26]. The adaptive-switching four-order LESO proposed in [27] can realize a mode switching between traditional observer gain (during steady state) and optimized observer gain (during transient state), which can simultaneously suppress the steady-state noise and achieve fast dynamic response. Unfortunately, the increase of order results in more serious numerical problems and demands higher storage and arithmetic capability from the digital signal processor. An extended state differential is creatively incorporated into the conventional LESO to remove the poles on the imaginary axis [28], which presents a better disturbance performance; nevertheless, the measurement noise is not addressed. In [29], without increasing the complexity of the LESO algorithm, an ADRC controller using phase-locking loop observer (PLLO) is proposed, which demonstrates a better tracking performance than traditional LESO (TLESO). However, the PLLO is more susceptible to system noises; besides, the influences of bandwidth on the performances of TLESO and PLLO are not discussed in detail.

In this article, the advantages of noise suppression offered by TLESO and the anti-interference ability of PLLO are integrated into an adaptive mechanism. The quantitative relationship between the bandwidths of TLESO and PLLO is discussed, which facilitates the parameter tuning of adaptive LESO (ALESO). It is found that the proposed ALESO can achieve good dynamic response and noise suppression without requiring a high bandwidth. To demonstrate the superiorities of the proposed method, it is applied to a DAB converter, which is widely used for interfacing the PLLs [30], [31].

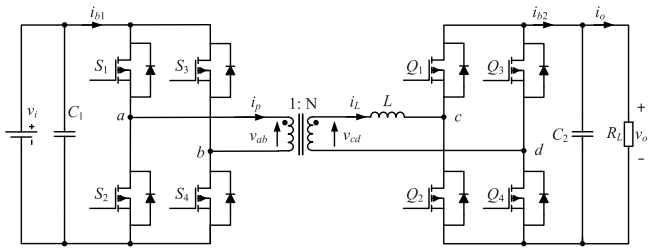

Fig. 1. Topology of DAB converter.

The main contributions of this article can be summarized as follows.

1) It is revealed that with the same observer's bandwidth, TLESO has better noise suppression performance while PLLO has better disturbance rejection performance.
2) By incorporating both the merits of TLESO and PLLO, an ALESO is proposed, which utilizes TLESO in steady state and PLLO during transient state. The proposed ALESO inherits the advantages of both observer designs, and balances the trade-off between disturbance rejection and noise immunity, without increasing the observer's bandwidth.
3) The detailed parameter tuning of ALESO is provided and the ALESO-based ADRC control is successfully applied to a 500 W DAB converter.

The rest of this article is organized as follows. Section II derives a reduced-order model of DAB converter and introduces the controller structures of TLESO and PLLO. Section III introduces the proposed ALESO's control structure and provides guidelines for its parameter design. Section IV verifies the proposed control method by implementing it on a DAB converter's experimental hardware prototype. Finally, Section V concludes this article.

II. Traditional ADRC Controller Design

A. Reduced-Order Model of DAB Converter

Fig. 1 shows the topological structure of a DAB converter. Single-phase-shift (SPS) modulation is the simplest and most widely used modulation scheme for DAB converter, and it is adopted in this article. SPS modulation utilizes only one phase-shift ratio d between the primary and secondary bridges for power control, where power flows from the side with a leading phase to the side with a lagging phase. The steady-state output power P_o of an SPS-modulated DAB converter is given as

$$P_o = \frac{N v_i v_o d(1-d)}{2 f_s L} \tag{1}$$

where $N = N_s/N_p$ is transformer's turn ratio, v_i is the input voltage, v_o is the output voltage, f_s is the switching frequency, and L is the energy transfer inductance.

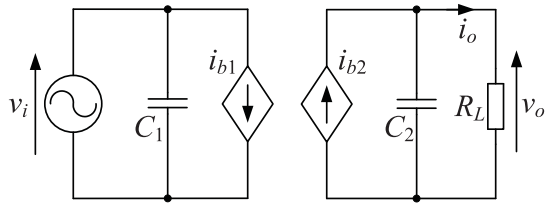

Fig. 2. Reduced-order model of DAB converter.

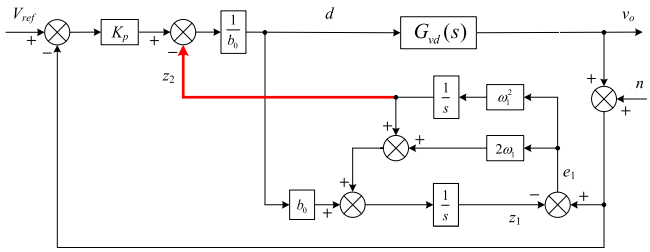

Fig. 3. Block diagram of the TLESO for DAB converter.

A reduced-order model of DAB converter is depicted in Fig. 2. Recognizing that the output power can be expressed as $P_o = v_o\langle i_{b2}\rangle$, the average output current of the secondary H-bridge can be derived as

$$\langle i_{b2}\rangle = \frac{Nv_i d(1-d)}{2f_s L}. \tag{2}$$

By introducing small-signal perturbations to (2), the small-signal transfer function from $\tilde{d}$ to $\tilde{v}_o$ can be obtained as

$$G_{vd}(s) = \frac{\tilde{v}_o}{\tilde{d}} = \frac{NV_i(1-2D)}{2f_s L}\frac{R_L}{R_L C_2 s + 1} \tag{3}$$

where V_i and D are the steady-state values of v_i and d, and $\tilde{d}$ and $\tilde{v}_o$ are the small-signal variations of d and v_o. In the following sections, two ADRC designs based on TLESO and PLLO are discussed, and their relative merits and drawbacks are compared.

B. Controller Design Based on TLESO

In this section, an ADRC based on TLESO is designed, as shown in Fig. 3. Referring to Fig. 2 and using (3), the differential equation describing the dynamics of a DAB converter's output voltage is given by

$$\frac{d\tilde{v}_o}{dt} = -\frac{\tilde{v}_o}{R_L C_2} + \frac{NV_i(1-2D)}{2f_s LC_2}\tilde{d}. \tag{4}$$

Let $x_1 = v_o$, $x_2 = f$, (4) can be written in the matrix form as

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}0 & 1\\ 0 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}b_0\\ 0\end{bmatrix}d + \begin{bmatrix}0\\ 1\end{bmatrix}\dot{f} \tag{5}$$

$$f = a\tilde{v}_o + (b - b_0)\tilde{d} \tag{6}$$

where f represents the lumped disturbance comprising the external disturbances, unknown modeling uncertainties, circuit parameter variations, etc., [17], with

$$a = -\frac{1}{R_L C_2} \tag{7}$$

$$b = \frac{NV_i(1-2D)}{2f_s LC_2} \tag{8}$$

$$b_0 = \frac{NV_{i0}(1-2D_0)}{2f_s L_0 C_{20}} \tag{9}$$

where V_{i0}, L_0, and C_{20} are the nominal values of the input voltage, energy transfer inductance, and output capacitance, respectively.

Typically, TLESO can be designed using

$$\frac{dz_1}{dt} = z_2 + \beta_1(v_o - z_1) + b_0 d \tag{10}$$

$$\frac{dz_2}{dt} = \beta_2(v_o - z_1) \tag{11}$$

where z_1 and z_2 represent the estimated values of v_o and f, respectively. Equations (10) and (11) can be written in the matrix form as

$$\begin{bmatrix}\dot{z}_1\\ \dot{z}_2\end{bmatrix} = \begin{bmatrix}-\beta_1 & 1\\ -\beta_2 & 0\end{bmatrix}\begin{bmatrix}z_1\\ z_2\end{bmatrix} + \begin{bmatrix}b_0 & \beta_1\\ 0 & \beta_2\end{bmatrix}\begin{bmatrix}d\\ v_o\end{bmatrix}. \tag{12}$$

Defining the estimation errors e_1 and e_2 as $e_1 = v_o - z_1$ and $e_2 = f - z_2$, these errors can be written in the matrix form as

$$\begin{bmatrix}\dot{e}_1\\ \dot{e}_2\end{bmatrix} = A_{e1}\begin{bmatrix}e_1\\ e_2\end{bmatrix} + \begin{bmatrix}0\\ \dot{f}\end{bmatrix} \tag{13}$$

where $A_{e1} = \begin{bmatrix}-\beta_1 & 1\\ -\beta_2 & 0\end{bmatrix}$. It should be noted that if β_1 and β_2 are strictly positive, the roots of the characteristic polynomial of A_{e1} are found to exist in the left-half region of the s-plane, thus A_{e1} is Hurwitz stable.

For simplicity, the bandwidth parameterization method proposed by Gao [17] is used with the following parameter definitions: $\beta_1 = 2\omega_1$ and $\beta_2 = {\omega_1}^2$ are chosen such that the two poles of the observer are located at $-\omega_1$, with ω_1 being the observer's bandwidth.

According to (5) and (12), the transfer function from the lumped disturbance f to the estimated value Z_2 can be obtained as

$$M_1(s) = \frac{z_2(s)}{f(s)} = \frac{\omega_1^2}{s^2 + 2\omega_1 s + \omega_1^2}. \tag{14}$$

Further, the transfer function of the estimation error of the lumped disturbance can be obtained from (14) as

$$E_1(s) = 1 - M_1(s) = \frac{s^2 + 2\omega_1 s}{s^2 + 2\omega_1 s + \omega_1^2}. \tag{15}$$

From the control block diagram of Fig. 3, the phase-shift ratio d required for compensating all disturbances is given as

$$d = \frac{K_p(V_{\text{ref}} - v_o) - z_2}{b_0}. \tag{16}$$

Finally, when the controller can accurately estimate and compensate for all disturbances, it can be shown that the system

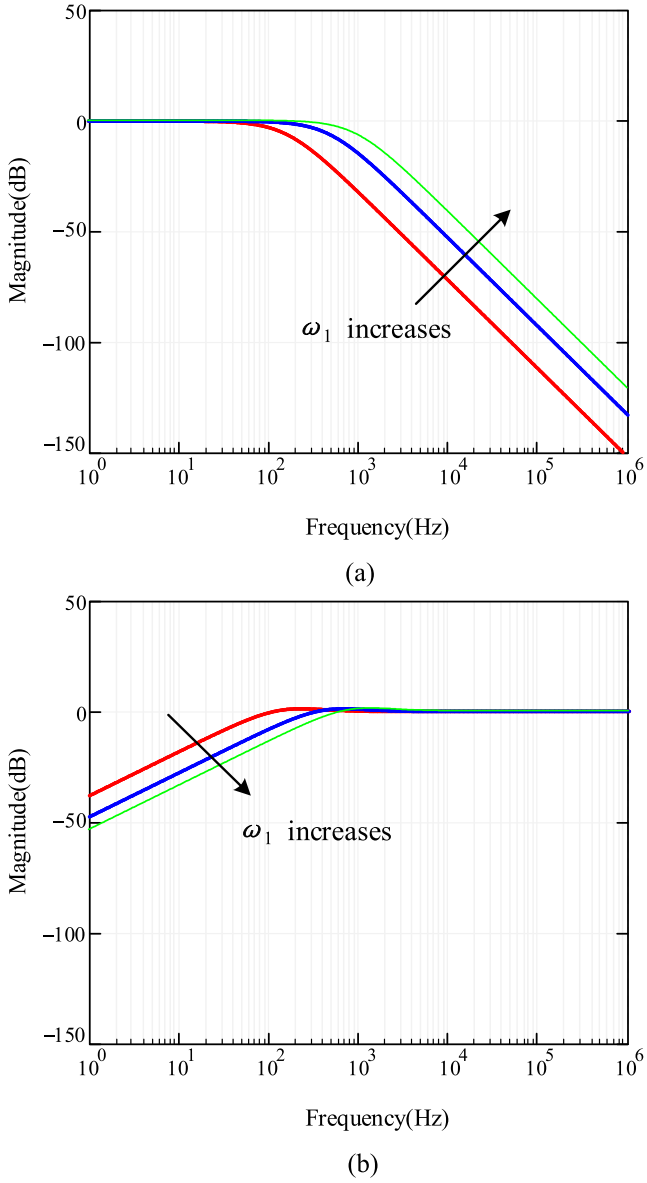

Fig. 4. Bode diagram of $M_1(s)$ and $E_1(s)$. (a) $M_1(s)$ with different bandwidths. (b) $E_1(s)$ with different bandwidths.

under control resembles a pure integrator, and its closed-loop transfer function can be approximated as

$$\Phi(s) \approx \frac{K_p/s}{1+K_p/s} = \frac{K_p}{s+K_p} \tag{17}$$

where $K_p = \omega_c$ represents the 3-dB frequency.

Fig. 4 shows the frequency characteristics of $M_1(s)$ and $E_1(s)$ with different observer's bandwidths. Typically, disturbances occur in the low frequency band, while the noise occurs in the high frequency band. Thus, it can be seen that with the increase of observer's bandwidth, the disturbance rejection performance of TLESO becomes better, but its noise suppression performance deteriorates. This implies that there exists a tradeoff between the disturbance rejection and noise suppression performance of TLESO.

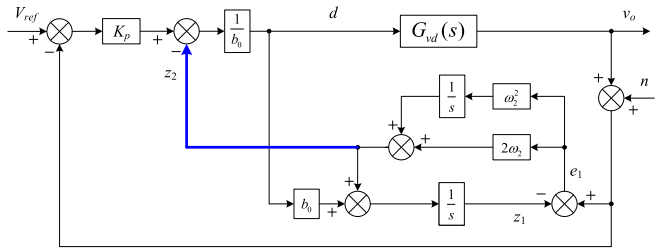

Fig. 5. Block diagram of the PLLO for DAB converter.

C. Controller Design Based on PLLO

To improve the disturbance tracking capability of TLESO, a PLLO-based ADRC controller is proposed in [29] without increased algorithm complexity. Fig. 5 shows the block diagram of a PLLO for DAB converter, which can be designed using as

$$\frac{dz_1}{dt} = z_2 + b_0 d \tag{18}$$

$$\frac{dz_2}{dt} = \beta_2(v_o - z_1) + \beta_1 \frac{d(v_o - z_1)}{dt}. \tag{19}$$

By comparing the structure of TLESO and PLLO in Figs. 3 and 5, the main difference is that the estimated disturbance z_2 of TLESO is the integral of the output voltage estimation error e_1, whereas the estimated disturbance z_2 of PLLO is the proportional-integral of e_1. Rewriting (18) and (19) in matrix form yields

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\beta_2 & -\beta_1 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \end{bmatrix} + \begin{bmatrix} b_0 & 0 & 0 \\ -\beta_1 b_0 & \beta_2 & \beta_1 \end{bmatrix} \begin{bmatrix} d \\ v_o \\ \dot{v}_o \end{bmatrix}. \tag{20}$$

According to the definitions of observation errors e_1 and e_2, the following equation can be obtained:

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \end{bmatrix} = A_{e2} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \dot{f} \end{bmatrix} \tag{21}$$

where $A_{e2} = \begin{bmatrix} 0 & 1 \\ -\beta_2 & -\beta_1 \end{bmatrix}$. Since the characteristic polynomials of A_{e2} and A_{e1} have the same roots, they have the same stability property, so β_1 and β_2 need to be strictly positive. By selecting $\beta_1 = 2\omega_2$ and $\beta_2 = {\omega_2}^2$, the transfer function from the disturbance f to estimated disturbance z_2 can be obtained as

$$M_2(s) = \frac{z_2(s)}{f(s)} = \frac{2\omega_2 s + \omega_2^2}{s^2 + 2\omega_2 s + \omega_2^2} \tag{22}$$

from which the disturbance estimation error can be obtained as

$$E_2(s) = 1 - M_2(s) = \frac{s^2}{s^2 + 2\omega_2 s + \omega_2^2}. \tag{23}$$

Fig. 6 depicts the bode plots of $M_2(s)$ and $E_2(s)$ with different observer's bandwidths. It can be seen that, with the increase of observer's bandwidth, the disturbance rejection performance of PLLO improves while its noise suppression performance becomes poorer, which is similar to the characteristics of TLESO.

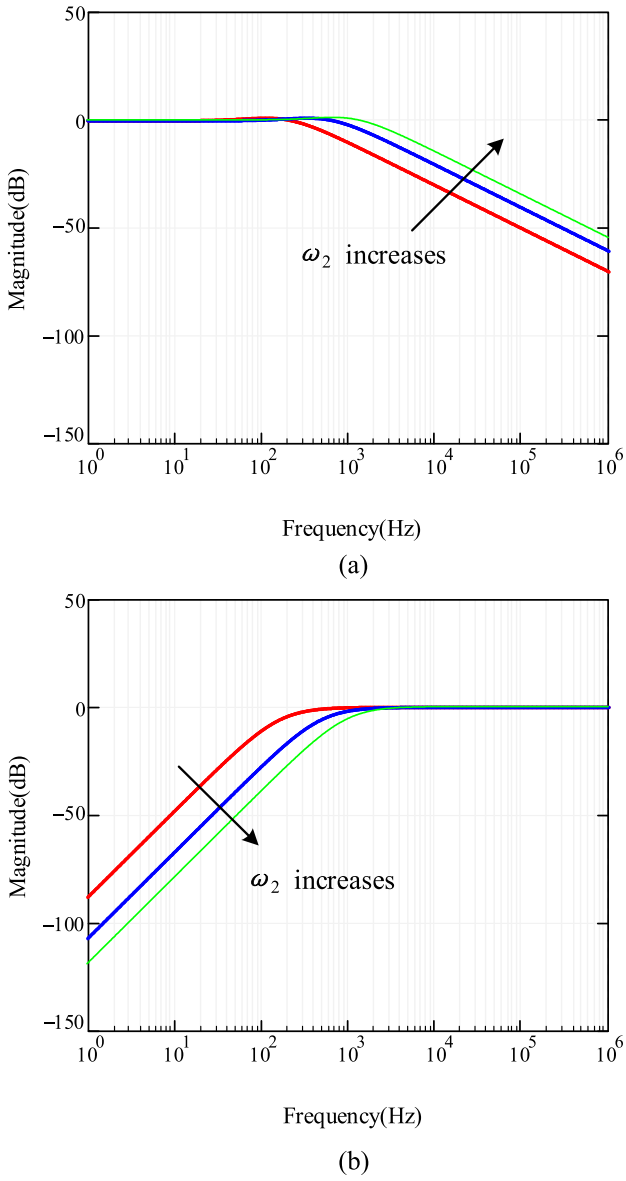

Fig. 6. Bode diagram of $M_2(s)$ and $E_2(s)$. (a) $M_2(s)$ with different bandwidths. (b) $E_2(s)$ with different bandwidths.

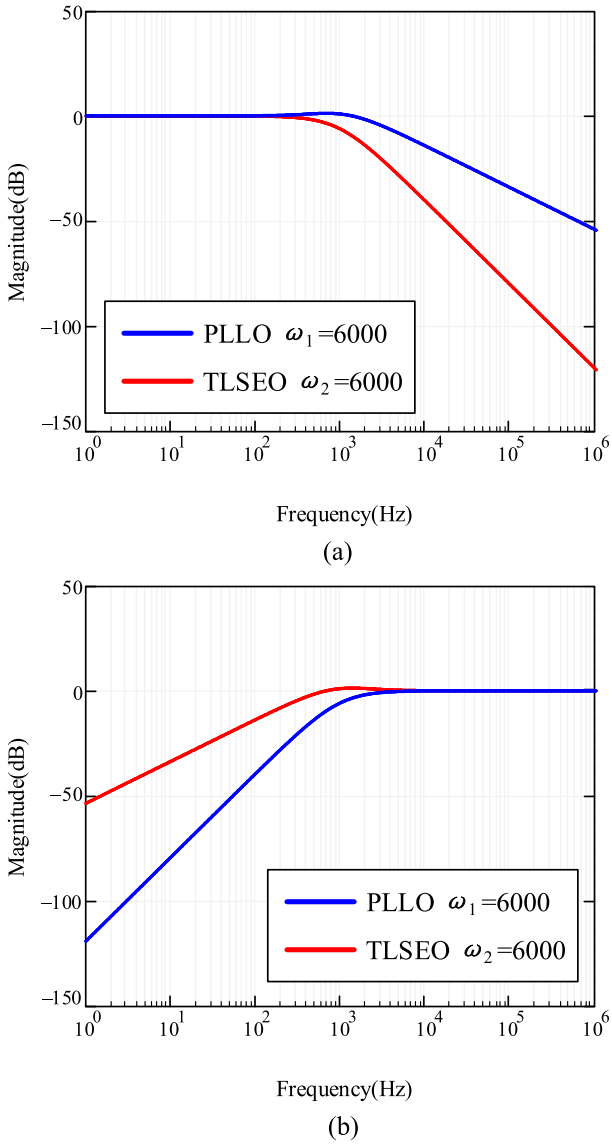

Fig. 7. Comparison between TLESO and PLLO. (a) $M_1(s)$ and $M_2(s)$ when $\omega_1 = \omega_2 = 6000$ rad/s. (b) $E_1(s)$ and $E_2(s)$ when $\omega_1 = \omega_2 = 6000$ rad/s.

Thus, similar to TLESO, there is a tradeoff between the disturbance rejection performance and noise immunity for both PLLO and TLESO.

The bode plots of M(s) and E(s) with TLSEO and PLLO are compared in Fig. 7. Obviously, with the same observer's bandwidth, PLLO exhibits a stronger anti-interference ability, but is more sensitive to measurement noise. Therefore, it is proposed that the combined use of TLESO and PLLO will inherit the advantages of both observer designs and balance the tradeoff between disturbance rejection performance and noise immunity.

III. Principle and Design of Adaptive LESO

To deal with the problems mentioned in Section II, an ALESO, which utilizes TLESO in steady state and PLLO during transient state, is proposed in this section. The block diagram of the proposed ALESO is depicted in Fig. 8, where a switch S is adaptively toggled to select between TLESO or PLLO, and ω_0 is defined as the observer bandwidth of ALESO.

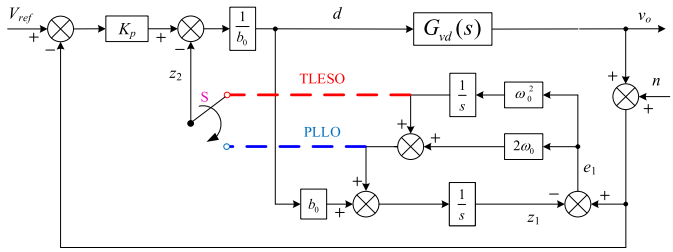

Fig. 8. Block diagram of the ALESO for DAB converter.

A. Relationship Between the Observer Bandwidth of TLESO and PLLO

For PLLO and TLESO, observer bandwidth is the most important design parameter. However, even with exactly the same observer bandwidth, the characteristics of both observers are different. To establish the basis for designing ALESO, this section discusses the quantitative relationship between TLESO and PLLO based on their properties depicted in Fig. 7.

When considering the influence of measurement noise, the transfer function of TLESO disturbance and noise to output voltage can be obtained as

$$G_{f1}(s) = \frac{v_o(s)}{f(s)} = \frac{E_1(s)}{s + K_p} \tag{24}$$

$$G_{n1}(s) = \frac{v_o(s)}{n(s)} = -\frac{K_p + sM_1(s)}{s + K_p}. \tag{25}$$

Similarly, the transfer function of PLLO disturbance and noise to output voltage can be obtained as

$$G_{f2}(s) = \frac{v_o(s)}{f(s)} = \frac{E_2(s)}{s + K_p} \tag{26}$$

$$G_{n2}(s) = \frac{v_o(s)}{n(s)} = -\frac{K_p + sM_2(s)}{s + K_p}. \tag{27}$$

To determine a suitable relationship between ω_1 and ω_2, both frequencies are expressed as functions of ω_0

$$\begin{cases} \omega_1 = k\omega_0 \\ \omega_2 = \omega_0 \end{cases}. \tag{28}$$

According to Fig. 7, PLLO performs better than TLESO in terms of disturbance rejection ability when the following conditions are met as:

$$20\log_{10}|G_{f1}(j\omega)| > 20\log_{10}|G_{f2}(j\omega)|. \tag{29}$$

By substituting (24) and (26), (29) can be simplified to

$$|E_1(j\omega)| > |E_2(j\omega)|. \tag{30}$$

Then, substitute (15) and (23) into (30), and let $p = \omega_0 / \omega$, we have

$$k^4 - 2\left(\frac{1}{p^2} + 2p^2 + 4\right)k^2 - \left(\frac{2}{p^2} + 1\right) < 0. \tag{31}$$

As both ω_0 and ω are positive numbers, the condition $p > 0$ holds true, which leads to

$$k < \sqrt{\frac{1}{p^2} + 2p^2 + 4 + \sqrt{\left(\frac{1}{p^2} + 2p^2 + 4\right)^2 + \frac{2}{p^2} + 1}}. \tag{32}$$

The minimum value of the right side of the inequality (32) is derived as k_1 when p approaches 0.8

$$k_1 \approx 3.7. \tag{33}$$

That is, when $k < k_1$ is satisfied, the inequality (32) and thus (29) can always be true. In other words, if the observer bandwidth of TLESO is not k_1 times larger than the observer bandwidth of PLLO, PLLO has better disturbance rejection performance. The boundary case when $\omega_1 = 3.7\omega_2$ is given in Fig. 9(a).

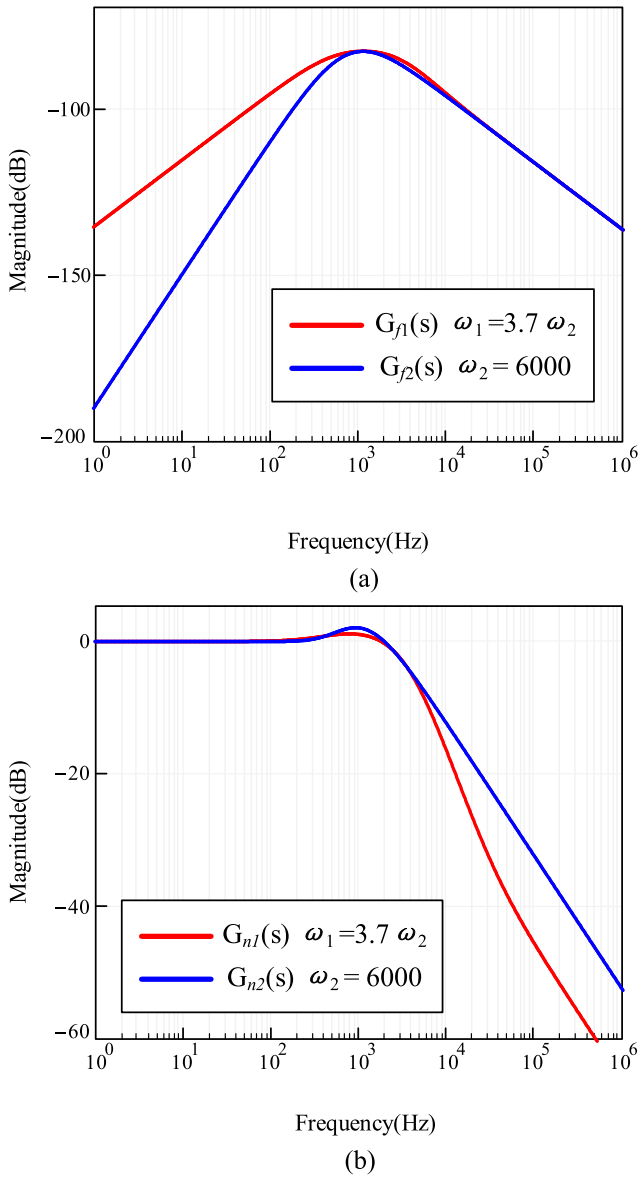

Fig. 9. Disturbance rejection and noise suppression performances of PLLO and TLESO for $k = 3.7$. (a) $G_{f1}(s)$ and $G_{f2}(s)$ when $\omega_0 = 6000$ rad/s. (b) $G_{n1}(s)$ and $G_{n2}(s)$ when $\omega_0 = 6000$ rad/s.

Similarly, according to Fig. 7, the noise suppression performance of TLESO is better than PLLO when the following conditions are met

$$20\log_{10}|G_{n1}(j\omega)| < 20\log_{10}|G_{n2}(j\omega)|. \tag{34}$$

By substituting (25) and (27), (34) can be simplified to

$$|M_1(j\omega)| < |M_2(j\omega)|. \tag{35}$$

Then, substitute (14) and (22) into (35), and let $q = \omega / \omega_0$, we have

$$\left(1 - \frac{2}{q^2}\right)k^4 - 2\left(4 + \frac{1}{q^2}\right)k^2 - \left(1 + 4q^2\right) < 0. \tag{36}$$

As the observer bandwidth ω_0 is much smaller than the noise frequency of interest ω, the value of q is considered to be larger

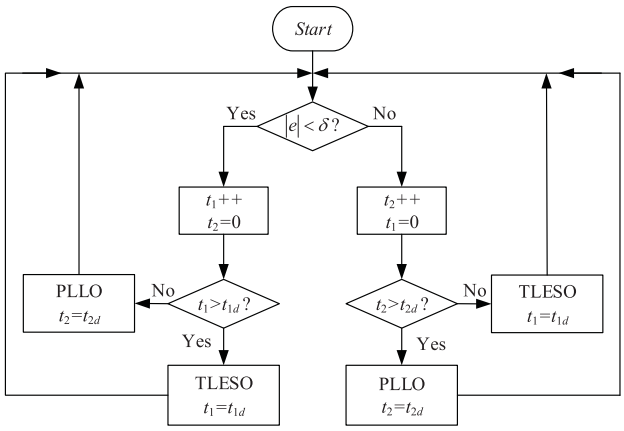

Fig. 10. Flowchart of ALESO.

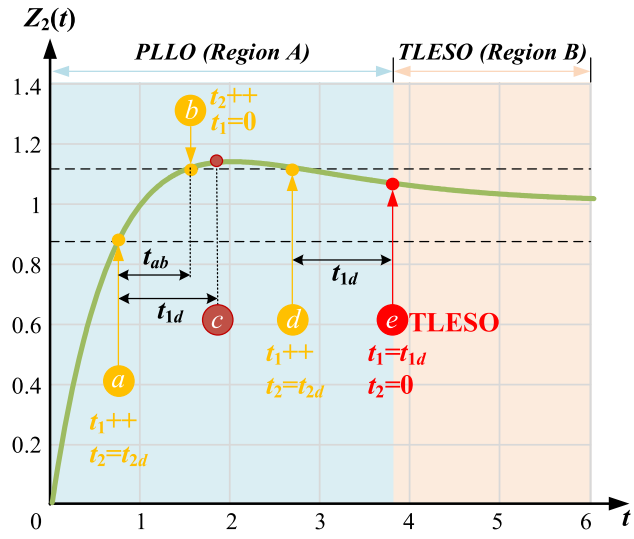

Fig. 11. Switching of two controllers.

than $\sqrt{2}$, thus the inequality (36) can be solved as

$$k < \sqrt{\frac{4+\frac{1}{q^2}+\sqrt{\left(4+\frac{1}{q^2}\right)^2+\left(1-\frac{2}{q^2}\right)(1+4q^2)}}{1-\frac{2}{q^2}}}. \quad (37)$$

The minimum value of the right side of the inequality (37) is derived as k_2 when q approaches 3.2

$$k_2 \approx 3.7. \quad (38)$$

When $k < k_2$ is satisfied, the inequality (37) and thus (34) can always be true. That is, if the observer bandwidth of TLESO is k_2 times smaller than the observer bandwidth of PLLO, TLESO has better noise suppression performance. The boundary case when $\omega_1 = 3.7\omega_2$ is given in Fig. 9(b).

B. Switching Criteria of ALESO

The criteria for switching the control structure between the PLLO and TLESO should also be determined. The flowchart is given by Fig. 10.

1) Threshold Value δ: The difference between the actual output voltage and the reference is e. When $e < \delta$ is satisfied, the system is considered to be in a steady state. Otherwise, it is considered to be in a transient state. The δ is set as

$$\delta = \frac{1}{2}\Delta V_o + \delta' \quad (39)$$

where ΔV_o represents the maximum voltage ripple of the DAB converter, and an extra margin δ' is set to avoid possible interference to the hardware circuit, such as electromagnetic interference, sampling error, etc.

2) Delay Time t_{2d}: When the converter's output voltage deviates from its steady state value for $t_2 \geq t_{2d}$ time, switch S will be toggled to activate PLLO operation. In fact, t_{2d} is set to exclude possible disturbance effects and ensure that the system has entered the transient state. $t_{2d} = (2\sim3)\ T_s$ is required.

3) Delay Time t_{1d}: When the converter's output voltage reaches its steady state and remains in the state for $t_1 \geq t_{1d}$, the dynamic process is assumed to have ended, and switch S will be toggled to activate TLESO operation. The t_{1d} should be carefully set to avoid frequent switching of switch S.

Assuming the disturbance is a step function $f(s) = \frac{K}{s}$, the response of PLLO is

$$z_2(s) = \frac{2\omega_2 s + \omega_2^2}{s^2 + 2\omega_2 s + \omega_2^2}\frac{K}{s}. \quad (40)$$

The time-domain function is obtained by inverse Laplace transformation as

$$z_2(t) = K(\omega_2 t e^{-\omega_2 t} - e^{-\omega_2 t} + 1). \quad (41)$$

Taking the derivative of (41) with respect to t, the extreme point occurs at time

$$t_e = \frac{2}{\omega_2}. \quad (42)$$

By setting the parameters $K = 1$ and $\omega_2 = 1$, the function $z_2(t)$ is plotted in Fig. 11, where the switching of two controllers is illustrated in detail. If the $z_2(t)$ enters the region limited by the two dotted lines, it is considered that the system enters the steady state. At point a, the system first reaches the steady state, and the counter t_1 starts counting. The PLLO will be activated until $t_1 = t_{1d}$. During the interval $b \sim d$, as the output exceeds the threshold, the PLLO still takes effect. Due to the fast regulation of PLLO, the output voltage reaches the steady state again at point d. After delay time t_{1d}, the TLESO operation is activated. In Fig. 11, the PLLO is activated in region A, and the TLESO is activated in Region B. It is worth mentioning that insufficient delay time of t_{1d} can lead to chattering between PLLO/TLESO operations. Therefore, a larger t_{1d}, such as $t_{1d} = 1.5t_e$, is set, where the condition of $t_{1d} > t_{ab}$ is satisfied.

IV. Experimental Verification

In order to verify the performance of the proposed ALESO control, different control strategies are performed on a 500 W DAB experimental prototype, the circuit parameters are given

TABLE I
SPECIFICATIONS OF EXPERIMENTAL PROTOTYPE

Circuit Parameters	Value
Input Voltage , V_i	300 V
Output Voltage , V_o	100 V
Inductance , L	17 μH
Primary dc capacitor , C_1	200 μF
Secondary dc capacitor , C_2	100 μF
Transformer's Turn Ratio , N	1:3
Switching Frequency , f_s	100 kHz
Control Update Frequency	100 kHz
Rated Output Power , P_o	500 W

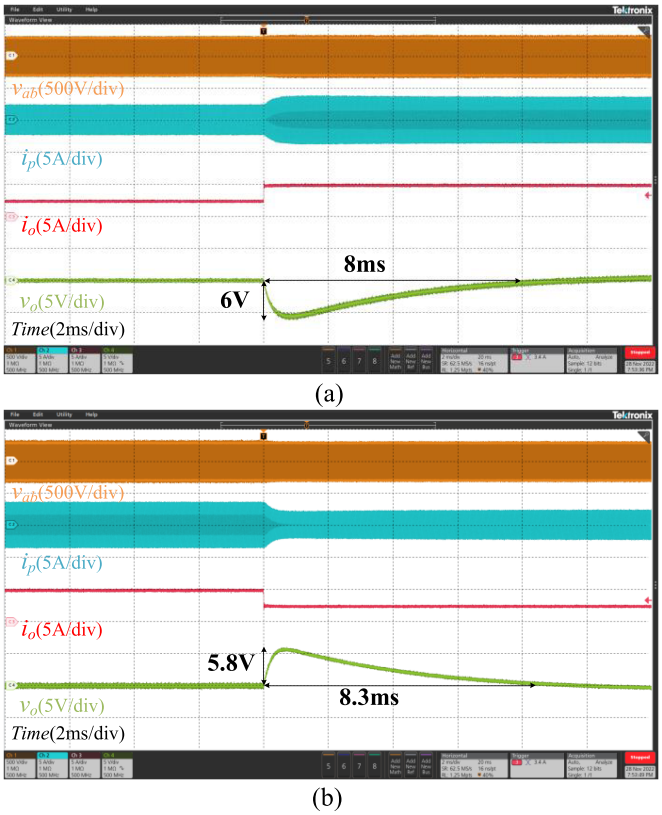

Fig. 12. Transient performances of PI controller. (a) Load increases from 250 W to 500 W. (b) Load decreases from 500 W to 250 W.

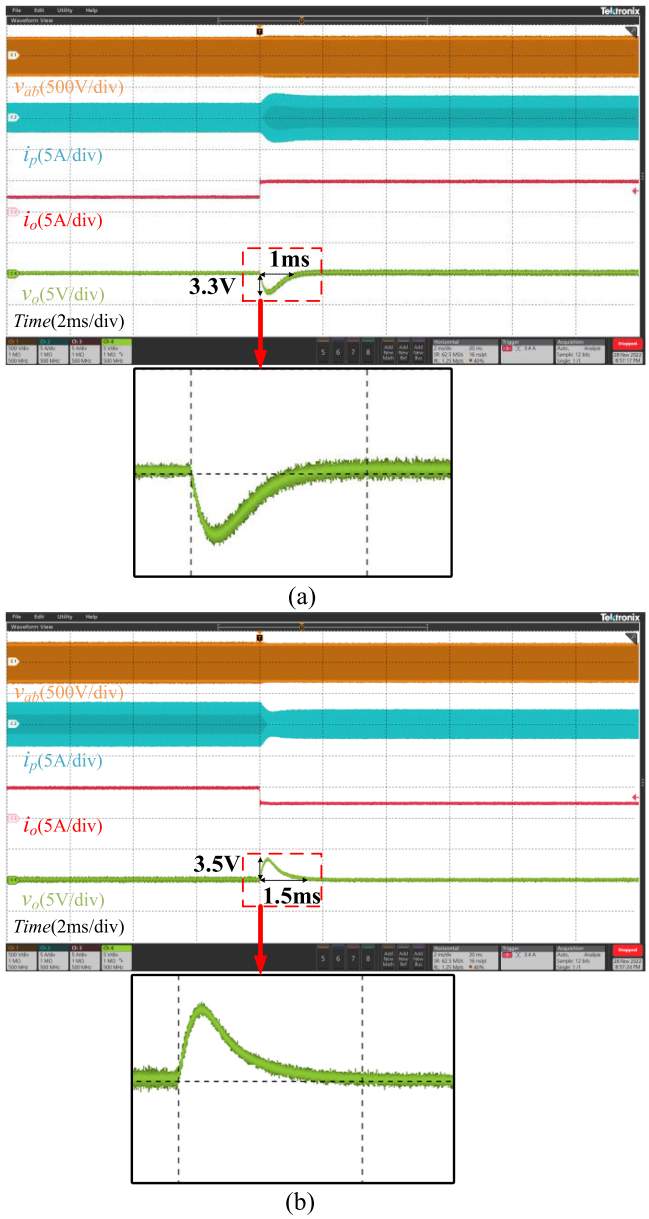

Fig. 13. Transient performances of TLESO controller. (a) Load increases from 250 W to 500 W. (b) Load decreases from 500 W to 250 W.

in Table I. All control strategies are implemented on a TMS320F28335 DSP platform. Each case is designed with a crossover frequency of approximately 500 Hz and a phase margin of 90°. The observer bandwidth of ALESO is set to be that of TLESO and PLLO, i.e., $\omega_0 = \omega_1 = \omega_2$ for $k = 1$, in accordance with the analysis in Section III-A, such that ALESO exhibits both good disturbance rejection and noise suppression performances.

A. Step Load Changes

For benchmarking, Fig. 12 shows the transient response of PI controller when the load is stepped up/down between 500 and 250 W. When the load is stepped up, the output voltage undershoot is 6 V and the settling time is about 8 ms. When the load is stepped down, the output voltage overshoot is 5.8 V and the settling time is approximately 8.3 ms.

Figs. 13, 14, and 15 show the transient responses of three observers (TLESO, PLLO, and ALSEO) with an equal observer's bandwidth of 6000 rad/s. Table II gives the measured output voltage derivations and setting times associated with three different control schemes.

Fig. 13 shows the transient response of TLESO controller. The output voltage derivation is 3.3 V with a settling time of 1 ms when load increases and the output voltage overshoot is 3.5 V with a setting time of 1.5 ms when load decreases, showing the improved performance of TLESO over PI controller.

TABLE II
PERFORMANCE COMPARISON BETWEEN DIFFERENT CONTROL SCHEMES

ω	Control scheme	Load increases		Load decreases	
		Output voltage deviation (V)	Settling time (ms)	Output voltage deviation (V)	Settling time (ms)
6000	PI	6	8	5.8	8.3
	TLESO	3.3	1	3.5	1.5
	PLLO	1.9	0.3	1.9	0.4
	ALESO	2.2	0.4	2.2	0.4

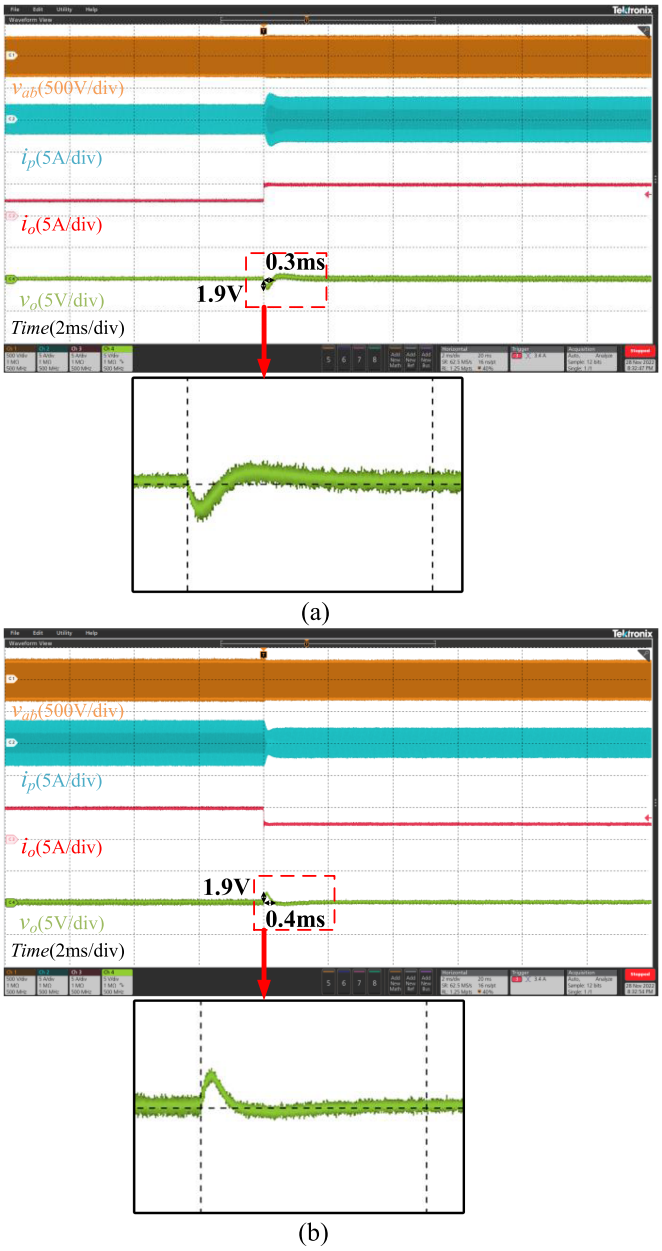

Fig. 14. Transient performances of PLLO controller. (a) Load increases from 250 W to 500 W. (b) Load decreases from 500 W to 250 W.

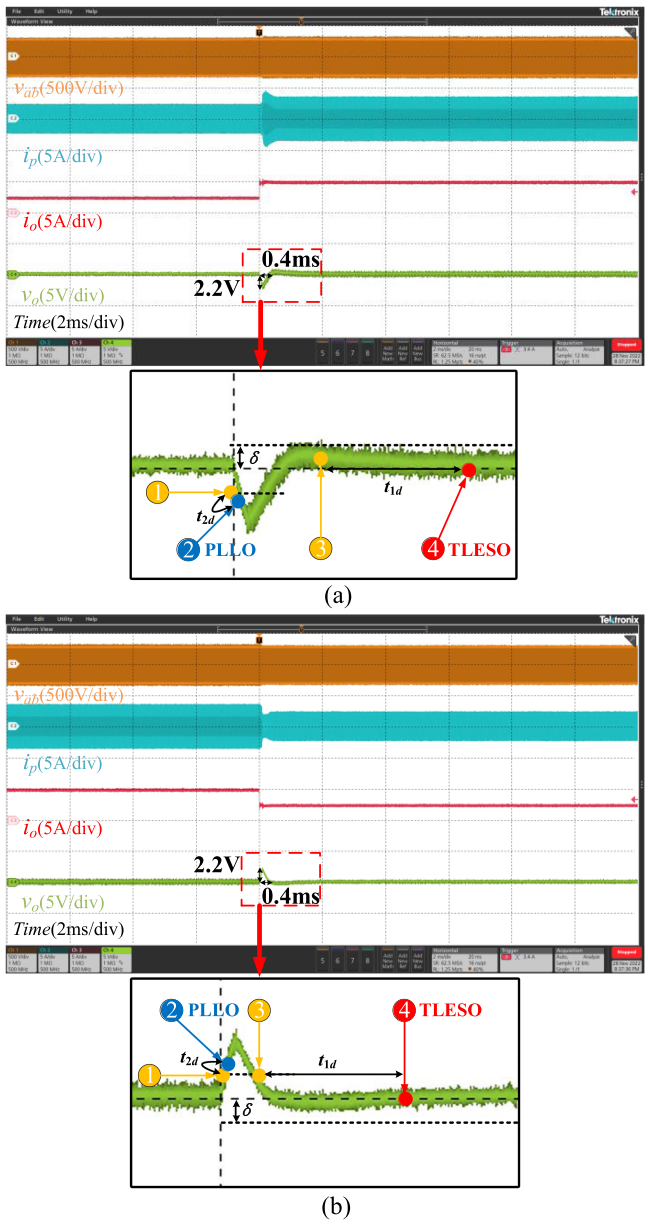

Fig. 15. Transient performances of ALESO controller. (a) Load increases from 250 W to 500 W. (b) Load decreases from 500 W to 250 W.

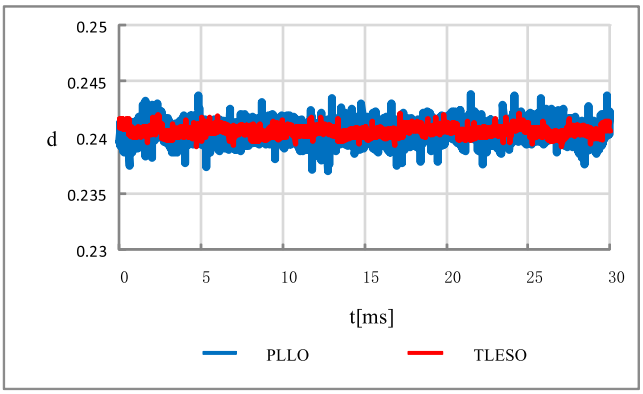

Fig. 16. Measured controller's output at steady state $\omega_1 = \omega_2 = 6000$.

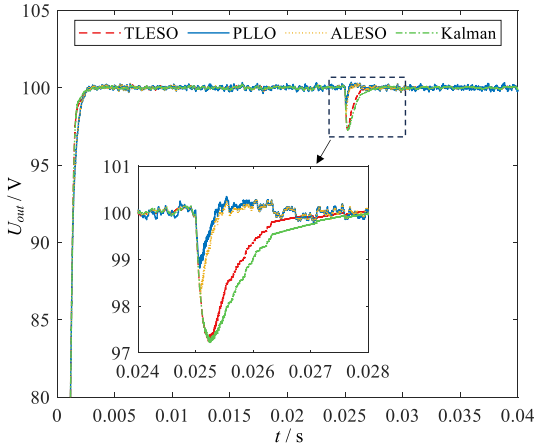

Fig. 17. Simulation results under load variation with different observers.

Fig. 14 shows the transient response of PLLO controller. The output voltage undershoot is 1.9 V with a settling time of 0.3 ms when load increases and the voltage overshoot is 1.9 V with a settling time of 0.4 ms when load decreases, which outperforms TLESO.

Fig. 15 shows the transient response of the proposed ALESO. The adaptive switching parameters are designed as: $\delta = 0.75$ V, $t_{1d} = 1$ ms ($100T_s$) and $t_{2d} = 30$ μs ($3T_s$). When the load is stepped up/down, the voltage undershoot/overshoot is 2.2 V with a settling time of 0.4 ms, which is similar to the performance of PLLO. In comparison with TLESO, the proposed ALESO has resulted in 33.3%/37.1% and 60%/73.3% reductions in output voltage undershoot/overshoot and setting time, respectively, under load step-up/down.

The detailed switching process is also illustrated in Fig. 15. Four typical states are marked.

1) *State* 1: The voltage error e exceeds the threshold value δ and then t_2 starts counting.
2) *State* 2: When the output voltage deviates from its steady state value for $t_2 \geq t_{2d}$ time, PLLO operation is activated.
3) *State* 3: Due to the fast regulation of PLLO, the output voltage reaches the steady state, and t_1 starts counting.
4) *State* 4: After delay time t_{1d}, TLESO operation is activated, which provides good noise immunity.

B. Steady-State Noise

To compare the noise rejection capability of the three controllers, the controller's steady-state output of TLESO and PLLO with 6000 rad/s bandwidth are measured and compared in Fig. 16. For comparison, the standard deviation is calculated to quantify the noise, where a smaller standard deviation indicates a smaller noise level. Assume the sampling matrix of the control signal is $D = \{d_1, d_2, \ldots, d_n\}$, which is recorded by the CCS, the standard deviation is

$$\sigma = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(d_i - \bar{d})^2}, \bar{d} = \frac{1}{n}\sum_{i=1}^{n} d_i \tag{43}$$

where $\bar{d}$ is the average of d_i.

The standard deviation of TLESO and PLLO is calculated to be 0.000467 and 0.001971, respectively, showing that a noise level reduction of 76.3% is achieved by TLESO compared to that resulting from PLLO with equal bandwidth. As the proposed ALESO is designed to adopt TLESO during steady state, a smooth control signal is guaranteed, which is an advantage of the proposed ALESO controller.

C. Performance Comparison Between Different Observers

Fig. 17 shows the simulation results under load variation with TLESO, PLLO, ALESO, and Kalman filter. The output voltage deviation and setting time resulting from the four controllers are summarized in the first and second column of Table III. It demonstates that the proposed ALESO has superior voltage deviation and setting time.

Noise signal having normal distribution with a mean value of 0 and a variance of 0.05 is added to the sampled output signal, which is fed back to the control loop. The standard deviation for each controller is calculated in the third column of Table III.

The susceptibility to parameter errors for each controller is also studied by deviating the inductance L and capacitance C_2 by $\pm 30\%$ from their nominal values. In total, four conditions corresponding to $L = 0.7L_0$, $L = 1.3L_0$, $C_2 = 0.7C_{20}$, and $C_2 = 1.3C_{20}$ are simulated and compared. The largest undershoot deviation among the four conditions is recorded for each controller in the fourth column of Table III. The transient responses of the four controllers for the case of $C_2 = 0.7C_{20}$ are shown as Fig. 18. It shows that the ALESO is more robust to parameter errors than TLESO and Kalman filter.

To compare the execution time of different controllers, the control programs were looped for 100 000 times. Table III records the execution time for different control schemes. It can be seen that ALESO takes slightly longer than PLLO and TLESO due to its adaptive mechanism. In particular, in executing each loop of the program, ALESO needs to determine whether the system is in steady or transient state. Nevertheless, there is no significant increase in the execution time of ALESO compared to PLLO and TLESO. In contrast, the longest execution time is

TABLE III
SIMULATION RESULTS BETWEEN DIFFERENT CONTROL SCHEMES

Control scheme	Output voltage deviation (V)	Settling time (ms)	Standard deviation	The largest undershoot deviation (V)	Execution time for 100 000 times (ms)
TLESO	2.8	2	0.004579	1	6.946
PLLO	1.2	0.8	0.012712	0.3	6.921
ALESO	1.8	0.8	0.004618	0.5	8.890
Kalman filter	2.8	2	0.004561	0.8	527.803

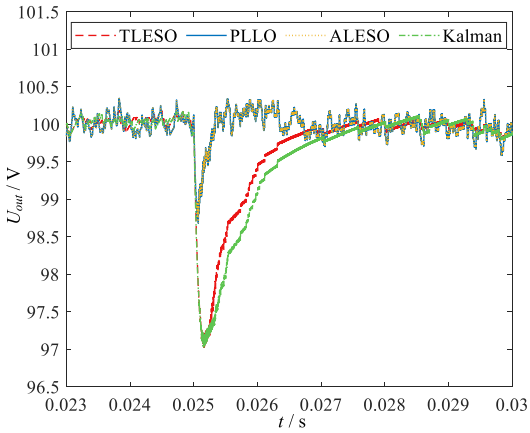

Fig. 18. Simulation results under load variation with different observers when $C_2 = 0.7C_{20}$.

required for Kalman filter due to the complex matrix operations involved.

It has been verified that the proposed ALESO has superior dynamic performance, noise rejection, susceptibility to parameter errors, and short exection time compared to other state-of-the-art observers.

V. CONCLUSION

This article proposes an ALESO that mitigates the conflict between the disturbance rejection and noise immunity in an ESO-controlled DAB converter. Through a comparative analysis of both TLESO and PLLO, a detailed comparison of their advantages and disadvantages under the same bandwidth is performed. The proposed adaptive mechanism combines both of these basic observers and achieves a variable-structure control that ensures both reduced steady-state noise and improved dynamic response without resolving to use high bandwidth. A further advantage of ALESO is that it can be analyzed by using classical control theory, and the parameter design of ALESO can be obtained by analyzing the bandwidth relationship between TLESO and PLLO, making it easy to implement in practice. The proposed ALESO is very promising, especially for the applications where both fast-tracking performance and good tracking accuracy are required.

REFERENCES

[1] R. A. Gardenghi and R. C. Houlne, "Power supply consideration for pulsed solid-state radar," in *Proc. IEEE Power Modulator Symp.*, 1990, pp. 146–152.
[2] X. Gao, H. Wu, S. Gao, Z. Zhang, and Y. Xing, "A two-stage pulsed power supply for low-dc-voltage and low-frequency pulsed-current loads," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2298–2309, Feb. 2021.
[3] X. Huang, X. Ruan, F. Du, F. Liu, and L. Zhang, "A pulsed power supply adopting active capacitor converter for low-voltage and low-frequency pulsed loads," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9219–9230, Nov. 2018.
[4] W. Ao, J. Chen, and W. Lv, "Coordinate sizing and control of the onboard pulse power supply system," *IEEE Trans. Ind. Electron.*, vol. 71, no. 8, pp. 9034–9043, Aug. 2024.
[5] L. Cao, K. H. Loo, and Y. M. Lai, "Systematic derivation of a family of output-impedance shaping methods for power converters—A case study using fuel cell-battery-powered single-phase inverter system," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5854–5869, Oct. 2015.
[6] Y. Liu, W. Zhang, Y. Sun, M. Su, G. Xu, and H. Dan, "Review and comparison of control strategies in active power decoupling," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14436–14455, Dec. 2021.
[7] H. Qin and J. W. Kimball, "Closed-loop control of DC-DC dual-active-bridge converters driving single-phase inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 1006–1017, Feb. 2014.
[8] S. Dutta, S. Hazra, and S. Bhattacharya, "A digital predictive current-mode controller for a single-phase high-frequency transformer-isolated dual-active bridge DC-to-DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5943–5952, Sep. 2016.
[9] Y. Jeung and D. Lee, "Voltage and current regulations of bidirectional isolated dual-active-bridge dc-dc converters based on a double-integral sliding mode control," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6937–6946, Jul. 2019.
[10] W. Gao, Y. Wang, and A. Homaifa, "Discrete-time variable structure control systems," *IEEE Trans. Ind. Electron.*, vol. 42, no. 2, pp. 117–122, Apr. 1995.
[11] J. Han, "From PID to active disturbance rejection control," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 900–906, Mar. 2009.
[12] Zhiqiang Gao, Shaohua Hu, and Fangjun Jiang, "A novel motion control design approach based on active disturbance rejection," in *Proc. 40th IEEE Conf. Decis. Control*, 2001, pp. 4877–4882.
[13] B Sun and Z Gao, "A DSP-based active disturbance rejection control design for a 1-kW H-bridge DC–DC power converter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1271–1277, Oct. 2005.
[14] M. Ali, M. Y aqoob, L. Cao, and K. H. Loo, "Disturbance-observer-based DC-bus voltage control for ripple mitigation and improved dynamic response in two-stage single-phase inverter system," *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 6836–6845, Sep. 2019.
[15] S. Shao et al., "Modeling and advanced control of dual-active-bridge DC–DC converters: A review," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1524–1547, Feb. 2022.
[16] L. Deng, G. Zhou, Y. Li, and Z. Chen, "Communication-free pulsed power distribution and tracking method for hybrid energy storage system based on active disturbance rejection control," *IEEE Trans. Power Electron.*, vol. 39, no. 3, pp. 3024–3036, Mar. 2024.
[17] Z. Gao, "Scaling and bandwidth-parameterization based controller tuning," *Proc. Am. Control Conf.*, vol. 6, pp. 4989–4996, 2003.

[18] S. Ahmad and A. Ali, "On active disturbance rejection control in presence of measurement noise," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11600–11610, Nov. 2022.

[19] G. Tang, W. Xue, H. Peng, Z. Yang, and Y. Zhao, "Parallel multiple extended state observers based ADRC with application to high-speed precision motion stage," *IEEE Trans. Ind. Electron.*, vol. 71, no. 8, pp. 9639–9648, Aug. 2024.

[20] K. Łakomy and R. Madonski, "Cascade extended state observer for active disturbance rejection control applications under measurement noise," *ISA Trans.*, vol. 109, pp. 1–10, 2021.

[21] K. Łakomy et al., "Active disturbance rejection control design with suppression of sensor noise effects in application to DC–DC buck power converter," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 816–824, Jan. 2022.

[22] Y. Zeng et al., "Active disturbance rejection control using artificial neural network for dual-active-bridge-based energy storage system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 1, pp. 301–311, Feb. 2023.

[23] S. Zhuo, A. Gaillard, L. Guo, L. Xu, D. Paire, and F. Gao, "Active disturbance rejection voltage control of a floating interleaved DC–DC boost converter with switch fault consideration," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12396–12406, Dec. 2019.

[24] L. Xu, S. Zhuo, Y. Huangfu, J. Liu, and F. Gao, "Adaptive active disturbance rejection control for DC-DC converter with time-varying disturbance," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 5, no. 3, pp. 868–879, Jul. 2024.

[25] C. Liu, G. Luo, X. Duan, Z. Chen, Z. Zhang, and C. Qiu, "Adaptive LADRC-based disturbance rejection method for electromechanical servo system," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 876–889, Jan./Feb. 2020.

[26] S. Zhuo, A. Gaillard, L. Xu, H. Bai, D. Paire, and F. Gao, "Enhanced robust control of a DC–DC converter for fuel cell application based on high-order extended state observer," *IEEE Trans. Transp. Electrific.*, vol. 6, no. 1, pp. 278–287, Mar. 2020.

[27] S. Zhu et al., "Robust speed control of electrical drives with reduced ripple using adaptive switching high-order extended state observer," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2009–2020, Feb. 2022.

[28] L. Tao, P. Wang, X. Ma, Y. Wang, and X. Zhou, "Variable form LADRC-based robustness improvement for electrical load interface in microgrid: A disturbance response perspective," *IEEE Trans. Ind. Inform.*, vol. 20, no. 1, pp. 432–441, Jan. 2024.

[29] Y. Zuo, X. Zhu, L. Quan, C. Zhang, Y. Du, and Z. Xiang, "Active disturbance rejection controller for speed control of electrical drives using phase-locking loop observer," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1748–1759, Mar. 2019.

[30] L. Chen, S. Shao, Q. Xiao, L. Tarisciotti, P. W. Wheeler, and T. Dragičević, "Model predictive control for dual-active-bridge converters supplying pulsed power loads in naval DC micro-grids," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1957–1966, Feb. 2020.

[31] Q. Xiao, L. Chen, H. Jia, P. W. Wheeler, and T. Dragičević, "Model predictive control for dual active bridge in naval DC microgrids supplying pulsed power loads featuring fast transition and online transformer current minimization," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 5197–5203, Jun. 2020.