Design of a High-Bandwidth Compact DC-Bus Embedded Planar Rogowski Coil for SiC MOSFET Current Sensing

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***Abstract*—This article quantitatively investigates the design considerations for a planar Rogowski coil. Within one printed circuit board (PCB), the Rogowski coil is placed between the overlapping dc-bus traces, the dc-link capacitor, and the half-bridge. This integration allows for measuring both dc-bus currents with one Rogowski coil, hence enabling the Silicon Carbide (SiC) MOSFET switch transient current measurement of both half-bridge MOSFETs with one coil. A parametric mutual inductance equation and the Rogowski coil transfer function are proposed to simplify the design process of a planar Rogowski coil. Design considerations are evaluated. In additionally, the induced measurement error due to current crowding within the dc bus is investigated, and the impact of Rogowski coil windings exceeding the dc-bus trace width as a measure to reduce the mutual inductance error is explored and experimentally validated. A 106 mm^2 small planar Rogowski coil current sensor with a maximum bandwidth of 185 MHz is built. The prototype is evaluated for its parasitic parameters. Its current measurement performance is compared to that of a commercial Rogowski coil. Measurement results compare well between the planar Rogowski coil and the commercial Rogowski coil. In addition, measurements show that the mutual inductance of the proposed Rogowski coil is insusceptible to current crowding within the dc bus.**

***Index Terms*—Current measurement, gallium nitride, half-bridge, Rogowski coil, silicon carbide.**

I. Introduction

ROGOWSKI coils have become increasingly popular as current sensors with the emergence of wide-bandgap semiconductor devices. The sensor combines a small footprint and, respectively, a minimized impact of the sensor on the stray inductance of the current commutation due to the reduction in sensor bandwidth, and an electric isolated current measurement [1].

A typical application of Rogowski coils is overcurrent detection. The standard desaturation (DESAT) overcurrent measurement for wide-bandgap transistors is deemed to be nonideal since the equivalent die area of wide-bandgap devices under similar operating conditions is smaller than that of their silicon counterparts [2], [3], [4]. The small Silicon Carbide (SiC) die area complicates the dissipation of joule heating during short-circuit events and, thus, reduces the short-circuit withstand time [5], [6]. Furthermore, wide-bandgap devices operate mainly during overcurrent events in the ohmic region. The drain-source on-state voltage drop in the ohmic region is highly temperature dependent. Therefore, DESAT overcurrent protection is accurate only for a specific operating temperature for SiC MOSFETs [7].

In addition to overcurrent detection, Rogowski coils are used to measure fast switching transients. The sensor's switch current amplitude information can be used to reconstruct the ac output current of a half-bridge. This potentially allows for the replacement of Hall-effect sensors to measure ac output current [8].

With the emergence of wide bandgap devices, the switching speed increased. To capture fast switching transients and high-frequency oscillations, the bandwidth of helical Rogowski coils increased to more than 110 MHz and 300 MHz, respectively [9], [10]. The high bandwidth is achieved as a result of the reduction in the Rogowski coil size and the reduction in the number of coil windings. The current carrying trace is routed through the coil for helical Rogowski coils. Thus, the placement of the current sensor alters, in most cases, the design of the current commutation loop and adds additional stray inductance to the commutation loop. This increases the drain-source overshoot voltage during the turn-OFF switch transient.

Zhao et al. [11] first proposed using a planar Rogowski coil where the current carrying trace circumvents the straight/planar coil. Due to the proximity of the coil windings to the current carrying traces, planar Rogowski coils require fewer windings for an equivalent mutual inductance to that of regular helical Rogowski coils. With fewer windings, the parasitic self-inductance

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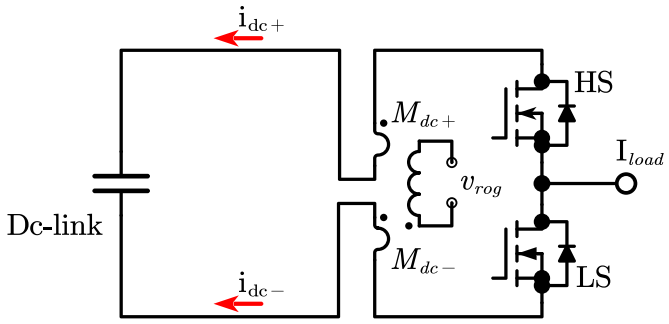


Fig. 1. Simplified equivalent electric circuit of the DC-bus structure, MOSFET half-bridge, and planar Rogowski coil.

and parasitic self-capacitance are reduced, and thus, the coil's bandwidth is increased. This makes the planar Rogowski coils particularly attractive for fast switching transient current measurements for Gallium Nitride (GaN)- and SiC-field effect transistors (FETs) [12], [13], [14], [15], [16], [17].

Kuwabara et al. [16], [17] first introduced the placement of a planar Rogowski coil between the dc-link capacitor and the switching half-bridge. This integration allows for a simplified trace design, a decrease in the high current carrying trace length, and a great mutual inductance cancelation between the forward and return paths of the dc-bus trace layout. The coil placement simultaneously allows for the measurement of short-circuit events and the measurement of switch transient currents.

In [18], the function principle and the Rogowski coil operating states are explained. In addition, qualitative design recommendations were made. This work builds on the abovementioned previous work. First, the operating states are explained in a more condensed manner in Section II. Based on the design parameters of the coil and the high-current trace design, Section III derives the total mutual inductance equation. The derived equation is then compared concerning its accuracy to the total mutual inductance extracted from finite-element simulations carried out in Ansys Q3D. In Section IV, the transfer function of the planar Rogowski coil is derived. Section V extends the previously presented design guidelines. In addition, a quantitative evaluation of the mutual inductance error resulting from current density crowding within the dc-bus traces is carried out. The section also highlights how extending the planar Rogowski coil beyond the dc-bus trace width decreases the mutual inductance error. Section VI details the Rogowski coil prototype design and the experimental results. The measurement of the sensor's parasitics is covered. Switch transient measurements are performed at 600 V and a drain current of 50 A. The impact of current crowding within the dc-bus traces on the sensor accuracy is evaluated. The planar Rogowski coil is compared to a commercial Rogowski coil. Finally, Section VII concludes this article.

II. Function Principle of a Planar Rogowski Coil

The detailed function principle was first investigated in [18]. A planar Rogowski coil can be placed adjacent to one or two current carrying traces. A change in current through the conducting trace creates a magnetic field density change, which the planar Rogowski coil can pick up. The coil is placed between the overlapping dc-bus traces, the MOSFET half-bridge, and the dc-link capacitor. The resulting simplified electric circuit of the proposed integration is displayed in Fig. 1. Fig. 2 shows an exploded view and side view of a possible planar Rogowski coil integration between two dc-bus traces. The lower U-shaped dc-trace provides space between the dc− and dc+ trace to place the Rogowski coil. The design of the displayed current sensor marginally increases the overall length of the dc-busbar.

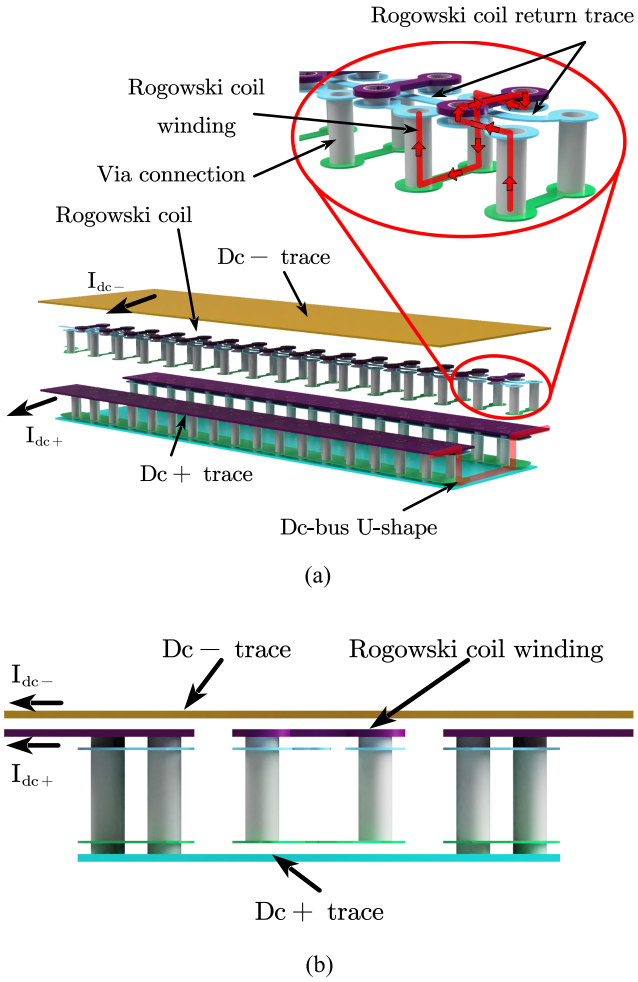


Fig. 2. General design of the planar Rogowski coil. (a) Exploded 3-D model of a planar Rogowski coil integrated into a printed circuit board (PCB). (b) Side view of the Rogowski coil windings and the DC-bus trace layout. The Rogowski coil windings are created with a combination of PCB traces and vias.

The planar Rogowski coil measures the change in magnetic flux density created by the change in current through the dc− trace and the dc+ trace. The coil's output voltage can be expressed as follows:

$$v_{\mathrm{rog}} = M_{\mathrm{dc+}} \cdot \frac{di_{\mathrm{dc+}}}{dt} + M_{\mathrm{dc-}} \cdot \frac{di_{\mathrm{dc-}}}{dt}. \tag{1}$$

The mutual inductance between the dc+ trace and the Rogowski coil is denoted by $M_{\mathrm{dc+}}$, while the change in current through the dc+ trace is represented by $di_{\mathrm{dc+}}/dt$. Similarly,

$M_{\mathrm{dc}-}$ is the mutual inductance between the dc− trace and the Rogowski coil, and $di_{\mathrm{dc}-}/dt$ is the change in current through the dc− trace.

The planar Rogowski coil can experience the following three different operational states:

1) continuous current conduction through one of the dc-bus traces;
2) half-bridge switching transient;
3) short-circuit events.

The operating state during conduction is described first.

The high- or low-side MOSFET conducts, causing the switch node current (I_{load}) to flow through one of the dc− or dc+ busbar traces. Thus, any switch node current change induces a magnetic flux density change around the dc-busbar trace, which the Rogowski coil can pick up. For the conduction operating state, (1) can be expressed as follows:

$$v_{\mathrm{rog}} = \begin{cases} M_{\mathrm{dc}+} \cdot \dfrac{di_{\mathrm{dc}+}}{dt}, & \text{if HS is conducting} \\ M_{\mathrm{dc}-} \cdot \dfrac{di_{\mathrm{dc}-}}{dt}, & \text{if LS is conducting.} \end{cases} \tag{2}$$

Next, the Rogowski coil's operating state during the switching transient is explained. Before the switch transient occurs, the load current conducts through one of the dc-bus traces. At the switch transient start, the conducting transistor starts to open. This introduces a change in current through the current carrying trace. If the half-bridge's switch node is in series with an inductor, the load current can be assumed constant during the short switch transient interval. This prompts the constant load current to flow through the other MOSFET's body diode. Thus, the change in current is equal through both dc-bus traces during the switch transient. The current direction is the same in both dc-bus traces. This results in a magnetic flux density cancelation in the space between the two traces. Following (1), as $di_{\mathrm{dc}+}/dt$ equals $di_{\mathrm{dc}-}/dt$, the output voltage of the Rogowski coil is dependent on the summed total mutual inductance as follows:

$$v_{\mathrm{rog}} = (M_{\mathrm{dc}+} + M_{\mathrm{dc}-}) \cdot \frac{di_{\mathrm{dc}-}}{dt}. \tag{3}$$

During a short-circuit event, both high- and low-side MOSFETs are conducting. A large current surge through the dc-bus traces is observed. The current change through the dc+ and dc− traces is equal. Thus, (3) also applies to calculating the output voltage of the Rogowski coil during short-circuit events.

III. Switching Transient Mutual Inductance Equation

In this section, a mutual inductance equation is introduced. The derived equation calculates the summed total mutual inductance. Section III-A highlights the equation derivation. In Section III-B, the derived equation is compared at 20 different coil design configurations with finite-element simulation results carried out in Ansys Q3D.

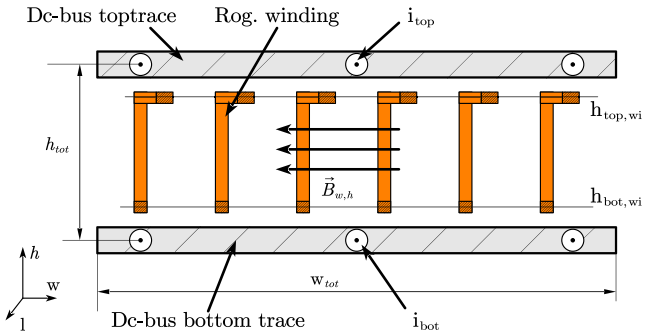


Fig. 3. Simplified cross-section of planar Rogowski coil, highlighting the current DC-bus current direction and Rogowski coil winding.

A. Mutual Inductance Derivation

No mathematical model has been presented in the literature addressing the mutual inductance calculation between the dc-bus traces and a planar Rogowski coil. This chapter derives the mutual inductance on the basis of the Rogowski coil geometry.

The total mutual inductance is calculated on the basis of the magnetic flux density change created by the changing current through the dc-bus traces. The simplified geometry of the Rogowski coil, displayed in Fig. 3, is used as a base to derive the magnetic flux density between the two dc-bus traces, and thus, the mutual inductance between the dc-bus traces and the Rogowski coil.

First, the magnetic flux density within the 2-D space defined by the height and dc-bus width is derived. The two dc-bus traces are treated as two parallel conductors with infinite length, finite dc-bus width w_{tot}, and a trace distance of h_{tot}. The horizontal magnetic flux density at any point, defined by height h and width w, and the current at uniform current density through each dc-bus trace, can be expressed as follows:

$$\begin{aligned} \vec{B}_{h,w} &= \vec{B}_{h,w}(I_{\mathrm{bot}}) + \vec{B}_{h,w}(I_{\mathrm{top}}) \\ \vec{B}_{h,w} &= \frac{\mu_0 \cdot I_{\mathrm{bot}}}{2\pi \cdot w_{\mathrm{tot}}} \cdot \left[\arctan\left(\frac{w_{\mathrm{tot}} - w}{h}\right) \right. \\ &\quad \left. - \arctan\left(\frac{-w}{h}\right) \right] \\ &\quad + \frac{\mu_0 \cdot I_{\mathrm{top}}}{2\pi \cdot w_{\mathrm{tot}}} \cdot \left[- \arctan\left(\frac{w_{\mathrm{tot}} - w}{-h_{\mathrm{tot}} + h}\right) \right. \\ &\quad \left. + \arctan\left(\frac{-w}{-h_{\mathrm{tot}} + h}\right) \right] \end{aligned} \tag{4}$$

where μ_0 is the permeability, I_{top} is the constant current flowing through the top busbar trace, and I_{bot} is the constant bottom trace current.

The magnetic flux density change between the dc-bus traces can be expressed as follows:

$$\begin{aligned} \frac{d\vec{B}_{h,w}}{dt} &= \frac{\mu_0}{2\pi \cdot w_{\mathrm{tot}}} \cdot \left[\arctan\left(\frac{w_{\mathrm{tot}} - w}{h}\right) \right. \\ &\quad \left. - \arctan\left(\frac{-w}{h}\right) \right] \cdot \frac{di_{\mathrm{bot}}}{dt} \end{aligned}$$

$$+\frac{\mu_0}{2\pi\cdot w_{\text{tot}}}\cdot\left[-\arctan\left(\frac{w_{\text{tot}}-w}{-h_{\text{tot}}+h}\right)+\arctan\left(\frac{-w}{-h_{\text{tot}}+h}\right)\right]\cdot\frac{di_{\text{top}}}{dt}. \tag{5}$$

The magnetic flux density changes along the width of the dc-bus traces. Thus, the Rogowski coil winding inductance to the dc-bus traces depends on the winding location. The winding inductance is described in the following equation:

$$L_w(w)=\frac{\mu_0\cdot l_{\text{wi}}}{2\pi\cdot w_{\text{tot}}}\cdot\int_{h_{\text{bot,wi}}}^{h_{\text{top,wi}}}\left[\arctan\left(\frac{w_{\text{tot}}-w}{h}\right)-\arctan\left(\frac{-w}{h}\right)-\arctan\left(\frac{w_{\text{tot}}-w}{-h_{\text{tot}}+h}\right)+\arctan\left(\frac{-w}{-h_{\text{tot}}+h}\right)\right]dh \tag{6}$$

where l_{wi} is the length of the winding between the midpoints of the vias which create the vertical winding trace, $h_{\text{top,wi}}$ is the center height of the top of the winding trace referenced to the origin, $h_{\text{bot,wi}}$ is the center height of the bottom of the winding referenced to the origin. The sum of each winding inductance of the planar Rogowski coil winding equals the total mutual inductance between the dc-bus traces and the planar Rogowski coil

$$M_{\text{tot}}=\sum_{1}^{N}L_w(w) \tag{7}$$

where N equals the total amount of Rogowski coil windings. Note that parts of the dc-bus structure represent a U-shape, and the vertical trace elements impact the magnetic flux density seen by the Rogowski coil. This changes the mutual inductance distribution between $M_{\text{dc+}}$ and $M_{\text{dc-}}$, yet the mutual inductance sum is unaffected. The derived equations can accurately calculate the summed mutual inductances.

B. Mutual Inductance Error Between Calculation and Simulation

The accuracy of the derived mutual inductance equation is evaluated. The equation parameters are swept, and their impact on the mutual inductance is compared with the Ansys Q3D finite-element simulation results. Each iteration involves altering one variable. Five simulation points are selected for each variable. The equation is tested for the following:

1) the distance (h_{tot}) between the current carrying traces while keeping the winding height constant;
2) the winding height $h_{\text{top,wi}}-h_{\text{bot,wi}}$ while the h_{tot} increases accordingly;
3) the Rogowski coil length (l_{wi});
4) the number of windings (N).

Fig. 4 compares the mutual inductances and errors between the calculation and the simulation. Appendix A lists the simulation results, the equation results, and the error for each selected value. The maximum observed error is 12.7%, which highlights the precision of the equation in calculating the total mutual inductance between the current carrying traces and the Rogowski planar coil.

IV. Transfer Function Derivation

Fig. 1 is expanded to depict the parasitic capacitances and inductances in the equivalent electric circuit. The detailed equivalent electric circuit is depicted in Fig. 5. Where $L_{p,\text{dc+}}$ is the introduced stray inductance in the dc+ trace, $L_{p,\text{dc-}}$ is the stray inductance in the dc− trace, $C_{\text{dc+,Rog}}$ is the parasitic equivalent parallel capacitance (EPC) between the Rogowski coil and the positive dc-bus trace, $C_{\text{dc-,Rog}}$ is the parasitic plate capacitance between the Rogowski coil and the negative dc-bus trace, $C_{\text{sen,dc}}$ is the parasitic plate capacitance between the dc+ and dc− traces, L_s is the coil's self-inductance, R_s is the winding resistance, C_s is the coil's winding capacitance, and $v_{\text{rog,out}}$ is the output voltage of the Rogowski coil. In contrast to [19], the parasitic plate capacitances between the Rogowski coil and the dc-bus traces are in series rather than in parallel.

The transfer function is derived based on the assumption that the two dc-bus traces are shorted at the SiC MOSFET location on the printed circuit board (PCB). Thus, the dc current $i_{\text{dc+}}$ is equal to $i_{\text{dc-}}$. The equivalent electric circuit can be simplified, as shown in Fig. 6. Where

$$M=M_{\text{dc+}}+M_{\text{dc-}} \tag{8}$$

$$L_p=L_{p,\text{dc+}}+L_{p,\text{dc-}} \tag{9}$$

$$C_e=\frac{C_{\text{dc+,Rog}}\cdot C_{\text{dc-,Rog}}}{C_{\text{dc+,Rog}}+C_{\text{dc-,Rog}}}. \tag{10}$$

The resulting fourth-order transfer function is as follows:

$$\frac{v_o}{i_{\text{dc}}}=\frac{s^3\left(C_eL_pL_s-C_eM^2\right)+C_eL_pR_ss^2+Ms}{F_As^4+F_Bs^3+F_Cs^2+s(C_eR_s+C_sR_s)+1}$$

$$F_A=C_eC_sL_pL_s-C_eC_sM^2$$

$$F_B=C_eC_sL_pR_s$$

$$F_C=C_eL_p+C_eL_s-2C_eM+C_sL_s. \tag{11}$$

Assuming that the values of the variables L_p, C_e, and C_s are much smaller than the other parameters, any term in which the variables are multiplied with each other can be omitted. The simplified second-order transfer function is as follows:

$$\frac{v_o}{i_{\text{dc}}}=\frac{Ms\left(1-C_eMs^2\right)}{s^2(L_s(C_e+C_s)-2C_eM)+s(R_s(C_e+C_s))+1}. \tag{12}$$

The transfer function gain of both transfer functions and the, in LTSpice, simulated transfer function are plotted in Fig. 7. For illustration purposes, a slight offset gain is applied to the

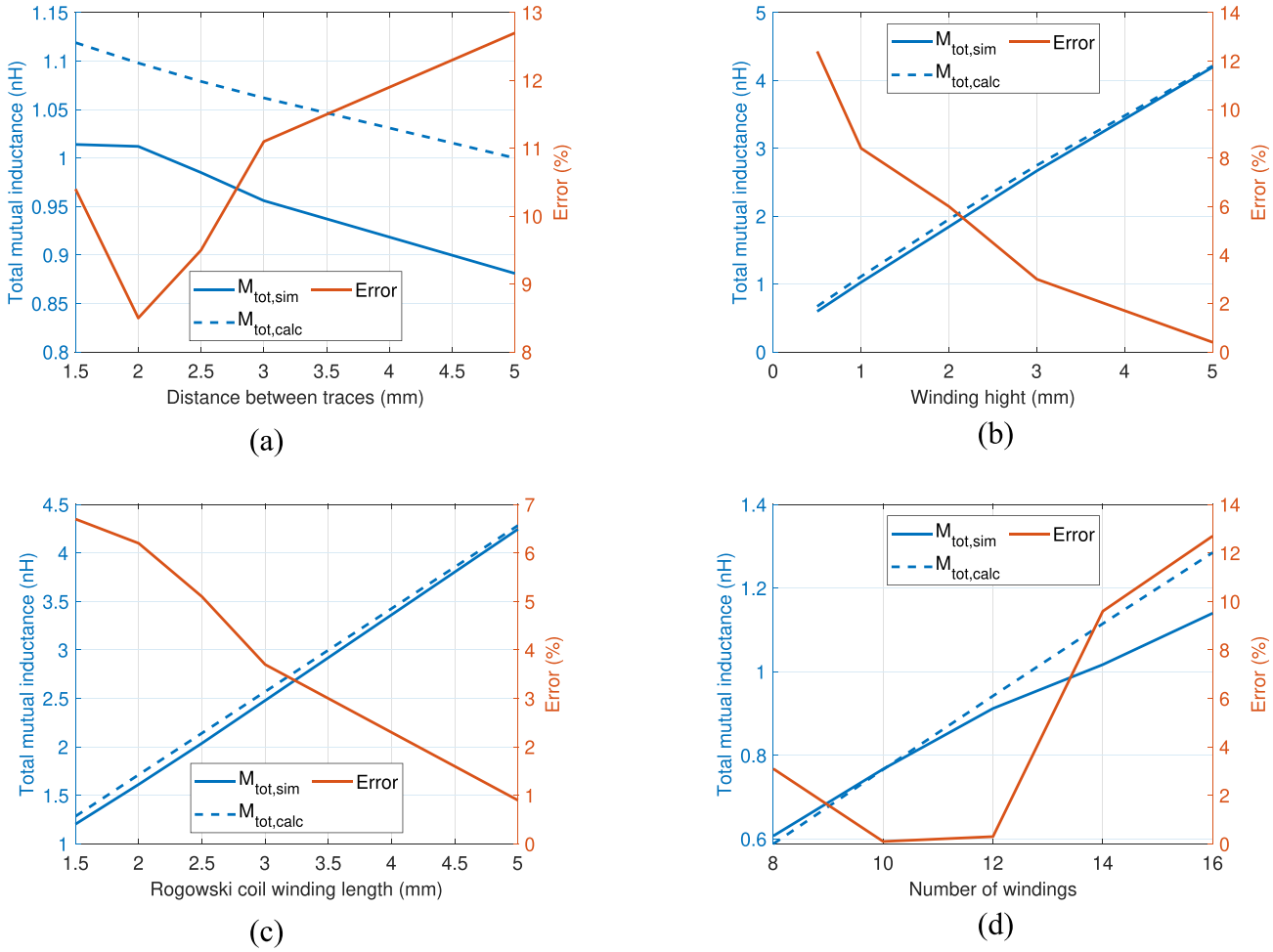


Fig. 4. Comparison of Ansys Q3D finite-element simulation total mutual inductance results to the calculated mutual inductance results. (a) Coil winding parameters are constant and the distance between the DC-bus traces is varied. (b) Winding heights are varied, while the DC-bus trace distance increases accordingly. (c) Rogowski coil length is varied. (d) Number of windings is varied.

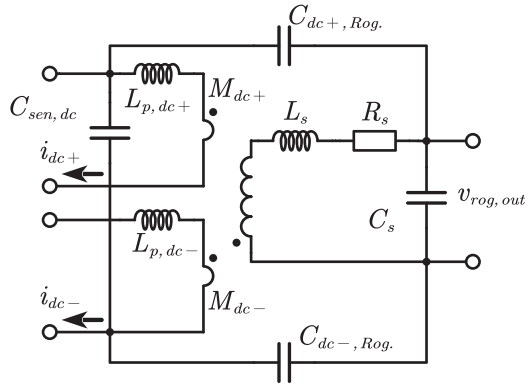


Fig. 5. Equivalent electric circuit of the planar Rogowski coil current sensor.

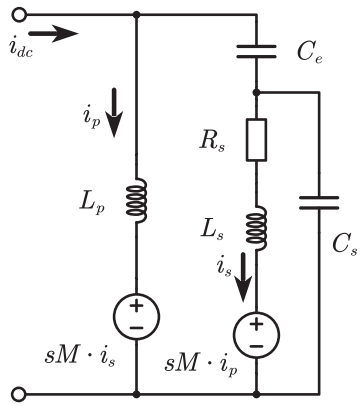


Fig. 6. Equivalent electric circuit used for the transfer function derivation.

second-order transfer function gain. Table I lists the passive components' values used to plot the transfer function. It can be observed that the derived transfer functions overlap nicely with the transfer function of the simulated equivalent electric circuit and match the transfer function from simulation until the first resonance. The resonant frequency of the planar Rogowski coil can be estimated by

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L_s\left(C_e + C_s\right) - 2C_eM}}. \tag{13}$$

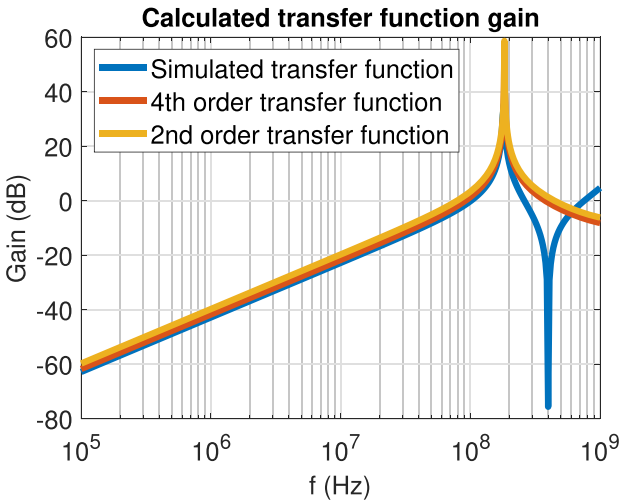


Fig. 7. Calculated and simulated transfer function gain of the fourth-order transfer function and its simplified second-order transfer function.

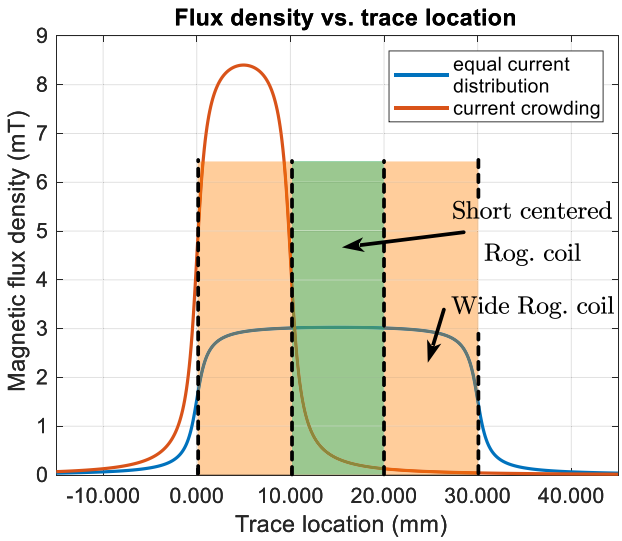
TABLE I
ROGOWSKI COIL DESIGN COMPARISON BETWEEN FINITE-ELEMENT SIMULATION RESULTS AND MEASURED RESULTS

Parameter	Simulated planar Rogowski coil	Measured planar Rogowski coil
Turn number (N)	16	-
Mutual inductance to dc+ ($M_{\mathrm{dc}+}$)	0.584 nH	-
Mutual inductance to dc− ($M_{\mathrm{dc}-}$)	0.564 nH	-
Self-inductance (L_s)	62.55 nH	58 nH
Coil EPC (C_s)	N.A.	5.5 pF
Coil EPC to dc+ ($C_{\mathrm{dc}+,Rog}$)	13.19 pF	16.5 pF
Coil EPC to dc− ($C_{\mathrm{dc}-,Rog}$)	12.24 pF	14.9 pF
dc-bus parasitic capacitance ($C_{\mathrm{dc}-,\mathrm{dc}+}$)	775.53 pF	723.4 pF
Coil series resistance (R_s)	155.8 mΩ	341.4 mΩ
Rogowski coil loop inductance ($L_{\mathrm{rog,\,stray}}$)	399 pH	-
Sensor size	106 mm^2	-

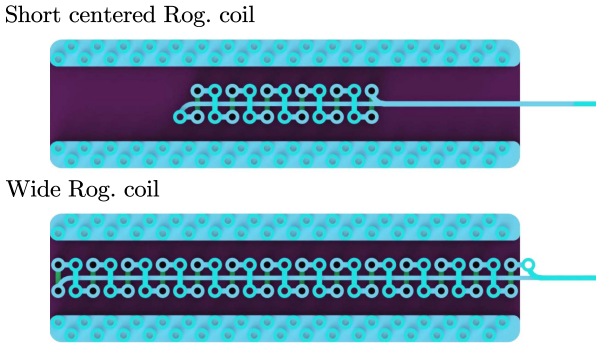
It can be observed that the resonant peak is not only influenced by the self inductance L_s and self capacitance C_s, but is also impacted by the parasitic plate capacitances $C_{\mathrm{dc}+,\mathrm{Rog.}}$ and $C_{\mathrm{dc}-,\mathrm{Rog.}}$, as well as the mutual inductance M.

V. PLANAR ROGOWSKI COIL DESIGN

Compared to a standard helical Rogowski coil, the planar Rogowski coil is open-ended. Thus, any magnetic flux density change outside the planar Rogowski coil dimensions is not measured. A helical Rogowski coil surrounds the current carrying conductor and does not face this issue. Spieler et al. [18] highlighted the considerations of the Rogowski coil planar design. However, it assessed them qualitatively. This article builds on previous findings and quantitatively evaluates their impact on the coil behavior.



(a)



(b)

Fig. 8. Impact of current crowding on the magnetic flux density distribution. (a) Magnetic flux density calculation plot for different current density distributions within a dc-busbar trace layout. (b) Top views of a short centered Rogowski coil and a wide Rogowski coil.

A. Mutual Inductance Error

Publications of planar Rogowski coils typically design the coil to be shorter than the current carrying trace [13], [14], [17]. Fig. 8 illustrates the magnetic flux density depending on the current distribution in a dc-bus, which is 30 mm wide. The top view of a short, centered, and a wide Rogowski coil is depicted. The blue curve displays the current density at a uniformly distributed current throughout the dc bus. The magnitude of the magnetic flux density remains relatively constant, with a sudden decrease at the boundaries of the dc-bus trace. Short-centered planar Rogowski coils will accurately measure the current. However,

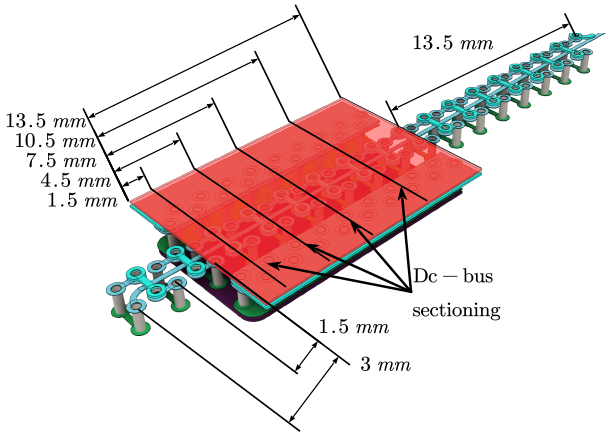


Fig. 9. Rogowski coil geometry simulated in Ansys Q3D. The DC bus is sectioned to restrict the constant DC-bus current toward the DC-bus trace edge. Multiple Rogowski coil windings are added to evaluate their impact on the mutual inductance error.

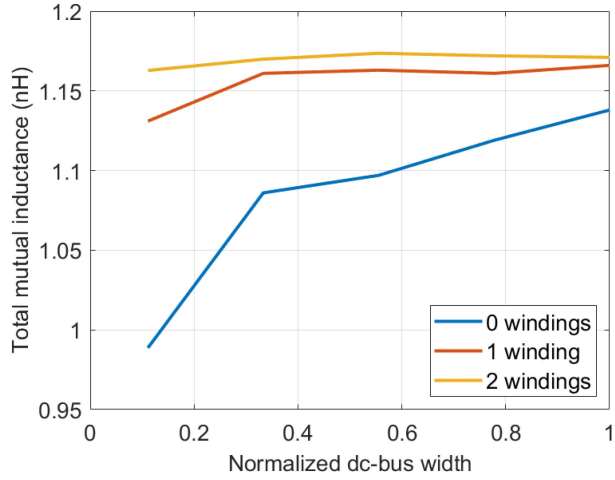


Fig. 10. Mutual inductance drop with DC-bus current crowing toward the DC-bus trace edge in dependence on added Rogowski coil windings exceeding the DC-bus width. The simulated DC-bus widths are normalized with respect to the maximum simulated DC-bus trace width of 13.5 mm.

as indicated in [20] and [21], the current density within the dc bus is not equal throughout the dc bus. Suppose that the same current accumulates in the left third of the dc-bus trace and, thus, the magnetic flux density shifts to the left third, as highlighted by the red curve. In that case, a short, planar Rogowski coil will measure the current inaccurately because the magnetic flux density change within the short planar Rogowski coil windings is small. This problem can be solved by extending the planar Rogowski coil to cover the entire width of the dc-bus trace, as shown in Fig. 8. The next section addresses how the planar Rogowski coil design can reduce the mutual inductance error due to current crowding in the dc-bus trace.

B. Mutual Inductance Error Dependence

The area beneath the flux density curves outside the Rogowski coil width in Fig. 8 equals the coil measurement error. To solve this issue, the authors recommend designing a planar Rogowski coil that exceeds the width of the dc-bus trace.

To simulate and evaluate the mutual inductance error reduction of a planar Rogowski coil, with coil windings exceeding the dc-bus width, finite-element simulations were carried out in Ansys Q3D. The three simulated designs differ in the number of Rogowski coil windings that exceed the dc-bus trace. Fig. 9 shows the different Rogowski coil design geometries used for finite-element simulations. The coil exceeds one side of the dc-bus trace by 13.5 mm in the image's top right area. Therefore, the mutual inductance error at this end of the Rogowski coil is minimized. At the other end of the coil, the number of windings that exceed the dc-bus trace width is increased stepwise from zero to two windings. The respective Rogowski coil widths that exceed the dc-bus trace are 0 mm, 1.5 mm, and 3 mm, as indicated in the bottom left of Fig. 9.

Multiple simulations are carried out with increasing current crowding toward the dc-bus edges. A constant current is constrained to a stepwise narrower dc-bus trace located at the dc-bus trace edge. The simulated dc-bus trace widths (w_{tot}) are 13.5 mm, 10.5 mm, 7.5 mm, 4.5 mm, and 1.5 mm. The resulting mutual inductance error for all simulated designs is shown in Fig. 10.

The results show a general trend for mutual inductance increase with additional windings. In addition, the mutual inductance error, caused by current crowding toward the dc-bus edge, is reduced.

The mutual inductance error is 149 pH or 13% if the Rogowski coil windings end at the dc-bus trace edge. Coils extending beyond the bus traces have a smaller mutual inductance error. The mutual inductance drop is 35 pH or 3%, and 8.2 pH or 0.72% if the coil exceeds the dc bus by one winding and two windings, respectively. Although it is unlikely that all of the dc-bus current flows through the outer section of the dc-bus trace, the simulations and comparison highlight the benefits in sensor accuracy if the planar Rogowski coil windings exceed the dc-bus trace width.

C. Current Commutation Loop Increase

The planar Rogowski coil location between the dc-link capacitor and switching half-bridge elevates the importance of reducing the sensor's impact on the current commutation loop. A higher current commutation loop increases the maximum overshoot voltage during the turn-OFF switching transient, as the following maximum MOSFET overshoot voltage equation indicates

$$V_{\text{DS,max}} = V_{\text{dc}} + L_{\text{loop}} \cdot \frac{di}{dt} \tag{14}$$

where V_{dc} is the dc-bus voltage, di/dt is the change in current during the switch transient, and L_{loop} is the current commutation loop stray inductance. It is typically the sum of all parasitic inductances within the commutation loop, as shown in the following equation:

$$L_{\text{loop}} = L_{\text{rog},s} + L_{\text{DC-link}} + L_{\text{pkg}} + L_{\text{trace}} \tag{15}$$

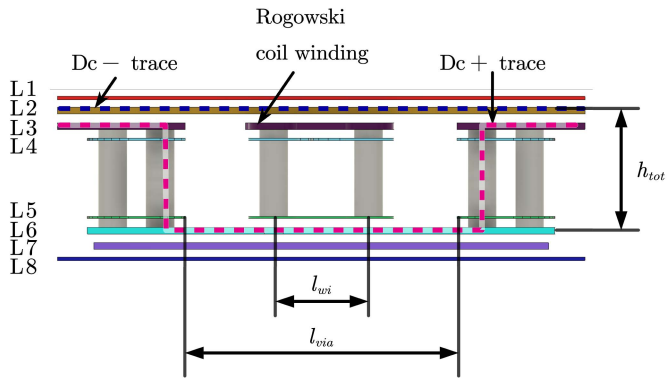


Fig. 11. Cross-sectional view of the designed Rogowski coil.

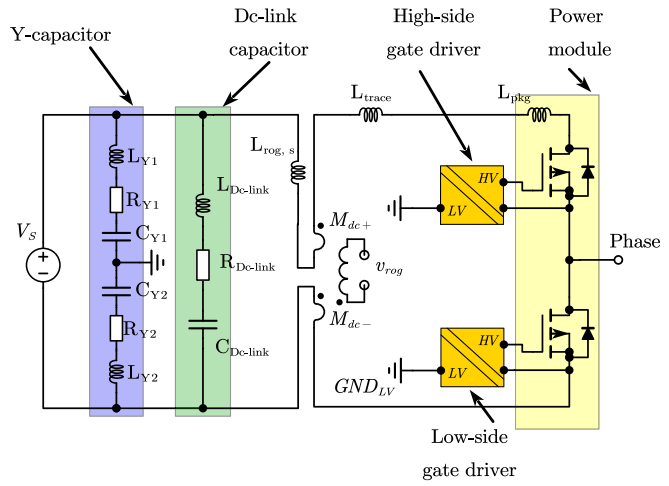


Fig. 12. Isolation architecture of the half-bridge.

where $L_{\text{DC-link}}$ is the ESL of the dc link capacitor, L_{trace} is the trace inductance, L_{pkg} is the parasitic stray inductance of the MOSFET package, $L_{\text{rog},s}$ is the introduced increase in the stray inductance of the current commutation loop due to the planar Rogowski coil. The parasitic stray inductances are highlighted in Fig. 12. An increase in the overshoot voltage could cause an increase in the field-effect transistor failure rate [22]. The geometry of the Rogowski coil mainly guides the increase in the inductance of the current commutation loop. Fig. 11 shows a cross section of the current sensor. The simplified loop inductance equation can be used to calculate the increase in stray inductance due to the planar geometry of the Rogowski coil [23]

$$L_{\text{rog},s} = \mu_0 \cdot \frac{h_{\text{tot}}}{w_{\text{tot}}} l_{\text{via}} \cdot \left(\frac{1}{1 + \dfrac{h_{\text{tot}}}{w_{\text{tot}}}} + 0.024 \right). \tag{16}$$

The added inductance can be minimized mainly by increasing the mutual inductance cancelation between the current paths dc− and dc+. As highlighted in the upper equation, four variables can be varied to decrease the current commutation loop inductance, respectively:

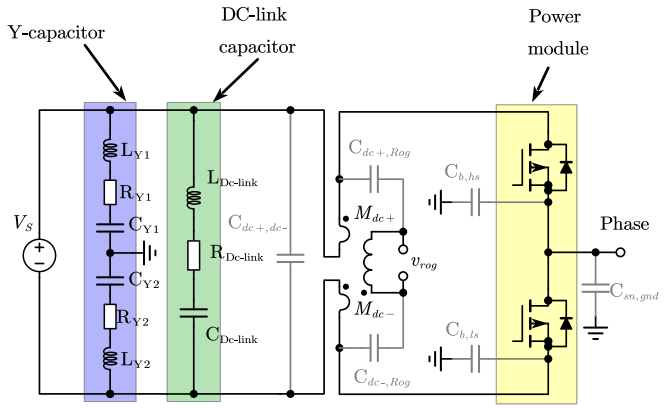


Fig. 13. Common-mode model of half-bridge.

1) reducing the clearance between the dc-bus traces and the Rogowski coil and ultimately decreasing the distance (l_{via}) between the vias creating the U-shaped dc−;
2) decreasing the coil's height and thus decreasing the space between the dc-bus traces (h_{tot});
3) decreasing the length of the coil winding (l_{wi}) to decrease (l_{via});
4) increasing the dc-bus trace width (w_{tot}). The first three approaches shrink the area between the dc-bus traces to achieve better mutual inductance cancelation.

D. Analysis of Common-Mode Noise Propagation

Due to the isolated current measurement, the Rogowski coil's application ranges from low voltage to higher voltage use cases. With the emergence of wide bandgap transistors, the switching speed increased significantly. The parasitic capacitances between the half-bridge switch node and the low voltage ground create common-mode currents as indicated as follows:

$$i_{\text{cm}} = C_{\text{cm}} \cdot \frac{dv}{dt} \tag{17}$$

where C_{cm} is the lumped common-mode capacitance between the half-bridge switch node and the low voltage ground, dv/dt is the switch node switching speed. Fig. 12 shows the isolation architecture of the half-bridge and Rogowski coil.

Contributors to the lumped common-mode capacitance in higher power applications are primarily the parasitic plate capacitance between the switch node traces and traces plus components on the low-voltage ground potential, heatsink, and the barrier capacitance of the high-side gate driver. The equivalent electric circuit is displayed in Fig. 13. The high-side gate driver barrier capacitance $C_{b,\text{hs}}$ is parallel to the capacitance between the switch node and the ground $C_{\text{sw,gnd}}$. The sum of these capacitances is the lumped common-mode capacitance C_{cm} and is the source of the common-mode noise.

The common-mode current returns from the low voltage ground through impedances to the dc-bus traces and the switch node. Due to the proximity of the planar Rogowski coil windings to the dc-bus traces, the parasitic capacitances $C_{\text{dc}-,\text{rog}}$ and $C_{\text{dc}+,\text{rog}}$ are higher compared to the helical Rogowski coils [18].

As one node of the Rogowski coil is typically referenced to the low-voltage ground potential, the capacitances provide a return path for the common-mode current. The resulting voltage drop over the Rogowski coil can cause a current measurement error. The common-mode return path is in parallel with the Y-capacitors. When the common-mode noise impedance of the Rogowski coil is increased, most of the common-mode current is bypassed through the Y-capacitors. Zhao et al. [24] outline approaches to decrease the influence of the common-mode current on the measurement of the Rogowski coil current.

First, the parasitic capacitance can be decreased by reducing the number of coil windings.

Second, the distance between the coil windings and the dc-bus traces can be increased to decrease their capacitive coupling.

Third, a low-voltage ground shielding can be added between the dc-bus trace and the coil windings. The shielding allows the common-mode current to bypass the Rogowski coil windings.

Fourth, by using a differential amplifier to carry out the signal integration, both Rogowski coil output pins see a high impedance. This reduces the magnitude of common-mode current flowing through the Rogowski coil windings.

E. Planar Rogowski Coil Design Guideline

This section outlines the high-level design steps for a planar Rogowski coil. The design flow chart is shown in Fig. 14. It aims to achieve a Rogowski coil design that meets the mutual inductance requirement while minimizing the coil's impact on the current commutation loop stray inductance. The first four processes help to design a base Rogowski coil geometry, which is adjusted in later processes to achieve the required mutual inductance. The first processes are described in detail below. Lastly, finite-element simulations can be performed to verify the mutual inductance of the Rogowski coil sensor.

1) PCB Parameters: A PCB with a minimum of four layers is required to design a planar Rogowski coil, where the dc-bus traces circumvent the coil windings. The trace layer and prepreg thickness define the Rogowski coil winding height and distance between the current carrying trace and coil. PCB parameters, such as the minimum trace thickness and via diameter, and the Rogowski coil winding structure, affect the minimum winding length ($l_{\text{wi,min}}$) and the minimum winding width ($w_{\text{wi,min}}$). The papers [9], [25], [26], [27] outline possible winding structures that can be used for the planar Rogowski coil design.

2) Minimum Winding Length: The winding length (l_{wi}) is required to calculate the mutual inductance of the Rogowski coil sensor. The minimum trace clearance, minimum via diameter, and winding geometry define the minimum winding length. The minimum winding length should be used to design the first Rogowski coil iteration.

3) Maximum Possible Number of Windings: The maximum number of windings should be used for the first Rogowski coil design iteration. The minimum winding width ($w_{\text{wi,min}}$) is used to determine the maximum number of windings of the planar Rogowski coil. The minimum winding width depends on the PCB parameters mentioned above. The maximum number of

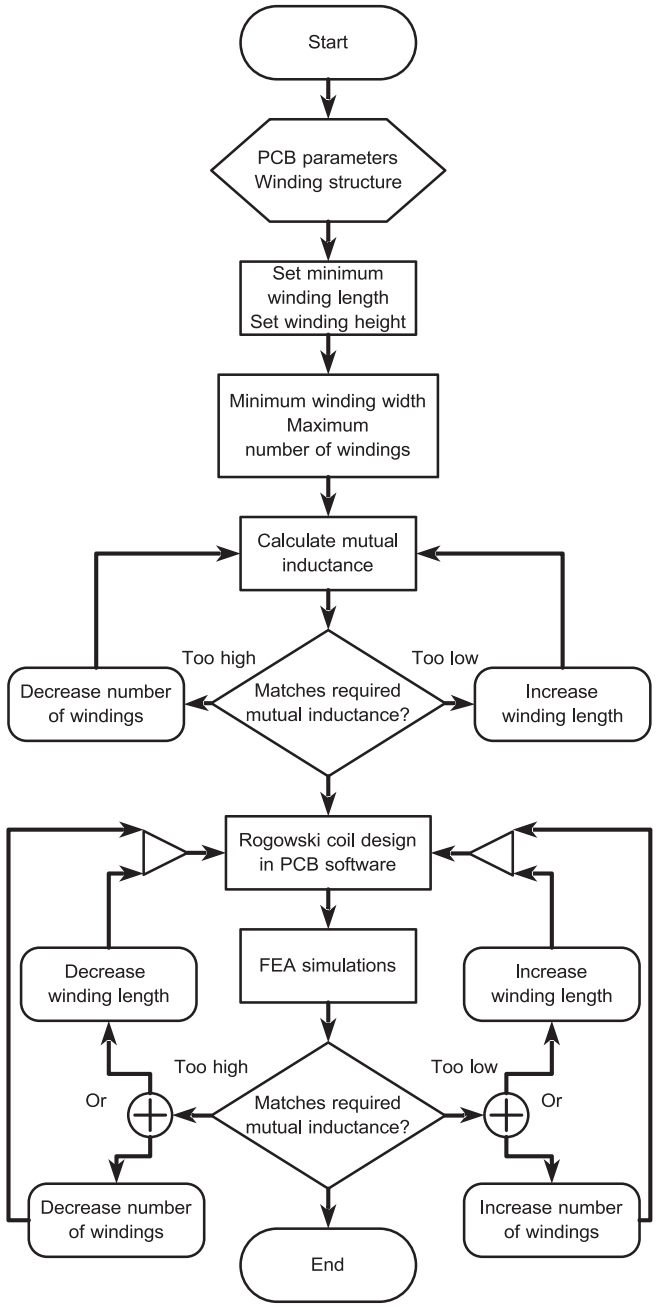


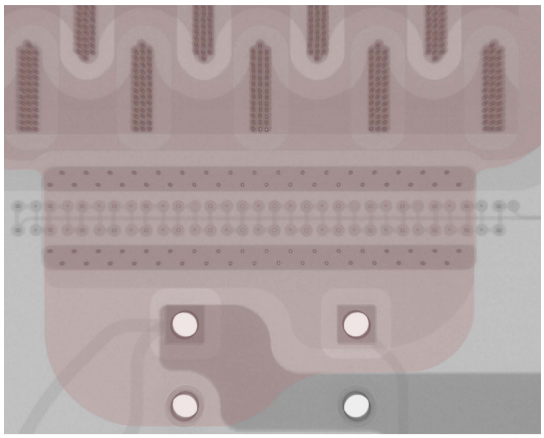
Fig. 14. Planar Rogowski coil design flow chart.

Rogowski coil windings can be calculated as follows:

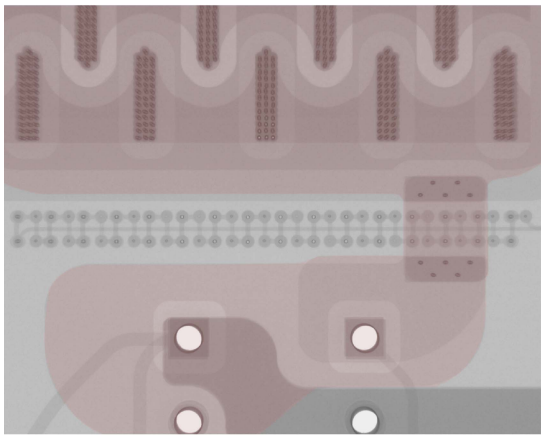
$$N_{\text{max}} = \left\lfloor \frac{w_{\text{tot}}}{w_{\text{wi,min}}} \right\rfloor + N_{\text{ex}} \tag{18}$$

where $N_{\text{ex.}}$ is the additional number of windings exceeding the dc-bus width.

4) Calculate Mutual Inductance: The total mutual inductance can be calculated based on (6) and (7). Note that the winding inductance in (6) depends on the winding location (w) along the width of the dc bus. Assuming an equal winding distribution on the dc-bus width, the winding location is based



(a)



(b)

Fig. 15. X-ray of the planar Rogowski coil PCB. (a) Highlights the wide DC-bus trace. (b) Highlights the narrow DC-bus trace.

on the winding width, the number of windings, and the spacing of the windings.

F. Rogowski Coil Prototype Design

The required mutual inductance of the Rogowski coil should be within the 1 nH range. Based on the geometry constraints mentioned in the previous section and the derived mutual inductance equation, the number of windings is chosen to be 16 with a winding spacing of 2 mm. The Rogowski coil windings exceed the dc-bus trace width on each side by 1.5 mm. The mutual inductance of the coil is calculated based on the (7). The total calculated mutual inductance is 1.113 nH.

A PCB with eight layers integrates the dc bus, decoupling capacitors, the SiC MOSFET half-bridge, gate current boosters, and the planar Rogowski coil. Layer stackup constraints result in a clearance of 140 μm between the coil and the upper dc− trace and the lower dc+ trace, respectively. The Rogowski coil return trace, as highlighted in Fig. 2, and the minimum trace clearance define the minimum winding length of 1.5 mm. The horizontal clearance between the coil winding and the dc bus is designed to comply with the IPC-2221B standard on minimum

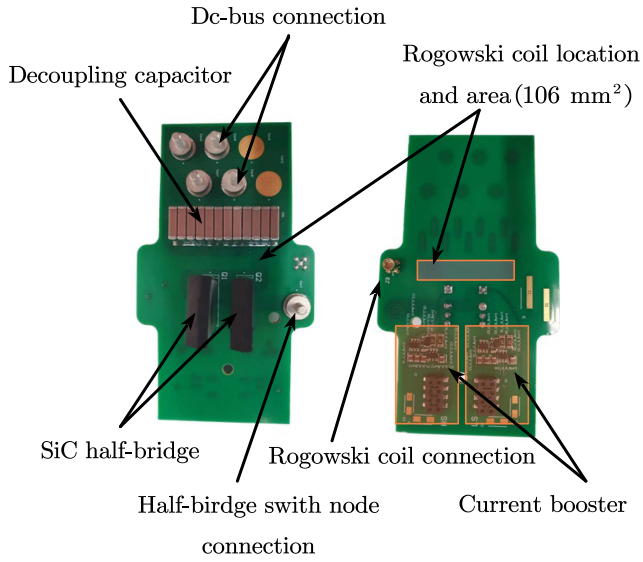


Fig. 16. SiC MOSFET half-bridge prototype with integrated planar Rogowski coil.

trace clearance. The Rogowski coil increases the dc-bus length by 3.5 mm.

Two planar Rogowski coils are designed for a 1.2 kV SiC MOSFET half-bridge application. The two designs differ in the dc-bus trace layout to evaluate the impact of current crowding on the mutual inductance error. Fig. 15 shows an x-ray image of the PCB, highlighting the planar Rogowski coil windings within the PCB. The dc-bus trace of one design is altered to artificially create a dc-bus current crowding to the edges of the planar Rogowski coil. Both designs will be later compared in switch transient current measurements.

The Rogowski coil, the decoupling capacitors, the current booster stage, and the SiC MOSFET TO-247 half-bridge are incorporated into an eight-layer PCB. Fig. 16 displays the fully assembled half-bridge. The planar Rogowski coil location is highlighted. The coil is placed between the decoupling capacitor and the half-bridge. One winding on each side of the Rogowski coil exceeds the width of the dc-bus trace.

VI. Experimental Results

A. Current Sensor Design

An analog integrator is required as the Rogowski coil output voltage represents the derivative of the dc-bus current. A reset switch is placed in parallel to the integration capacitor. The reset switch and potentiometer are required to compensate for the input voltage bias of the opamp, as the integrator's output voltage v_{out} would otherwise, over time, hit the supply rails of the opamp.

The equivalent electric circuit of the Rogowski coil based current sensor is displayed in Fig. 17. Where R_{int} is the input resistance of the integrator, C_{int} is the integration capacitance, and R_{trim} is the aforementioned potentiometer. The transfer function of the current sensor during the switching transient is based on the simplified Rogowski transfer function, as shown in

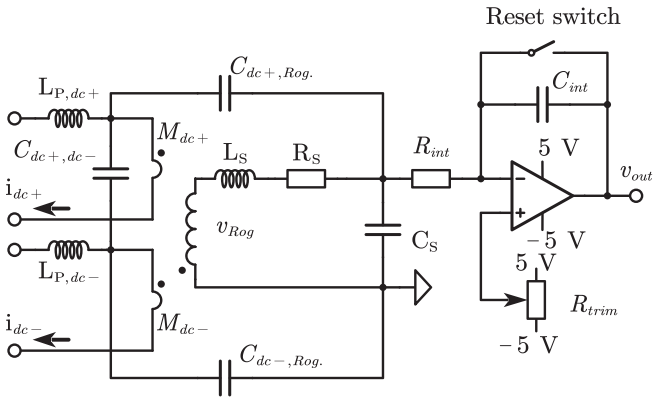


Fig. 17. Equivalent electric circuit of planar Rogowski coil.

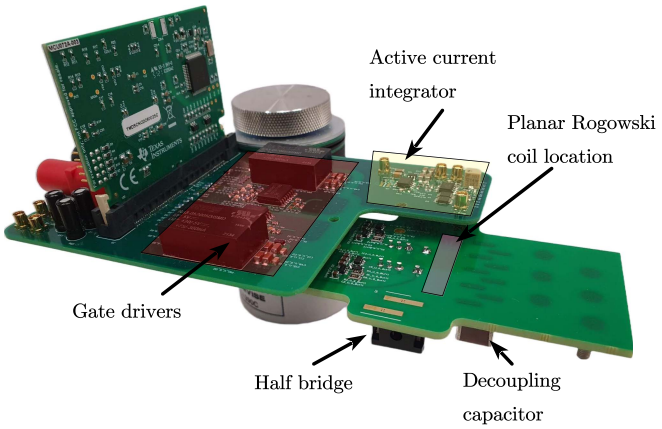


Fig. 18. Planar Rogowski coil half-bridge prototype and gate driver PCB with active current integrator circuit and digital signal processor.

(12). Thus, the transfer function is as follows:

$$\frac{v_{\text{out}}}{i_{\text{dc}}} = \frac{M\left(1 - C_e M s^2\right)}{s^2(L_s(C_e + C_s) - 2C_e M) + s(R_s(C_e + C_s)) + 1} \cdot \frac{1}{C_{\text{int}} \cdot R_{\text{int}}}. \tag{19}$$

The assembled prototype current sensor is shown in Fig. 18. The digital signal processor generates the pulse width modulated signal. The controller also resets the integrator circuit prior to each switching transient.

B. Parasitic Value Extraction

Finite-element simulations are performed in Ansys Q3D to determine the Rogowski coil parasitic parameters. The simulation results are listed in Table I. The simulation results are compared with the measurement results. The capacitance between the coil and the dc+ trace ($C_{\text{dc+,Rog}}$), the parasitic capacitance of the coil to the dc− trace ($C_{\text{dc−,Rog}}$), and the parasitic capacitance of the dc bus ($C_{\text{dc−,dc+}}$), are measured with an impedance analyzer (Keysight, E4990A). The self-inductance

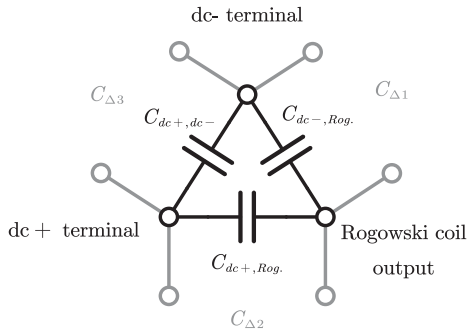


Fig. 19. Equivalent parasitic capacitor delta connection.

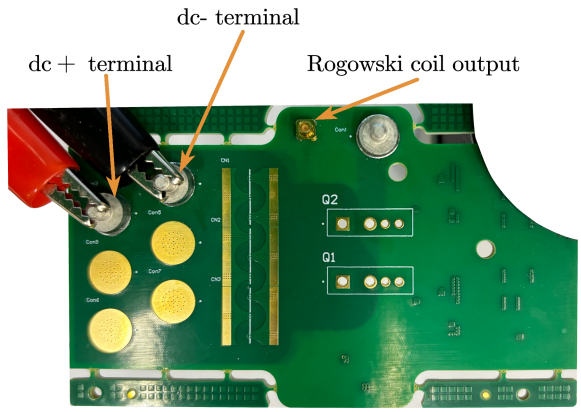


Fig. 20. Parasitic capacitance measurement setup.

of the Rogowski coil (L_S), the series resistance of the coil (R_S), the coil's parasitic capacitance (C_S), and the Rogowski coil's transfer function are extracted with a network analyzer (Keysight, E5061B).

1) Parasitic Plate Capacitance Extraction: The impedance analyzer measures the effective capacitances between the power terminals and the Rogowski coil connector. Fig. 17 can be simplified to show the delta connection of the measured parasitic capacitances. The simplified equivalent electric circuit is displayed in Fig. 19. The measurement setup and connections are displayed in Fig. 20. Measurement cables are twisted. The open-circuit parasitic capacitance ($C_{p,c}$) of the measurement cable is 15.3 pF and is in parallel to the measured delta connection capacitance. The capacitance $C_{\Delta 1}$ is measured between the Rogowski coil output pin and the dc− power terminal. The capacitance $C_{\Delta 2}$ is measured between the Rogowski coil output pin and the dc+ power terminal. $C_{\Delta 3}$ is measured between the dc-bus power terminals. Based on the three measurements, the three unknown capacitances ($C_{\text{dc+,Rog}}$, $C_{\text{dc−,Rog}}$, $C_{\text{dc+,dc−}}$) can be calculated. The measured capacitances, $C_{\Delta 1}$, $C_{\Delta 2}$, and $C_{\Delta 3}$ are 48.5 pF, 48.5 pF, and 765.3 pF, respectively. Based on the equivalent electric circuit in Fig. 19, the measured delta capacitances are expressions of the unknown parasitic capacitances ($C_{\text{dc+,Rog}}$, $C_{\text{dc−,Rog}}$, $C_{\text{dc+,dc−}}$)

$$C_{\Delta 1} = C_{\text{dc−,Rog.}} + \frac{C_{\text{dc+,dc−}} \cdot C_{\text{dc+,Rog.}}}{C_{\text{dc+,dc−}} + C_{\text{dc+,Rog.}}} + C_{p,c} \tag{20}$$

Fig. 21. Test setup to measure the Rogowski coil transfer function. The Rogowski coil DC bus is connected to port one. The output is connected to port two. To measure the output impedance of the planar Rogowski coil, the MMCX cable was removed.

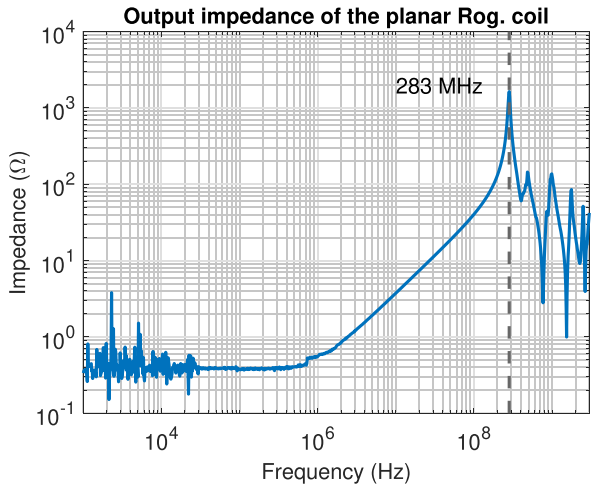


Fig. 22. Output impedance plot of the planar Rogowski coil. The first resonant point is at 283 MHz.

$$C_{\Delta 2} = C_{\mathrm{dc+,Rog.}} + \frac{C_{\mathrm{dc+,dc-}} \cdot C_{\mathrm{dc-,Rog.}}}{C_{\mathrm{dc+,dc-}} + C_{\mathrm{dc-,Rog.}}} + C_{p,c} \tag{21}$$

$$C_{\Delta 3} = C_{\mathrm{dc-,dc+}} + \frac{C_{\mathrm{dc-,Rog.}} \cdot C_{\mathrm{dc+,Rog.}}}{C_{\mathrm{dc-,Rog.}} + C_{\mathrm{dc+,Rog.}}} + C_{p,c}. \tag{22}$$

The three equations can be solved for unknown capacitances: $C_{\mathrm{dc+,Rog}}$, $C_{\mathrm{dc-,Rog}}$, and $C_{\mathrm{dc+,dc-}}$. The resulting values are: 16.5 pF, 14.9 pF, and 723.4 pF, respectively. The results are summarized in Table I. The maximum percentile deviation between the measured and simulated values is 24.9%.

2) Coil Parasitics: A network analyzer, with a bandwidth of 3 GHz, is used to measure the Rogowski coil parasitics. The network analyzer is directly connected to the planar Rogowski coil via the MMCX connector for an accurate impedance measurement. The test setup is depicted in Fig. 21. The series resistance R_S, the coil's self-inductance L_S, and the Rogowski coil output impedance are measured. The results are listed in Table I. The series resistance is a factor of 2.18 greater than the simulated resistance value. The measured self-inductance is well matched to the simulated coil self-inductance. The error between measurement and simulation is 4.55 nH or 7.3%. The measured output impedance is plotted in Fig. 22. Based on the resonant point and the self-inductance, the self-capacitance of the Rogowski coil can be calculated. The capacitance is 5.5 pF.

3) Rogowski Coil Transfer Function: The network analyzer is used to measure the transfer function of the Rogowski coil. Fig. 21 shows the measurement setup to measure the scattering parameters (s-parameters) of the two-port system. Based on [28], the scattering parameters are transformed into the impedance parameters (Z-parameters). The Z_{21} parameter equals the impedance from the input current to the output voltage, which equals the Rogowski coil transfer function. The measured Rogowski coil transfer function and the calculated second-order transfer function are shown in Fig. 23.

The first small resonance at 69 MHz is caused by the MMCX measurement connector of the measurement setup. The major resonance peak at 185 MHz is equal to the maximum bandwidth of the planar Rogowski coil. The resonant peak matches the calculated resonant frequency, see (13). The good overlap between the measured transfer function and the derived transfer function until the first resonance peak highlights the accuracy of the derived transfer function.

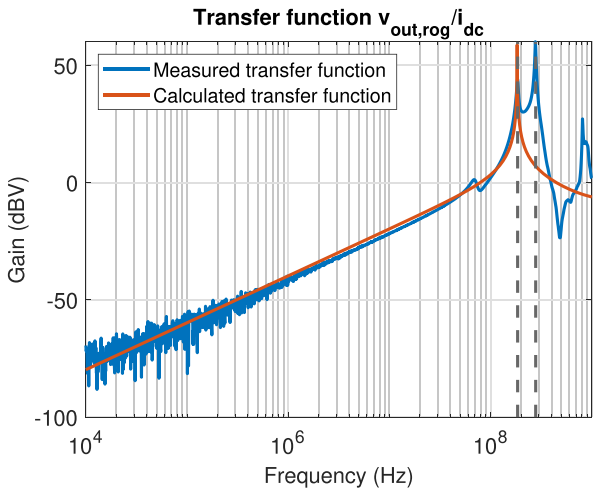


Fig. 23. Measured transfer function gain of the planar Rogowski coil. The sensor bandwidth is 185 MHz.

C. Double-Pulse Tests

Double-pulse tests are performed to compare the simulated mutual inductance and the resulting gain with the measured Rogowski coil gain. In addition, the switching transients allow for the comparison of the planar Rogowski coil sensor with the commercial Rogwoski coil CWT Ultra Mini. Lastly, the impact of current crowding toward the dc-bus trace edge on the current measurement accuracy is evaluated.

The double-pulse tests are carried out at a dc-bus voltage of 600 V and a drain current of 50 A. A lower gate resistance is

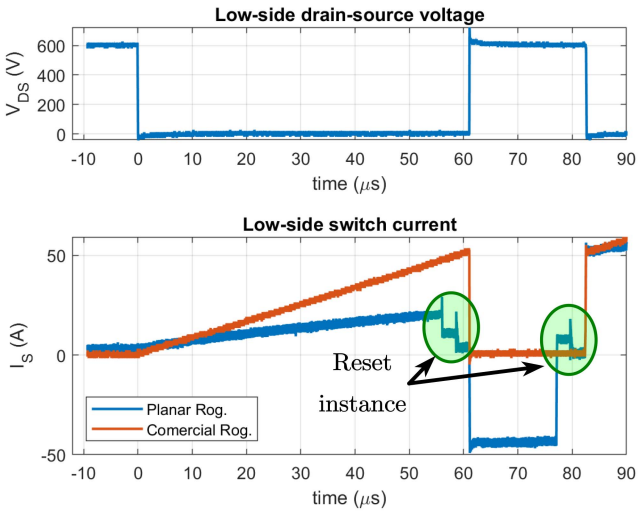


Fig. 24. Double-pulse waveform. The reset instances are highlighted.

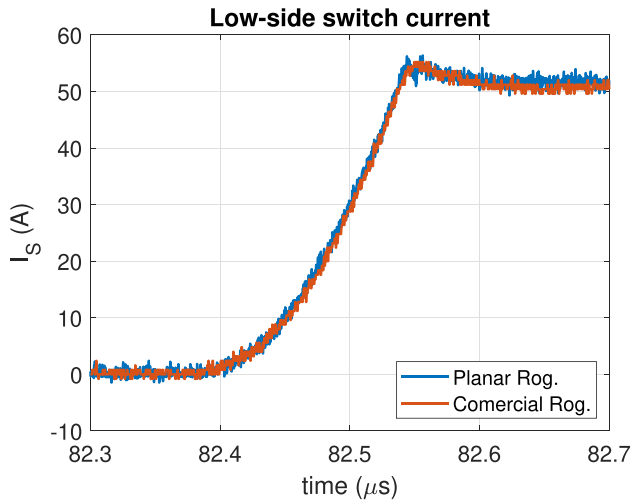


Fig. 25. Zoomed in turn-ON switching transient current comparison.

selected for the MOSFET turn-OFF switch transient. This allows for a sensor comparison at different di/dt.

The complete double-pulse waveform is shown in Fig. 24. The upper plot shows the drain-source voltage of the low-side SiC-MOSFET. The lower plot compares the output of the planar Rogowski current sensor with a commercial Rogowski coil. During the time period from 0 to 60 μs, the load inductor is charged. Equation (1) can help explain the lower current slope of the planar Rogowski coil compared to the commercial Rogowski coil. As no current flows through the dc+ trace, the gain of the current sensor is reduced, and the current slope is smaller.

The integration capacitor is discharged through the reset switch before the first two switching transients. Thus, the switching transients are always referenced to 0 V. Figs. 25 and 26 depict the zoomed-in turn-ON and turn-OFF switching transient waveforms, respectively. For the turn-OFF switching transient waveform, the planar Rogowski coil current is offset by 52 A

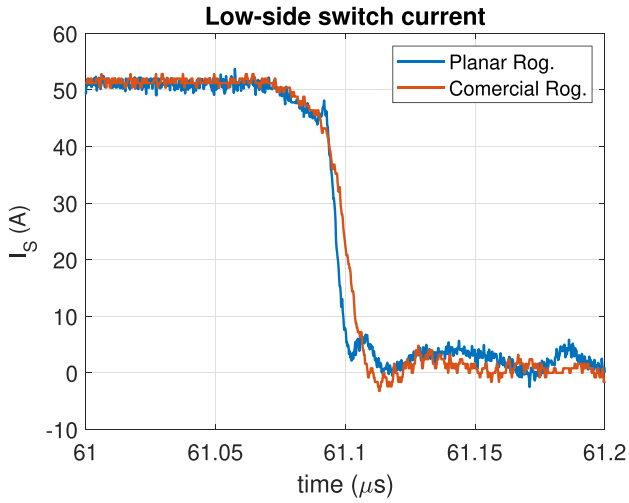


Fig. 26. Zoomed in turn-OFF switching transient current comparison.

for easier comparison between the two current measurements. The attenuation of the planar Rogowski coil current sensor is selected to match the commercial Rogowski coil. The resulting sensitivity of the planar Rogowski coil is 54.3 mV/A. Based on (19) and the component values of the integration resistance R_{int} and capacitance C_{int}, the total mutual inductance of the planar Rogowski coil can be calculated. The measured total mutual inductance is 1.08 nH, which is a 6% error compared to the simulated total mutual inductance.

The planar Rogowski and commercial Rogowski coil waveforms match nicely during the turn-ON switching transient. The amplitude of both measurements is equal. The measured di/di is 0.41 A/ns.

During the turn-OFF switching transient, the amplitude is the same for both Rogowski coils. However, the planar Rogowski coil has a steeper current slope of -4.84 A/ns, compared to the commercial Rogowski coil with a current slope of -2.44 A/ns. The maximum bandwidth of both current sensors can explain the difference in the current slope. The planar Rogowski coil sensor bandwidth is limited by the op amp's bandwidth to 120 MHz, whereas the commercial Rogowski coil has a maximum bandwidth of 30 MHz. The higher sensor bandwidth allows one to measure steeper current slopes.

D. Current Crowding Measurement

The two dc-bus trace structures, as shown in Fig. 15, are tested to evaluate the effectiveness of a planar Rogowski coil extending beyond the width of the dc bus in reducing the mutual inductance error due to current crowding within the dc bus. One dc bus is narrowed and emulates current crowding toward the dc-bus trace edge. For comparison purposes, the two different PCBs were tested at the same dc-bus voltage of 600 V and a drain current of 50 A. The measurement results are combined and plotted in Fig. 27. A moving average is applied to slightly reduce the noise level and highlight the amplitudes of the waveforms. It can be observed that the switch transient current waveforms

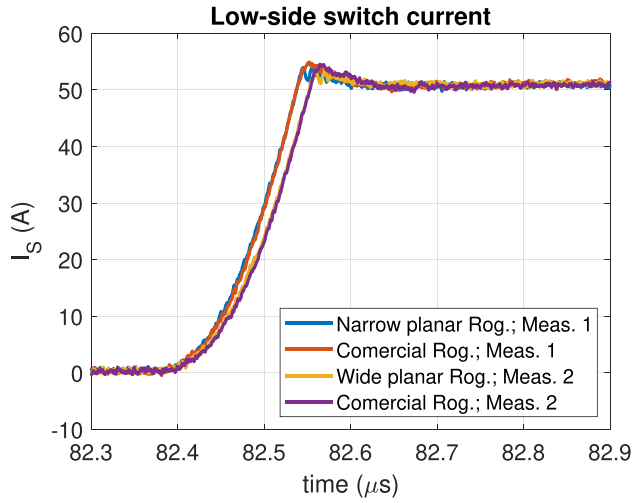


Fig. 27. Zoomed in turn-ON switching transient current. The first measurement was conducted on the narrow DC-bus trace PCB. The second measurement is conducted on the wide DC-bus trace PCB.

differ for the two PCBs. This is likely due to threshold voltage variations in the two half-bridges. The current amplitudes of both dc-bus structures are similar, highlighting the improvement of coil windings exceeding the dc bus in the reduction of mutual inductance error for current crowding toward the dc-bus trace edges.

VII. Conclusion

Planar Rogowski coil design considerations are qualitatively explored. The derived total mutual inductance equation accurately equates the mutual inductance between the dc-bus traces and the planar Rogowski coil as a function of the sensor design parameters. The Rogowski coil transfer function accurately equates the Rogowski coil gain to the first resonant peak. Design considerations related to a nonuniform current density distribution in the dc-bus traces are evaluated, and the effectiveness of Rogowski coil windings exceeding the dc-bus trace width on the mutual inductance error is shown. A planar Rogowski coil was designed with a combined mutual inductance of 1.08 nH, a bandwidth of up to 185 MHz, and a compact sensor size of 106 mm^2.

Two PCBs with different dc-bus structures were compared to evaluate the mutual inductance error caused by current crowding within the dc bus. Measurement results indicate little error if the coil windings exceed the dc-bus trace.

Finally, the performance of switching transient current measurement was assessed. Double pulse measurements were conducted at 600 V and with a drain current of 50 A. The designed planar Rogowski coil accurately measures the turn-ON and turn-OFF switch transient current amplitude. The planar Rogowski coil exhibits a higher bandwidth compared to its commercial counterpart, leading to the possibility of measuring steeper switching transient current slopes during high-speed switching.

Appendix A
Mutual Inductance Error Between Calculation and Simulation

TABLE II
Mutual Inductance Error Between Equation and FEM Simulation Based on Distance Between Current Carrying Traces

Distance between traces (mm)	Sim. M_{top} (nH)	Sim. M_{bot} (nH)	Sim. M_{tot} (nH)	Calc. M_{tot} (nH)	Error (%)
1.5	0.513	0.501	1.014	1.119	10.4
2	0.507	0.505	1.012	1.098	8.5
2.5	0.485	0.500	0.985	1.079	9.5
3	0.471	0.485	0.956	1.062	11.1
5	0.441	0.440	0.881	1.000	12.7

The coil winding parameters are constant.

TABLE III
Mutual Inductance Error Between Equation and FEM Simulation Based on Different Coil Winding Heights

Winding height (mm)	Sim. M_{top} (nH)	Sim. M_{bot} (nH)	Sim. M_{tot} (nH)	Calc. M_{tot} (nH)	Error (%)
0.5	0.325	0.273	0.598	0.672	12.4
1	0.516	0.511	1.027	1.113	8.4
2	0.845	1.000	1.845	1.955	6.0
3	1.148	1.521	2.669	2.750	3
5	1.611	2.585	4.196	4.214	0.4

TABLE IV
Mutual Inductance Error Between Equation and FEM Simulation Based on Different Winding Length

Winding length (mm)	Sim. M_{top} (nH)	Sim. M_{bot} (nH)	Sim. M_{tot} (nH)	Calc. M_{tot} (nH)	Error (%)
1.5	0.615	0.589	1.204	1.285	6.7
2	0.826	0.788	1.614	1.714	6.2
2.5	1.042	0.995	2.038	2.142	5.1
3	1.283	1.196	2.479	2.570	3.7
5	2.449	1.797	4.246	4.284	0.9

TABLE V
Mutual Inductance Error Between Equation and FEM Simulation Based on Number of Windings

Number of windings	Sim. M_{top} (nH)	Sim. M_{bot} (nH)	Sim. M_{tot} (nH)	Calc. M_{tot} (nH)	Error (%)
8	0.314	0.293	0.607	0.588	3.1
10	0.395	0.372	0.767	0.766	0.1
12	0.474	0.438	0.912	0.942	0.3
14	0.533	0.484	1.017	1.115	9.6
16	0.598	0.542	1.140	1.285	12.7

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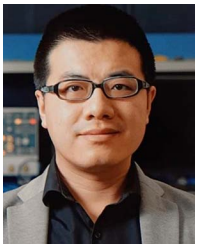

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