An Optimized DPWM With Reduced Leakage Current for Three-Phase Three-Level Inverters With Unbalanced Neutral-Point Voltage

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***Abstract*—Leakage current causes alternating output current distortion and severe electromagnetic interference in photovoltaic generation systems. This article proposes an optimized discontinuous pulsewidth modulation (O-DPWM) method to reduce leakage current in three-phase three-level inverters under various neutral point (NP) voltage conditions. First, the relationship between common-mode voltage (CMV) and leakage current is revealed. Then, the CMV characteristics of space vectors under different NP conditions are analyzed, and the switching-state sequence is optimized to minimize CMV magnitude, thereby reducing leakage current. Furthermore, by clamping the switching state of one phase in each switching cycle, switching losses are also reduced. Finally, a 3-kW grid-tied inverter prototype is built, and experimental results demonstrate that the proposed O-DPWM scheme achieves lower leakage current and higher efficiency compared to existing reduction schemes across different NP voltage conditions.**

***Index Terms*—Common-mode voltage, discontinuous pulsewidth modulation (PWM), leakage current, neutral point (NP) voltage imbalance, three-phase three-level inverters.**

I. Introduction

THREE-LEVEL inverters are widely used in photovoltaic (PV) generation systems for their low voltage stress and low current ripple [1], [2], [3], [4]. However, due to the parasitic capacitor of PV panels, high-frequency variation of the common-mode voltage (CMV) causes severe leakage current, which distorts the alternating output current and causes severe electromagnetic interference [5], [6], [7]. Consequently, the VDE 0126-1-1 standard mandates a shutdown within 0.3 s if the leakage current exceeds 300 mA [8].

Improving the output filter design can effectively reduce the leakage current. In [9], the star point of three-phase capacitors in an *RLC* filter was connected with the neutral point (NP) of the dc-link capacitors, and the leakage current was reduced by using an optimized parameter design. Chen et al. [10] combined the *RLC* filter and coupled common-mode transformer to achieve higher impedance in the leakage current path, and the leakage current is suppressed. In [11], damping resistors were integrated with a conventional *LCL* filter. By designing the value of damping resistors, the leakage current was reduced while the system stability was not affected. In [12], an *LCCL* filter was proposed by splitting filter capacitors into two parts. The star point of the smaller one is connected to the NP of the dc-link capacitors. It offers a low-impedance path to avoid leakage currents flowing through the utility grid. Besides, the high-order filter can also lower the leakage current [13]. However, modifying the passive output filter increases hardware costs and power loss.

Using switching states with lower CMV is a more cost-effective way to reduce the leakage current. Many continuous pulsewidth modulation (CPWM) schemes with low leakage current were proposed. In [14], zero vectors were removed, and other vectors were divided into two categories according to their CMV values. In each switching period, the reference vector was synthesized by three vectors from the same category. Thus, the CMV variation was reduced. The leakage current can also be reduced by using active zero vectors, which are formed by using two opposite vectors with the same dwelling duty [15]. In [16], the CMV reduction was achieved by configuring the comparing logic of modulation and carrier signals of conventional seven-segment space-vector PWM. The effect of dead time was further considered in [17] to avoid the CMV spike during the dead time. In [18], the large, medium, and small vectors are combined to clamp the CMV at different constant levels. The CMV can be controlled at zero by using only medium vectors and one specific zero vector [19], [20]. Constant CMV can also be achieved by injecting a dedicated zero-sequence component (ZSC) and using a pair of opposite carrier signals [21], [22], [23]. However, these methods cause one phase's switching state to vary twice within a switching period, leading to high switching loss. In [24], small

Received 7 April 2024; revised 13 July 2024; accepted 22 August 2024. Date of publication 26 August 2024; date of current version 7 October 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 52322705, in part by the Natural Science Foundation of Jiangsu Province under Grant BK20230037, and in part by the Special Fund of Jiangsu Province for the Transformation of Scientific and Technological Achievements under Grant BA2023108. Recommended for publication by Associate Editor E. Babaei. *(Corresponding author: Li Zhang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3450409.

Digital Object Identifier 10.1109/TPEL.2024.3450409

vectors were not adopted, and large vectors, medium vectors, and a specific zero vector were employed. In [25], the CMV of small vectors was further analyzed, and six high-CMV small vectors were unused. Thus, leakage current and switching times are both reduced. However, the CPWM scheme leads to high switching loss, degrading the efficiency.

Compared with CPWM schemes, discontinuous PWM (DPWM) schemes reduce the switching times by 1/3, which improves the inverter efficiency [26]. By configuring the clamping regions in a fundamental period, DPWM schemes could reduce switching loss by 1/2 at a certain range of power factor [27], [28]. However, conventional DPWM schemes do not deal with the leakage current issue. Many improved DPWM schemes were proposed to lower the leakage current. In [29], three long vectors closest to the reference vector were utilized to synthesize the reference vector, by which one phase switching state was clamped. Thus, the CMV was reduced. However, its low CMV characteristic can only be achieved in regions with a high modulation index (MI). This disadvantage can be solved by employing a CPWM scheme in regions with low MIs [30]. Hybrid utilization of DPWM and CPWM was also reported in [31] and [32] to achieve low CMV at different MIs. However, the CPWM scheme increases switching loss. Xu et al. [33] proposed the low-CMV discontinuous switching-state sequences, which can be used in full MI ranges. A 240-degree clamped DPWM was proposed in [34]. It only uses two switching states in each switching period to reduce CMV and switching loss. In [35], the CMV was reduced by removing high-CMV small vectors in the conventional space-vector PWM scheme. Since one of the redundant small vectors is no longer used, the switching state of one phase is clamped during a switching period. In [36] and [37], different clamping modes with low CMV magnitude were investigated based on the space-vector diagram formed by low-CMV vectors. As a result, both the low CMV and high efficiency were achieved. However, when the neutral-point (NP) voltage is unbalanced, the position and CMV of each vector are varied accordingly, which is not considered by the above schemes. As a result, these schemes cannot achieve CMV reduction and lead to alternating output current distortion under unbalanced NP voltage conditions.

In some PV generation systems, as reported in [2] and [3], the upper and lower capacitors could be connected to different dc sources, as shown in Fig. 1, leading to an unbalanced NP voltage. The previous works, which deal with the unbalanced NP voltage, mainly focus on eliminating the alternating output current distortion caused by the unbalanced NP voltage [38], [39]. Modifying the carrier signals, modifying the modulation signals, and employing dynamic space vectors are all effective ways to avoid alternating output current distortion. However, only a few pieces of literature further considered the CMV reduction. In [40], the relationship between NP voltage and the CMV of each switching state was analyzed, achieving CMV reduction through opposite carrier signals and limiting injected ZSCs within variable upper and lower boundaries. However, this remains a CPWM scheme, resulting in high switching loss.

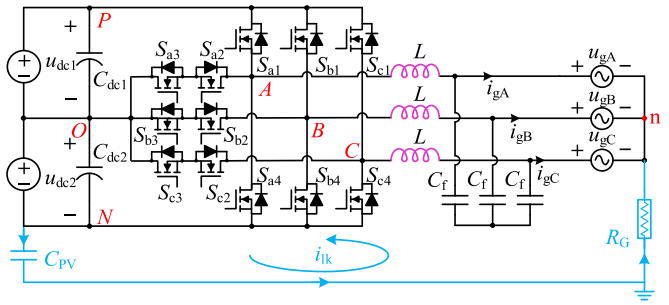

Fig. 1. Topology of T-type three-level inverter with dual DC input ports.

TABLE I
SUMMARIZATION OF THE EXISTING MODULATION SCHEMES

Reference	Leakage Current Reduction	Operating with unbalanced NP voltage	PWM type		Applicable topology	
			CPWM	DPWM	Two-level	Three-level
[14]	√		√		√	
[19]	√		√			√
[25]	√		√			√
[27]				√	√	
[29]	√			√	√	
[36]	√			√		√
[38]		√		√		√
[39]		√		√		√
[40]	√	√	√			√

Table I summarizes significant existing modulation schemes reviewed above, highlighting the absence of a DPWM scheme that reduces leakage current under unbalanced NP voltages. Thus, previous works fail to achieve both low leakage current and low switching loss under unbalanced NP voltage conditions.

This article proposes an optimized DPWM (O-DPWM) scheme to reduce the leakage current for three-level inverters under different NP voltage conditions. The clamping modes of each subsector are composed of vectors with low CMV variation, and the space-vector diagram is dynamically adjusted according to the NP voltage. As a result, both the low leakage current and high efficiency are achieved under unbalanced NP voltage conditions. The rest of this article is organized as follows. In Section II, the relationship between the leakage current and CMV is analyzed. Then, the implementation of the proposed O-DPWM scheme is presented in Section III. Simulation results and comparative analysis are given as well. In Section IV, a 3-kW grid-tied inverter prototype was built to conduct experiments. Finally, Section V concludes this article.

II. ANALYSIS OF THE LEAKAGE CURRENT

A simplified circuit model, which was reported in [41], is adopted to analyze the leakage current, as shown in Fig. 2. C_{PV} represents the parasitic capacitor of PV panels. R_G is the parasitic resistance of the common-mode circuit. i_{lk} is the leakage current. u_{CM} is the CMV, as expressed in (1). u_{XO} represents the voltage between terminal X and terminal O, as

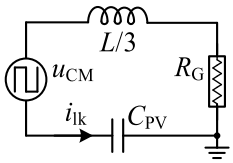

Fig. 2. Circuit model of leakage current path.

depicted in Fig. 1. (X = A, B, C)

$$u_{CM} = (u_{AO} + u_{BO} + u_{CO})/3. \tag{1}$$

According to the study reported in [42], since u_{CM} is a periodic function in terms of both fundamental frequency and switching frequency, it can be decomposed by using double Fourier integral analysis, as shown in (2). f_g is the fundamental frequency of the utility grid voltage. f_s is the switching frequency. Therefore, the spectrum of u_{CM} consists of harmonics at the integral multiples and its sidebands of the switching frequency

$$u_{CM} = \sum_{k=0}^{\infty} \sum_{l=-\infty}^{\infty} U_{CM}(k,l) \cos\left[2\pi\left(kf_s + lf_g\right)t\right],$$
$$l = \pm 3p, p \in \mathbf{N}. \tag{2}$$

Thus, from Fig. 2, the root-mean-square (rms) value of the harmonic component of i_{lk} at the frequency of $(kf_s + lf_g)$ can be calculated by (3). Furthermore, the rms value of i_{lk} can be calculated by (4)

$$I_{lk}(k,l) = \frac{U_{CM}(k,l)}{\sqrt{2}} \times \left| \frac{1}{\frac{1}{\mathrm{j}\cdot 2\pi(kf_s+lf_g)C_{PV}} + \mathrm{j}\cdot 2\pi\left(kf_s + lf_g\right)\frac{L}{3} + R_G} \right| \tag{3}$$

$$I_{lk} = \sum_{k=0}^{\infty} \sum_{l=-\infty}^{\infty} \sqrt{I_{lk}^2(k,l)},\ l = \pm 3p, p \in \mathbf{N}. \tag{4}$$

As a result, reducing $U_{CM}(k,l)$, the magnitude of u_{CM} at different frequencies can lower the leakage current.

III. Proposed Optimized DPWM Scheme

In this section, an O-DPWM scheme is proposed to achieve low leakage current and low switching loss.

A. Switching-State Sequence of the Proposed O-DPWM Scheme

To avoid alternating output current distortion, the space vector diagram should be regulated in accordance with the NP voltage [38], as shown in Fig. 3, where u_{dc1} and u_{dc2} represent the upper and lower capacitor voltage, respectively. Assuming that the space vector diagram is normalized, the radius of its inscribed circle is 1. The NP voltage imbalance degree is defined as (5), and u_{dc} is equal to the sum of u_{dc1} and u_{dc2}. Then, vector $\boldsymbol{V}_{[\boldsymbol{S_A},\boldsymbol{S_B},\boldsymbol{S_C}]}$ can be determined by (6) shown at the bottom of the next page

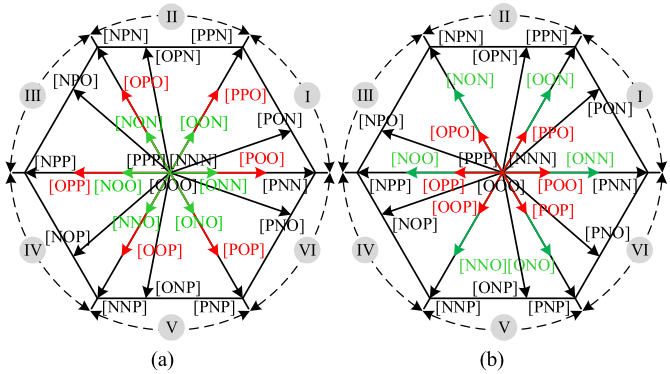

Fig. 3. Space-vector diagram under unbalanced NP voltage conditions. (a) $u_{dc1} > u_{dc2}$. (b) $u_{dc1} < u_{dc2}$.

TABLE II
Common-Mode Voltage of Different Vectors

Vector type		Vectors	u_{CM}
Zero vector	Type-I	[OOO]	0
	Type-II	[PPP]	u_{dc1}
	Type-III	[NNN]	$-u_{dc2}$
Small vector	Type-I	[POO] [OPO] [OOP]	$u_{dc1}/3$
	Type-II	[OON] [NOO] [ONO]	$-u_{dc2}/3$
	Type-III	[PPO] [OPP] [POP]	$2u_{dc1}/3$
	Type-IV	[NNO] [ONN] [NON]	$-2u_{dc2}/3$
Medium vector		[PON] [OPN] [NPO] [NOP] [PNO] [ONP]	$(u_{dc1}-u_{dc2})/3$
Large vector	Type-I	[PPN] [NPP] [PNP]	$(2u_{dc1}-u_{dc2})/3$
	Type-II	[PNN] [NPN] [NNP]	$(u_{dc1}-2u_{dc2})/3$

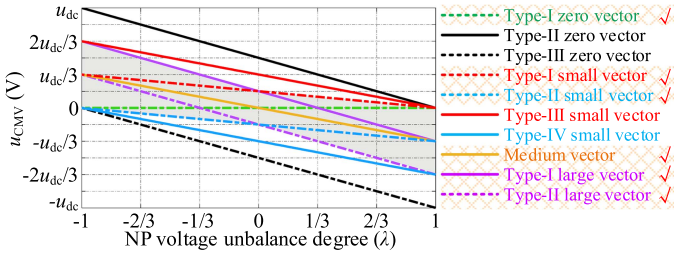

Fig. 4. Relationship between the NP voltage and the u_{CM} with different vectors.

$$\lambda = (u_{dc2} - u_{dc1})/u_{dc} \tag{5}$$

The u_{CM} of different vectors is listed in Table II. According to their u_{CM}, vectors are divided into different types. The relationship between the NP voltage and the u_{CM} of different vectors is shown in Fig. 4.

From Fig. 4, the u_{CM} of different vectors varies with the NP voltage. Thus, only the vector with low CMV magnitude under different NP voltage conditions can be utilized.

First, the used vectors should be able to synthesize the reference vector when it is located at the outer hexagon formed by six large vectors. Thus, large vectors should be used in subsectors 5 and 6. Then, to reduce the CMV magnitude the CMV of the other used vectors should be close to that of large vectors. From

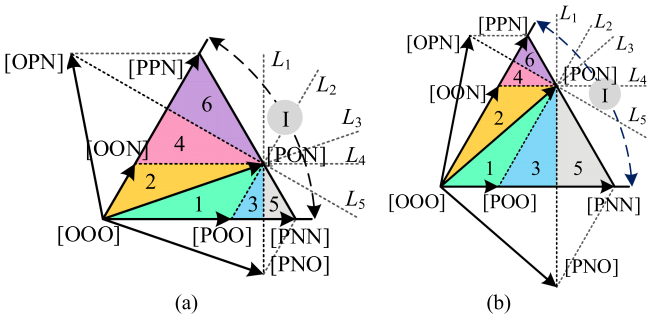

Fig. 5. Space-vector diagram of Section I by using the proposed O-DPWM scheme under unbalanced NP voltage conditions. (a) $u_{\mathrm{dc1}} > u_{\mathrm{dc2}}$. (b) $u_{\mathrm{dc1}} < u_{\mathrm{dc2}}$.

TABLE III
SWITCHING-STATE SEQUENCES OF THE PROPOSED O-DPWM

Sub-sector	Switching-state sequence				
	V_1	V_2	V_3	V_2	V_1
1	[PON]	[POO]	[OOO]	[POO]	[PON]
	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$u_{\mathrm{dc1}}/3$	0	$u_{\mathrm{dc1}}/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$
2	[PON]	[OON]	[OOO]	[OON]	[PON]
	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$-u_{\mathrm{dc2}}/3$	0	$-u_{\mathrm{dc2}}/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$
3	[PON]	[POO]	[PNO]	[POO]	[PON]
	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$u_{\mathrm{dc1}}/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$u_{\mathrm{dc1}}/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$
4	[PON]	[OON]	[OPN]	[OON]	[PON]
	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$-u_{\mathrm{dc2}}/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$-u_{\mathrm{dc2}}/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$
5	[PON]	[PNN]	[PNO]	[PNN]	[PON]
	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$(u_{\mathrm{dc1}}$-$2u_{\mathrm{dc2}})/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$(u_{\mathrm{dc1}}$-$2u_{\mathrm{dc2}})/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$
6	[PON]	[PPN]	[OPN]	[PPN]	[PON]
	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$(2u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$(2u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$	$(u_{\mathrm{dc1}}$-$u_{\mathrm{dc2}})/3$

Fig. 4, type-I zero vectors, type-I small vectors, type-II small vectors, and all the large vectors meet this requirement and are employed by the proposed O-DPWM scheme.

Sector I is taken as an example for analyzing the switching state sequence. One sector is divided into six subsectors, as presented in Fig. 5. The switching-state sequences in each subsector are listed in Table III. *X*-*Y* represents the phase-*X* switching state clamping to *Y* state (*X* = A, B, C; *Y* = P, O, N). During each switching cycle, the switching state of one phase is clamped to reduce the switching loss.

The switching state sequences when the reference vector is located at other sectors can be derived through the symmetrical characteristic of the space-vector diagram.

B. Implementation of the Proposed O-DPWM Scheme

The normalized reference vector $\boldsymbol{V}_{\mathbf{ref}}$ can be expressed by

$$\boldsymbol{V}_{\mathbf{ref}} = \mathrm{MI} \cdot e^{\mathrm{j}\theta} = V_\alpha + \mathrm{j}V_\beta \tag{7}$$

TABLE IV
BOUNDARY LINE BETWEEN EACH SUBSECTOR AT SECTOR I

Boundary line	Expressions
L_1	$\alpha = (3-\lambda)/2\sqrt{3}$
L_2	$\beta = \sqrt{3}\alpha + \lambda - 1$
L_3	$\beta = \sqrt{3}(1+\lambda)\alpha/(3-\lambda)$
L_4	$\beta = (\lambda+1)/2$
L_5	$\beta = -\alpha/\sqrt{3} + (3+\lambda)/3$

where θ represents the phase angle of the reference vector. V_α and V_β are the α-axis and β-axis components of the reference vector, respectively. MI represents the modulation index, as expressed by

$$\mathrm{MI} = \sqrt{6}U_{\mathrm{ac}} \Big/ (u_{\mathrm{dc1}} + u_{\mathrm{dc2}}) \tag{8}$$

where U_{ac} represents the rms value of the utility grid voltage.

From Fig. 3, it can be seen that, the region of each big sector is not affected by the NP voltage, and can be easily identified by the phase angle of the reference vector.

Sector I is taken as an example for presenting the implementation of the proposed O-DPWM scheme in a digital signal processor (DSP). First, the subsector should be identified. The expressions for the boundary line between each subsector, as shown in Fig. 5, are listed in Table IV. (α, β) represents the coordinates of any point in $\alpha\beta$ coordinate system. By comparing the coordinates of reference vectors (V_α, V_β) with the boundary line listed in Table IV, the subsector can be easily determined.

Then, the dwelling time of each vector can be calculated by (9), where $V_{x\alpha}$ and $V_{x\beta}$ represent the α-axis and β-axis component of $\boldsymbol{V}_x$, respectively. $\boldsymbol{V}_x$ has been listed in Table III. δ_x is the dwelling duty of $\boldsymbol{V}_x$, representing the ratio of the dwelling time of $\boldsymbol{V}_x$ to the switching period T_{s} (x = 1, 2, 3). By solving (9), the dwelling duty of each vector of the proposed O-DPWM at big Sector I is listed in Table V

$$\begin{bmatrix} V_{1\alpha} & V_{2\alpha} & V_{3\alpha} \\ V_{1\beta} & V_{2\beta} & V_{3\beta} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \end{bmatrix} = \begin{bmatrix} V_\alpha \\ V_\beta \\ 1 \end{bmatrix}, \delta_x = \frac{t_x}{T_{\mathrm{s}}} \ (x = 1, 2, 3). \tag{9}$$

The proposed O-DPWM scheme has four types of switching-state sequences, as shown in Fig. 6. m_X represents the phase-*X* modulation signal. u_{c} represents the carrier signal, whose peak value is *H*. These four different types of switching-state sequences can be easily realized in a DSP with an enhanced PWM (ePWM). In an ePWM unit, the value of the counter-compare (CMP) register represents the modulation signal, and the value

$$\begin{cases} \mathbf{V}_{[s_{\mathrm{A}},s_{\mathrm{B}},s_{\mathrm{C}}]} = \frac{1}{\sqrt{3}}\left(s_{\mathrm{A}}e^{\mathrm{j}0} + s_{\mathrm{B}}e^{\mathrm{j}\frac{2\pi}{3}} + s_{\mathrm{C}}e^{-\mathrm{j}\frac{2\pi}{3}}\right) \\ s_X = \begin{cases} 2u_{\mathrm{dc1}}/u_{\mathrm{dc}} = 1-\lambda, & \text{Switching state is P} \\ 0, & \text{Switching state is O} \\ -2u_{\mathrm{dc2}}/u_{\mathrm{dc}} = -1-\lambda, & \text{Switching state is N.} \end{cases} \quad (X = A, B, C) \end{cases} \tag{6}$$

TABLE V
DWELLING DUTY OF EACH VECTOR OF O-DPWM AT BIG SECTOR I

Subsector	δ_1	δ_2	δ_3
1	$\frac{2V_\beta}{\lambda+1}$	$\frac{-\sqrt{3}(\lambda+1)V_\alpha+(3-\lambda)V_\beta}{\lambda^2-1}$	$\frac{\sqrt{3}V_\alpha-V_\beta+\lambda-1}{\lambda-1}$
2	$\frac{-\sqrt{3}V_\alpha+V_\beta}{\lambda-1}$	$\frac{\sqrt{3}(\lambda+1)V_\alpha-(3-\lambda)V_\beta}{\lambda^2-1}$	$\frac{-2V_\beta}{\lambda+1}$
3	$\frac{\sqrt{3}V_\alpha+V_\beta+\lambda-1}{\lambda+1}$	$\frac{-2\sqrt{3}V_\alpha+3-\lambda}{\lambda+1}$	$\frac{\sqrt{3}V_\alpha+V_\beta+\lambda-1}{\lambda+1}$
4	$\frac{-\sqrt{3}V_\alpha-V_\beta+\lambda+1}{\lambda-1}$	$\frac{\sqrt{3}V_\alpha+3V_\beta-\lambda-3}{\lambda-1}$	$\frac{-2V_\beta+\lambda+1}{\lambda-1}$
5	$\frac{-\sqrt{3}V_\alpha+V_\beta+2}{\lambda+1}$	$\frac{-2\sqrt{3}V_\alpha+\lambda-3}{\lambda+1}$	$\frac{-\sqrt{3}V_\alpha-V_\beta+2}{\lambda+1}$
6	$\frac{2V_\beta-2}{\lambda-1}$	$\frac{-\sqrt{3}V_\alpha-3V_\beta+\lambda+3}{\lambda-1}$	$\frac{\sqrt{3}V_\alpha+V_\beta-2}{\lambda-1}$

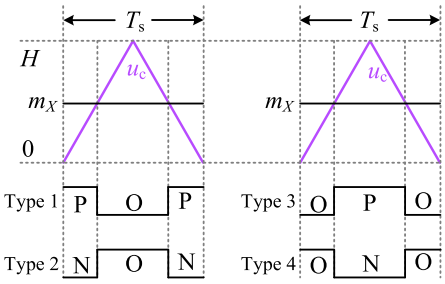

Fig. 6. Four types of switching-state sequence by using the proposed O-DPWM scheme.

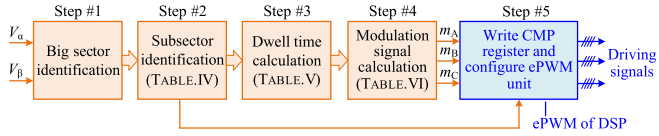

Fig. 7. Implementation of the proposed O-DPWM scheme.

of the time-base (TB) counter represents the carrier signal. By configuring the comparing logic of ePWM units, these four types can be changed in real-time during each switching period.

The relation between the modulation signal m_X and the type of switching-state sequence can be derived from Fig. 6, as expressed by (10). δ_X^{O} represents the ratio of the dwelling time of O-level to the switching period in phase-X bridge-leg voltage. (X = A, B, C)

$$m_X = \begin{cases} H\left(1-\delta_X^{\mathrm{O}}\right), & \text{type 1 and 2} \\ H\delta_X^{\mathrm{O}}, & \text{type 3 and 4} \end{cases}. \tag{10}$$

Combining (10) with Tables III, IV, and V, three-phase modulation signals when the reference vector is located at Sector I can be derived, as listed in Table VI. The configurations of the types of switching-state sequences at each subsector are given as well.

The same calculation process can be conducted when the reference vector is located at other big sectors. The overall implementation process of the proposed O-DPWM scheme is depicted in Fig. 7. From step#1 to step#3, the dwelling time of

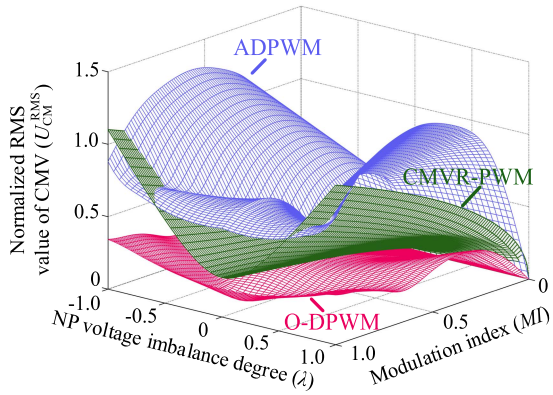

Fig. 8. Calculated normalized rms values of CMV by using different schemes.

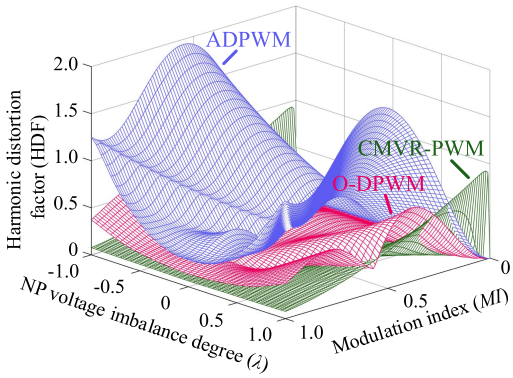

Fig. 9. Calculated HDF by using different schemes.

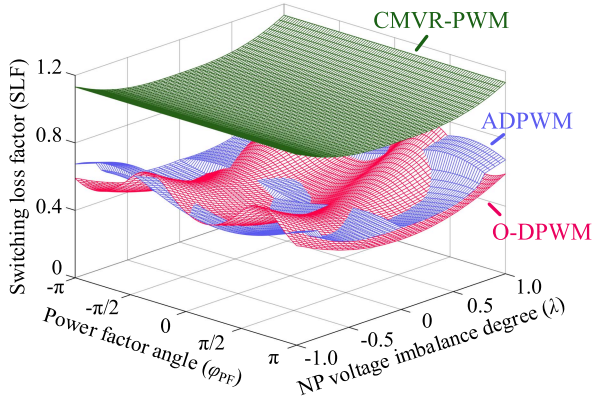

Fig. 10. Calculated SLFs by using different schemes (MI = 0.898).

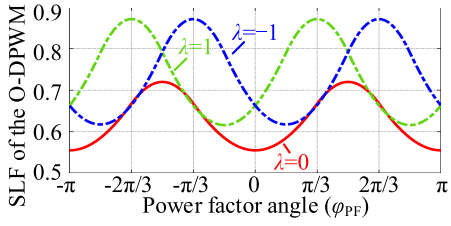

Fig. 11. Calculated SLFs by using the proposed O-DPWM scheme.

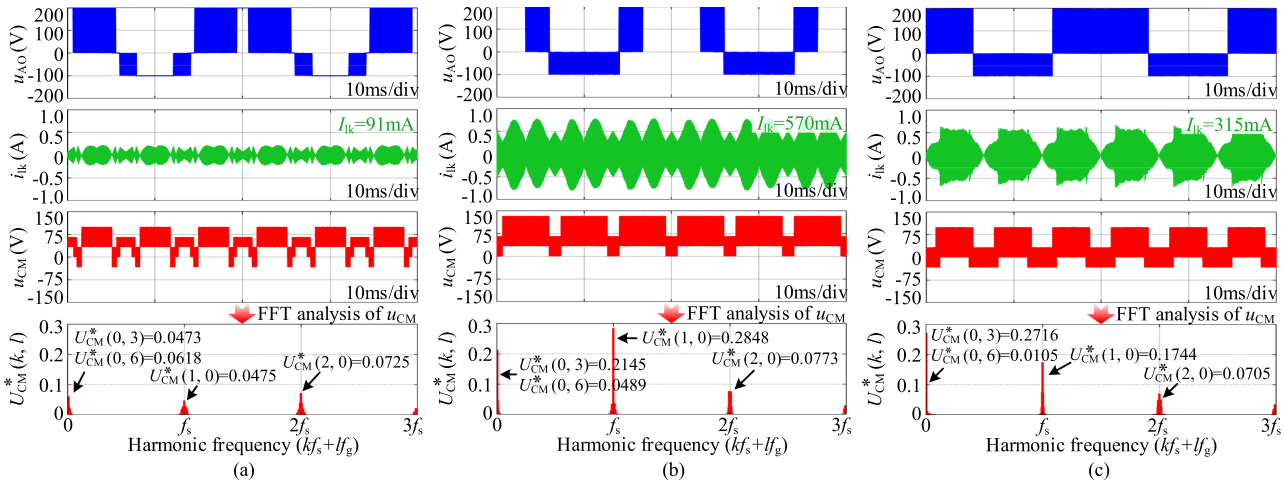

Fig. 12. Simulation results and FFT analysis by using different schemes under the unbalanced NP voltage condition. (a) O-DPWM scheme. (b) ADPWM scheme. (c) CMVR-PWM scheme.

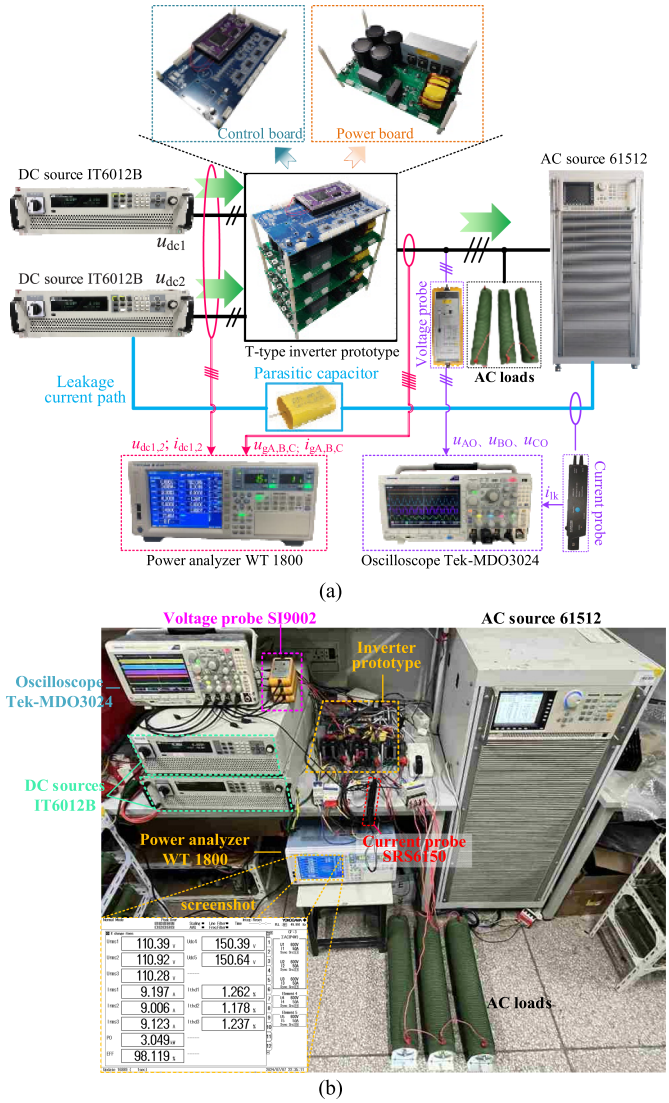

Fig. 13. Overall experimental setup and photograph of the prototype. (a) Hardware setup. (b) Photograph of the experimental platform.

TABLE VI
MODULATION SIGNALS OF O-DPWM AT BIG SECTOR I

	Subsector	Phase A	Phase B	Phase C
1	Modulation signal (m_X)	$H(\delta_1+\delta_2)$	H	$H\delta_1$
	Sequence type configuration	Type 1	Type 4	Type 2
2	Modulation signal (m_X)	$H\delta_1$	H	$H(\delta_1+\delta_2)$
	Sequence type configuration	Type 1	Type 3	Type 2
3	Modulation signal (m_X)	H	$H(\delta_1+\delta_2)$	$H\delta_1$
	Sequence type configuration	Type 1	Type 4	Type 2
4	Modulation signal (m_X)	$H\delta_1$	$H(\delta_1+\delta_2)$	H
	Sequence type configuration	Type 1	Type 3	Type 2
5	Modulation signal (m_X)	H	$H\delta_1$	$H(\delta_1+\delta_2)$
	Sequence type configuration	Type 1	Type 4	Type 2
6	Modulation signal (m_X)	$H(\delta_1+\delta_2)$	$H\delta_1$	H
	Sequence type configuration	Type 1	Type 3	Type 2

each vector is calculated based on the space-vector algorithm. Then, step#4 calculates modulation signals according to vector dwelling times. Finally, step#5 configures the ePWM to generate driving signals of switching devices. In step#5, modulation signals are written to the CMP registers to compare with the TB counter, and the comparing logic is configured according to the subsector.

C. CMV Characteristic Analysis

According to the analysis in Section II, the rms value and spectrum of the CMV are calculated to demonstrate the low leakage current characteristic of the O-DPWM scheme.

According to [33], the normalized rms value of the CMV can be calculated as

$$\begin{aligned} U_{\mathrm{CM}}^{\mathrm{RMS}} &= \frac{2}{u_{\mathrm{dc}}}\sqrt{\frac{1}{T_{\mathrm{g}}}\int_0^{T_{\mathrm{s}}} u_{\mathrm{CM}}^2 \mathrm{d}t} \\ &= \frac{2}{u_{\mathrm{dc}}}\sqrt{\frac{1}{T_{\mathrm{g}}}\sum_{p=0}^{N_{\mathrm{f}}-1}\int_{pT_{\mathrm{s}}}^{(p+1)T_{\mathrm{s}}} u_{\mathrm{CM}}^2 \mathrm{d}t} \\ &= \frac{2}{u_{\mathrm{dc}}}\sqrt{\frac{1}{T_{\mathrm{g}}}\sum_{p=0}^{N_{\mathrm{f}}-1}\sum_{x=1}^{N_{\mathrm{v}}}\delta_x T_{\mathrm{s}} U_{\mathrm{CM}.p.Vx}^2} \end{aligned} \tag{11}$$

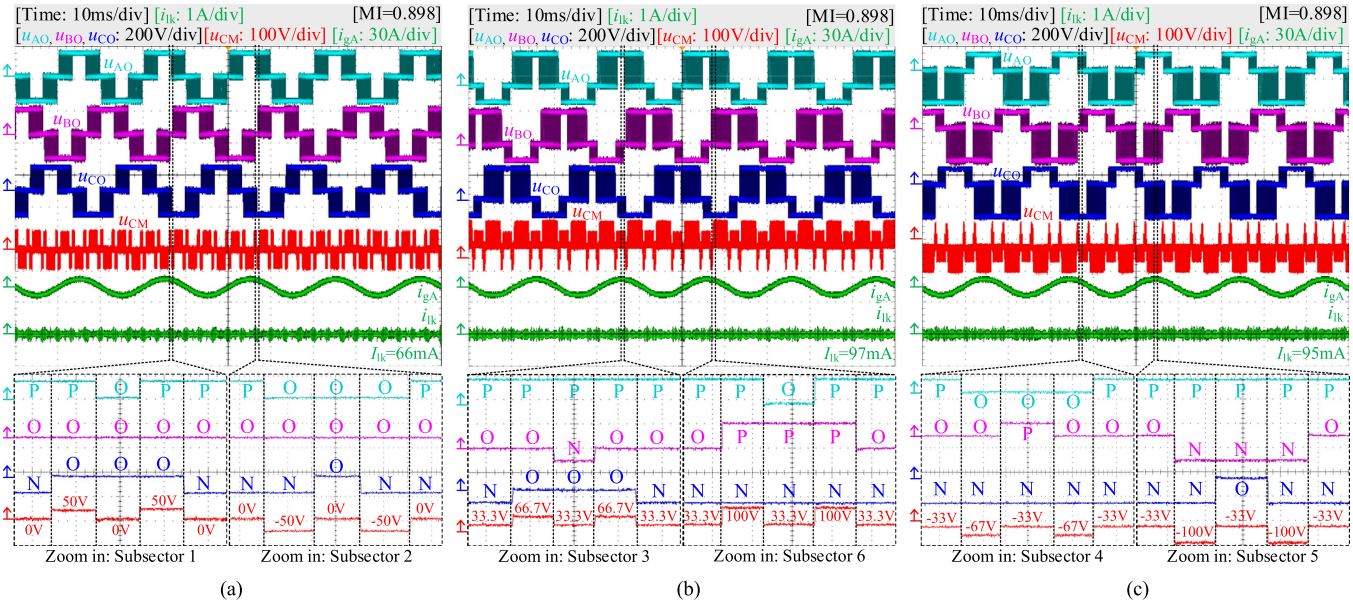

Fig. 14. Experimental results by using the proposed O-DPWM scheme under rated operation conditions (MI = 0.89). (a) $\lambda = 0$ ($u_{dc1} = u_{dc2}$). (b) $\lambda = -0.33$ ($u_{dc1} > u_{dc2}$). (c) $\lambda = 0.33$ ($u_{dc1} < u_{dc2}$).

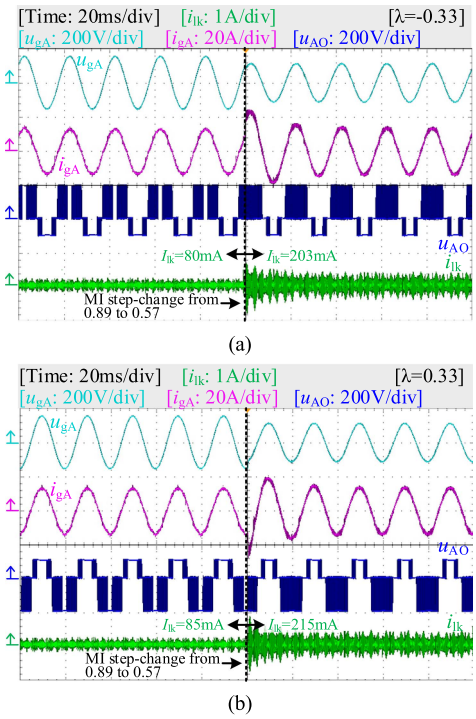

Fig. 15. Dynamic experimental waveforms of MI step-change by using the proposed O-DPWM scheme under unbalanced NP voltage conditions. (a) $\lambda = -0.33$ ($u_{dc1} > u_{dc2}$). (b) $\lambda = 0.33$ ($u_{dc1} < u_{dc2}$).

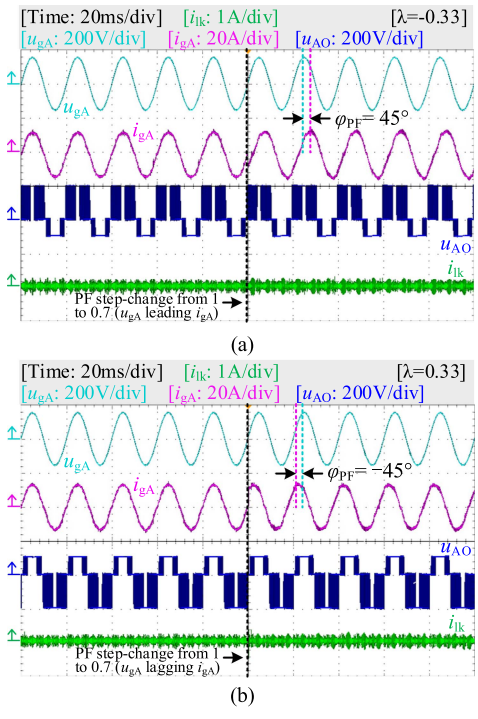

Fig. 16. Dynamic experimental waveforms of power factor step-change by using the proposed O-DPWM scheme under unbalanced NP voltage conditions. (a) φ_{PF} step-change from 0° to 45°, and $\lambda = -0.33$. (b) φ_{PF} step-change from 0° to −45°, and $\lambda = 0.33$.

where $N_f = f_g/f_s$, representing switching times in a fundamental period. T_g and T_s are the fundamental period and switching period, respectively. N_v represents the number of the used vectors in a switching period. Especially, when the proposed O-DPWM scheme is employed, N_v is 3. $U_{CM.p.Vx}$ represents the CMV magnitudes of V_x in pth switching period. V_x represents the used vectors, as listed in Table III ($x = 1, 2, 3$).

Calculated normalized rms values of the CMV by using different schemes are depicted in Fig. 8. The proposed O-DPWM is compared with the analytical DPWM (ADPWM) scheme

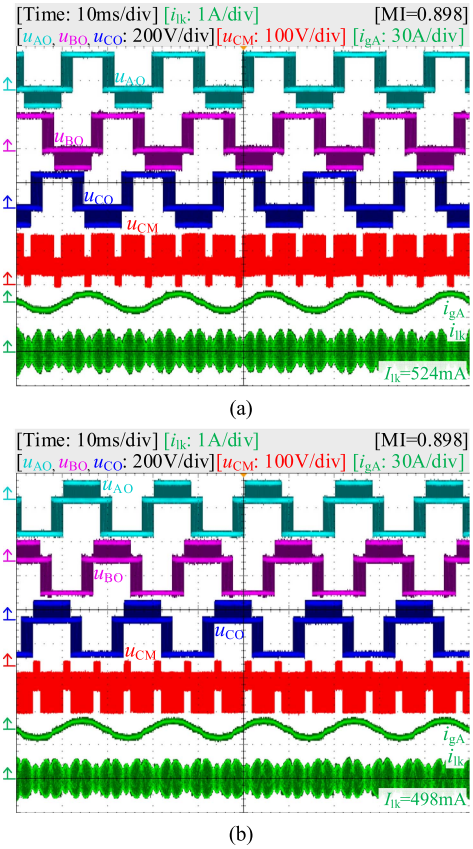

Fig. 17. Steady-state waveforms by using the ADPWM scheme proposed in [39] under rated operation conditions (MI = 0.89). (a) $\lambda = -0.33$ ($u_{dc1} > u_{dc2}$). (b) $\lambda = 0.33$ ($u_{dc1} < u_{dc2}$).

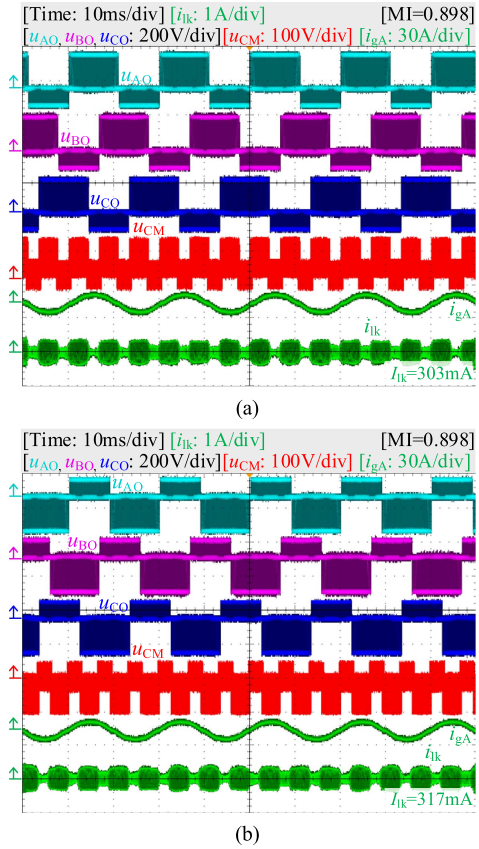

Fig. 18. Steady-state waveforms by using the CMVR-PWM scheme proposed in [40] under rated operation conditions (MI = 0.89). (a) $\lambda = -0.33$ ($u_{dc1} > u_{dc2}$). (b) $\lambda = 0.33$ ($u_{dc1} < u_{dc2}$).

proposed in [39] and the CMV reduction PWM (CMVR-PWM) scheme proposed in [40]. The ADPWM can improve efficiency and the alternating output current distortion under unbalanced NP voltage. The CMVR-PWM can lower the leakage current under different NP voltage conditions.

From Fig. 8, it can be seen that, the proposed O-DPWM scheme has the lowest rms value of the CMV with different NP voltage imbalance degrees and modulation indices. As a result, the proposed O-DPWM scheme could effectively lower the leakage current compared with these existing schemes.

The double Fourier integral analysis is used to analyze the spectrum of CMVs. According to [33] and [43], the amplitude of u_{CM} at the frequency of (kf_c+lf_g) can be expressed as

$$U_{\mathrm{CM}}(k,l) = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} u_{\mathrm{CM}} e^{-\mathrm{j}(k\theta_c + l\theta_g)}\mathrm{d}\theta_c \mathrm{d}\theta_g. \quad (12)$$

The fundamental period can be divided into each switching period, and one switching period can be further divided into several switching states, which have different CMV magnitudes. Thus, (13) can be further derived from (12), as

$$\begin{aligned} &U_{\mathrm{CM}}(k,l) \\ &= \sum_{p=0}^{N_f-1}\frac{1}{2\pi^2}\int_{p\theta_{sw}}^{(p+1)\theta_{sw}}\int_0^{2\pi} u_{\mathrm{CM}} e^{-\mathrm{j}(k\theta_c + l\theta_g)}\mathrm{d}\theta_c \mathrm{d}\theta_g \\ &= \sum_{p=0}^{N_f-1}\frac{1}{2\pi^2}\int_{p\theta_{sw}}^{(p+1)\theta_{sw}}\left[\sum_{q=1}^{N_s}\int_{\theta_{q-1}}^{\theta_q} U_{\mathrm{CM}.p.Vq} e^{-\mathrm{j}(k\theta_c + l\theta_g)}\mathrm{d}\theta_c\right]\mathrm{d}\theta_g \\ &= \begin{cases} \frac{-1}{2\pi^2 lk}\sum_{p=0}^{N_f-1} \\ \left[\frac{e^{-\mathrm{j}l\theta_{sw}}-1}{e^{\mathrm{j}lk\theta_{sw}}}\sum_{q=1}^{N_s}\left(e^{-\mathrm{j}k\theta_q} - e^{-\mathrm{j}k\theta_{q-1}}\right)U_{\mathrm{CM}.p.Vq}\right], lk \neq 0 \\ \frac{\mathrm{j}}{2\pi^2 l}\sum_{p=0}^{N_f-1}\left[\frac{e^{-\mathrm{j}l\theta_{sw}}-1}{e^{\mathrm{j}lk\theta_{sw}}}\sum_{q=1}^{N_s}\left(\theta_q - \theta_{q-1}\right)U_{\mathrm{CM}.p.Vq}\right], k = 0 \\ \frac{\mathrm{j}}{2\pi^2 k}\sum_{p=0}^{N_f-1}\left[\theta_{sw}\sum_{q=1}^{N_s}\left(e^{-\mathrm{j}k\theta_q} - e^{-\mathrm{j}k\theta_{q-1}}\right)U_{\mathrm{CM}.p.Vq}\right], l = 0 \end{cases} \end{aligned} \quad (13)$$

where $N_f = f_g/f_s$, representing the number of switching periods in a fundamental period. $\theta_{sw} = 2\pi/N_f$. θ_c and θ_g are the phase angle related to the switching period and fundamental period, respectively. N_s represents the segments of switching-state sequences in each switching period. As listed in Table III, when the proposed O-DPWM scheme is employed, N_s is 5. $U_{\mathrm{CM}.p.Vq}$ represents the CMV magnitudes of the qth switching state in pth switching period.

The normalized magnitude of $U_{\mathrm{CM}}(k,l)$ is defined as

$$U^*_{\mathrm{CM}}(k,l) = 2\left|U_{\mathrm{CM}}(k,l)\right|/u_{dc}. \quad (14)$$

TABLE VII
HARMONIC MAGNITUDE COMPARISON

Harmonic order		$U^*_{\mathrm{CM}}(k,l)$		
k	l	O-DPWM	ADPWM	CMVR-PWM
0	3	0.0451	0.2144	0.2383
	6	0.063	0.049	0.0117
1	0	0.0462	0.285	0.218
	3	0.0119	0.0303	0.0943
	6	0.0144	0.0366	0.0232
	9	0.0281	0.0349	0.0014
2	0	0.073	0.077	0.0719
	3	0.0299	0.0251	0.0046
	6	0.0306	0.0223	0.0246
	9	0.0155	0.026	0.0454
3	0	0.0553	0.0688	0.0615
	3	0.0196	0.0064	0.0037
	6	0.0109	0.0017	0.0128
	9	0.0133	0.0297	0.0123

Calculated dominant harmonic components with different schemes are listed in Table VII. The NP voltage imbalance degree for calculation is set at −0.33. MI is set at 0.898. These parameters are the same as those used in simulations and experiments. From Table VII, the CMV has dominant harmonic components at the frequency of $3f_{\mathrm{g}}$ or integral multiples of switching frequency. By using the proposed O-DPWM scheme, all the normalized magnitudes of dominant harmonic components are lower than 0.1, which cannot be achieved by the ADPWM or CMVR-PWM scheme.

Compared with these two existing schemes, although the proposed O-DPWM scheme slightly increases $U^*_{\mathrm{CM}}(0, 6)$ and some sidebands harmonics near integral multiples of switching frequency, it reduces $U^*_{\mathrm{CM}}(0, 3)$ and $U^*_{\mathrm{CM}}(1, 0)$ significantly, which leads to lower rms value as presented in Fig. 8 and contributes to the leakage current reduction.

D. Alternating Output Current Harmonic Analysis

Defining normalized harmonic flux vector as the integral of the difference between the reference vector $\boldsymbol{V}_{\mathbf{ref}}$ and the used vectors, as expressed by

$$\boldsymbol{\Psi} = \int_0^t (\boldsymbol{V} - \boldsymbol{V}_{\mathrm{ref}})\,\mathrm{d}t. \tag{15}$$

The rms value of Ψ in each switching period can be calculated by

$$\boldsymbol{\Psi}_p^{\mathrm{rms}} = \sqrt{\frac{1}{T_{\mathrm{s}}}\int_{pT_{\mathrm{s}}}^{(p+1)T_{\mathrm{s}}} |\boldsymbol{\Psi}|^2 \mathrm{d}t}. \tag{16}$$

According to [27], the harmonic performance of the output current can be evaluated by harmonic distortion factor (HDF), which is defined as

$$\mathrm{HDF} = \frac{288}{\pi^2}\frac{1}{T_{\mathrm{g}}}\int_0^{T_{\mathrm{g}}} |\boldsymbol{\Psi}|^2 \mathrm{d}t = \frac{288}{\pi^2}\frac{1}{T_{\mathrm{g}}}\sum_{p=0}^{N_{\mathrm{f}}-1}\left(\boldsymbol{\Psi}_p^{\mathrm{rms}}\right)^2 T_{\mathrm{s}}. \tag{17}$$

Calculated HDFs are shown in Fig. 9. Fig. 9 indicates that the imbalance degrees hardly affect the HDF with the proposed O-DPWM scheme or CMVR-PWM scheme. Under most conditions, the HDF of the CMVR-PWM scheme is the lowest, and the HDF of the proposed O-DPWM scheme takes second place. Therefore, the current harmonic performance of the proposed O-DPWM is better than that of the ADPWM scheme, and it is slightly worse than that of the CMVR-PWM scheme.

E. Switching Loss Analysis

Assuming the switching devices have linear turn-ON and turn-OFF characteristics and only the fundamental component of the alternating output current is considered, the switching energy of a single switching device during pth switching period can be calculated by [33]

$$E^{mn}_{\mathrm{sw}.p} = \begin{cases} 0.5U^{mn}_{\mathrm{OFF}.p} I^{mn}_{\mathrm{ON}.p}\,(t_{\mathrm{on}} + t_{\mathrm{off}}), & \text{unclamped} \\ 0, & \text{switching stateis clamped} \end{cases}. \tag{18}$$

$E^{mn}_{\mathrm{sw}.p}$ represents the switching energy of the switching device S_{mn}, as shown in Fig. 1, in pth switching period (m = a, b, or c; n = 1, 2, 3, or 4). $U^{mn}_{\mathrm{OFF}.p}$ represents the OFF-state voltage of the switching device S_{mn} at the pth switching period. $I^{mn}_{\mathrm{D}.p}$ represents the ON-state current of the switching device S_{mn} at the pth switching period. (m = a, b, or c; n = 1, 2, 3, or 4). t_{ON} and t_{OFF} are the turn-ON and turn-OFF times of the switching device, respectively. When the switching state is clamped, switching loss is not generated in pth switching period. When the switching state is switched between P-level and O-level, the OFF-state voltage of the switching device is u_{dc1}. When the switching state is switched between N-level and O-level, the OFF-state voltage of the switching device is u_{dc2}. The ON-state current is determined by the alternating output current at pth switching period. Then, switching loss can be calculated by

$$P_{\mathrm{sw}} = \frac{1}{T_{\mathrm{g}}} \times \sum_{p=0}^{N_{\mathrm{f}}-1}\left(\sum_{m=a,b,c}\sum_{n=1}^{4} E^{mn}_{\mathrm{sw}.p}\right). \tag{19}$$

According to [27], the switching loss factor (SLF) can be used to evaluate the switching loss performance of different schemes. SLF is defined by (20), which normalizes P_{sw} to $P_{\mathrm{sw.CPWM}}$, the switching loss by using a CPWM scheme under balanced NP voltages

$$\mathrm{SLF} = \frac{P_{\mathrm{sw}}}{P_{\mathrm{sw.CPWM}}} = \frac{P_{\mathrm{sw}}}{\frac{1}{T_{\mathrm{g}}}\sum_{p=0}^{N_{\mathrm{f}}-1}\left(\sum_{m=a,b,c}\sum_{n=1}^{4}\frac{0.5u_{\mathrm{dc}}I^{mn}_{\mathrm{ON}.p}(t_{\mathrm{on}}+t_{\mathrm{off}})}{4}\right)}. \tag{20}$$

Calculated SLFs by using different schemes are shown in Fig. 10. The power factor angle φ_{PF} represents the phase angle that the utility grid voltage leads the alternating output current. Fig. 10 shows that the switching loss is affected by both power factor and NP voltage imbalance degree. The CMVR-PWM scheme is a CPWM scheme that has more switching times than DPWM schemes. Thus, the SLFs of the CMVR-PWM scheme

TABLE VIII
EXPERIMENT AND SIMULATION SPECIFICATIONS

Parameter	Value
Rated output power	3 kW
Rated utility grid voltage (u_{gA}, u_{gB}, u_{gC})	110 V/50 Hz
Dc-link voltage (u_{dc})	300 V
Switching frequency (f_s)	40 kHz
Filter inductor (L)	590 μH
Filter capacitor (C_f)	3.3 μF
Dc-link capacitor (C_{dc1}, C_{dc2})	1.4 mF
MOSFETS	IV1Q12080T3

are much higher than those of the O-DPWM scheme and the ADPWM scheme. Since the O-DPWM scheme and ADPWM scheme have different clamping regions, the relationship between their SLFs varies with different power factors and NP voltage imbalance degrees.

Additionally, it can be observed that under a certain power factor angle, the SLF of the proposed O-DPWM increases with the absolute value of λ. Consequently, the SLF of the proposed O-DPWM reaches its minimum value when the NP voltage is balanced, and its maximum value when λ equals ±1. Fig. 11 depicts the calculated SLFs using the proposed O-DPWM scheme with different NP voltage imbalance degrees. The minimum SLF achieved with the proposed O-DPWM is approximately 0.55 when the NP voltage is balanced and the power factor angle is zero. Therefore, the proposed O-DPWM can reduce switching loss by 45%, achieving the lowest switching loss under unit power factor and balanced NP voltage. When λ equals ±1 and the power factor is 0.5, the proposed O-DPWM reaches its maximum SLF, approximately 0.867. This indicates that, under the worst conditions, the proposed O-DPWM scheme can still reduce switching loss by 13.3%.

F. Simulation Results

A 3-kW grid-tied T-type inverter simulation model was built in MATLAB/Simulink. Simulation specifications are the same as experiments, as listed in Table VIII. According to the study reported in [44], typical values of the parasitic capacitor range between 50 and 150 nF/kW for glass-faced modules. Thus, C_{PV} is 450 nF in the simulation model. According to the IEEE standards, the recommended ground resistance is within the limit of 2 Ω–5 Ω [45], [46]. Thus, R_G is 2 Ω in the simulation model, representing the worst ground leakage current issue in PV grid-tied systems.

Simulation results by using different schemes under the unbalanced NP voltage condition are presented in Fig. 12. NP voltage imbalance degree (λ) is set at −0.33. u_{AO} represents the voltage between terminal A and terminal O, as depicted in Fig. 1. i_{lk} and I_{lk} are the instantaneous value and rms value of the leakage current, respectively. The spectrum of the CMV is presented as well. The fast fourier transform (FFT) analysis tool calculates the normalized magnitude of the CMV harmonic component, called $U^*_{CM}(k, l)$. The FFT analysis results show that, although the proposed O-DPWM scheme slightly increases $U^*_{CM}(0, 6)$, it reduces $U^*_{CM}(0, 3)$ and $U^*_{CM}(1, 0)$ significantly. Therefore, compared with the ADPWM scheme and CMVR-PWM scheme, the proposed O-DPWM scheme has the lowest leakage current.

The FFT analysis results presented in Fig. 12 are in accordance with the calculated results listed in Table VII, which indicates the CMV harmonic analysis presented in Section III-C is correct.

IV. EXPERIMENTAL RESULTS AND COMPARISON ANALYSIS

A 3-kW T-type grid-tied inverter prototype was built, and the specifications of the prototype are listed in Table VIII. The prototype is controlled by a DSP TMS320F28377D. Fig. 13(a) shows the hardware setup of experiments. The inverter is powered by two dc sources (IT6012B), and its output is connected with a programmable ac source (Chroma-61512), which is utilized to simulate a utility grid. Three-phase resistances are also connected with the programmable ac source to simulate ac loads in a utility grid. Voltage waveforms are measured by voltage probe (SI9002), and current waveforms are measured by current probe (SRS6150) with 50 MHz bandwidth. All the waveforms are recorded by an oscilloscope (Tek-MDO3024). Efficiencies and total harmonic distortion (THD) values are tested by a power analyzer WT-1800. According to the study reported in [44], [45], and [46], the used parasitic capacitor C_{PV} is 450 nF (150 nF/kW), and the ground resistance R_G is 2 Ω. Fig. 13(b) shows the photo of the experimental platform, along with a screenshot of the power analyzer (WT-1800), when the inverter operates at rated output power and rated utility grid voltages.

A. Verification of the Proposed O-DPWM

Steady-state waveforms with the proposed O-DPWM scheme are shown in Fig. 14. It can be seen that the switching states are the same as listed in Table III, indicating that the proposed O-DPWM scheme is enabled. Since the space-vector diagram varies with the NP voltage by using the O-DPWM scheme, there is no apparent alternating output current distortion under unbalanced NP voltage conditions. The leakage current of the O-DPWM scheme is always lower than 100 mA. Thus, the proposed O-DPWM scheme features low leakage current under different NP voltage conditions. Besides, the bridge-leg voltage of one phase is clamped, indicating that the proposed O-DPWM scheme reduces the switching times. Dynamic waveforms of the proposed O-DPWM scheme under step-changed MIs and unbalanced NP voltage conditions are shown in Fig. 15. The MI step-change is achieved by changing the rms value of utility grid voltage from 110 V to 70 V. Fig. 15 shows that the proposed method can operate with different MIs. Although the leakage current increases when the MI is step-changed from 0.89 to 0.57, the leakage current is still lower than 300 mA. Therefore, the proposed O-DPWM scheme achieves low leakage current with different MIs.

Dynamic waveforms of the proposed O-DPWM scheme under step-changed power factors and unbalanced NP voltage conditions are shown in Fig. 16. Fig. 16 shows that the leakage current is hardly affected by the power factor, indicating the

proposed O-DPWM scheme features low leakage current with different power factors.

B. Comparison Analysis

Steady-state waveforms by using the ADPWM scheme under rated operation conditions are shown in Fig. 17. It can be seen that, by using the ADPWM scheme, the bridge-leg voltage of one phase is clamped, indicating the ADPWM scheme also reduces switching times. However, the leakage current of the ADPWM scheme is always higher than 300 mA. Thus, compared with the ADPWM scheme, the proposed O-DPWM scheme features lower leakage currents.

Steady-state waveforms using the CMVR-PWM scheme under rated operation conditions are shown in Fig. 18. From Fig. 18, it can be seen that, although the CMVR-PWM scheme has reduced the CMV, its leakage current is still higher than that of using O-DPWM scheme. Besides, there are no clamping regions in the bridge-leg voltage. As a result, compared with the CMVR-PWM scheme, the proposed O-DPWM scheme reduces the leakage current and features fewer switching times.

The spectrums of the CMV and leakage current by using different schemes under the unbalanced NP voltage condition are shown in Fig. 19. λ is set at -0.33. The waveforms of CMV and leakage current presented in Figs. 14(b), 17(a), and 18(a) are recorded by the oscilloscope Tek-MDO3024. The FFT analysis tool calculates the spectrums of the CMV and leakage current. $U_{\mathrm{CM}}(k,\ l)$ and $I^{\mathrm{p}}_{\mathrm{CM}}(k,\ l)$ represent the amplitude of u_{CM} and i_{lk} at the frequency of $(kf_{\mathrm{c}}+lf_{\mathrm{g}})$, respectively. Fig. 19 shows that the measured spectrums of the CMV with different schemes are consistent with calculation and simulation results. The dominant harmonic frequency of leakage currents is the switching frequency. Compared with the ADPWM scheme and the CMVR-PWM scheme, the proposed O-DPWM scheme significantly reduces $I^{\mathrm{p}}_{\mathrm{CM}}(1,\ 0)$. Thus, the proposed O-DPWM has the lowest leakage current.

Measured rms values of the leakage current under different NP voltage conditions are shown in Fig. 20. From Fig. 20, it can be seen that, by using the proposed O-DPWM scheme, the leakage current is always lower than 300 mA. Compared with the ADPWM scheme, the proposed O-DPWM scheme reduces the leakage current by about 80%. Compared with the CMVR-PWM scheme, when the proposed O-DPWM scheme is employed, the leakage current does not significantly increase with the increased NP voltage imbalance degrees.

Measured rms values of the leakage current with different parasitic capacitances under the unbalanced NP voltage condition are shown in Fig. 21. From Fig. 21, it can be seen that, the leakage current increases with a greater parasitic capacitance. Compared with the ADPWM scheme and CMVR-PWM scheme, the proposed O-DPWM scheme reduces the leakage current under different parasitic capacitances.

Measured rms values of the leakage current with different switching frequencies under unbalanced NP voltage conditions are shown in Fig. 22. From Fig. 22, it can be seen that, since the used switching frequencies are higher than the resonant

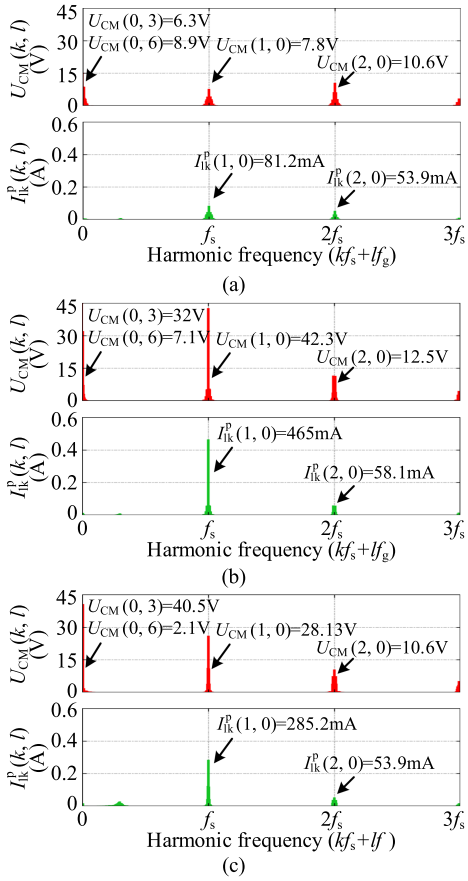

Fig. 19. Spectrum comparison by using different schemes under unbalanced NP voltage conditions where $\lambda = -0.33$ ($u_{\mathrm{dc1}} > u_{\mathrm{dc2}}$). (a) O-DPWM scheme. (b) ADPWM scheme. (c) CMVR-PWM scheme.

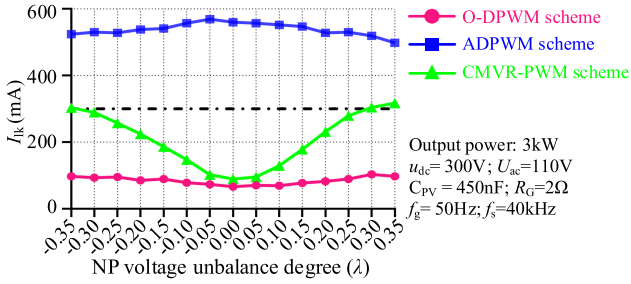

Fig. 20. Measured leakage current under different NP voltage imbalance degrees by using different schemes at rated output power.

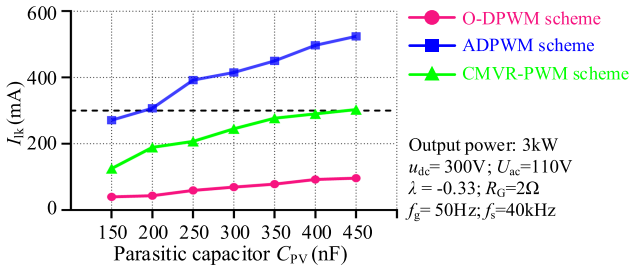

Fig. 21. Measured leakage current with different parasitic capacitor values and different schemes under the unbalanced NP voltage condition.

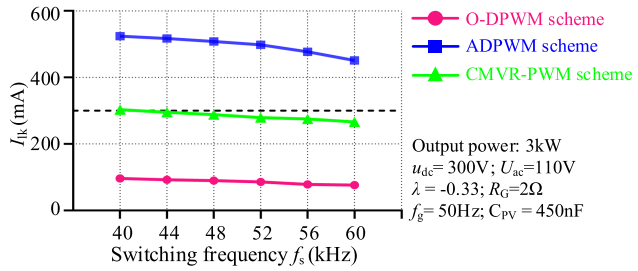

Fig. 22. Measured leakage current with different switching frequencies and different schemes under the unbalanced NP voltage condition.

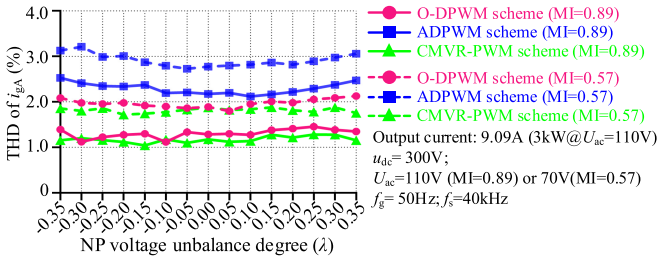

Fig. 23. Measured current THDs with different NP voltage imbalance degrees by using different schemes.

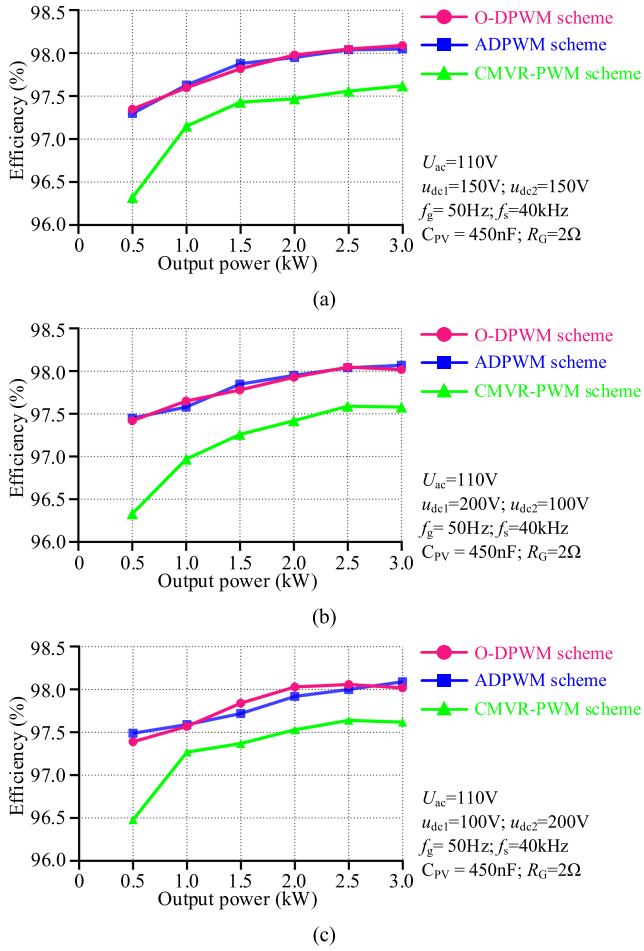

Fig. 24. Measured efficiencies with different output power and NP voltage imbalance degrees by using different schemes. (a) $\lambda = 0$ ($u_{dc1} = u_{dc2}$). (b) $\lambda = -0.33$ ($u_{dc1} > u_{dc2}$). (c) $\lambda = 0.33$ ($u_{dc1} < u_{dc2}$).

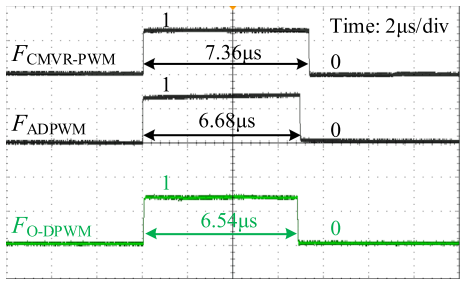

Fig. 25. Measured program execution time by using different schemes.

frequency of the leakage current path, the leakage current is reduced with higher switching frequency [24]. Compared with the ADPWM and CMVR-PWM schemes, the proposed O-DPWM scheme strongly reduces the leakage current at different switching frequencies.

Measured current THDs under different MIs and different NP voltage conditions are shown in Fig. 23. The rms value of the alternating output current is set at 9.09 A, by which the inverter outputs the rated power under a rated utility grid voltage. From Fig. 23, all three schemes do not lead to high current THD under unbalanced NP voltage. The proposed O-DPWM scheme has lower current THDs than the ADPWM scheme. Furthermore, with the proposed O-DPWM scheme, the current THDs are only slightly higher than that of the CMVR-PWM scheme when the leakage current is significantly reduced.

Measured efficiencies under different output power and NP voltage conditions are shown in Fig. 24. The proposed scheme has similar efficiencies with the ADPWM scheme. Compared with the CMVR-PWM scheme, whether the NP voltage is balanced or not, the proposed O-DPWM scheme improves efficiency by about 0.5% at rated output power.

The program execution time comparison between the proposed O-DPWM scheme, ADPWM scheme, and CMVR-PWM scheme is shown in Fig. 25. The programs are executed in the DSP-TMS320F28377D, whose clock frequency is 200 MHz. When F_X is set to 1, the X scheme is executed (X = O-DPWM, CMVR-PWM, or ADPWM). From Fig. 25, it can be seen that, the total program execution times of these three schemes are similar. The program execution time of the CMVR-PWM scheme is slightly longer than that of the proposed O-DPWM scheme and ADPWM scheme. Thus, compared with the existing schemes, the proposed O-DPWM reduces the leakage current without increasing the program execution time.

Based on the above experiments, a comprehensive comparison is listed in Table IX. From Table IX, it can be seen that, compared with existing schemes, the proposed O-DPWM features lower leakage current and higher efficiency, while the THD performance and program execution time are also commendable.

TABLE IX
COMPREHENSIVE COMPARISON

Scheme	Leakage current	THD	Efficiency	Program execution time
ADPWM scheme [39]	High	Moderate	High	Short
CMVR-PWM scheme [40]	Moderate	Low	Low	Long
O-DPWM scheme	Low	Low	High	Short

V. CONCLUSION

This article proposes an O-DPWM scheme to achieve both low leakage current and high efficiency. Analysis and experimental results demonstrate the following advantages.

1) The leakage current is significantly reduced under unbalanced NP voltage conditions. Compared with the ADPWM scheme proposed in [39], the proposed O-DPWM scheme reduces the leakage current by 80%. Compared with the CMVR-PWM scheme proposed in [40], the proposed O-DPWM scheme also significantly lowers the leakage current under unbalanced NP voltage conditions.
2) The switching times are reduced by 1/3 by clamping one bridge-leg voltage at each switching cycle. Compared with CPWM schemes, the proposed O-DPWM reduces switching losses by 13.3% to 45%. Thus, compared with the existing CMVR-PWM scheme, the proposed scheme almost improves efficiencies by 0.5% at rated power.
3) The current THD performance and program execution time of the proposed O-DPWM scheme are also commendable.

Therefore, the proposed scheme is an excellent method for three-phase three-level inverters with independent dual dc ports.

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