An Improved 3L APF Control Strategy Utilizing the Oscillated DC-Link Voltage Command to Enhance the Harmonic-Compensation Performance

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***Abstract*—Given interactions exist between dc-link voltage oscillations and ac currents in three-level active power filters (3L APF), the output of the outer voltage loop will inevitably affect the current control loop, impairing the harmonic-compensation performance. In this article, the oscillated dc-link voltage command is utilized to enhance the harmonic-compensation performance. First, the dc-link voltage oscillations caused by ac current harmonics in 3L APF converters are mathematically analyzed and derived. Then, to eliminate the dc bias in the integration for calculating the oscillated dc-link voltage command, the multiple second-order generalized integrator frequency-locked loop is adopted and improved by combining with low-pass filters. And an improved 3L APF control strategy utilizing the oscillated dc-link voltage command is proposed to enhance the harmonic-compensation performance. Finally, the proposed 3L APF control strategy is verified by simulations and experiments, presenting an improved harmonic-compensation performance, and a fast dynamic performance of the dc-link voltage can still be guaranteed.**

***Index Terms*—Active power filters (APF), current harmonic compensation, oscillated dc-link voltage command.**

I. INTRODUCTION

With the wide adoption of nonlinear loads, such as diode rectifiers, large quantities of current harmonics are generated, further impairing the power quality in power transmission systems [1], [2], [3]. The three-level active power filter (3L APF) is an effective solution, which can extract harmonics of nonlinear loads, and generate equal-amplitude and opposite-phase currents for compensation.

Given interactions exist between ac currents and dc-link voltage oscillations in 3L APF, the control strategies of ac currents and the dc-link voltage are both important for the harmonic compensation [4], [5], [6]. Regarding the control strategies for ac currents, the high gains of current controllers at harmonic frequencies are especially important for enhancing the control accuracy of current harmonics. In the conventional double-loop control strategy with proportional-integral (PI) controllers, increasing proportional and integral gains can obtain a better control accuracy. But the stability may be impaired by the increased gains [7], [8]. To overcome the drawback of PI controllers with low gains at harmonic frequencies, current controllers with high gains can be adopted to enhance the control accuracy of current harmonics, such as resonant (R) controllers [9], vector-proportional-integral (VPI) controllers [10], and repetitive controllers [11]. To achieve better dynamic and steady-state performances, as well as high gains at harmonic frequencies, combined controllers can be adopted, e.g., the P-R controllers [12], PI-R controllers [13], PI-VPI controllers [14], and PI-repetitive controllers [15]. However, with one R or VPI controller, only a pair of negative-and positive-sequence harmonics can be regulated. If multiple harmonic need to be compensated, multiple R or VPI controllers should be adopted [16], inevitably increasing the complexity of control strategies. In addition, other improved current control strategies can also be adopted to achieve a satisfying harmonic-compensation performance, such as the model predictive control [17] and the sliding mode control [18].

Regarding the control strategies related to the dc-link voltage, a modified APF control strategy is proposed in [19] with the model reference adaptive system based dc voltage estimation and the load current sensor reduction. In [20], the influence of supply-voltage fluctuation on the dc-link voltage of the APF is investigated. An APF control method is proposed in [21] for suppressing the dc capacitor voltage ripple caused by the third-order harmonic current compensation. An adaptive dc-link voltage control strategy for the APF is proposed in [22] based on the model predictive control. A robust dc-link voltage control strategy is proposed in [23] to enhance the performance of the APF without harmonic detection schemes.

Among the above APF control strategies, the most popular and widely-adopted strategies are still improved based on the conventional double-loop control strategy, which contains an outer dc-link voltage loop and two inner current loops in the *dq*

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coordinate. Different from other power-electronic control systems, e.g., photovoltaic inverters [24] and electric vehicles [25], no extra dc power source is connected to the dc-link capacitors of the APF converter. Therefore, dc-link voltage oscillations are more likely to be generated. And given interactions exist between dc-link voltage oscillations and ac current harmonics, the output of the outer voltage loop will affect the current control loop, inevitably impairing the harmonic-compensation performance. In this article, different from previous solutions, the oscillated dc-link voltage command will be mathematically derived and utilized to enhance the harmonic-compensation performance.

In the proposed 3L APF control strategy, it is quite important to precisely calculate the oscillated dc-link voltage command. However, the calculation of dc-link voltage oscillations includes integration algorithms, which can cause the dc bias issue. The dc bias can be generated in two cases if the pure integration is employed. The first case is caused by the starting point or the initial condition of the pure integration, which may lead to a dc bias at the output of the integrator. The second is related to the dc component in the input signal of the integrator, even with a quite small value, an increasing or decreasing dc bias will be generated, finally leading to the saturation of the integration [26].

Considering multi ac components exist in the oscillated dc-link voltage, the multiple second-order generalized integrator frequency-locked loop (MSOGI-FLL) can be utilized for the integration. The MSOGI-FLL has already been applied in several applications [26], [27], [28], [29], [30]. For example, in [27] the MSOGI-FLL is proposed for estimating not only the positive- and negative-sequence components of the power signal at the fundamental frequency but also other sequence components at harmonic frequencies. The flux estimator is implemented in [26] based on the MSOGI-FLL to output precise motor flux over a wide speed range. The MSOGI-FLL is adopted in [28] as a prefiltering stage under the various grid disturbances to enhance the converter synchronization during frequency drift. In [29] the MSOGI-FLL reference current generation strategy is implemented for the APF to mitigate the current harmonics by extracting the fundamental constituents from the nonlinear load currents. The MSOGI-FLL in [30] is employed for eliminating the current measurement noise and enhancing the phase angle tracking performance in the encoderless control of permanent magnet assisted synchronous reluctance generator based-stator current vector for wind generation systems. Different from the above MSOGI-FLL applications, in this article, an improved MSOGI-FLL with low-pass filters (LPFs) is designed for eliminating the dc bias, and the dc-link voltage oscillation command is calculated by the improved MSOGI-FLL, to enhance the harmonic-compensation performance of the 3L APF.

The main contribution of this article lies in the following aspects. First, the interaction between dc-link voltage oscillations and ac currents is analyzed, and the dc-link voltage oscillations caused by ac current harmonics in 3L APF converters are mathematically derived. Second, to eliminate the dc bias in the integration for calculating the oscillated dc-link voltage command, an improved MSOGI-FLL with LPFs is designed. Third, an improved 3L APF control strategy utilizing the oscillated dc-link voltage command is proposed. Compared with the conventional double-loop control strategy, the influence of the voltage loop on the current loop is suppressed, and the harmonic-compensation performance is effectively enhanced. Meanwhile, a fast dynamic performance of the dc-link voltage can still be guaranteed in the proposed strategy.

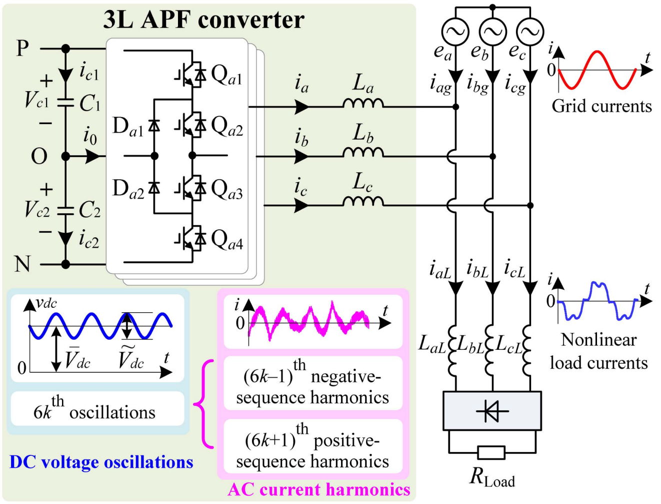


Fig. 1. DC-link voltage oscillations caused by AC current harmonics in 3L APF converters.

The rest of this article is organized as follows. In Section II, the dc-link voltage oscillations in 3L APF are mathematically derived. Section III presents the concept of the proposed 3L APF control strategy by utilizing the oscillated dc-link voltage command. In Section IV, the dc bias issue in the integration is presented, and an improved MSOGI-FLL with LPFs is designed for eliminating the dc bias. The effectiveness of the improved 3L APF control strategy is verified by simulations and experiments in Section V and Section VI, respectively. Finally, Section VII concludes this article.

II. MATHEMATICAL DERIVATION OF DC-LINK VOLTAGE OSCILLATIONS IN 3L APF

Fig. 1 shows the paralleled 3L APF system. The output currents i_a, i_b, i_c are used to compensate the harmonics in nonlinear load currents i_{aL}, i_{bL}, i_{cL}, so that the quality of the grid currents i_{ag}, i_{bg}, i_{cg} can be enhanced. However, there are interactions between dc-link voltage oscillations and ac output current harmonics. The interactions can inevitably impair the harmonic-compensation performance, which will be analytically derived as follows.

The negative-sequence $(6k-1)$th order harmonics can be expressed as

$$\begin{cases} i_{(6k-1)a} = I_{(6k-1)}\cos[(6k-1)\omega_1 t + \theta_{(6k-1)}] \\ i_{(6k-1)b} = I_{(6k-1)}\cos\left[(6k-1)\omega_1 t + \theta_{(6k-1)} + 2\pi/3\right] \\ i_{(6k-1)c} = I_{(6k-1)}\cos\left[(6k-1)\omega_1 t + \theta_{(6k-1)} - 2\pi/3\right] \end{cases} \quad (1)$$

TABLE I
EXPRESSION DERIVATION OF DC-LINK VOLTAGE OSCILLATIONS CAUSED BY PHASE A BRIDGE

Interval	$m_a \geq 0$ $i_{(6k-1)a} \geq 0$	$m_a < 0$ $i_{(6k-1)a} \geq 0$	$m_a < 0$ $i_{(6k-1)a} < 0$	$m_a \geq 0$ $i_{(6k-1)a} < 0$
Charge/discharge dc-link capacitors	Discharge	Charge	Discharge	Charge
Duty cycle during charge/discharge	$d_a = m_a$	$d_a = -m_a$	$d_a = -m_a$	$d_a = m_a$
Increased/decreased dc-link voltage	Decreased by $m_a i_{(6k-1)a} T_s/C_{dc}$	Increased by $-m_a i_{(6k-1)a} T_s/C_{dc}$	Decreased by $-m_a i_{(6k-1)a} T_s/C_{dc}$	Increased by $m_a i_{(6k-1)a} T_s/C_{dc}$
Unified dc-link voltage oscillations	$m_a i_{(6k-1)a} T_s/C_{dc}$			

where $(6k-1)\omega_1$, $I_{(6k-1)}$, and $\theta_{(6k-1)}$ are the frequency, the amplitude, and the phase angle of the negative-sequence $(6k-1)$th order harmonics, respectively.

The ideal three-phase modulation waves are defined as

$$\begin{cases} m_a = M\cos(\omega_1 t + \theta) \\ m_b = M\cos(\omega_1 t + \theta - 2\pi/3) \\ m_c = M\cos(\omega_1 t + \theta + 2\pi/3) \end{cases} \tag{2}$$

where M and θ are the modulation index and the phase angle, respectively.

The charge and discharge of dc-link capacitors in the neutral point clamped (NPC) 3L APF converter are illustrated in Fig. 2. Four cases are considered according to different polarities of modulation waves and currents. Taking Fig. 2(a) with $m_a \geq 0$ and $i_{(6k-1)a} \geq 0$ as an example, the modulation wave m_a is compared with cascaded carriers generating the complementary drive pulses S_{a1} and S_{a3}. When S_{a1} is high turning Q_{a1} ON, dc-link capacitors will be discharged by the current boosting path, decreasing the dc-link voltage. It should be noted that, the current flowing in/out of the dc-link midpoint can only generate the midpoint oscillations, but it does not affect the total dc-link voltage oscillations.

If the amplitudes of triangle carriers are set as 1, the duty cycle of current boosting path d_a will be equal to m_a. The expressions of dc-link voltage oscillations caused by Phase A bridge can be concluded in Table I and unified as

$$\Delta V'_{\mathrm{dc}N} = \frac{m_a i_{(6k-1)a} T_s}{C_{\mathrm{dc}}} \tag{3}$$

where C_{dc} equals to the upper or lower dc-link capacitance, i.e., $C_{\mathrm{dc}} = C_1 = C_2$, and T_s is the switching period.

Considering the influence of all three-phase bridges, the dc-link voltage oscillations in one switching period T_s can be further derived as

$$\Delta V_{\mathrm{dc}N} = \frac{T_s}{C_{\mathrm{dc}}}\left(m_a i_{(6k-1)a} + m_b i_{(6k-1)b} + m_c i_{(6k-1)c}\right). \tag{4}$$

Submitting (1) and (2) in (4), the oscillations generated by the negative-sequence $(6k-1)$th current harmonics can be finally derived as

$$\tilde{V}^*_{\mathrm{dc}N} = \int \frac{\Delta V_{\mathrm{dc}N}}{T_s} dt = \frac{I_{(6k-1)} M}{4k\omega_1 C_{\mathrm{dc}}} \cdot \sin[6k\omega_1 t + \theta_{(6k-1)} + \theta)]. \tag{5}$$

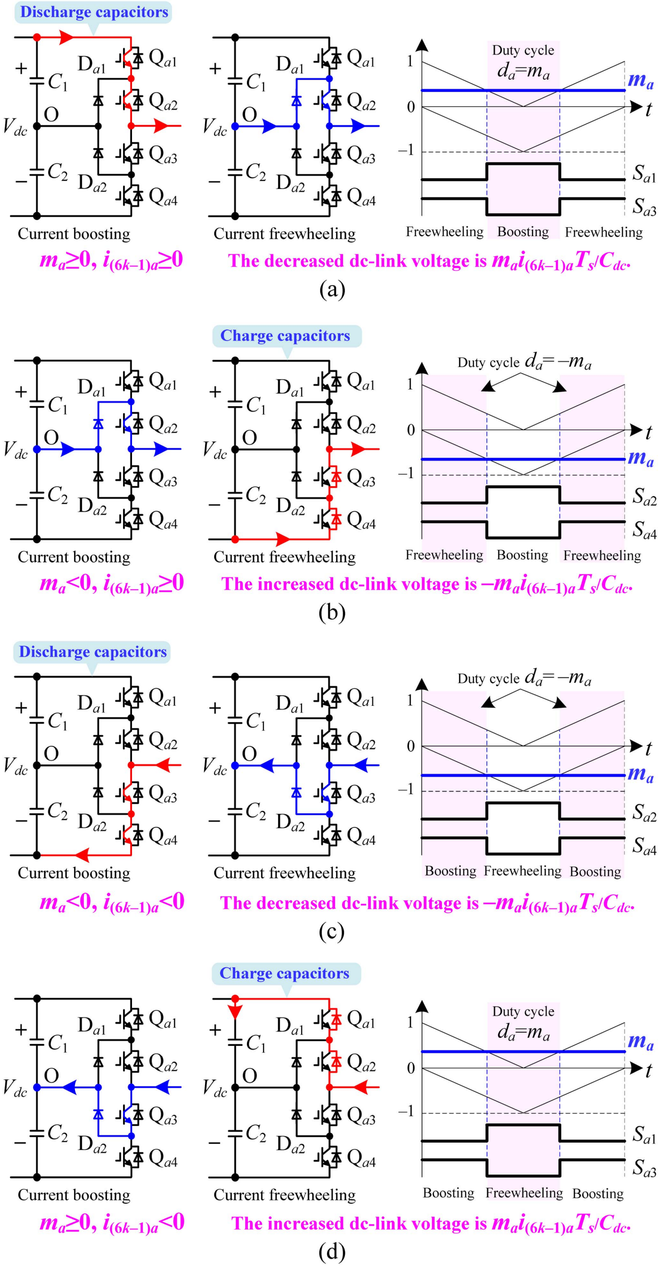


Fig. 2. Charge and discharge of dc-link capacitors in the NPC 3L APF converter. (a) $m_a \geq 0$ and $i_{(6k-1)a} < 0$. (b) $m_a \geq 0$ and $i_{(6k-1)a} \geq 0$. (c) $m_a < 0$ and $i_{(6k-1)a} \geq 0$. (d) $m_a < 0$ and $i_{(6k-1)a} < 0$.

Similarly, with the positive-sequence $(6k+1)$th current harmonics, the dc-link voltage oscillations can be derived as

$$\tilde{V}^*_{\mathrm{dc}P} = \int \frac{\Delta V_{\mathrm{dc}P}}{T_s} dt = \frac{-I_{(6k+1)} M}{4k\omega_1 C_{\mathrm{dc}}} \cdot \sin\left[6k\omega_1 t + \theta_{(6k+1)} - \theta\right]. \tag{6}$$

It can be indicated based on (5) and (6) that, the negative-sequence $(6k-1)$th harmonics and the positive-sequence $(6k+1)$th harmonics can both generate $6k$th dc-link voltage oscillations. Conversely, the dc-link voltage oscillations can also affect the ac output currents, which will further impair the harmonic-compensation performance.

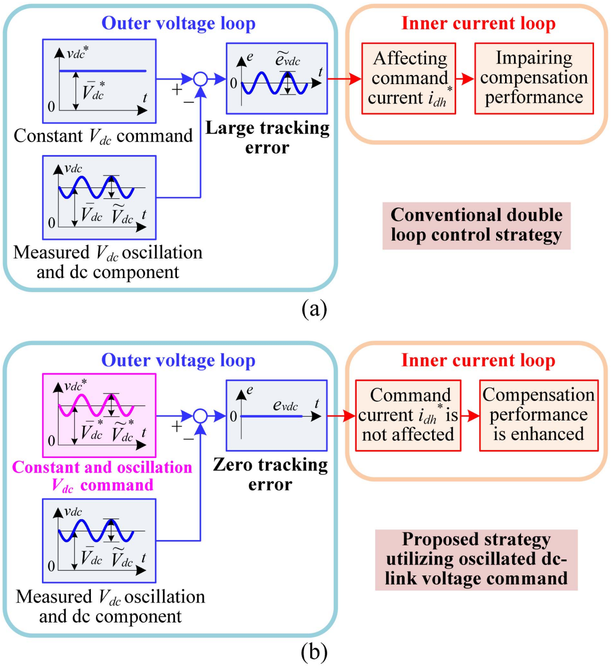


Fig. 3. Issues and improvements of voltage control loops for the 3L APF. (a) Issues in the conventional double-loop control strategy. (b) Improvements in the proposed strategy utilizing the oscillated dc-link voltage command.

In this article, a new control strategy will be proposed, where the calculated dc-link voltage oscillations are added as the command of the voltage control loop, to enhance the ability of compensating harmonic currents from nonlinear loads.

III. Improved 3L APF Control Strategy Utilizing the Oscillated DC-Link Voltage Command

Issues and improvements of voltage control loops for the 3L APF are illustrated in Fig. 3. As seen in Fig. 3(a), with the conventional double-loop control strategy, the constant command $\bar{V}_{\mathrm{dc}}^*$ is given to the outer voltage loop. Both dc and oscillated components $\bar{V}_{\mathrm{dc}}+\tilde{V}_{\mathrm{dc}}$ can be measured in the feedback dc-link voltage. A large tracking error is therefore generated, which will further affect the *d*-axis command current i_{dh}^*, and impair the harmonic-compensation performance.

To avoid the influence of the outer dc-link voltage loop, this article proposes an improved strategy, as presented in Fig. 3(b). In the outer voltage loop, the calculated dc-link voltage oscillation in Section II is added as the command of the dc-link voltage loop. The constant and oscillated voltage command $\bar{V}_{\mathrm{dc}}^*+\tilde{V}_{\mathrm{dc}}^*$ can together counteract the measured dc and oscillated components $\bar{V}_{\mathrm{dc}}+\tilde{V}_{\mathrm{dc}}$ in the feedback path, thus, a zero tracking error will be achieved. Consequently, the influence of the outer dc-link voltage loop on the current loop can be eliminated, and the harmonic-compensation performance will be enhanced.

Based on the idea in Fig. 3(b), the improved 3L APF control strategy utilizing the oscillated dc-link voltage command is further shown in Fig. 4 more specifically. Variables are transformed from *abc* coordinate to *dq* coordinate, where the output currents are controlled by proportional-integral-resonant

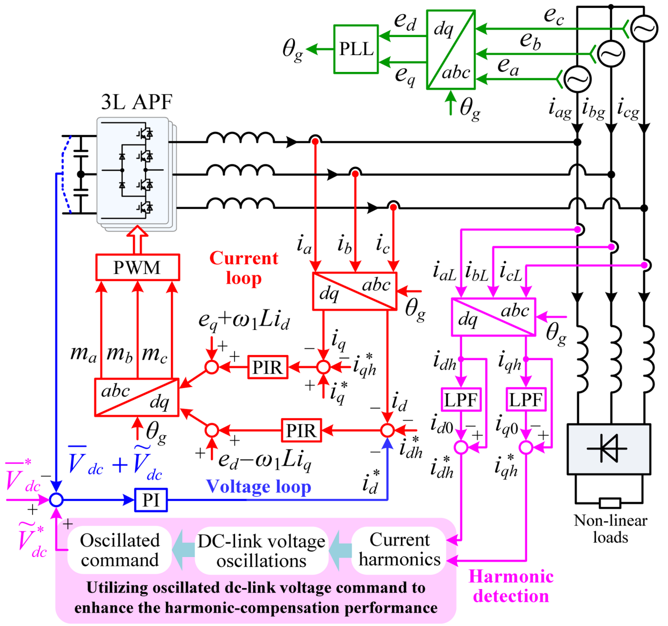


Fig. 4. Proposed 3L APF control strategy utilizing the oscillated DC-link voltage command to enhance the harmonic-compensation performance.

(PIR) controllers. In the harmonic detection, the nonlinear load currents i_{aL}, i_{bL}, and i_{cL} are first transformed as i_{dh} and i_{qh} in the *dq* coordinate, which contain both dc and multi ac components. Then, the LPFs are adopted to eliminate the ac components obtaining the pure dc components i_{d0} and i_{q0}. Afterwards, subtract i_{d0} and i_{q0} from i_{dh} and i_{qh}, obtaining the current harmonics i_{dh}^* and i_{qh}^* in the *dq* coordinate. It can be noted that, in the above harmonic detection process, the LPFs are used for obtaining the pure dc components i_{d0} and i_{q0}, which therefore will not cause phase delays.

After the harmonics in nonlinear load currents are extracted, the current commands with equal amplitudes and opposite phases are given to the current loop, to compensate the current harmonics in nonlinear loads. In the dc-link voltage loop, the oscillated dc-link voltage command is added to enhance the harmonic-compensation performance.

In the proposed 3L APF control strategy, it is quite important to precisely calculate the oscillated dc-link voltage command. However, the calculation of dc-link voltage oscillations in (5) and (6) includes integration algorithms, which can cause the dc bias issue. In the following section, the dc bias issue will be analyzed and solved.

IV. Elimination of the DC Bias in the Integration for Calculating DC-Link Voltage Oscillations

A. DC Bias Issue in the Pure Integration

Issues of the conventional $1/s$ pure integration are illustrated in Fig. 5. Two cases can cause the dc bias. The first case is shown in Fig. 5(a), where the integration is started at different transients. Note that, the integration results have been enlarged by ω for the convenient of comparison. As seen, even though no sampling dc

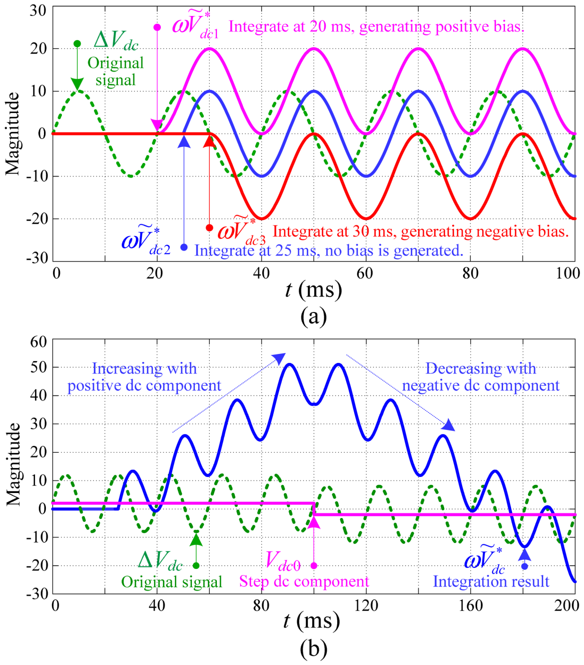


Fig. 5. Issues in the pure integration. (a) DC biases caused by the integration started at different transients. (b) Increasing/decreasing trends with different DC biases in the original signal.

component exists in the original signal ΔV_{dc}, different biases can still exist in the integration results with different starting transients. The second case is shown in Fig. 5(b), a positive-to-negative step dc component V_{dc0} is intentionally injected to the original signal. As seen, with a positive dc component, the dc bias will gradually increase in the integration result $\tilde{V}_{\mathrm{dc}}^*$. While with a negative dc component, the dc bias will gradually decrease in $\tilde{V}_{\mathrm{dc}}^*$.

In the proposed strategy shown in Fig. 4, before the calculated dc-link voltage oscillation is added to the command of the voltage loop, the dc bias in the integration result must be eliminated. Otherwise, the calculated dc-link voltage oscillation with dc bias will affect the control of dc-link voltage, even causing the instability of the 3L APF system.

B. DC Bias Issue in the Conventional SOGI-FLL

Other than adopting the conventional $1/s$ pure integration, the SOGI-FLL [31], [32], [33], [34] can be adopted to indirectly implement the integration in (5) and (6). Fig. 6 shows the integration implemented by the SOGI-FLL. The corresponding characteristic transfer functions can be given by

$$D(s) = \frac{\Delta V_{\mathrm{dc}}{'}(s)}{\Delta V_{\mathrm{dc}}(s)} = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \tag{7}$$

$$Q(s) = \frac{q\Delta V_{\mathrm{dc}}{'}(s)}{\Delta V_{\mathrm{dc}}(s)} = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \tag{8}$$

where ω' represents the frequency tracked by the FLL, $\Delta V_{\mathrm{dc}}{'}$(s) and $q\Delta V_{\mathrm{dc}}{'}$(s) are two in-quadrature signals.

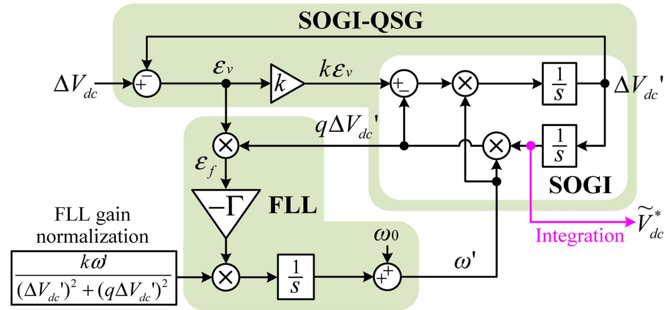


Fig. 6. Integration algorithm implemented by the conventional SOGI-FLL.

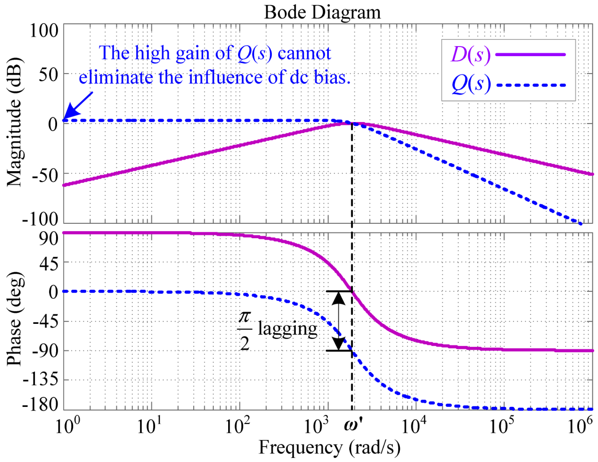


Fig. 7. Frequency responses of $D(s)$ and $Q(s)$ with $\omega' = 600\pi$ and $k = \sqrt{2}$.

Fig. 7 shows the responses plotted based on (7) and (8). As seen, $D(s)$ has a unit gain without phase shift at $\omega' = 600\pi$, indicating the SOGI-FLL can track the sixth-order dc-link voltage oscillation without errors. $Q(s)$ has a unit gain while the phase is delayed by $\pi/2$, thus, it can be taken as the integration result of the sixth-order signal. However, $Q(s)$ has low-pass filtering characteristics, which cannot eliminate the influence of very low-frequency signals and the dc bias. Therefore, in this article, an improved SOGI-FLL with dc bias elimination will be designed.

C. Improved SOGI-FLL With DC Bias Elimination

To overcome the dc bias issue, a LPF is added to the feedback path of the conventional SOGI-FLL, as shown in Fig. 8. The transfer function of the LPF can be expressed as

$$L(s) = \frac{v_{\mathrm{out}}(s)}{v_{\mathrm{in}}(s)} = \frac{k_0}{k_0 + s}. \tag{9}$$

The cut-off frequency ω_c of the LPF is equal to the gain k_0, which is selected as a relatively low-frequency of 4π (2 Hz) in this article, so that the dc bias of the input signal can be preciously extracted regardless of the influence from the other low-frequency components. Compared with the conventional SOGI-FLL in Fig. 7, only "k_0" and "$1/s$" are added in the diagram of the improved SOGI-FLL, as presented in Fig. 8. With the

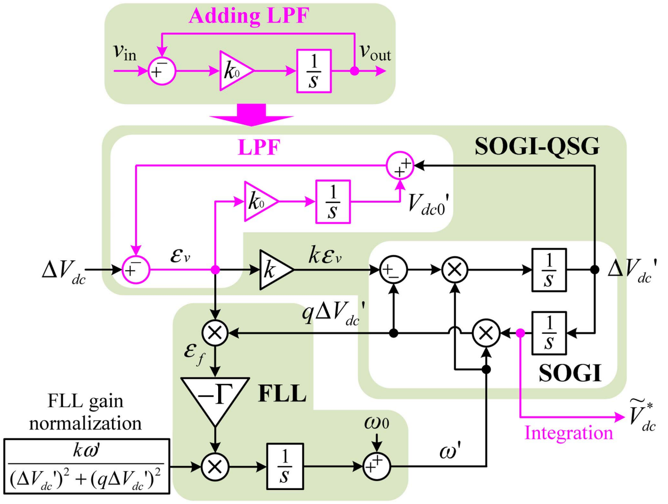


Fig. 8. Improved SOGI-FLL with a LPF added for eliminating the DC bias in the integration.

added LPF, the dc bias $V_{\mathrm{dc}0}$' in the tracking error ε_v is extracted and added in the feedback path, no extra phase delay will be generated in ac components.

With the added LPF, the transfer function of the improved SOGI-FLL in Fig. 8 can be derived as

$$Q'(s)=\frac{q\Delta V_{\mathrm{dc}}'(s)}{\Delta V_{\mathrm{dc}}(s)}=\frac{k\omega' s}{s^3+(k_0+k\omega')s^2+\omega'^2 s+k_0\omega'^2}. \tag{10}$$

Submitting $s=j\omega$ and $\omega=0$ (representing the dc bias) in (10), $Q'(s)$ can be calculated as 0. It is, therefore, theoretically verified that, the improved SOGI-FLL can effectively eliminate the dc bias of the input signal.

Fig. 9 shows the root locus of the improved SOGI-FLL. As seen, with varying k and k_0, all the roots are located at the left coordinate. The stability of the improved SOGI-FLL is, thus, proved. Fig. 10 shows the frequency responses of the conventional and improved SOGI-FLL. As seen, at different center frequencies, both the two SOGI-FLL schemes can achieve the same gain and phase responses as the pure integrator. While the improved SOGI-FLL has obvious lower gains at low frequencies, and presenting an ability on dc bias elimination.

To test the improved SOGI-FLL, ΔV_{dc} is structured by injecting a step dc component $V_{\mathrm{dc}0}$ into a sixth-order oscillation signal. The test results are presented in Fig. 11. As seen in Fig. 11(b), the dc bias $V_{\mathrm{dc}0}$' is gradually extracted by the added LPF. The steady state of Fig. 11(a) is zoomed in as Fig. 11(c). As seen, the dc bias has been successfully suppressed in the tracking signal $\Delta V_{\mathrm{dc}}'$, and no dc bias exists in the integration result $\tilde{V}_{\mathrm{dc}}^*$ as well.

More complicated situation is further analyzed, considering the dc-link voltage oscillations contain dc and multi ac components. Another signal is structured to further test the SOGI-FLL, which contains a sixth-order oscillation, a 12th-order oscillation, and a dc step signal, as expressed by

$$\Delta V_{dc}=\underbrace{10\sin(6\omega_1 t)}_{\text{6th oscillation}}+\underbrace{3\sin(12\omega_1 t+\pi/24)}_{\text{12th oscillation}}+\underbrace{2\varepsilon(t-0.1)}_{\text{dc component}}. \tag{11}$$

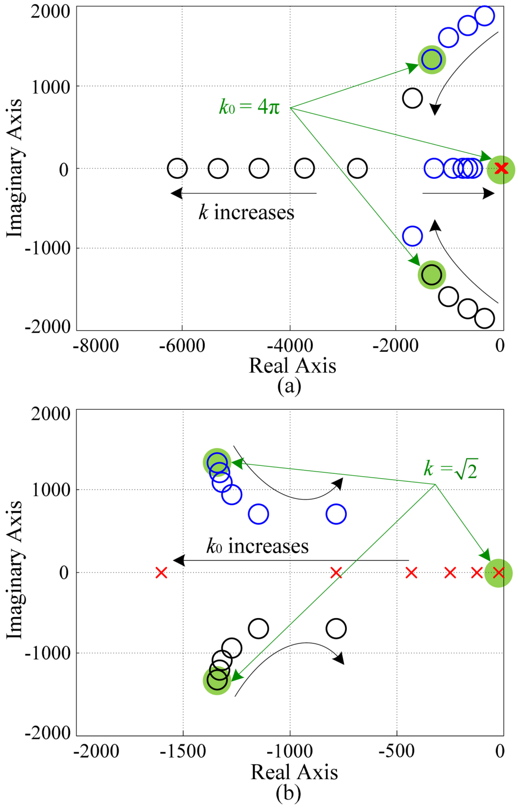


Fig. 9. Root locus of the improved SOGI-FLL. (a) With varying k ($k_0=4\pi$). (b) With varying k_0 ($k=\sqrt{2}$).

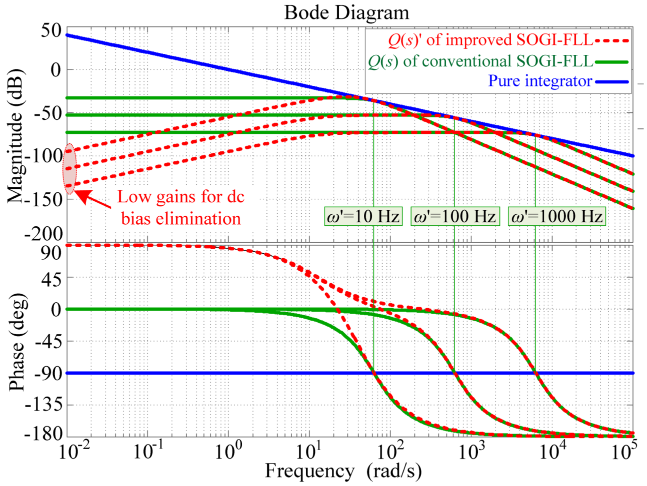


Fig. 10. Frequency responses of the conventional and improved SOGI-FLL with different center frequencies ($k_0=4\pi$ and $k=\sqrt{2}$).

The test results are presented in Fig. 12. Though the dc bias $V_{\mathrm{dc}0}$' can still be extracted in Fig. 12(b), but in Fig. 12(c) the shape of the tracking signal $\Delta V_{\mathrm{dc}}'$ has been changed compared with the input signal ΔV_{dc} due to the influence of the multi ac components. Consequently, the integration results will be no longer accurate. Therefore, an improved MSOGI-FLL with

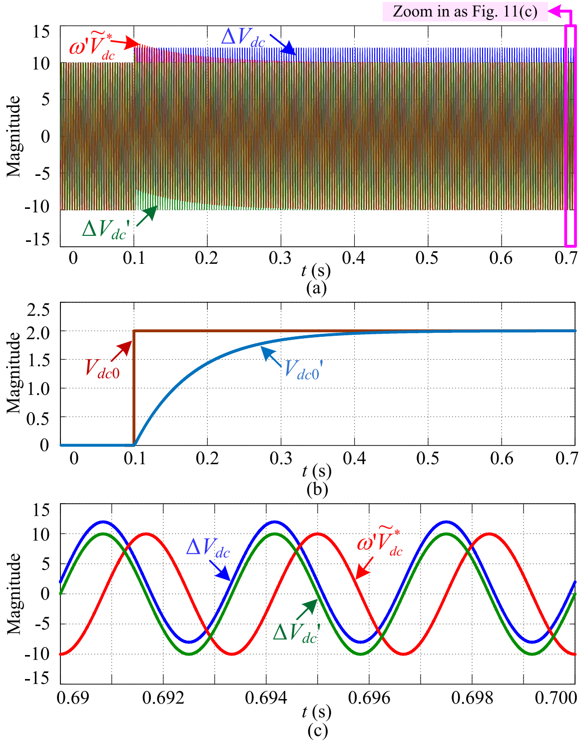


Fig. 11. Integration performance of the improved SOGI-FLL with sixth-order oscillation signal. (a) Structured signal ΔV_{dc}, the tracking signal $\Delta V_{\mathrm{dc}}'$, and the integration result $\omega\ \tilde{V}_{\mathrm{dc}}^{*}$. (b) Step dc component V_{dc0} and the extracted dc bias V_{dc0}'. (c) Signals in the steady state.

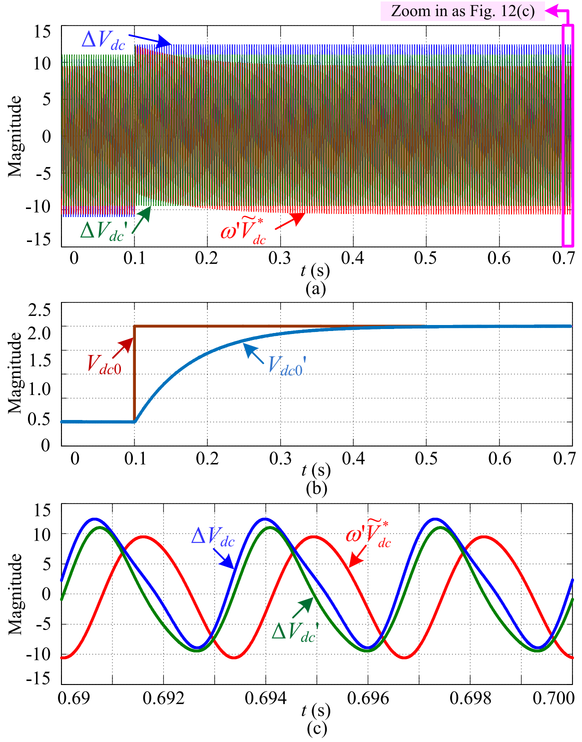


Fig. 12. Integration performance of the improved SOGI-FLL with DC and multi AC components. (a) Structured signal ΔV_{dc}, the tracking signal ΔV_{dc}', and the integration result $\omega\ \tilde{V}_{\mathrm{dc}}^{*}$. (b) Step DC component V_{dc0} and the extracted DC bias V_{dc0}'. (c) Signals in the steady state.

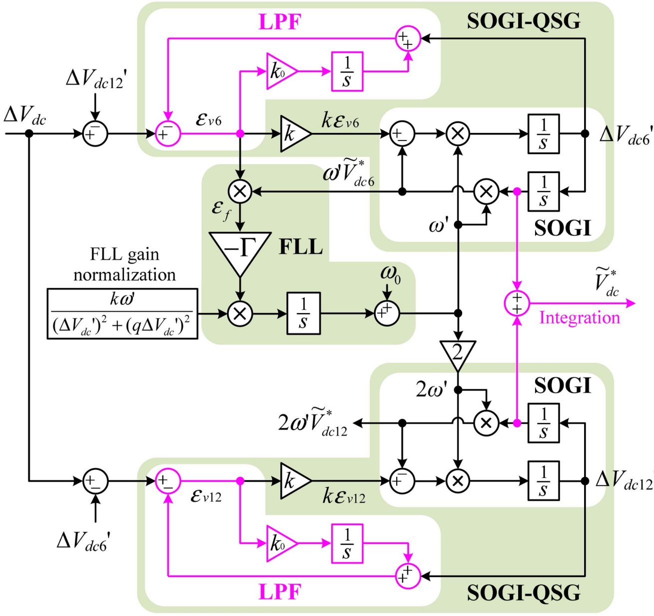


Fig. 13. Improved MSOGI-FLL with LPFs for eliminating the DC bias in the integration.

dc-bias elimination will be further designed for the application with multi ac components.

D. Improved MSOGI-FLL With DC Bias Elimination

Given the 3L APF is mainly used to compensate harmonics of low frequencies, the improved MSOGI-FLL for integrating the 6th- and 12th-order components is designed, as shown in Fig. 13. Correspondingly, the compensation performance of the negative 5th- and 11th-order harmonics, as well as the positive 7th- and 13th-order harmonics can be improved.

As seen in Fig. 13, the 12th-order frequency $2\omega'$ is doubled based on ω' which is tracked by the FLL. And compared with the conventional MSOGI-FLL, two LPFs are added to the feedback paths, so that the dc bias can be eliminated in the integration result.

The structured signal in (11) with dc and multi ac components is adopted again to test the integration performance of the improved MSOGI-FLL. The test results are shown in Fig. 14, where the dc component V_{dc0}' is gradually extracted by the added LPF. The steady states of Fig. 14(a) and (b) are zoomed in as Fig. 14(d) and (e), respectively. As seen, the 6th-order integration term $\omega'\tilde{V}_{\mathrm{dc6}}{}^{*}$ and the 12th-order integration term $2\omega'\tilde{V}_{\mathrm{dc12}}{}^{*}$ are effectively extracted, and the dc component is effectively suppressed. The final integration result of $\tilde{V}_{\mathrm{dc}}^{*}$ can be obtained by adding $\tilde{V}_{\mathrm{dc6}}{}^{*}$ and $\tilde{V}_{\mathrm{dc12}}{}^{*}$.

V. SIMULATION RESULTS OF THE IMPROVED 3L APF STRATEGY UTILIZING THE OSCILLATED DC-LINK VOLTAGE COMMAND

To test the improved 3L APF strategy, the negative-sequence fifth-order harmonics in (12), and the negative-sequence fifth and positive-sequence seventh-order combined harmonics in

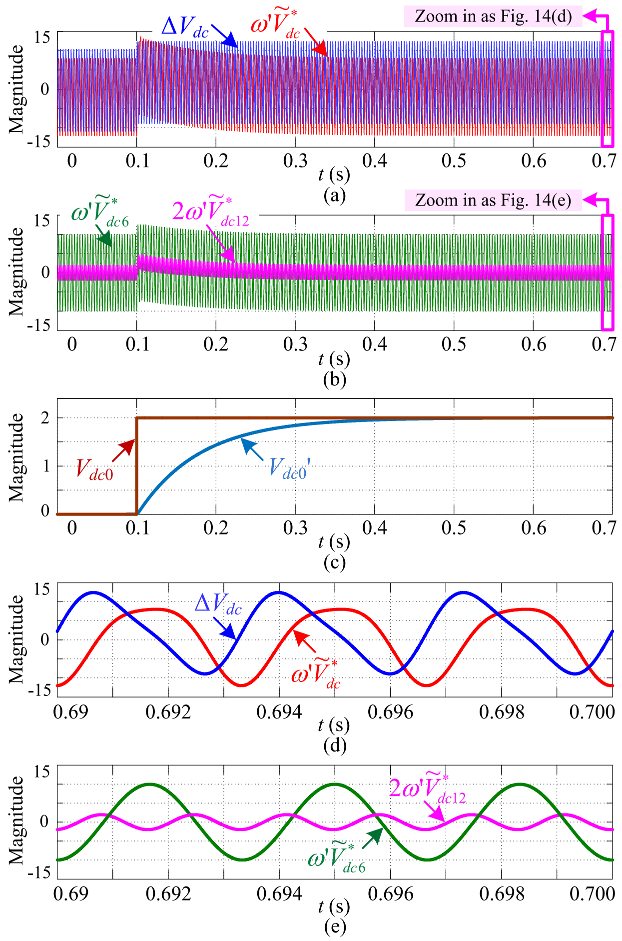


Fig. 14. Integration results of the designed MSOGI-FLL. (a) Structured signal $\Delta V_{\rm dc}$ and the integration result $\omega\ \tilde{V}^*_{\rm dc}$. (b) Sixth-order integration term $\omega'\tilde{V}_{\rm dc6}{}^*$ and the 12th order integration term $2\omega'\tilde{V}_{\rm dc12}{}^*$. (c) Step DC component $V_{\rm dc0}$ and the extracted DC bias $V_{\rm dc0}$'. (d) $\Delta V_{\rm dc}$ and $\omega\ \tilde{V}^*_{\rm dc}$ in the steady state. (e) $\omega'\tilde{V}_{\rm dc6}{}^*$ and $2\omega'\tilde{V}_{\rm dc12}{}^*$ in the steady state.

(13) are given to the current loop as commands, respectively, as follows:

$$\begin{cases} i^*_{5Na} = 10\cos(5\omega_1 t) \\ i^*_{5Nb} = 10\cos(5\omega_1 t + 2\pi/3) \\ i^*_{5Nc} = 10\cos(5\omega_1 t - 2\pi/3) \end{cases} \tag{12}$$

$$\begin{cases} i^*_{57a} = 10\cos(5\omega_1 t) + 2\cos(7\omega_1 t) \\ i^*_{57b} = 10\cos(5\omega_1 t + 2\pi/3) + 2\cos(7\omega_1 t - 2\pi/3) \\ i^*_{57c} = 10\cos(5\omega_1 t - 2\pi/3) + 2\cos(7\omega_1 t + 2\pi/3). \end{cases} \tag{13}$$

The diagram of the improved 3L APF strategy in Fig. 15 is adopted to generate fifth- and seventh-order current harmonics. As seen, the dc-link voltage oscillation is calculated by the integration based on (4), which is implemented by the improved SOGI-FLL. Besides the harmonic current commands i^*_{dh} and i^*_{qh} given to the inner current loop, the calculated dc-link voltage oscillation $\tilde{V}^*_{\rm dc}$ is employed as an extra command of outer dc-link voltage loop.

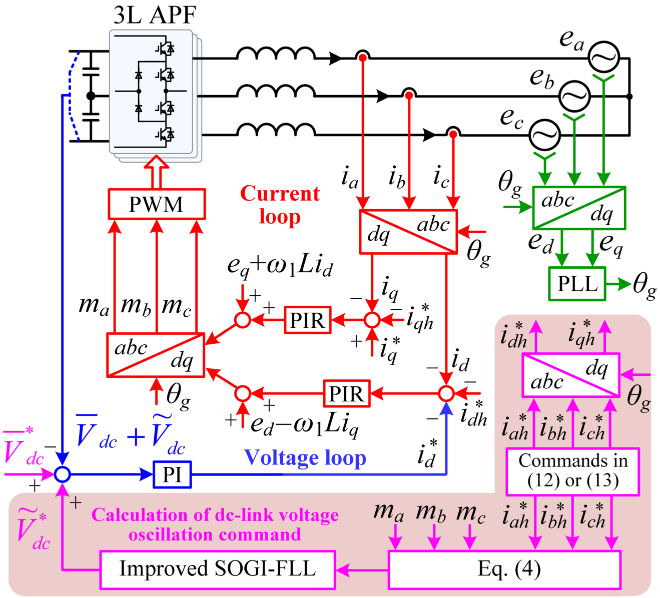


Fig. 15. Improved strategy utilizing the oscillated DC-link voltage command for generating fifth- and seventh-order current harmonics.

The simulated current harmonics are shown in Figs. 16 and 17. As seen in Fig. 16, with a constant dc-link voltage command, large errors exist between the dc-link voltage command $\bar{V}^*_{\rm dc}$ and the measured dc-link voltage $\bar{V}_{\rm dc} + \tilde{V}_{\rm dc}$, as well as between the output currents and the command currents. After the improved 3L APF strategy is applied, the dc-link voltage successfully tracks the oscillated command. And the fifth-order current harmonics are successfully generated, which can be further utilized to compensate the harmonics in nonlinear load currents. In Fig. 17, the negative-sequence fifth and positive-sequence seventh-order combined harmonics are accurately outputted after the improved 3L APF strategy is applied. It can also be seen that, the negative fifth- and positive seventh-order current harmonics are corresponded to the sixth-order dc-link voltage oscillation, which agrees well with the theoretical analysis in Section II. In addition, it can be noted that, high-frequency ripples are superposed on the currents in Figs. 16(b) and 17(b). The peak-to-peak values of current ripples are related to several factors [35], [36], [37], e.g., *L*/*LCL* filters, the converter topology, the switching frequency, the adopted modulation scheme, and the dc-link voltage. The high-frequency current ripple is the inherent characteristic of pulse width modulation (PWM) converters, which cannot be thoroughly avoided.

Finally, Fig. 18 shows the diagram of the improved 3L APF strategy for compensating nonlinear load current harmonics. The dc-link voltage oscillation is calculated by the improved MSOGI-FLL with LPFs, and added to the command of the dc-link voltage loop to enhance the harmonic-compensation performance, which will be tested experimentally in the following section.

VI. EXPERIMENTAL RESULTS

To verify the proposed strategy, a harmonic compensation system is built. As shown in Fig. 19, the grid voltage is obtained

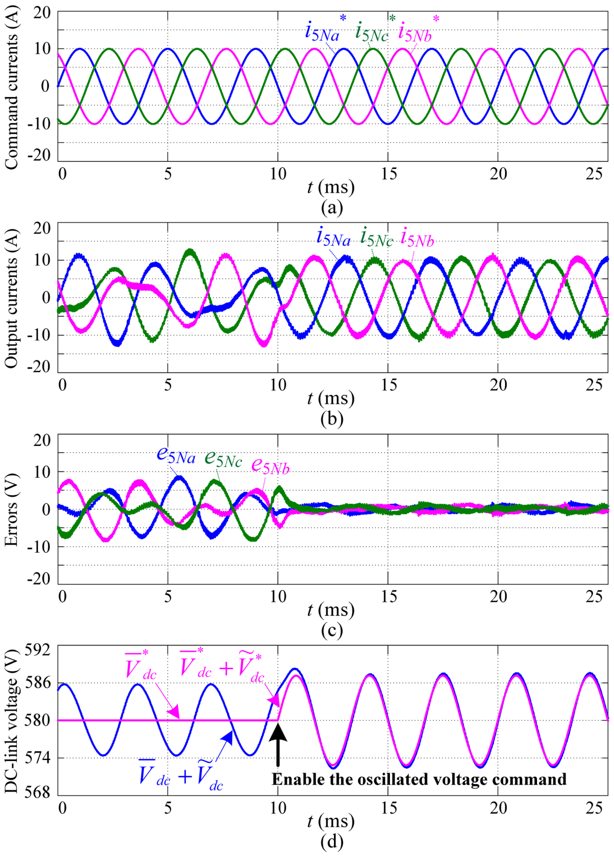


Fig. 16. Simulation results with negative-sequence fifth-order harmonics. (a) Harmonic commands. (b) Output harmonic currents. (c) Current errors. (d) DC-link voltage command and the measured DC-link voltage.

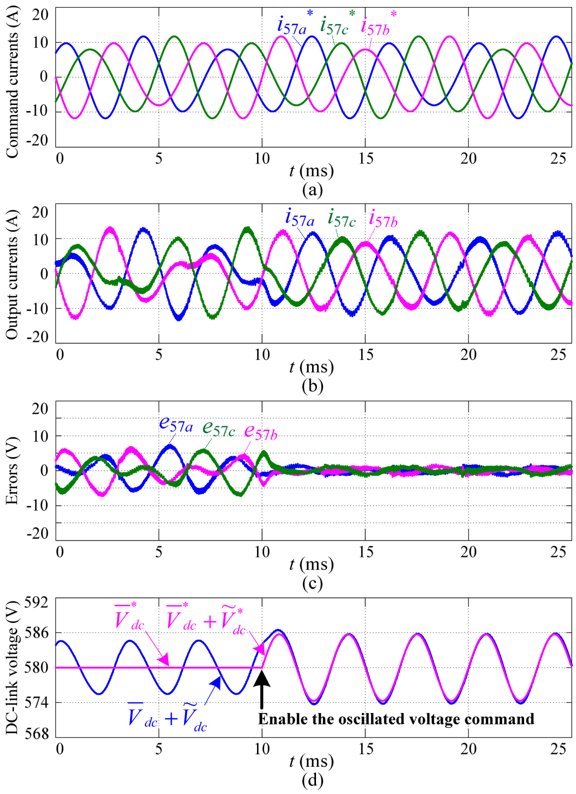


Fig. 17. Simulation results with fifth- and seventh-order harmonics. (a) Harmonic commands. (b) Output harmonic currents. (c) Current errors. (d) DC-link voltage command and the measured DC-link voltage.

TABLE II
PARAMETERS OF THE TEST SYSTEM

Symbol	Parameter	Value
e_a, e_b, e_c	Grid phase voltage (rms)	176 V
$\overline{V}_{dc}^*$	Dc-link voltage command	580 V
C_{dc}	Dc -link capacitance	960 μF
L_a, L_b, L_c	Filter inductance	1 mH
L_{aL}, L_{bL}, L_{cL}	Non-linear load inductance	25 mH
R_{Load}	Non-linear load resistance	27 Ω
f_{PWM}	Switching frequency	10 kHz
f_s	Sampling frequency	20 kHz

from a 380 V/304 V isolation transformer. A three-phase full-bridge diode rectifier is adopted to build the nonlinear load. The 3L APF is designed with the SKiiP 39MLI12T4V1 3L NPC power module, and connected in parallel with the nonlinear load to compensate current harmonics. The conventional double-loop control strategy and the proposed strategy are implement by the TMS320 28377D DSP.

Parameters of the experimental setup are provided in Table II. Regarding the design of the dc-link, usually film capacitors and/or electrolytic capacitors can be adopted as the dc-link capacitors. The film capacitors have the merits of high reliability, high rated voltage, low parasitic inductance, but the volume is large with high prices [38]. Besides, a high value of the dc-link capacitance can increase the filtering performance and the dc-link voltage stability, but the hardware cost will be increased and the dc-link voltage dynamic response will be impaired. In this article, the film capacitors with a total capacitance of 480 μF are adopted in the dc-link, to reach a compromise among low cost, high dc-link voltage stability, high filtering performance, and high reliability. As shown in Fig. 19(b), in the designed main power circuit, six film capacitors are adopted in series-parallel connection. Three upper film capacitors and three lower film capacitors are connected in parallel forming a dc-link capacitance C_{dc} of 960 μF, respectively, and then connected in series forming a total capacitance $C_{\mathrm{dc}}/2$ of 480 μF.

The control frequency and the sampling frequency f_{s} are set as 20 kHz, thus, the control period can be calculated as $1/f_{\mathrm{s}} = 50\ \mu$s. Even though an intensive computation exits in the control strategy, the computation should be always finished within one control period of 50 μs. Therefore, the longest computational delay is within 50 μs. In addition, the sampling delay can be generated by the conditioning circuit, the analog-to-digital converter. The computational and sampling delays have the same influence on the current and voltage control loops for both the conventional and the proposed strategies, e.g., affecting the control accuracy and reducing the control stability [39], [40], [41]. Besides, in the added control loop of the proposed strategy, the computational delay can only slightly affect the calculated dc-link voltage command $\bar{V}_{\mathrm{dc}}^* + \tilde{V}_{\mathrm{dc}}^*$. Regarding the

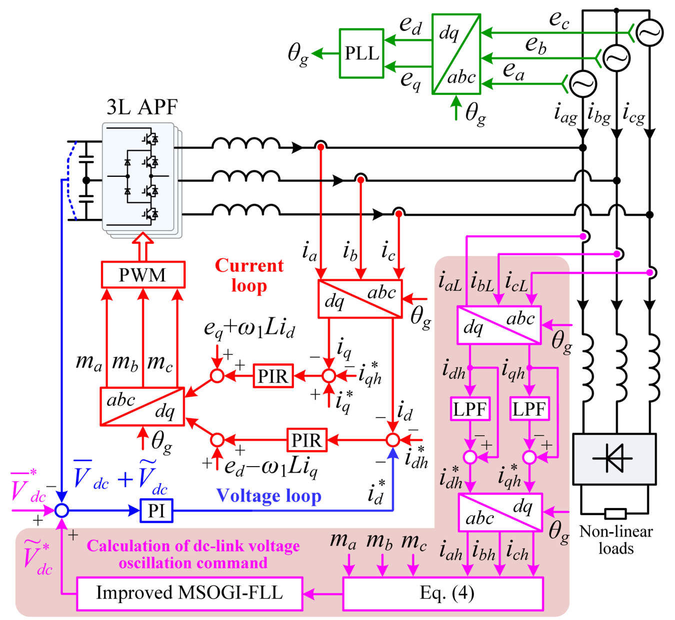
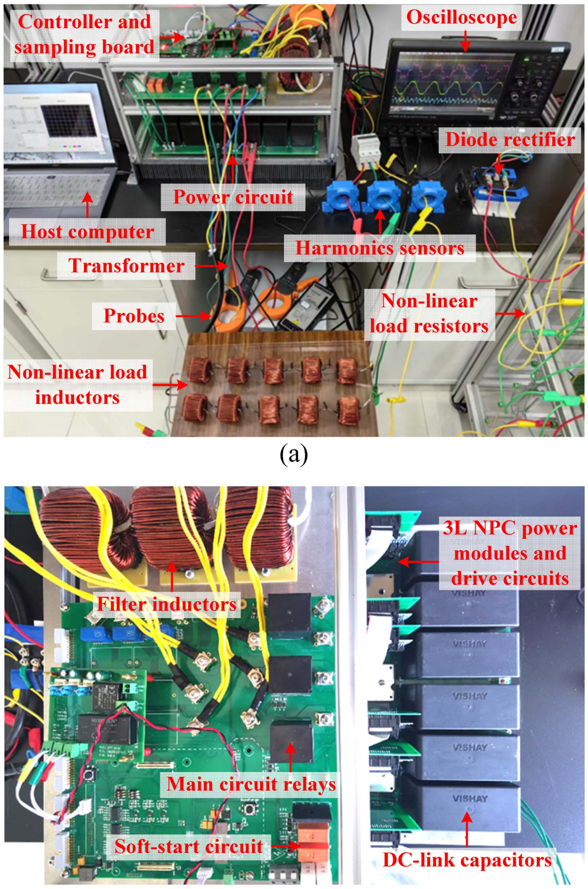


Fig. 18. Improved 3L APF control strategy utilizing the oscillated DC-link voltage command to enhance the harmonic-compensation performance.



(a)

(b)

Fig. 19. Experimental setup. (a) Three-phase 3L APF system. (b) Main power circuit.

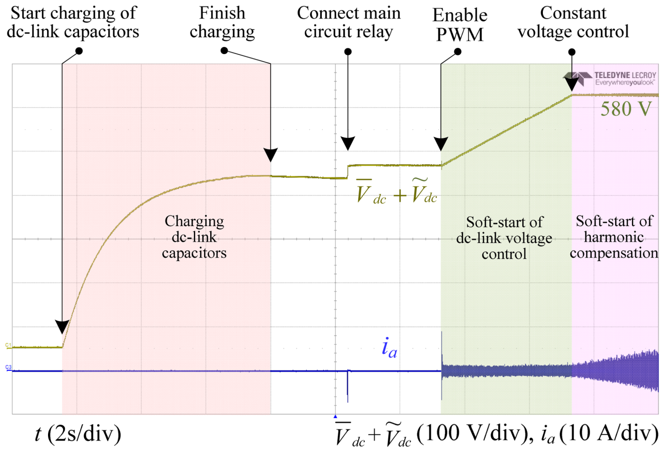


Fig. 20. Start process of the 3L APF system.

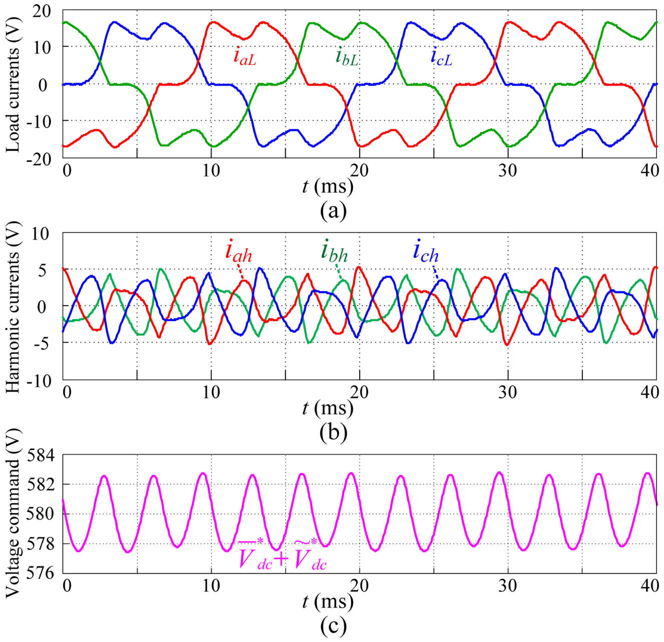


Fig. 21. Experimental results observed by the Ethernet interface software. (a) Nonlinear load currents. (b) Extracted current harmonics. (c) Calculated DC-link voltage oscillations.

influence on the harmonic-compensation performance, the short computational delay can be neglected.

The start process of the APF experiment setup is shown in Fig. 20. First, the dc-link voltage is gradually increased by charging dc-link capacitors with a hardware soft-start circuit. Then, the main circuit relay is connected and the PWM drive pulses are enabled. Afterwards, the dc-link voltage is further increased gradually to the final command value of 580 V by the outer dc-link voltage control loop. Finally, the harmonic compensation command is given in the inner current loop to compensate the current harmonics of the nonlinear load.

For the convenient of debugging and monitoring the experimental setup, an Ethernet interface software is compiled using the Visual Studio, which can observe voltages, currents and

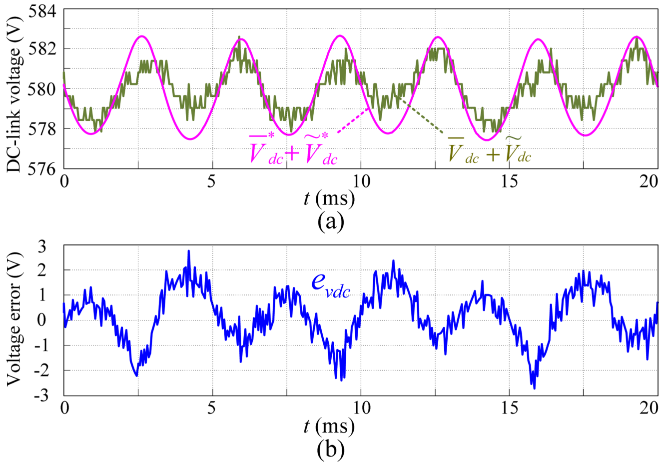


Fig. 22. Experimental results observed by the Ethernet interface software with the conventional double-loop control strategy. (a) Calculated and the sampled DC-link voltage oscillations. (b) DC-link voltage errors.

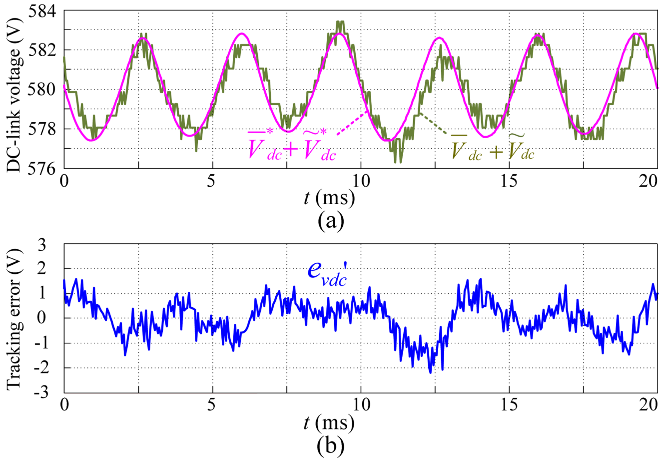


Fig. 23. Experimental results observed by the Ethernet interface software with the proposed strategy. (a) Calculated and the sampled DC-link voltage oscillations. (b) Tracking errors of the DC-link voltage.

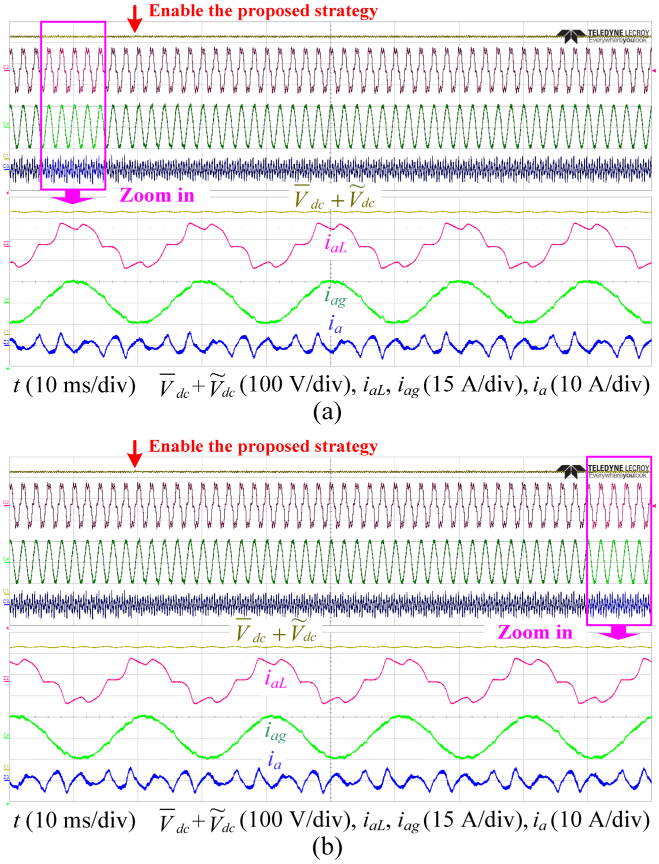
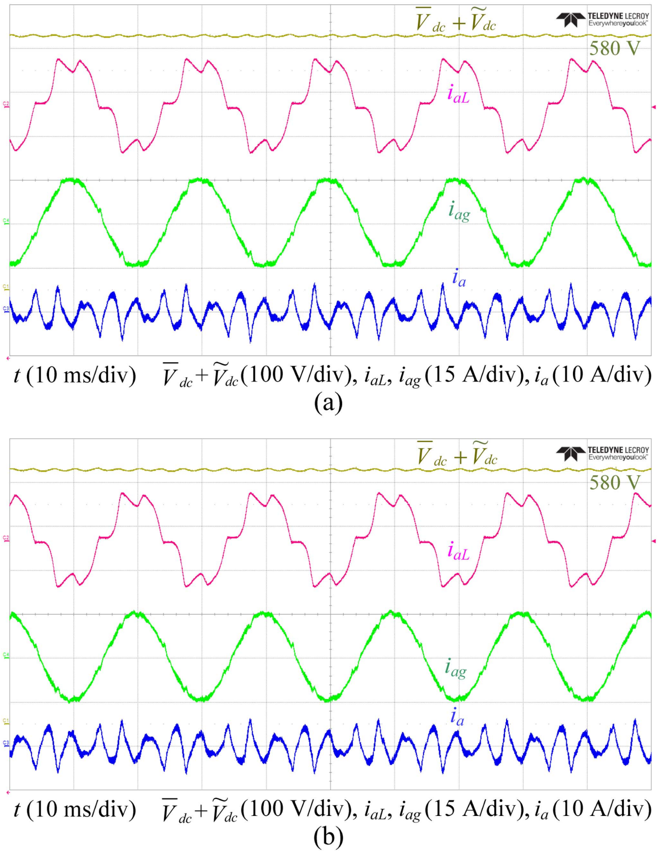


Fig. 24. Dynamic experimental results. (a) Zoomed-in waveforms with the conventional double-loop control strategy. (b) Zoomed-in waveforms with the proposed strategy.

internal-variable waveforms of the 3L APF system. Fig. 21 shows the experimental results observed by the Ethernet interface software. As seen, the current harmonics i_{ah}, i_{bh}, and i_{ch} are extracted from the sampled nonlinear load currents i_{aL}, i_{bL}, and i_{cL}. Then, the oscillated dc-link voltage $\bar{V}_{\mathrm{dc}}^{*}+\tilde{V}_{\mathrm{dc}}^{*}$ is further calculated, which will be further applied as the dc-link voltage command to enhance the harmonic-compensation performance.

Figs. 22 and 23 present the calculated and the sampled dc-link voltage oscillations observed by the Ethernet interface software. With the conventional double-loop control strategy, the calculated dc-link voltage oscillation is not adopted in the outer voltage loop. As seen in Fig. 22, a relative large voltage error $e_{v\mathrm{dc}}$ exists between the sampled and the calculated dc-link voltage oscillations. In the proposed strategy, the calculated dc-link voltage oscillation is added as the command of the voltage control loop. As seen in Fig. 23, the sampled dc-link voltage can overall track the oscillated dc-link voltage command, and a relative lower tracking error $e_{v\mathrm{dc}}{}'$ is achieved. It can be noted in both Figs. 22 and 23 that, though the dc component $\bar{V}_{\mathrm{dc}}^{*}$ in the dc-link voltage command is always set as 580 V, the amplitudes of the oscillated components $\tilde{V}_{\mathrm{dc}}^{*}$ and $\tilde{V}_{\mathrm{dc}}$ cannot be captured exactly the same. Nevertheless, the dc-link voltage error $e_{v\mathrm{dc}}{}'$ with the proposed strategy is always lower than the error $e_{v\mathrm{dc}}$ with the conventional double-loop control strategy. And the enhanced performance of compensating harmonics will be further verified experimentally in the remaining part of this section.

In addition, even with the proposed strategy, a relatively large tracking error $e_{v\mathrm{dc}}{}'$ can still be seen in Fig. 23(b). Several factors, which may cause the relatively large tracking error, have been investigated and optimized in both experiments and simulations, e.g., the controller gain of the dc-link voltage and the sampling bandwidth of the dc-link voltage. It turns out that, the nonideal grid voltage may be the main factor causing the relatively large tracking error $e_{v\mathrm{dc}}{}'$. The 3L APF is essentially a kind of grid-connected converter. When faced with the distorted grid voltage, more harmonics will appear in the output currents. The current harmonics on the ac side will generate extra oscillations in the dc-link voltage [42], [43], which are different from the dc-link voltage oscillations caused by nonlinear load harmonics. In the proposed strategy, the dc-link voltage command $\bar{V}_{\mathrm{dc}}^{*}+\tilde{V}_{\mathrm{dc}}^{*}$ is



(a)

(b)

Fig. 25. Steady-state harmonic-compensation results. (a) With the conventional double-loop control strategy. (b) With the proposed strategy.

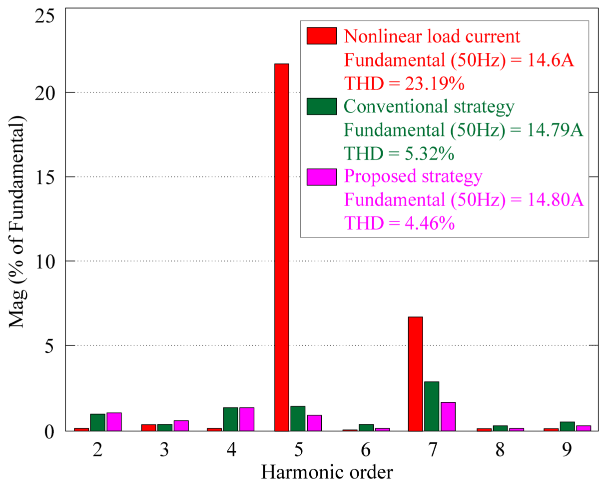
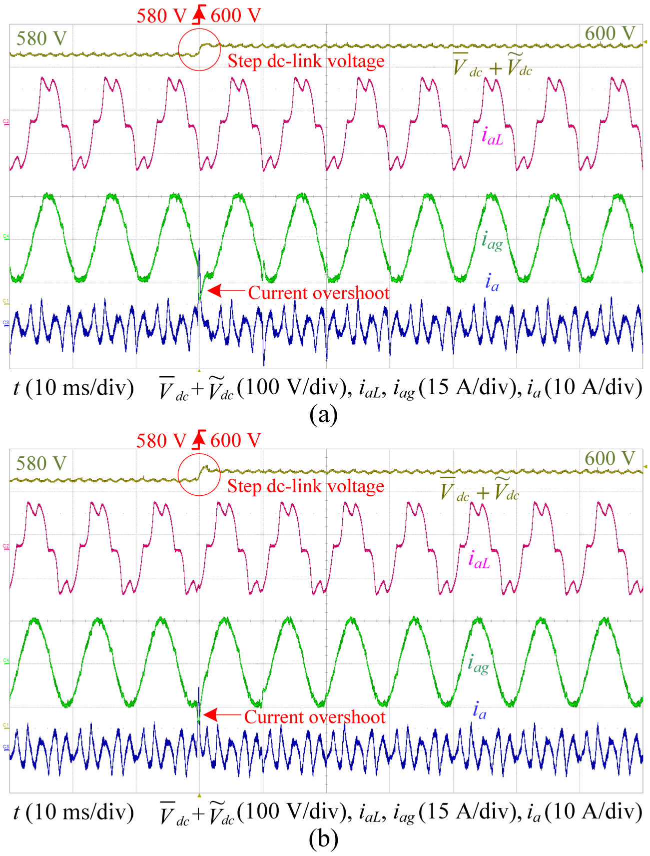


Fig. 26. FFT comparison of the harmonic-compensation results.

calculated only based on nonlinear load harmonics, therefore, a relatively large tracking error still exists, as presented in Fig. 23. To further reduce the tracking error, existing strategies for suppressing the influence of the distorted grid voltage [44], [45] can be applied in the 3L APF. And how to combine the existing strategies and the proposed strategy of this article could be our future work on the basis of the research of this article, to simultaneously suppress the influence of the distorted grid voltage and enhance the harmonic-compensation performance.



(a)

(b)

Fig. 27. Dynamic responses with a step dc-link voltage from 580 V to 600 V. (a) Using the conventional double-loop control strategy. (b) Using the proposed strategy.

Fig. 24 shows the dynamic experimental results before and after the proposed strategy is adopted. In Fig. 24(a), the waveforms with the conventional double-loop control strategy are zoomed in. And in Fig. 24(b), the waveforms with the proposed strategy are zoomed in, where the calculated the calculated $\bar{V}^*_{\rm dc} + \tilde{V}^*_{\rm dc}$ is adopted as the command of the outer voltage loop. Comparing Fig. 24(a) with Fig. 24(b), it can be seen that, the quality of the sinusoidal grid current i_{ag} has been enhanced after the proposed strategy is employed.

To compare the harmonic-compensation performance more preciously, experimental waveforms are captured with the two strategies in steady state, as seen in Fig. 25. And the corresponding fast Fourier transform (FFT) results are shown in Fig. 26. As seen, with the conventional double-loop control strategy, the total harmonic distortion (THD) of the grid current i_{ag} calculated up to 10 kHz is 5.32%. With the proposed strategy, the THD is reduced to 4.46%, and the overall harmonic spectra are lower, presenting a better ability of compensating harmonic currents.

To test the dynamic performance of the dc-link voltage loop, a step command from 580 V to 600 V is applied to the two strategies, respectively. As seen in Fig. 27, with both the conventional and the proposed strategies, the dc-link voltages can rise fast. After the current overshoot in the APF output current

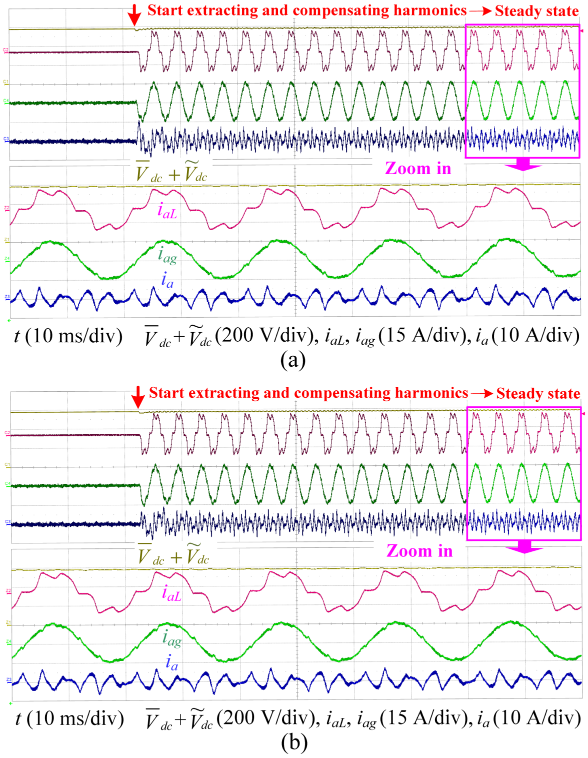


Fig. 28. Dynamic responses when the nonlinear load is applied. (a) Using the conventional double-loop control strategy. (b) Using the proposed strategy.

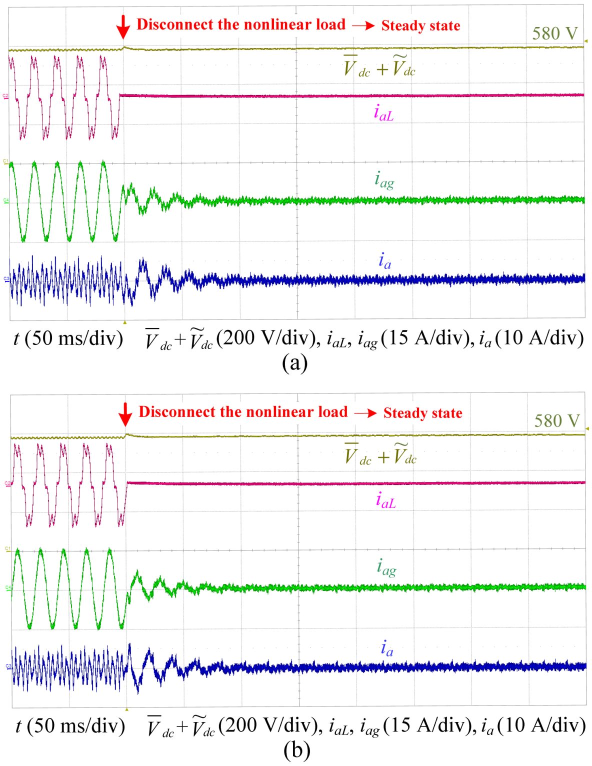


Fig. 29. Dynamic responses when the nonlinear load is disconnected. (a) Using the conventional double-loop control strategy. (b) Using the proposed strategy.

TABLE III

COMPARISON OF EXPERIMENTAL RESULTS WITH TESTED STRATEGIES

Comparisons		Conventional strategy	Proposed strategy
Dc -link voltage errors	Results	Fig. 22	Fig. 23
	Features	Large	Low
Harmonic-compensation performance	Results	Fig. 24(a) Fig. 25(a)	Fig. 24(b) Fig. 25(b)
	Features	Worse	Better
Dynamic responses with a step dc-link voltage	Results	Fig. 27(a)	Fig. 27(b)
	Features	Fast dynamic response in the dc-link voltage	
Dynamic responses when the nonlinear load is applied	Results	Fig. 28(a)	Fig. 28(b)
	Features	Fast dynamic response with varying nonlinear-load currents	
Dynamic responses when the nonlinear load is disconnected	Results	Fig. 29(a)	Fig. 29(b)
	Features	Fast dynamic response with varying nonlinear-load currents	

i_a, the current harmonics from the nonlinear load can still be compensated effectively. Therefore, it can be indicated that, the dynamic response with the step dc-link voltage is not impaired in the proposed strategy.

Fig. 28 presents the dynamic responses when the nonlinear load is adopted. In the dynamic process of Fig. 28(a), with the conventional double-loop control strategy, current harmonics are gradually extracted and compensated. Meanwhile, during the dynamic process of Fig. 28(b), with the proposed strategy, current harmonics are extracted and the dc-link voltage oscillation command should be calculated. In the steady state, a better quality of the sinusoidal grid current i_{ag} is obtained with the proposed strategy.

Afterwards, the dynamic responses, when the nonlinear load is disconnected, are also tested, as shown in Fig. 29. As seen, the nonlinear load current becomes zero suddenly, and the output current i_a of the APF for compensating harmonics becomes zero gradually. With the two strategies, similar dynamic responses are obtained.

Finally, the above experimental results are concluded in Table III to make the verification and comparison more clear. Through the verification, it can be indicated that, compared with the conventional double-loop control strategy, the proposed strategy has an improved harmonic-compensation performance, while a fast dynamic performance of the dc-link voltage can still be guaranteed.

Regarding the special case where the three-phase grid voltages and/or impedances are unbalanced [21], third-order harmonic currents and the negative-sequence currents can be generated. If the shunt APF is used to compensate current harmonics in this case, extra dc-link voltage oscillations will be generated. Theoretically, the proposed method in this article utilizing the oscillated dc-link voltage command can also be employed with unbalanced grid voltages and/or impedances. But extra researches need to be further carried out, e.g., the oscillated dc-link voltage command should be rederived considering the third-order harmonics and unbalanced grid voltages. This could be our future work on the basis of the research of this article.

VII. CONCLUSION

In this article, the oscillated dc-link voltage command has been utilized to enhance the harmonic-compensation performance. The interaction between dc-link voltage oscillations and ac currents has been analyzed, and the dc-link voltage oscillations caused by ac current harmonics have been mathematically derived. An improved MSOGI-FLL with LPFs has been designed to eliminate the dc bias in the integration for calculating the oscillated dc-link voltage command. An improved 3L APF control strategy utilizing the oscillated dc-link voltage command has been proposed, to suppress the influence of the voltage loop on the current loop. Simulation and experimental results have verified that, compared with the conventional double-loop control strategy, an improved harmonic-compensation performance has been achieved. And a fast dynamic performance of the dc-link voltage can still be guaranteed in the proposed strategy.

REFERENCES

[1] G. Li, F. Ma, C. Wu, M. Li, J. M. Guerrero, and M.-C. Wong, "A generalized harmonic compensation control strategy for mitigating subsynchronous oscillation in synchronverter based wind farm connected to series compensated transmission line," *IEEE Trans. Power Syst.*, vol. 38, no. 3, pp. 2610–2620, May 2023.

[2] G. T. Heydt, "Fifth harmonic spectral voltage components in EHV power transmission systems," *IEEE Trans. Power Del.*, vol. 37, no. 1, pp. 458–463, Feb. 2022.

[3] C. Luo, Q. Guo, Y. Hu, S. Li, Y. Zhu, and H. Guo, "Analysis and countermeasures of harmonic instability in a practical HVDC system with fixed series compensation and STATCOM," *IEEE Trans. Ind. Appl.*, vol. 59, no. 2, pp. 2509–2518, Mar. 2023.

[4] I. Khan, A. S. Vijay, and S. Doolla, "Nonlinear load harmonic mitigation strategies in microgrids: State of the art," *IEEE Syst. J.*, vol. 16, no. 3, pp. 4243–4255, Sep. 2022.

[5] Q.-R. Hong, W.-K. Sou, P.-I. Chan, C. Gong, and C.-S. Lam, "Review of different current control strategies for LC-coupling hybrid active power filter," in *Proc. IEEE 48th Annu. Conf. Ind. Electron. Soc.*, Brussels, Belgium, Oct. 2022, pp. 1–6.

[6] A. V. Barva and S. Joshi, "A comprehensive survey on hybrid active power filter topologies & controller and application in microgrid," in *Proc. IEEE Region 10 Symp.*, Mumbai, India, Jul. 2022, pp. 1–6.

[7] T. Abeyasekera, C. M. Johnson, D. J. Atkinson, and M. Armstrong, "Suppression of line voltage related distortion in current controlled grid connected inverters," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1393–1401, Nov. 2005.

[8] E. Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 888–895, May 2003.

[9] D. M. Stojić and T. B. Šekara, "Digital resonant current controller for LCL-filtered inverter based on modified current sampling and delay modeling," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7109–7119, Dec. 2022.

[10] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, "Frequency response analysis of current controllers for selective harmonic compensation in active power filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 337–347, Feb. 2009.

[11] H. Geng, Z. Zheng, T. Zou, B. Chu, and A. Chandra, "Fast repetitive control with harmonic correction loops for shunt active power filter applied in weak grid," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 3198–3206, May/Jun. 2019.

[12] P. Santiprapan, K. Areerak, and K. Areerak, "An adaptive gain of proportional-resonant controller for an active power filter," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1433–1446, Jan. 2024.

[13] H. Xu, J. Hu, and Y. He, "Operation of wind-turbine-driven DFIG systems under distorted grid voltage conditions: Analysis and experimental validations," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2354–2366, May 2012.

[14] H. Nian and Y. Song, "Direct power control of doubly fed induction generator under distorted grid voltage," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 894–905, Feb. 2014.

[15] M. S. Ali, L. Wang, H. Alquhayz, O. U. Rehman, and G. Chen, "Performance improvement of three-phase boost power factor correction rectifier through combined parameters optimization of proportional-integral and repetitive controller," *IEEE Access*, vol. 9, pp. 58893–58909, 2021.

[16] W.-K. Sou, C.-W. Chao, C. Gong, C.-S. Lam, and C.-K. Wong, "Analysis, design, and implementation of multi-quasi-proportional-resonant controller for thyristor-controlled LC-coupling hybrid active power filter (TCLC-HAPF)," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 29–40, Jan. 2022.

[17] J. Fei and L. Liu, "Real-time nonlinear model predictive control of active power filter using self-feedback recurrent fuzzy neural network estimator," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 8366–8376, Aug. 2022.

[18] J. Fei, L. Liu, and Y. Chen, "Finite-time disturbance observer of active power filter with dynamic terminal sliding mode controller," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 1604–1615, Apr. 2023.

[19] S. Sharma and V. Verma, "Modified control strategy for shunt active power filter with MRAS-based dc voltage estimation and load current sensor reduction," *IEEE Trans. Ind. Appl.*, vol. 57, no. 2, pp. 1652–1663, Mar./Apr. 2021.

[20] L. Wu, F. Zhuo, P. Zhang, H. Li, and Z. Wang, "Study on the influence of supply-voltage fluctuation on shunt active power filter," *IEEE Trans. Power Del.*, vol. 22, no. 3, pp. 1743–1749, Jul. 2007.

[21] T. Mannen, I. Fukasawa, and H. Fujita, "A new control method of suppressing dc capacitor voltage ripples caused by third-order harmonic compensation in three-phase active power filters," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6149–6158, Nov. 2018.

[22] J. Zhou, Y. Yuan, and H. Dong, "Adaptive dc-link voltage control for shunt active power filters based on model predictive control," *IEEE Access*, vol. 8, pp. 208348–208357, 2020.

[23] R. L. A. Ribeiro, T. O. A. Rocha, R. M. Sousa, E. C. Santos, and A. M. N. Lima, "A robust dc-link voltage control strategy to enhance the performance of shunt active power filters without harmonic detection schemes," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 803–813, Feb. 2015.

[24] Z. Xiang et al., "A residential miniboost photovoltaic inverter with maximum power point operation and power quality compensation," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 4320–4331, May 2023.

[25] A. Abuelrub, F. Hamed, J. Hedel, and H. M. K. Al-Masri, "Feasibility study for electric vehicle usage in a microgrid integrated with renewable energy," *IEEE Trans. Transp. Electrific.*, vol. 9, no. 3, pp. 4306–4315, Sep. 2023.

[26] R. Zhao, Z. Xin, P. C. Loh, and F. Blaabjerg, "A novel flux estimator based on multiple second-order generalized integrators and frequency-locked loop for induction motor drives," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6286–6296, Aug. 2017.

[27] P. Rodríguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 127–138, Jan. 2011.

[28] H. A. Beshr, M. S. E. Moursi, H. A. Hamed, and A. Al-Sumaiti, "Advanced type-1c FLL for enhancing converters synchronization during frequency drift," *IEEE Trans. Power Del.*, vol. 36, no. 2, pp. 1063–1078, Apr. 2021.

[29] P. N. Babu, J. M. Guerrero, P. Siano, R. Peesapati, and G. Panda, "An improved adaptive control strategy in grid-tied PV system with active power filter for power quality enhancement," *IEEE Syst. J.*, vol. 15, no. 2, pp. 2859–2870, Jun. 2021.

[30] M. M. Amin, A. S. Soliman, F. F. M. El-Sousy, and O. A. Mohammed, "Encoderless control of PMa-SynRG based-stator current vector for wind generation systems," *IEEE Trans. Ind. Appl.*, vol. 59, no. 3, pp. 2950–2962, May/Jun. 2023.

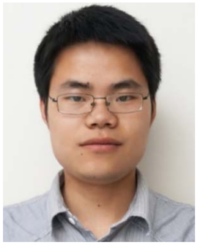
[31] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *Proc. 37th IEEE Power Electron. Specialists Conf.*, Jeju, South Korea, Jun. 2006, pp. 1–6.

[32] Z. Xin, X. Wang, Z. Qin, M. Lu, P. C. Loh, and F. Blaabjerg, "An improved second-order generalized integrator based quadrature signal generator," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8068–8073, Dec. 2016.

[33] Z. Xin, R. Zhao, P. Mattavelli, P. C. Loh, and F. Blaabjerg, "Re-investigation of generalized integrator based filters from a first-order-system perspective," *IEEE Access*, vol. 4, pp. 7131–7144, Nov. 2016.

[34] C. Zhang, X. Zhao, X. Wang, X. Chai, Z. Zhang, and X. Guo, "A grid synchronization PLL method based on mixed second- and third-order generalized integrator for dc offset elimination and frequency adaptability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1517–1526, Sep. 2018.

[35] Y. Jiao and F. C. Lee, "LCL filter design and inductor current ripple analysis for a three-level NPC grid interface converter," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4659–4668, Sep. 2015.
[36] D. Jiang and F. Wang, "Current-ripple prediction for three-phase PWM converters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 531–538, Jan./Feb. 2014.
[37] G. Grandi, J. Loncarski, and O. Dordevic, "Analysis and comparison of peak-to-peak current ripple in two-level and multilevel PWM inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2721–2730, May 2015.
[38] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.
[39] X. Zhang and J. W. Spencer, "Study of multisampled multilevel inverters to improve control performance," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4409–4416, Nov. 2012.
[40] J. R. Fischer, S. A. Gonzalez, M. A. Herran, M. G. Judewicz, and D. O. Carrica, "Calculation-delay tolerant predictive current controller for three-phase inverters," *IEEE Trans. Ind. Inform.*, vol. 10, no. 1, pp. 233–242, Feb. 2014.
[41] Q. Yan, X. Wu, X. Yuan, and Y. Geng, "An improved grid-voltage feedforward strategy for high-power three-phase grid-connected inverters based on the simplified repetitive predictor," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3880–3897, May 2016.
[42] Z. Hao, J. Gong, Y. Liu, S. Pan, and X. Zha, "Analytical calculation of the dc-link current harmonics in active power filter considering coupling effect," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 4, no. 3, pp. 767–780, Jul. 2023.
[43] S. Guenter, J. Yang, G. Buticchi, F. W. Fuchs, and M. Liserre, "DC-link voltage dynamics of three-level four-wire grid-connected converters during harmonics injection operations," *IEEE Trans. Ind. Electron.*, vol. 70, no. 8, pp. 8000–8008, Aug. 2023.
[44] M. K. Mishra and V. N. Lal, "An advanced proportional multiresonant controller for enhanced harmonic compensation with power ripple mitigation of grid-integrated PV systems under distorted grid voltage conditions," *IEEE Trans. Ind. Appl.*, vol. 57, no. 5, pp. 5318–5331, Sep./Oct. 2021.
[45] G. Lou, Q. Yang, W. Gu, X. Quan, J. M. Guerrero, and S. Li, "Analysis and design of hybrid harmonic suppression scheme for VSG considering nonlinear loads and distorted grid," *IEEE Trans. Energy Convers.*, vol. 36, no. 4, pp. 3096–3107, Dec. 2021.



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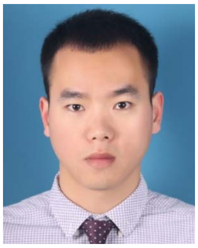

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